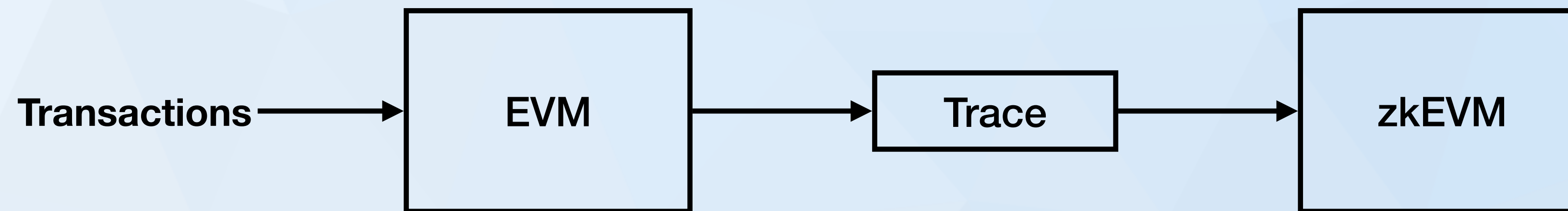




Finding Bugs in zkEVMs

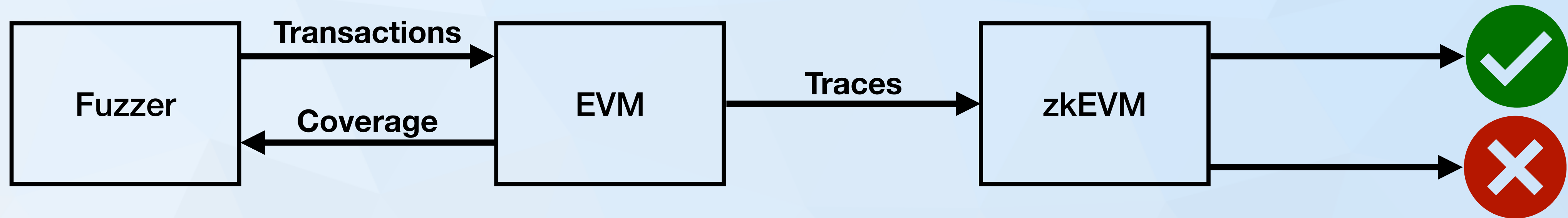
Amber Huang
BD, Veridise

Simplified Model of a zkEVM

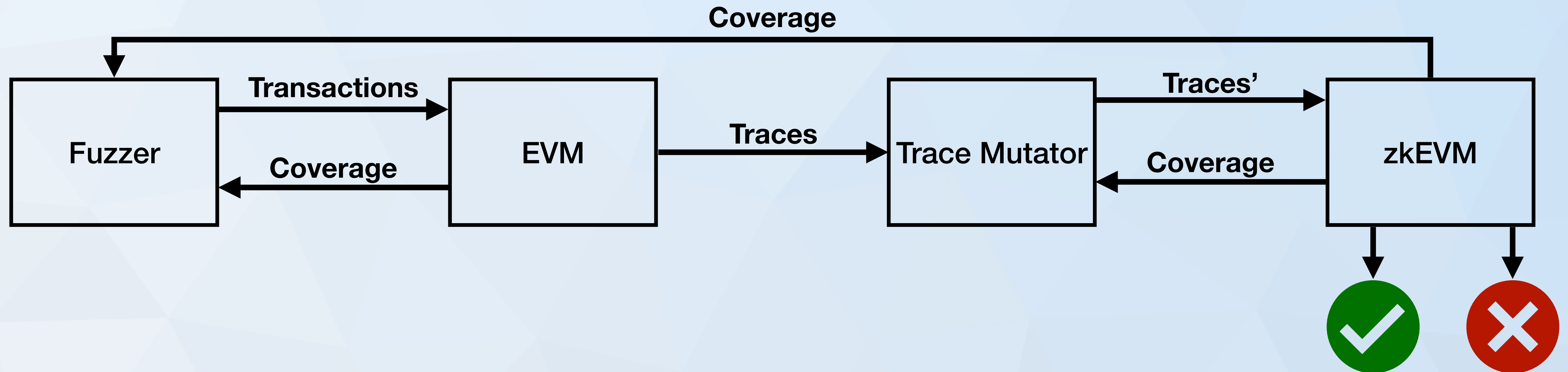


Goal: Find bugs in zkEVM's circuits

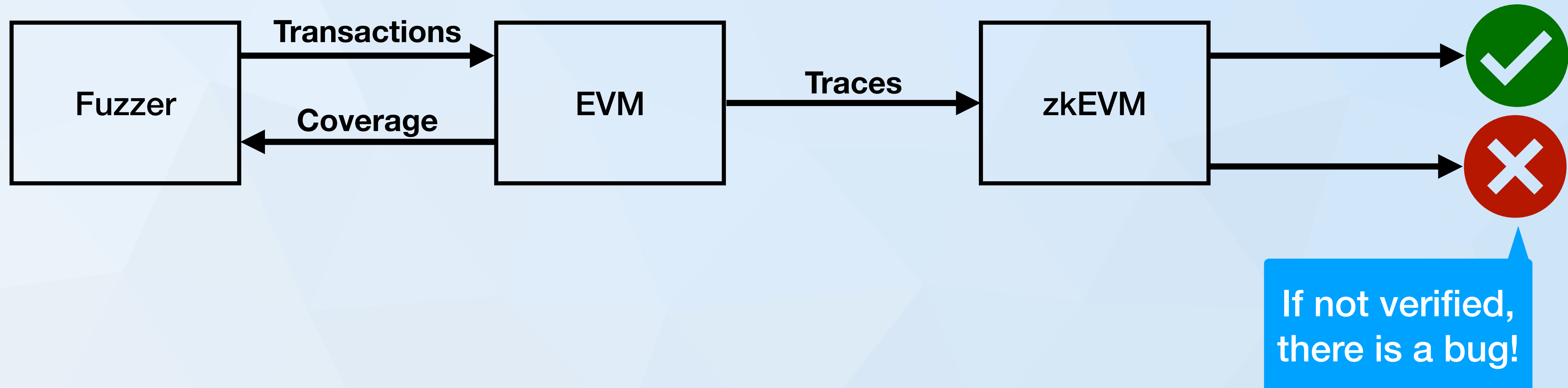
1. Whole System Fuzzing



2. Trace Mutation Fuzzing

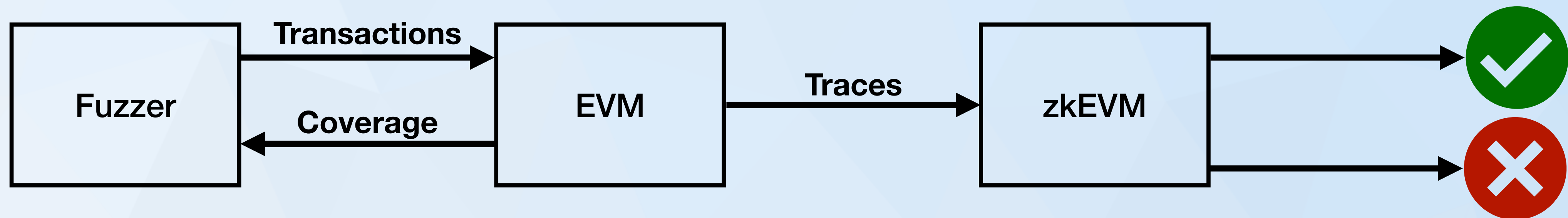


Looks for possible DoS Bugs in zkEVM



Unlikely to identify interesting bugs in ZK-Circuits

Found 11 DoS bugs in a ZK EVM!

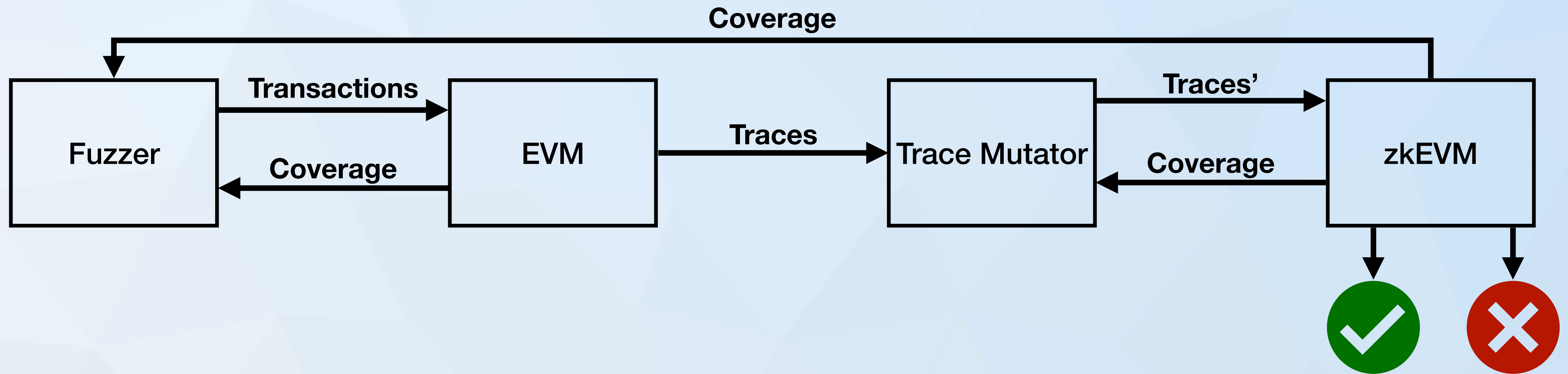


Bugs Found:

- 1 Verification Failed (State Circuit)
- 1 Invalid Call (TX Circuit)
- 3 Index Out of Bounds (EVM Circuit)
- 2 Integer Overflow (EVM Circuit)
- 2 Assertion Violation (EVM Circuit)
- 2 Invalid Calls (EVM Circuit)

Veridise. | Trace Mutation Fuzzing

Can identify complex bugs like under-constrained circuits using the trace mutator!



Can also find bugs if verified!

zkVanguard



Static analysis for common bugs in
ZK circuits

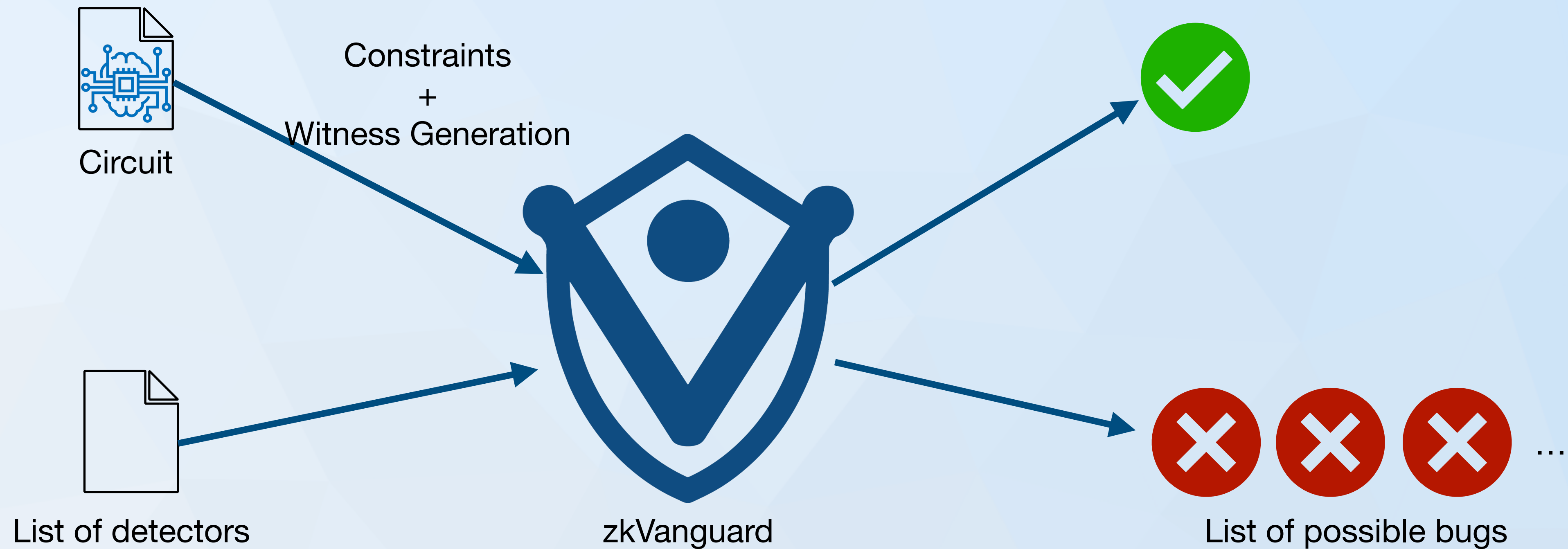
Picus



Proving whether or not ZK circuits
are properly constrained

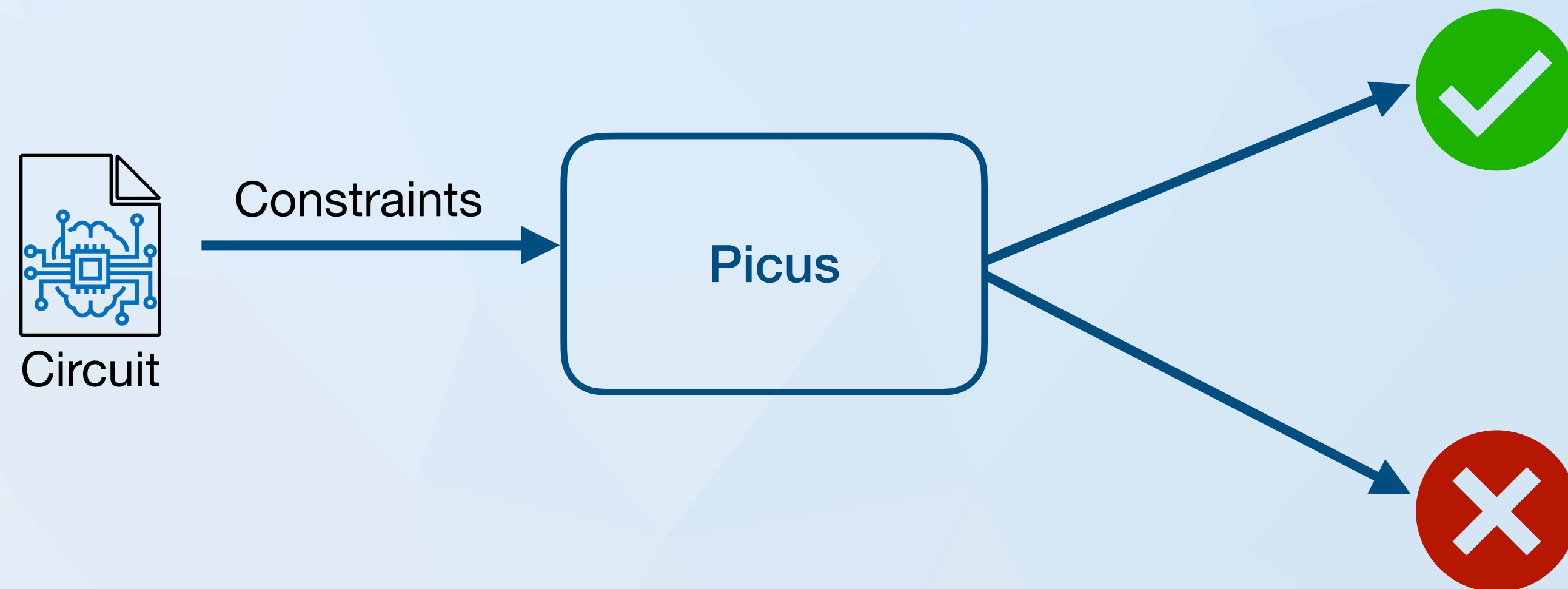
Finding common bugs with ZK Vanguard

ZK Vanguard has a set of detectors that search for common buggy patterns in Circuits



Verify that circuits are properly constrained

Picus formally proves that a circuit is deterministic



Veridise. | Helping auditors in ZK audits

We actively use Picus and zkVanguard in our audits

- Rate Limiting Nullifier (PSE)
- HydraS2 (Sismo)
- Manta Network
- Telepathy (Succinct Labs)
- Unirep (PSE)
- Scroll zkEVM
- CircomLib
- ...



<https://veridise.com/audits/>

<https://medium.com/veridise>



**SATISFIABILITY MODULO FINITE
FIELDS: UNLOCKING SMT FOR ZK
VERIFICATION**

Automated Detection of Under-Constrained Circuits in Zero-Knowledge Proofs

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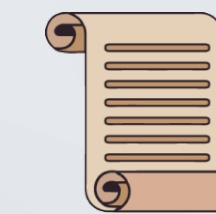
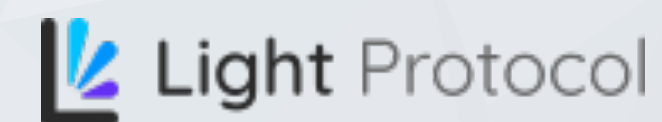
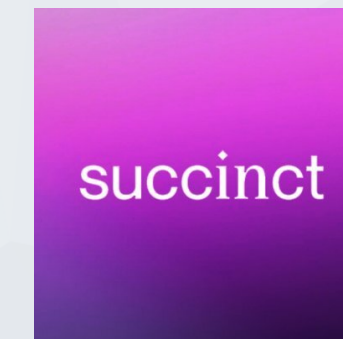
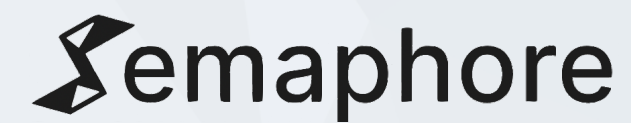
Trusted By:



Picus



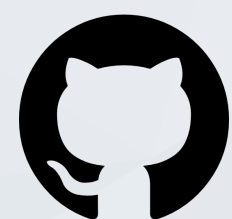
zkVanguard



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CircomLib



<https://github.com/Veridise/Picus>

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