Microprocedadores y Micrcontroladores

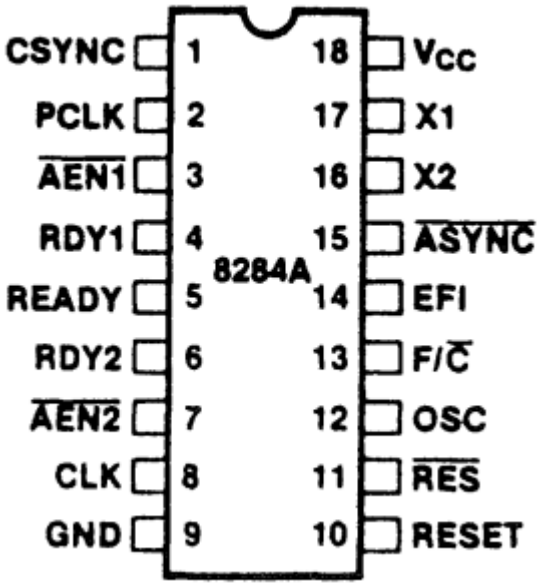
Microprocesador 80x86 – 16 bits

Generador de Reloj 8284

Demultiplexión de ductos

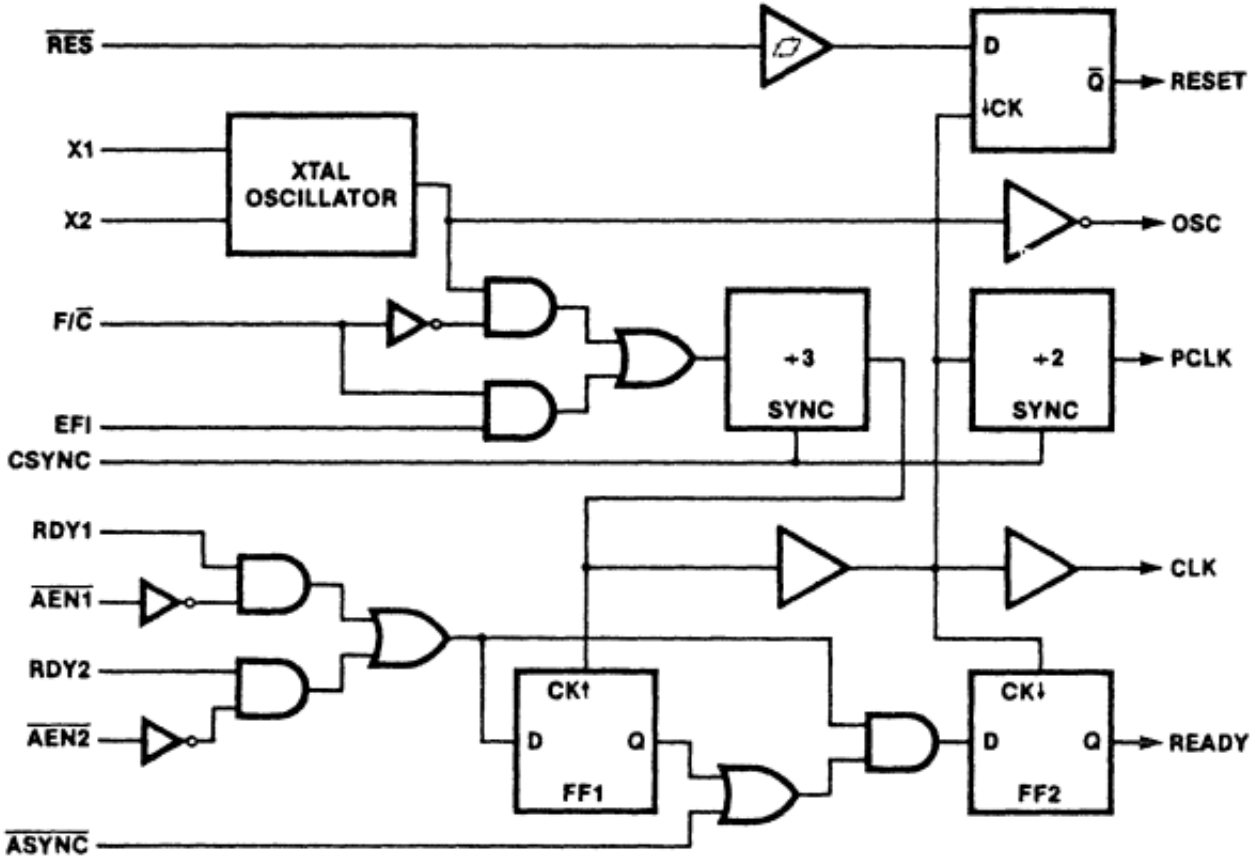
Generador de Reloj 8284A

- Terminales



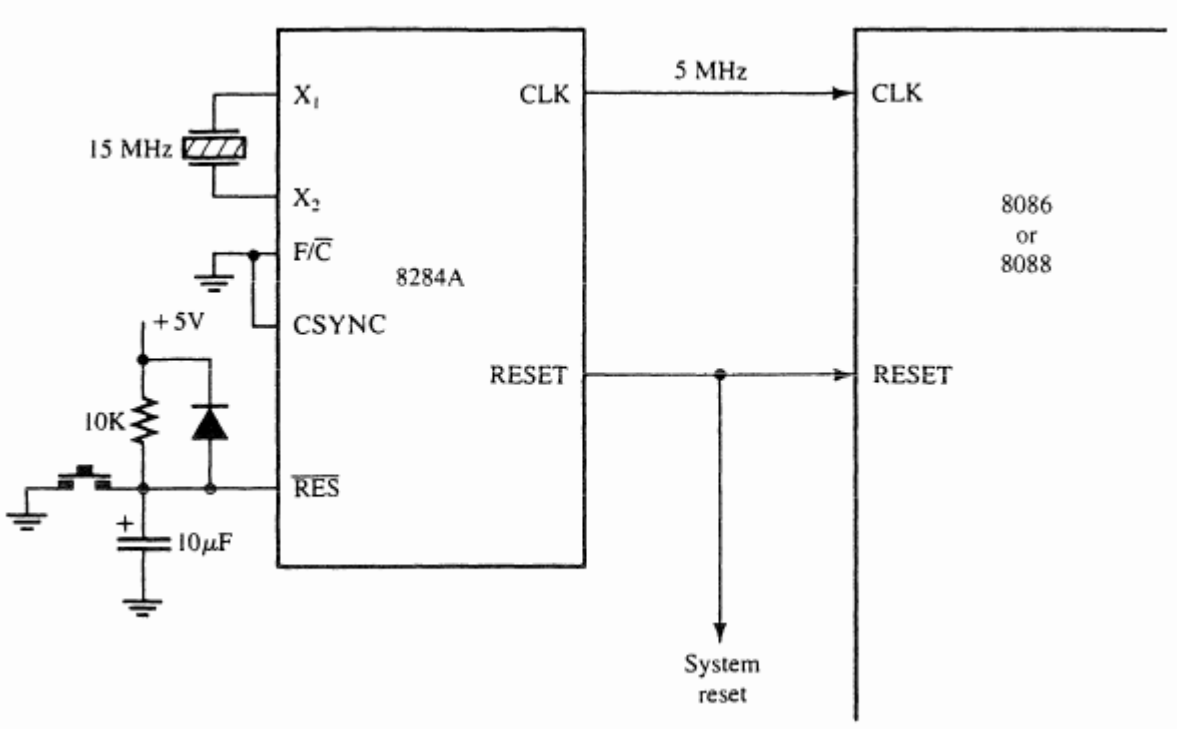
Generador de Reloj 8284A

- Diagrama de bloques interno

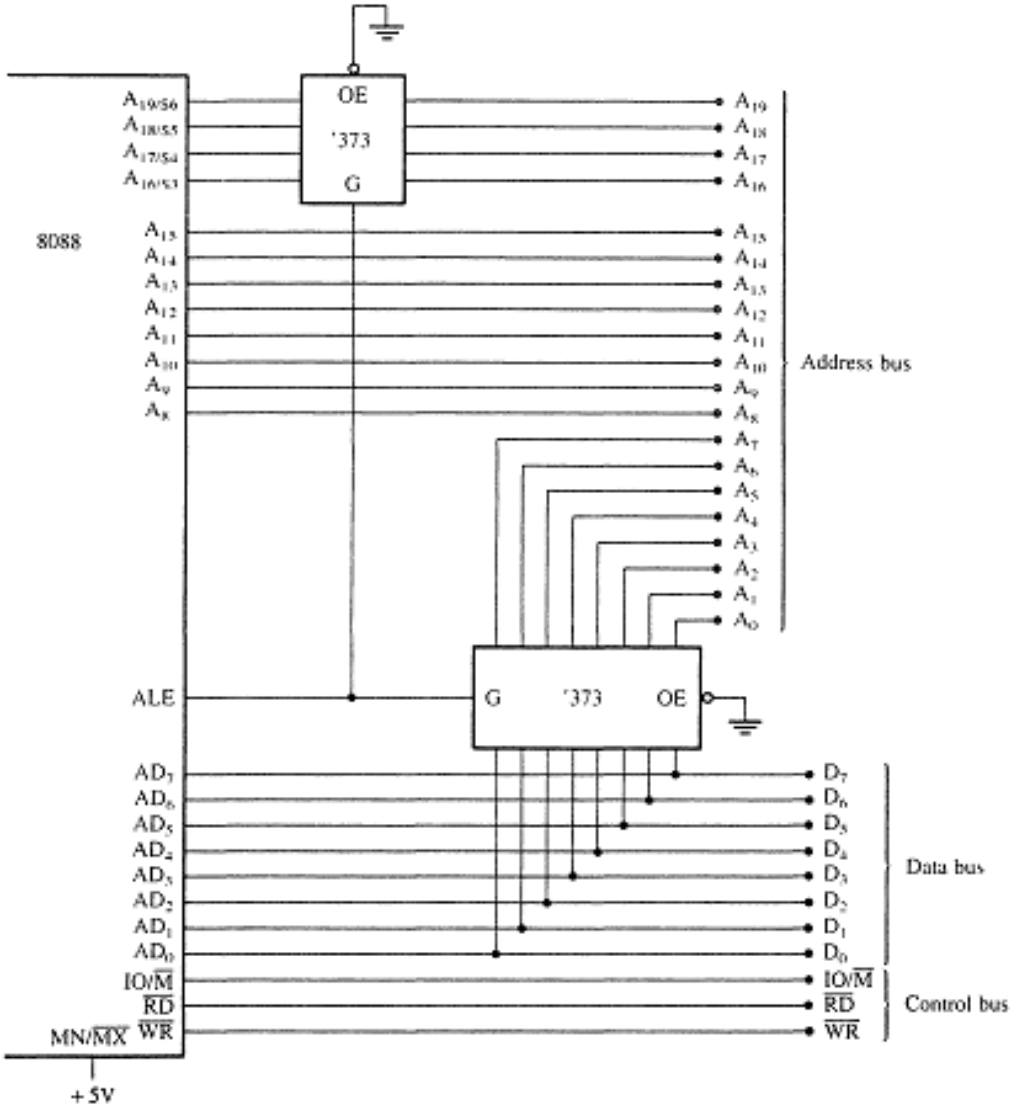


Generador de Reloj 8284A

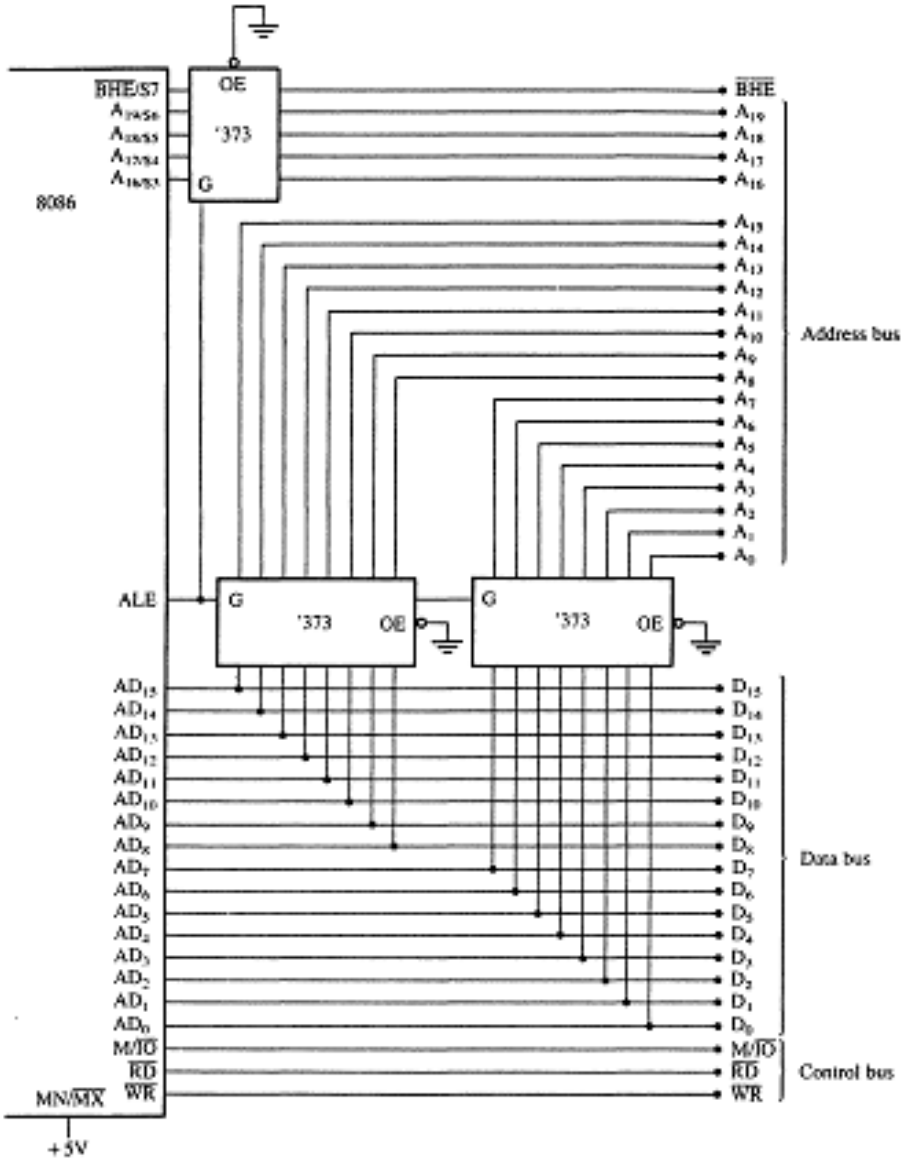
- Conexión con el microprocesador 8088



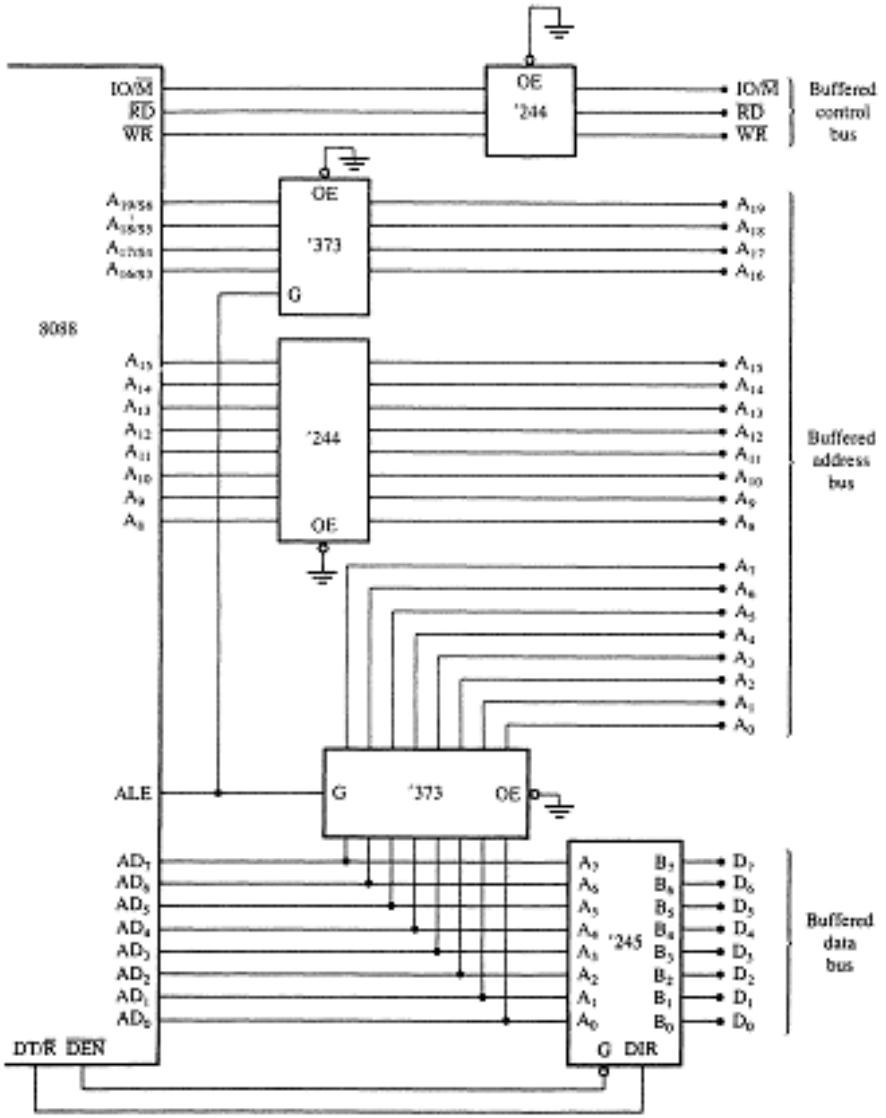
Demultiplexión de ductos (8088)



Demultiplexión de ductos (8086)

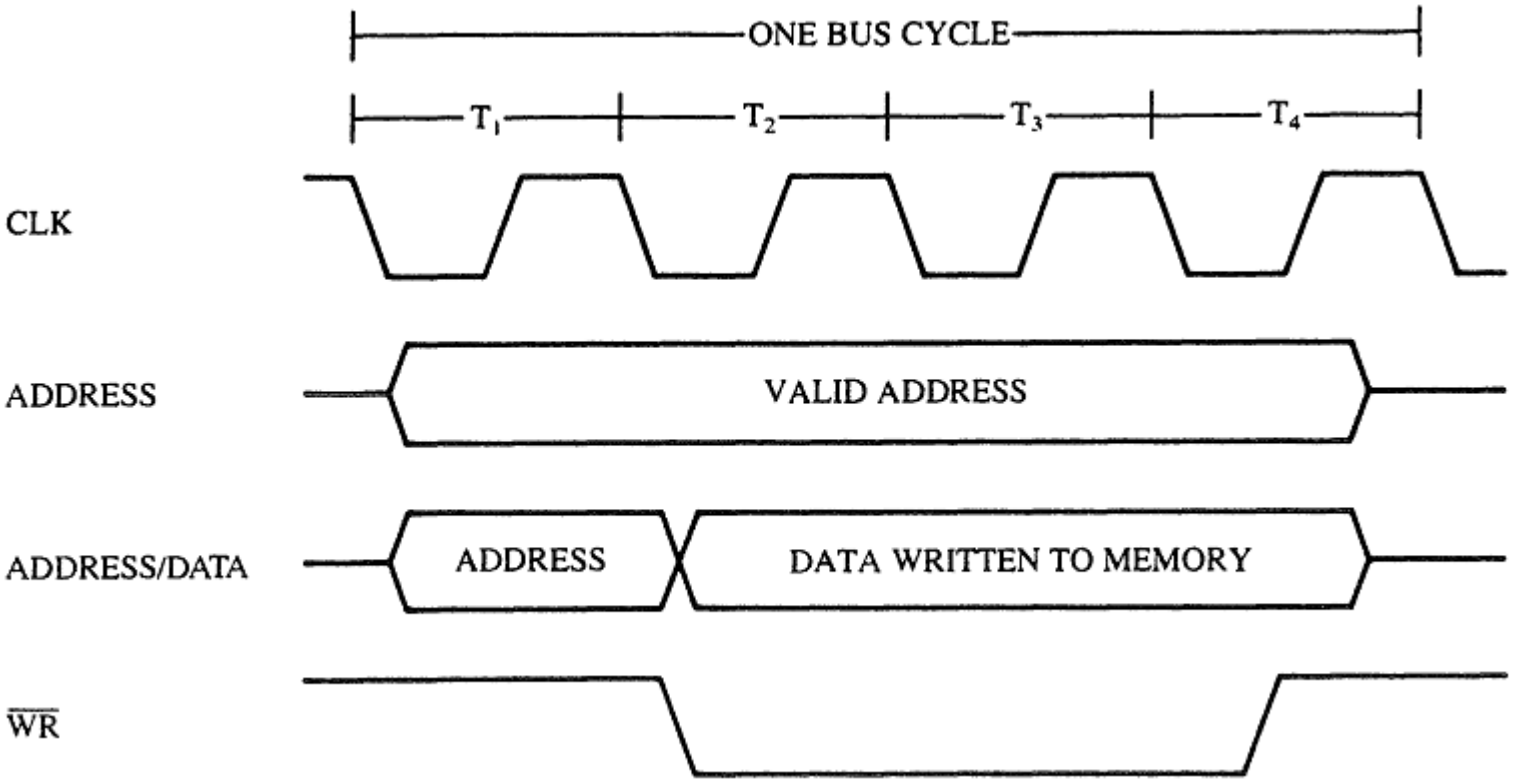


Ductos totalmente reforzados (8088)



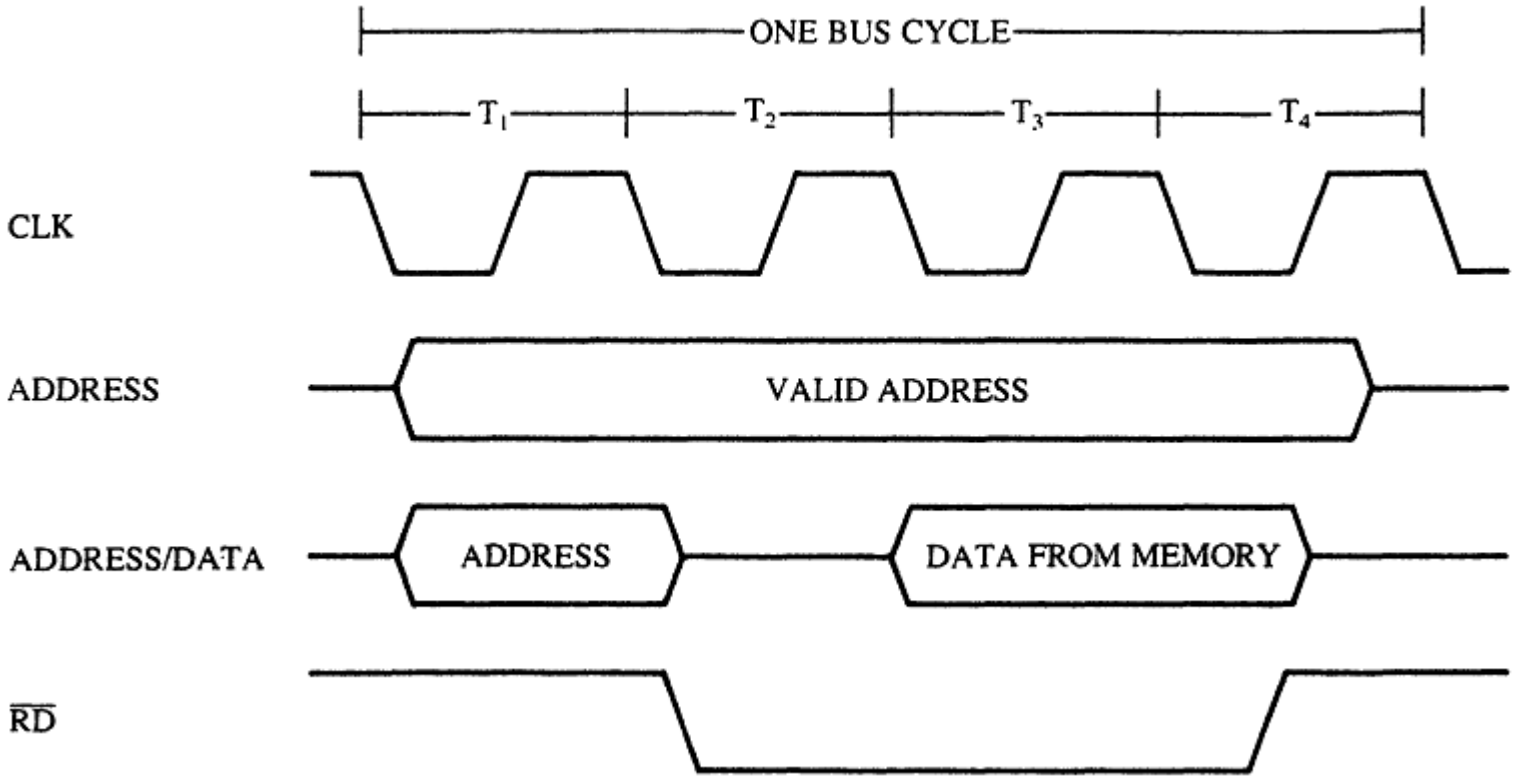
Temporización de ductos

Ciclo de escritura simplificado



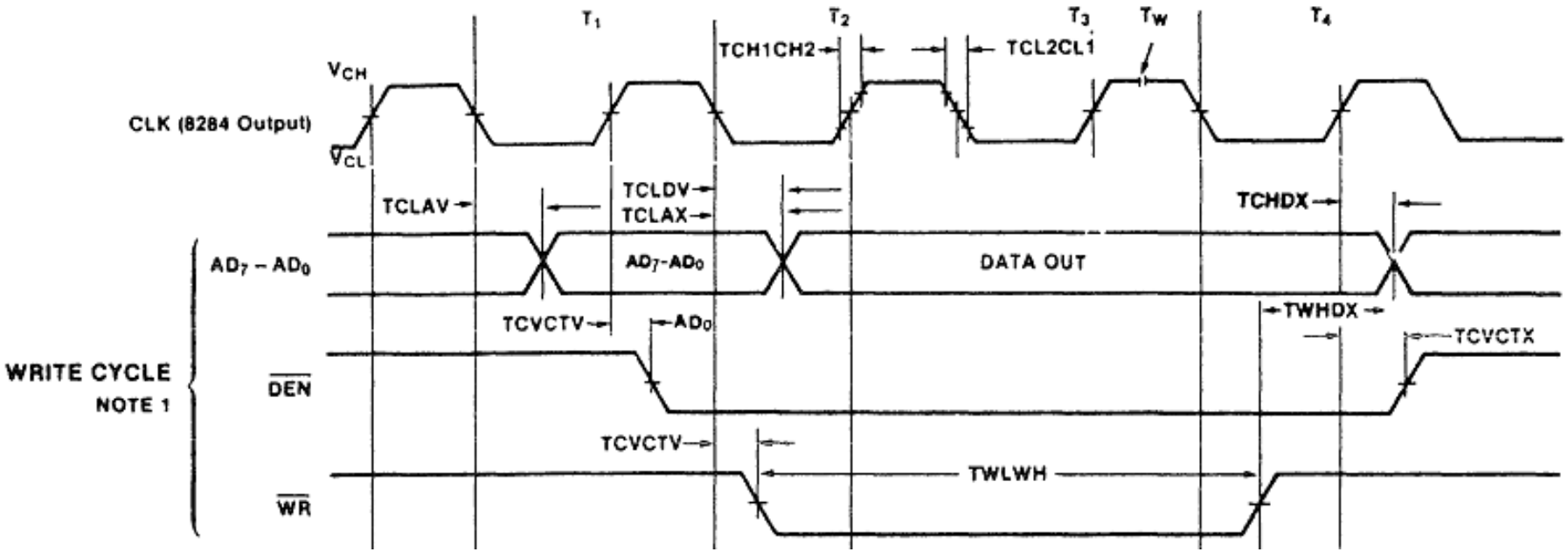
Temporización de ductos

Ciclo de lectura simplificado



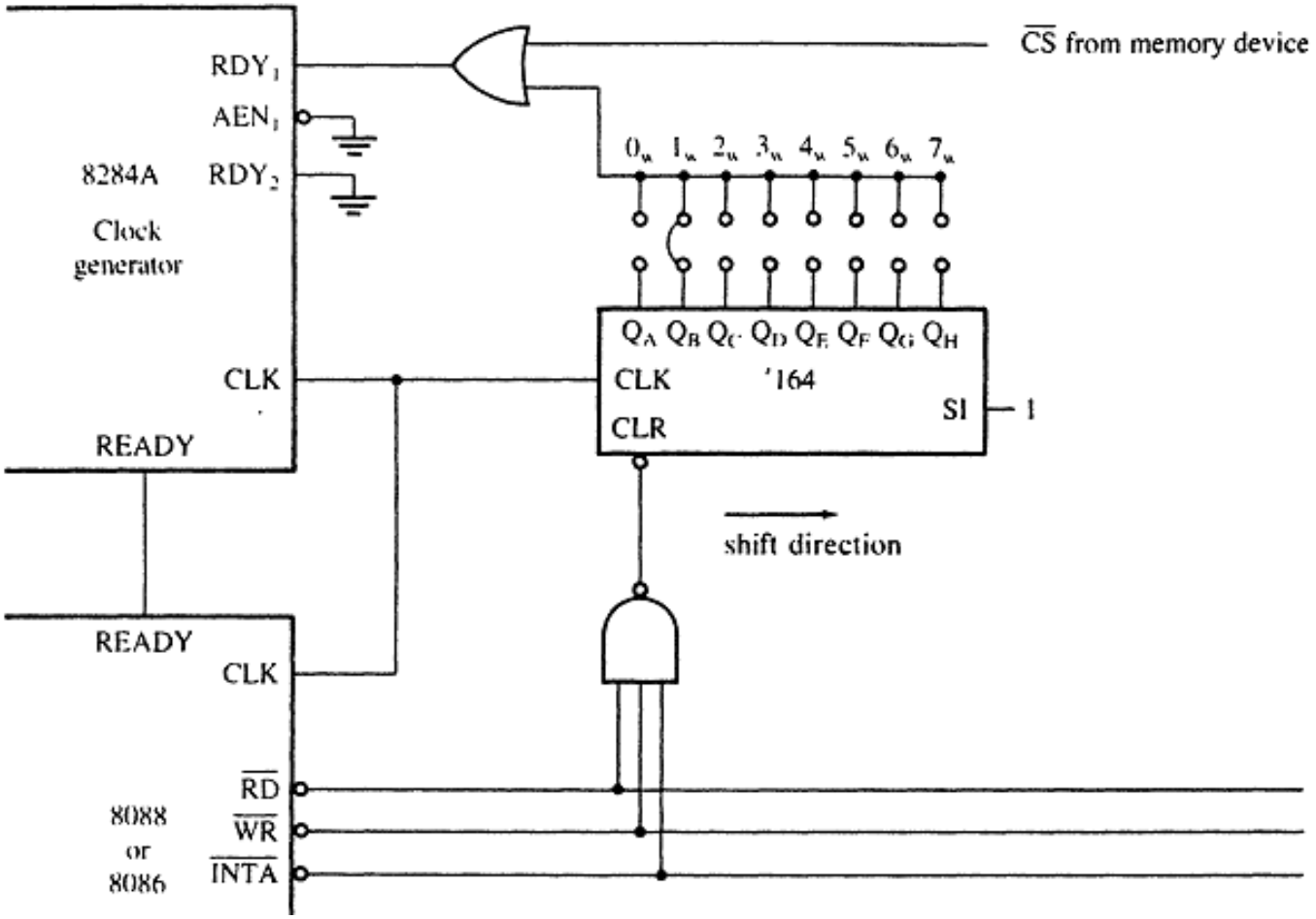
Temporización de ductos

Ciclo de escritura según especificaciones



Temporización de ductos

Circuito para generar ciclos de espera



Temporización de ductos

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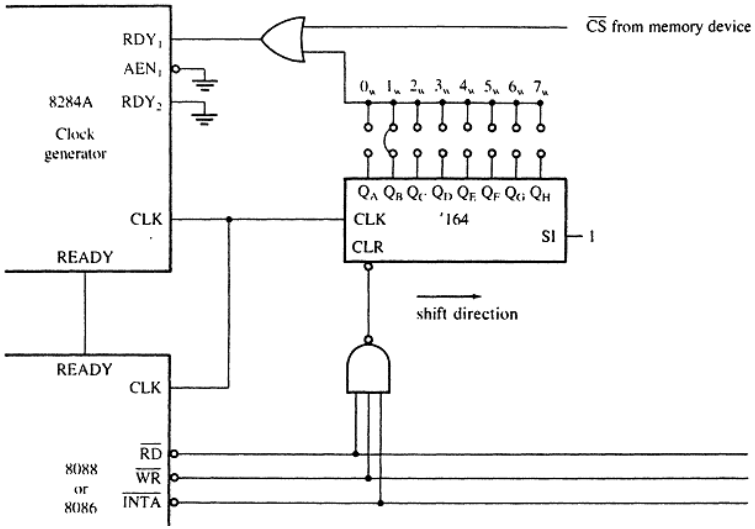
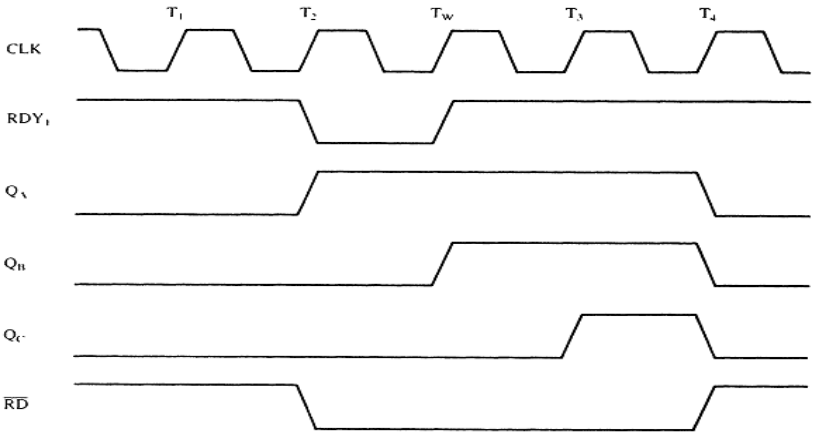
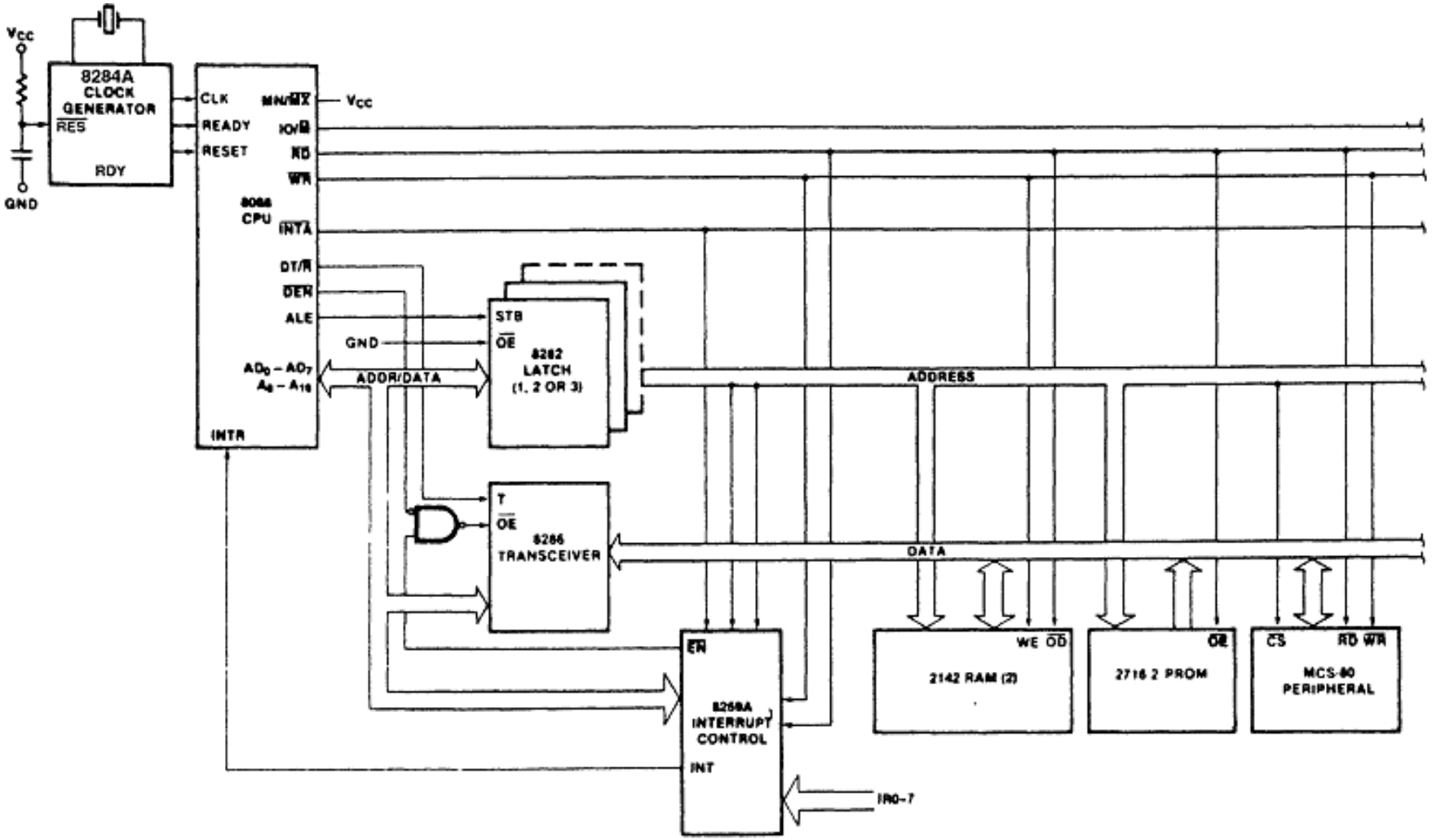
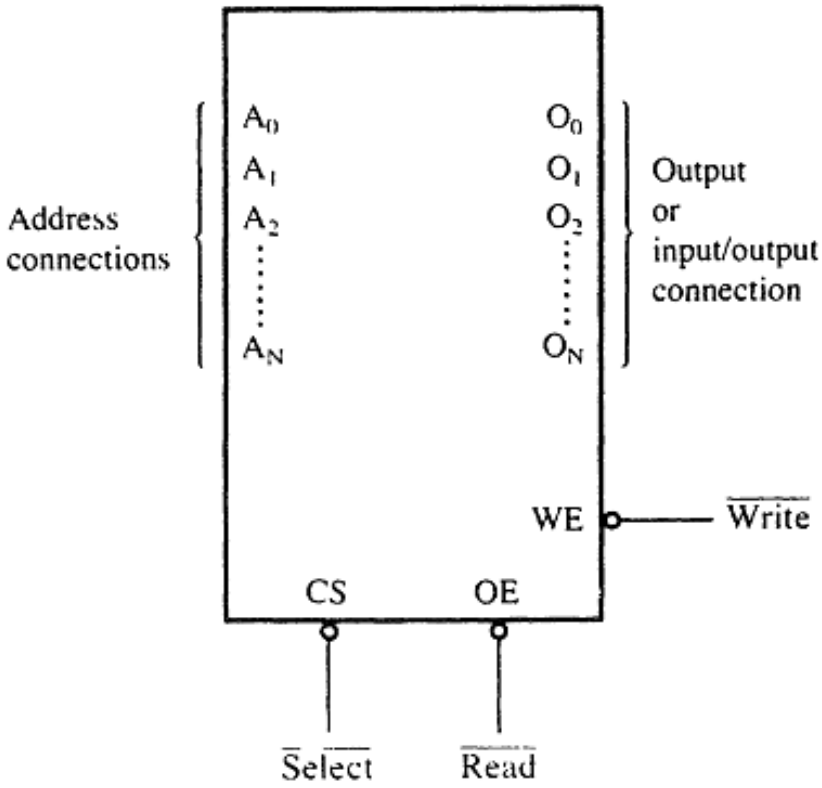




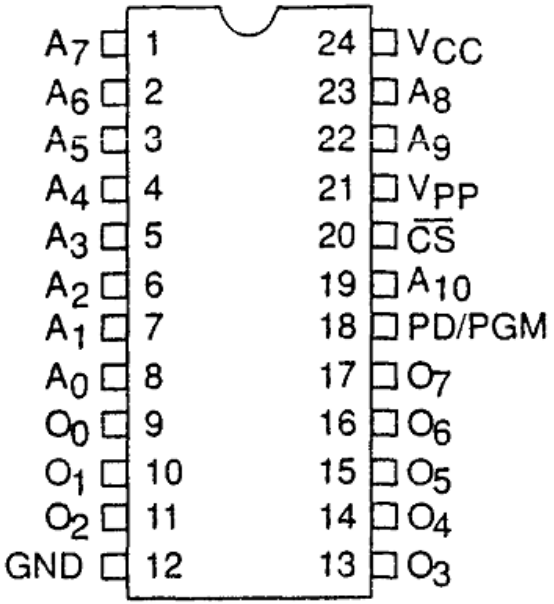
Sistema en modo mínimo

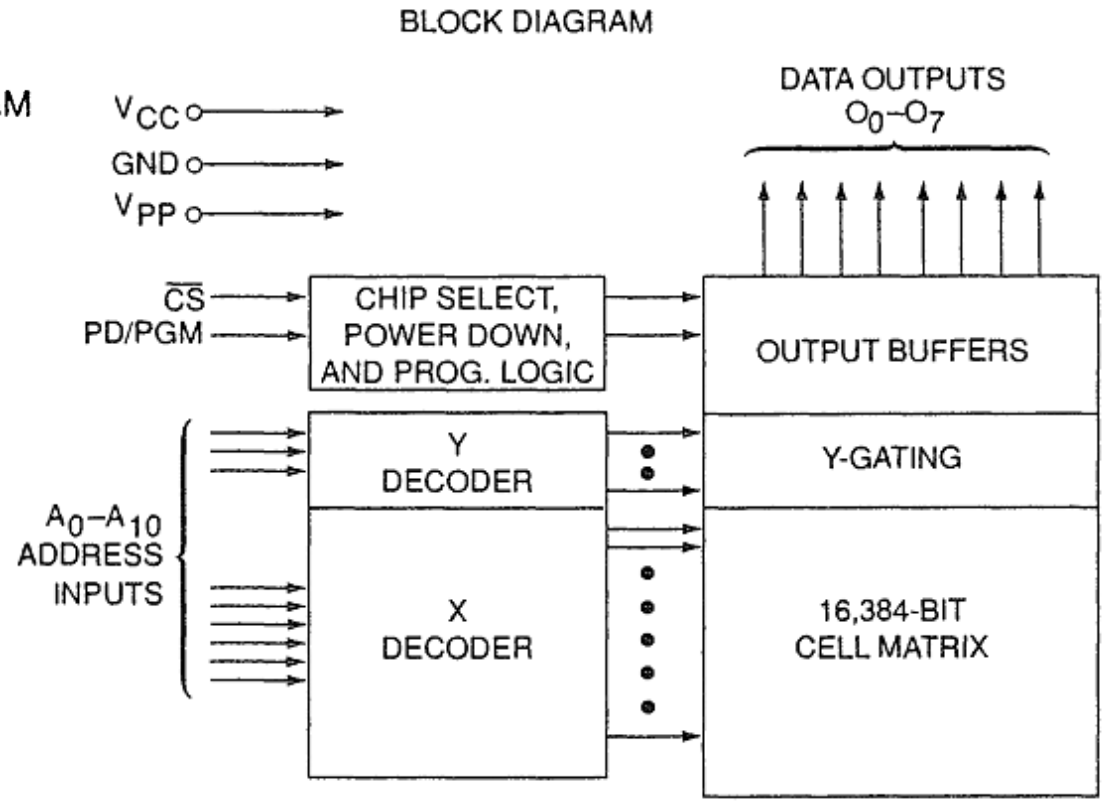


Interfaz a memoria



Memoria EPROM 2716 (2Kx8)





Memoria EPROM 2716 (2Kx8)

A.C. Characteristics

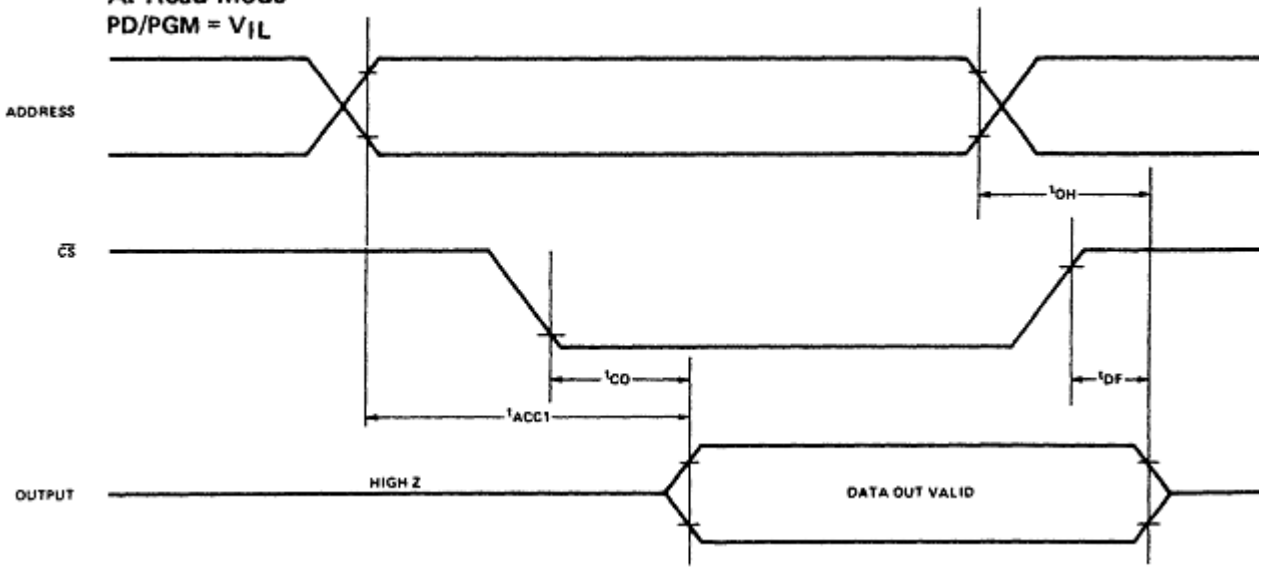
T_A = 0°C to 70°C, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

WAVEFORMS

A. Read Mode

PD/PGM = V_{IL}



Memoria EPROM 2716 (2Kx8)

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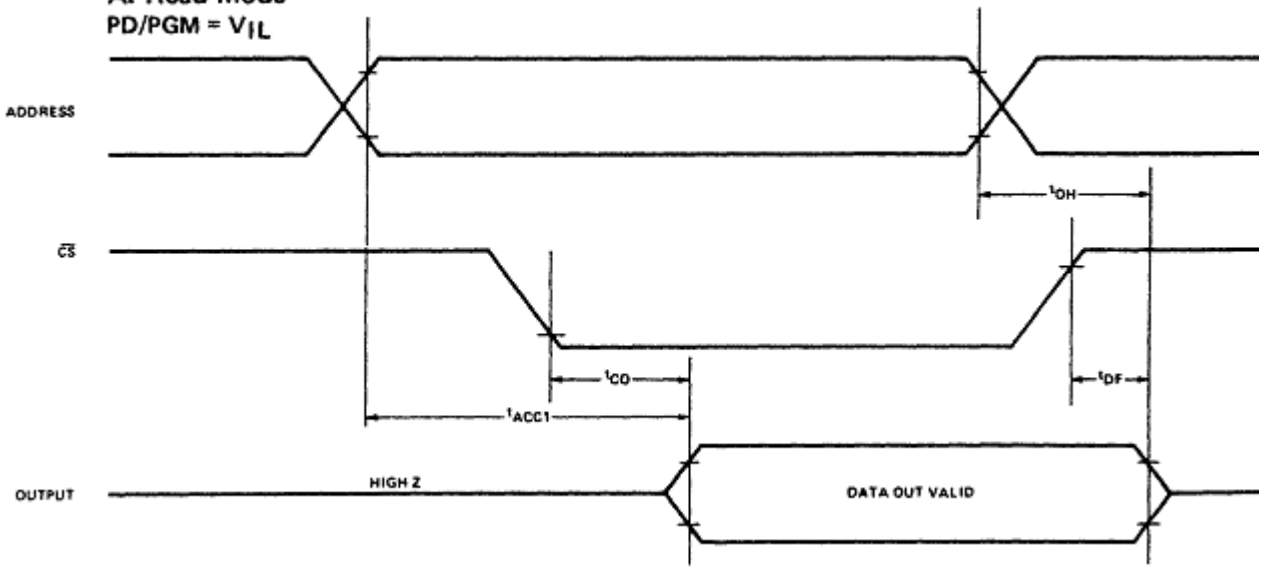
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

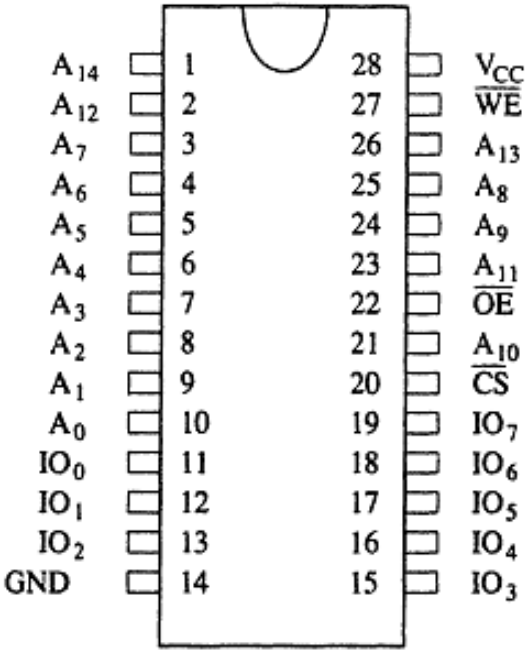
WAVEFORMS

A. Read Mode

PD/PGM = V_{IL}



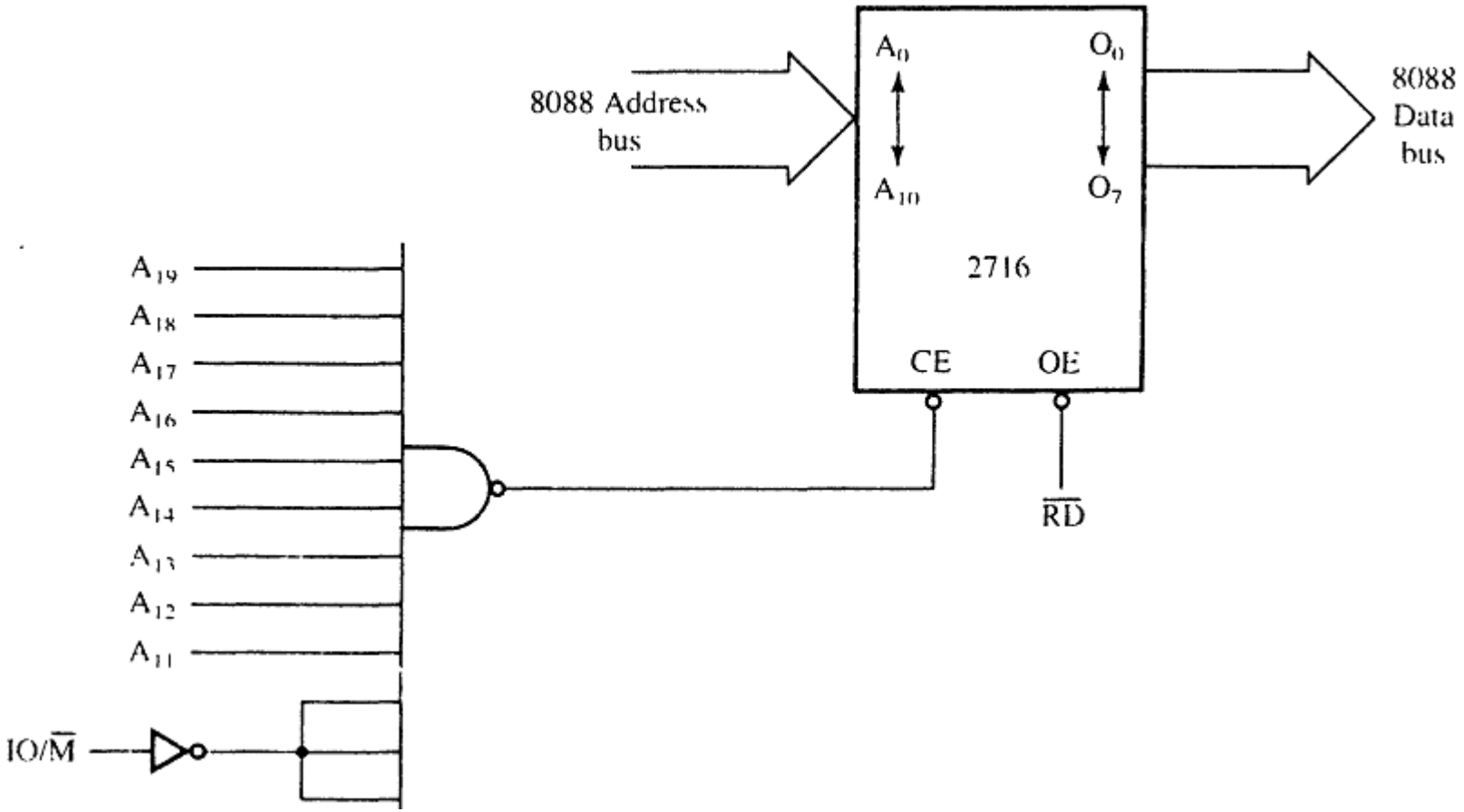
Memoria RAM 62256 (32Kx8)



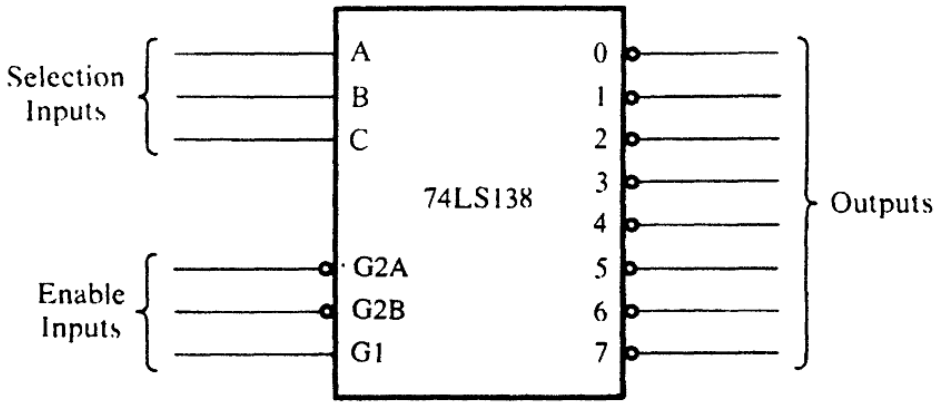
PIN FUNCTION

A_0 - A_{14}	Addresses
IO_0 - IO_7	Data connections
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V Supply
GND	Ground

Decodificador de Memoria

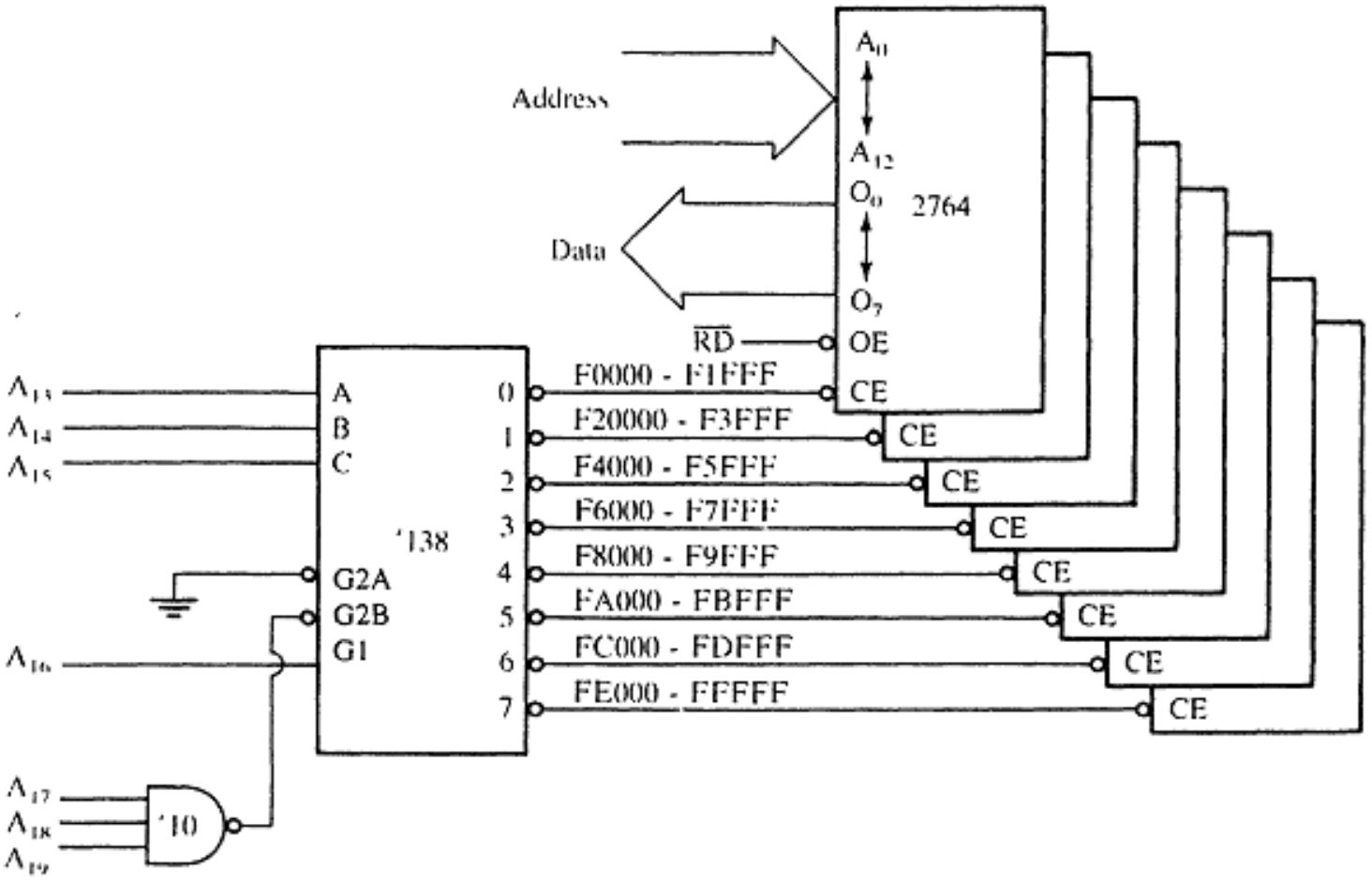


Decodificador de Memoria

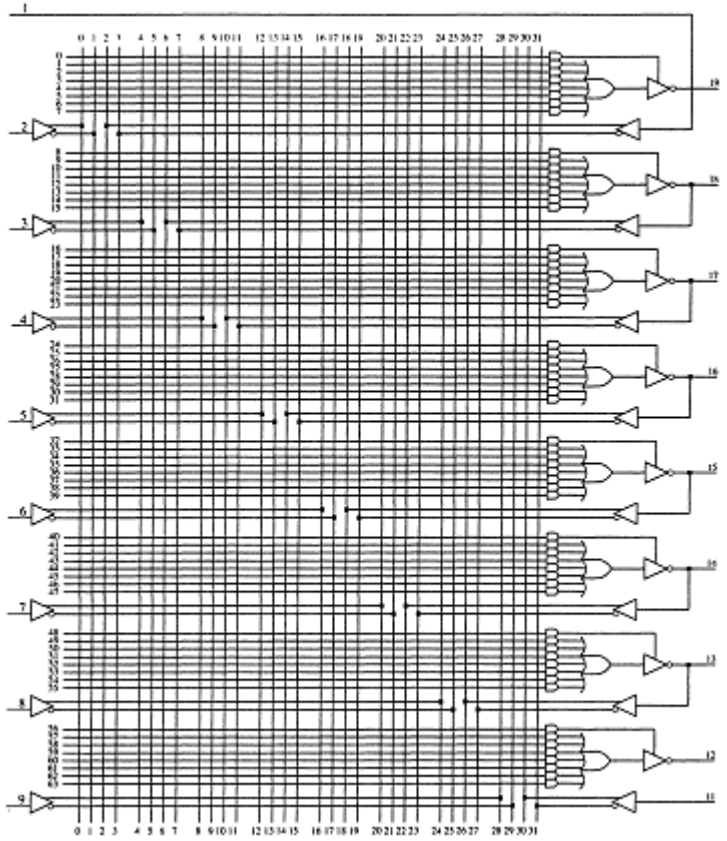


Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Decodificador de Memoria (múltiple)



Decodificador de Memoria (PLD)



```
TITLE       Address Decoder
PATTERN     Test 1
REVISION    A
AUTHOR      Barry B. Brey
COMPANY     BreyCo
DATE        6/6/96
CHIP        DECODER1 PAL16L8

;pins 1   2   3   4   5   6   7   8  9  10
      A19 A18 A17 A16 A15 A14 A13 NC NC GND

;pins 11  12  13  14  15  16  17  18 19  20
      NC  O8  O7  O6  O5  O4  O3  O2 O1 VCC

EQUATIONS

/O1 = A19 * A18 * A17 * A16 * /A15 * /A14 * /A13
/O2 = A19 * A18 * A17 * A16 * /A15 * /A14 * A13
/O3 = A19 * A18 * A17 * A16 * /A15 * A14 * /A13
/O4 = A19 * A18 * A17 * A16 * /A15 * /A14 * A13
/O5 = A19 * A18 * A17 * A16 * A15 * /A14 * /A13
/O6 = A19 * A18 * A17 * A16 * A15 * A14 * A13
/O7 = A19 * A18 * A17 * A16 * A15 * /A14 * /A13
/O8 = A19 * A18 * A17 * A16 * A15 * /A14 * A13
```

Decodificador de Memoria (múltiple PLD)