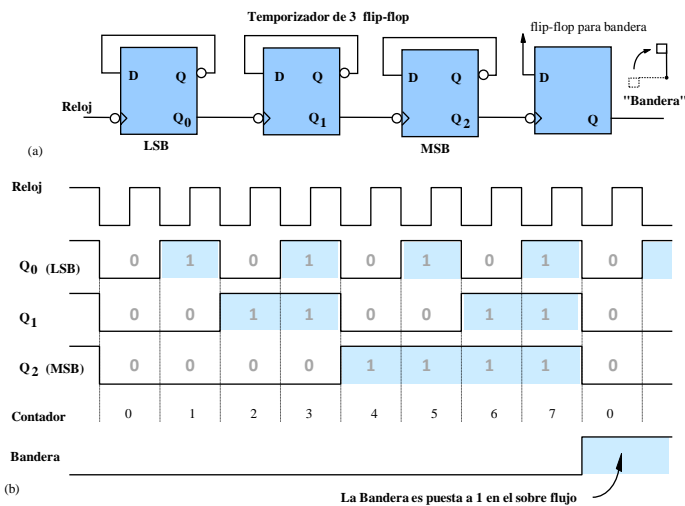



Microcontroladores

Timer0 (AVR)

Temporizador/Contador:





Timer0/Counter0 (8 bits):

- Dos unidades de Output Compare independientes
- Auto-carga (clear timer on compare match)
- Pre-escalador de 10-bits
- Contador de Eventos Externos
- PWM con periodo variable
- Generador de Frecuencia
- Tres fuentes de Interrupción (TOV0, OCF0A y OCF0B)


- 
- ## Timer0/Counter0 (8 bits):
- Dos unidades de Output Compare independientes
 - Auto-carga (clear timer on compare match)
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 - Contador de Eventos Externos
 - PWM con periodo variable
 - Generador de Frecuencia
 - Tres fuentes de Interrupción (TOV0, OCF0A y OCF0B)

Diagrama de bloques de Timer0/Counter0:

The diagram illustrates the internal architecture of the Timer0/Counter0 module. Key components and their interconnections are as follows:

- Control Logic:** Receives external inputs for Count, Clear, and Direction. It outputs clk_{TCn} to the Timer/Counter and clk_{Tn} to the Edge Detector. It also receives TOP and BOTTOM signals from the comparison logic.
- Timer/Counter (TCNTn):** Receives clk_{TCn} and provides a bidirectional connection to the DATA BUS.
- Edge Detector:** Receives clk_{Tn} and provides an input to the Clock Select multiplexer. It also receives a signal from the Prescaler.
- Clock Select:** A multiplexer that selects between the Edge Detector and the Prescaler to provide the clock signal to the Timer/Counter.
- Comparison Logic:** Consists of two comparators (labeled '=') that compare the value in TCNTn with OCRnA and OCRnB. The results are sent to the Control Logic as TOP and BOTTOM signals.
- Fixed TOP Value:** A constant value used in the comparison logic.
- Waveform Generation:** Two blocks that generate waveforms for OCnA and OCnB based on the comparison results and the TOP signal.
- Registers:** OCRnA, OCRnB, TCCRnA, and TCCRnB are all connected to the DATA BUS for configuration and reading.

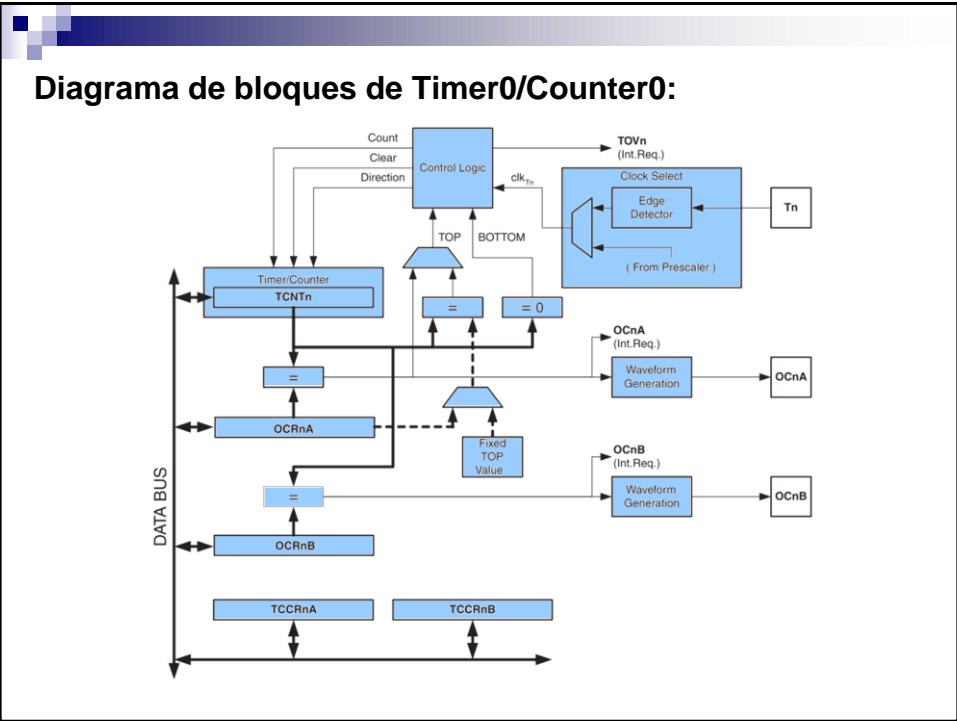


Diagrama de bloques de Timer0/Counter0:

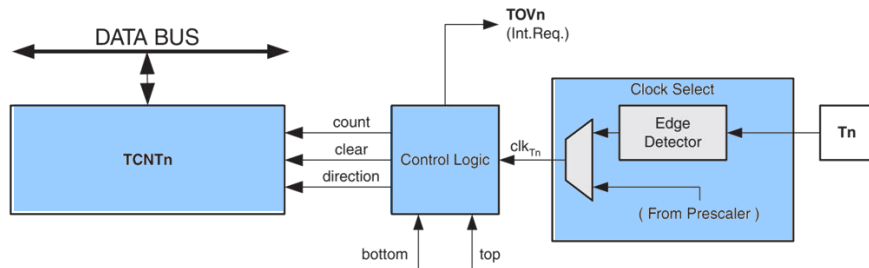


Diagrama de la unidad de comparación:

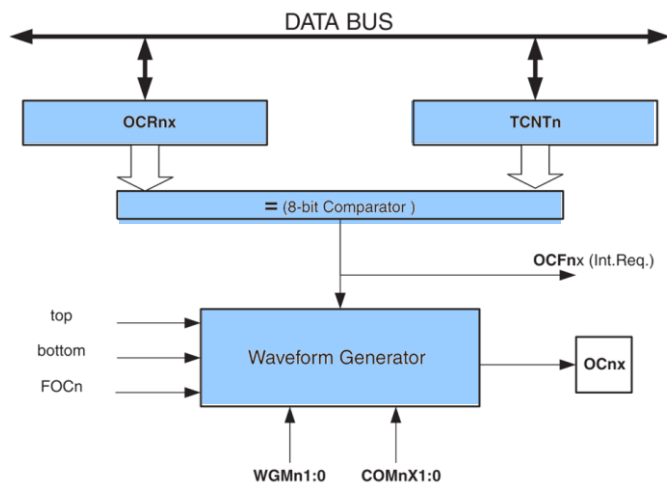


Diagrama de bloques de la salida de unidad de comparación:

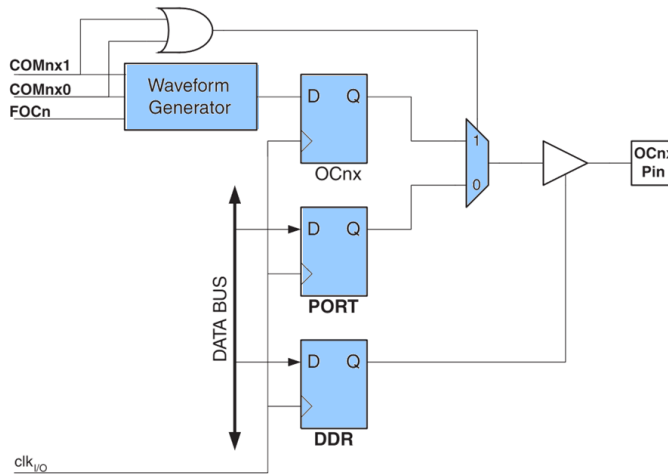


Diagrama de Tiempo (sin pre-escalador)

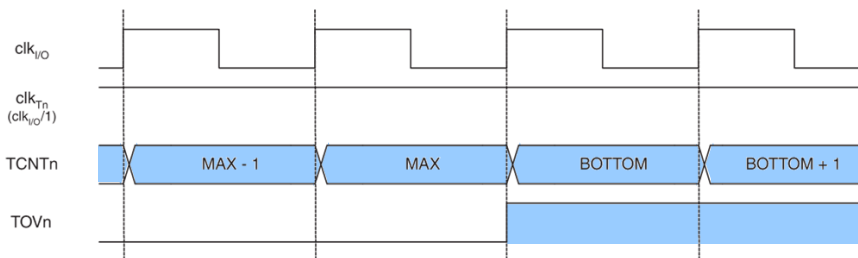


Diagrama de Tiempo (con pre-escalador de 8) Activación de la bandera TOV

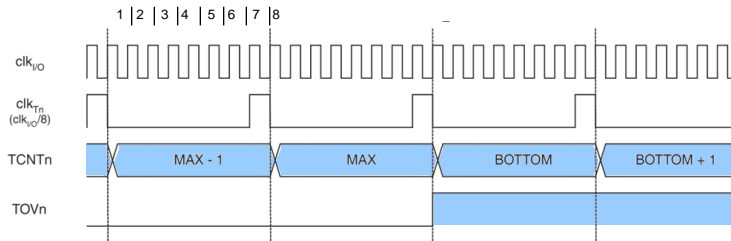


Diagrama de Tiempo (con pre-escalador de 8) Activación de la bandera OCF

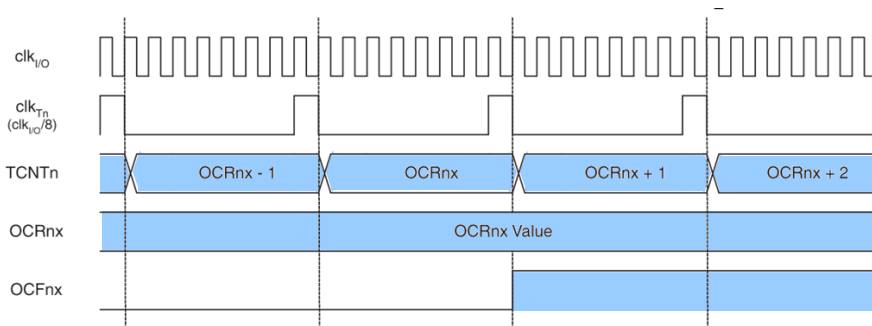
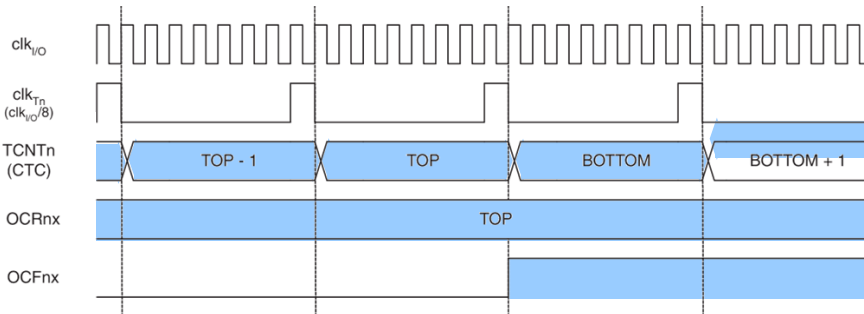


Diagrama de Tiempo (con pre-escalador de 8) Funcionalidad de CTC (Clear Timer on Compare Match mode)



Registros

TCCR0A

Bit	7	6	5	4	3	2	1	0
0x24 (0x44)	COM0A1	COM0A0	COM0B1	COM0B0	—	—	WGM01	WGM00
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- Bits 7:6 – COM0A1:0: Compare Match Output A Mode
- Bits 5:4 – COM0B1:0: Compare Match Output B Mode
- Bits 1:0 – WGM01:0: Waveform Generation Mode

Table 14-8. Waveform Generation Mode Bit Description

Mode	WGM2	WGM1	WGM0	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on ⁽¹⁾⁽²⁾
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	—	—	—
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	—	—	—
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Registros

TCCR0B

Bit	7	6	5	4	3	2	1	0
0x25 (0x45)	FOC0A	FOC0B	—	—	WGM02	CS02	CS01	CS00
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- Bit 7 – FOC0A: Force Output Compare A
- Bit 6 – FOC0B: Force Output Compare B
- Bit 3 – WGM02: Waveform Generation Mode
- Bits 2:0 – CS02:0: Clock Select

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	$\text{clk}_{I/O}$ (No prescaling)
0	1	0	$\text{clk}_{I/O}/8$ (From prescaler)
0	1	1	$\text{clk}_{I/O}/64$ (From prescaler)
1	0	0	$\text{clk}_{I/O}/256$ (From prescaler)
1	0	1	$\text{clk}_{I/O}/1024$ (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

Registros

TCNT0

Bit	7	6	5	4	3	2	1	0
0x26 (0x46)	TCNT0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

OCR0A

Bit	7	6	5	4	3	2	1	0
0x27 (0x47)	OCR0A[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

OCR0B

Bit	7	6	5	4	3	2	1	0
0x28 (0x48)	OCR0B[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Registros

TIMSK0

Bit	7	6	5	4	3	2	1	0
(0x6E)	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

TIFR0

Bit	7	6	5	4	3	2	1	0
0x15 (0x35)	-	-	-	-	-	OCF0B	OCF0A	TOV0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0