Microprocesadores y Microcontroladores

Instrucciones AVR

Instrucciones AVR

- Arithmetic and Logic instructions
- Branch instructions
- Bit and Bit-Test instructions
- Data Transfer instructions
- MCU Control instructions

Arithmetic and Logic instructions

ADD	ADD Rd, Rr	Add two Registers
	ADC Rd, Rr	Add with Carry two Registers
	ADIW Rdl,K	Add Immediate to Word
SUB	SUB Rd, Rr	Subtract two Registers
	SUBI Rd, K	Subtract Constant from Register
	SBC Rd, Rr	Subtract with Carry two Registers
	SBCI Rd, K	Subtract with Carry Constant from Reg.
	SBIW Rdl,K	Subtract Immediate from Word
AND	AND Rd, Rr	Logical AND Registers
	ANDI Rd, K	Logical AND Register and Constant

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Arithmetic and Logic instructions

OR	OR Rd, Rr	Logical OR Registers
	ORI Rd, K	Logical OR Register and Constant
	EOR Rd, Rr	Exclusive OR Registers
	COM Rd	One's Complement
	NEG Rd	Two's Complement
	SBR Rd,K	Set Bit(s) in Register (OR)
	CBR Rd,K	Clear Bit(s) in Register (AND)
	TST Rd	Test for Zero or Minus
	CLR Rd	Clear Register
	SER Rd	Set Register

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Arithmetic and Logic instructions

MUL	MUL Rd, Rr	Multiply Unsigned
	MULS Rd, Rr	Multiply Signed
	MULSU Rd, Rr	Multiply Signed with Unsigned
	FMUL Rd, Rr	Fractional Multiply Unsigned
	FMULS Rd, Rr	Fractional Multiply Signed
	FMULSU Rd, Rr	Fractional Multiply Signed with Unsigned

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Branch instructions

JMPs	RJMP k	Relative Jump	PC ← PC + k + 1
	IJMP	Indirect Jump to (Z)	PC ← Z
	JMP	k Direct Jump	PC ← k
CALLs	RCALL k	Relative Subroutine Call	PC ← PC + k + 1
	ICALL	Indirect Call to (Z)	PC ← Z
	CALL k	Direct Subroutine Call	PC ← k
RETs	RET	Subroutine Return	PC ← STACK
	RETI	Interrupt Return	PC ← STACK

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Branch instructions

CMP	CPSE Rd,Rr	Compare, Skip if Equal
	CP Rd,Rr	Compare
	CPC Rd,Rr	Compare with Carry
	CPI Rd,K	Compare Register with Immediate
Skips	SBRC Rr, b	Skip if Bit in Register Cleared
	SBRS Rr, b	Skip if Bit in Register is Set
	SBIC P, b	Skip if Bit in I/O Register Cleared
	SBIS P, b	Skip if Bit in I/O Register is Set

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Branch instructions

BRANCH	BRBS s, k	Branch if Status Flag Set
	BRBC s, k	Branch if Status Flag Cleared
	BREQ k	Branch if Equal
	BRNE k	Branch if Not Equal
	BRCS k	Branch if Carry Set
	BRCC k	Branch if Carry Cleared
	BRSH k	Branch if Same or Higher
	BRLO k	Branch if Lower
	BRMI k	Branch if Minus
	BRPL k	Branch if Plus
	BRGE k	Branch if Greater or Equal, Signed
	BRLT k	Branch if Less Than Zero, Signed

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Branch instructions

BRANCH

BRHS	k	Branch if Half Carry Flag Set
BRHC	k	Branch if Half Carry Flag Cleared
BRTS	k	Branch if T Flag Set
BRTC	k	Branch if T Flag Cleared
BRVS	k	Branch if Overflow Flag is Set
BRVC	k	Branch if Overflow Flag is Cleared
BRIE	k	Branch if Interrupt Enabled
BRID	k	Branch if Interrupt Disabled

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Bit and Bit-Test instructions

SBI P,b	Set Bit in I/O Register
CBI P,b	Clear Bit in I/O Register
LSL Rd	Logical Shift Left
LSR Rd	Logical Shift Right
ROL Rd	Rotate Left Through Carry
ROR Rd	Rotate Right Through Carry
ASR Rd	Arithmetic Shift Right
SWAP Rd	Swap Nibbles

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Bit and Bit-Test instructions

BSET s	Flag Set
BCLR s	Flag Clear
BST Rr, b	Bit Store from Register to T
BLD Rd, b	Bit load from T to Register
SEC	Set Carry
CLC	Clear Carry
SEN	Set Negative Flag
CLN	Clear Negative Flag
SEZ	Set Zero Flag
CLZ	Clear Zero Flag

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Bit and Bit-Test instructions

SEI	Global Interrupt Enable
CLI	Global Interrupt Disable
SES	Set Signed Test Flag
CLS	Clear Signed Test Flag
SEV	Set Twos Complement Overflow
CLV	Clear Twos Complement Overflow
SET	Set T in SREG
CLT	Clear T in SREG
SEH	Set Half Carry Flag in SREG
CLH	Clear Half Carry Flag in SREG

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Data Transfer instructions

MOVs	MOV Rd, Rr	Move Between Registers
	MOVW Rd, Rr	Copy Register Word

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Data Transfer instructions

LDs	LDI Rd, K	Load Immediate
	LD Rd, X	Load Indirect
	LD Rd, X+	Load Indirect and Post-Inc.
	LD Rd, - X	Load Indirect and Pre-Dec.
	LD Rd, Y	Load Indirect
	LD Rd, Y+	Load Indirect and Post-Inc.
	LD Rd, - Y	Load Indirect and Pre-Dec.
	LDD Rd,Y+q	Load Indirect with Displacement
	LD Rd, Z	Load Indirect
	LD Rd, Z+	Load Indirect and Post-Inc.
	LD Rd, -Z	Load Indirect and Pre-Dec.
	LDD Rd, Z+q	Load Indirect with Displacement
	LDS Rd, k	Load Direct from SRAM

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Data Transfer instructions

STs

ST X, Rr	Store Indirect
ST X+, Rr	Store Indirect and Post-Inc.
ST - X, Rr	Store Indirect and Pre-Dec.
ST Y, Rr	Store Indirect
ST Y+, Rr	Store Indirect and Post-Inc.
ST - Y, Rr	Store Indirect and Pre-Dec.
STD Y+q,Rr	Store Indirect with Displacement
ST Z, Rr	Store Indirect
ST Z+, Rr	Store Indirect and Post-Inc.
ST -Z, Rr	Store Indirect and Pre-Dec.
STD Z+q,Rr	Store Indirect with Displacement
STS k, Rr	Store Direct to SRAM

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Data Transfer instructions

Flash

LPM	Load Program Memory
LPM Rd, Z	Load Program Memory
LPM Rd, Z+	Load Program Memory and Post-Inc
SPM	Store Program Memory

I/O

IN Rd, P	In Port
OUT P, Rr	Out Port

Stack

PUSH Rr	Push Register on Stack
POP Rd	Pop Register from Stack

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MCU Control instructions

MCU	NOP	No Operation
	SLEEP	Sleep
	WDR	Watchdog Reset
	BREAK	Break (For On-chip Debug Only)