ECE 5720 Modeling and Synthesis of Digital Systems Using Verilog

Worcester Polytechnic Institute

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Homework Report 2: – Structural Description of Combinational Components

Submitted by

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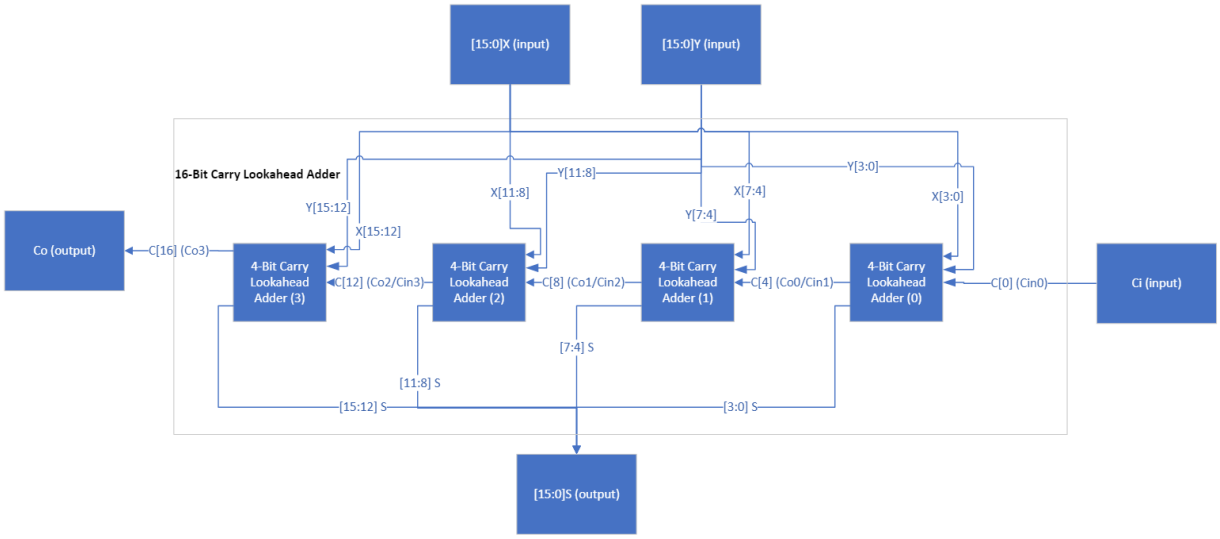
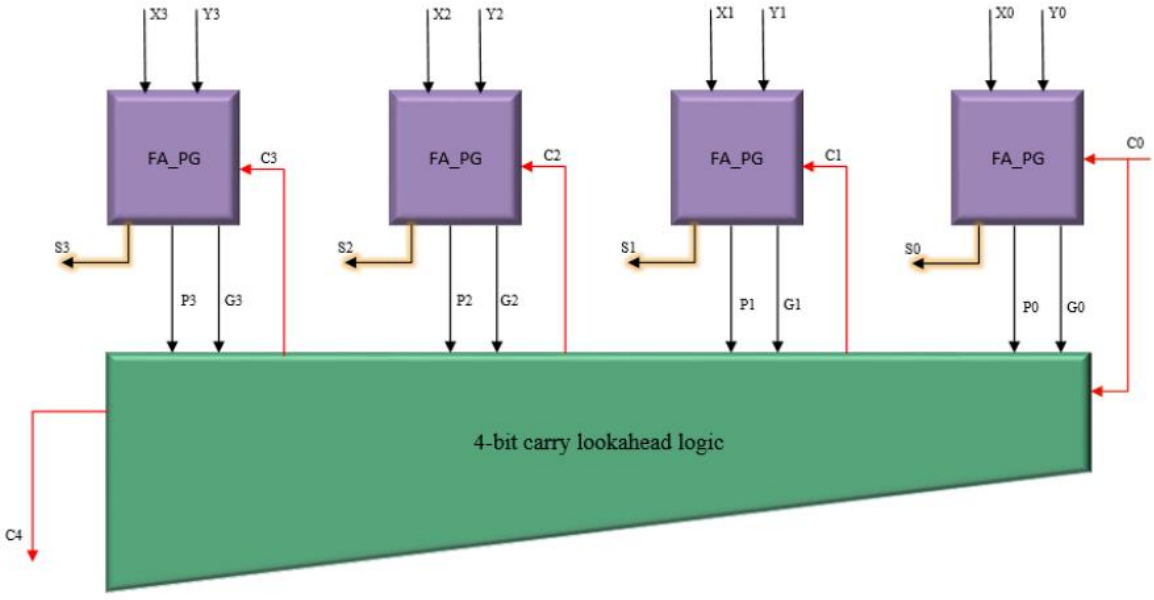
Sixteen-Bit Carry Lookahead Adder Schematic



The sixteen-bit carry lookahead adder was created by chaining together 4 4-bit carry lookahead adders. Just as with single-bit adders, these 4-bit adder modules have a carry in to be used in the addition of its LSB, and a carry out for the LSB of the following adder that is generated by the addition of the MSB's of their X and Y. The schematic of a single 4-bit carry adder module is shown below:

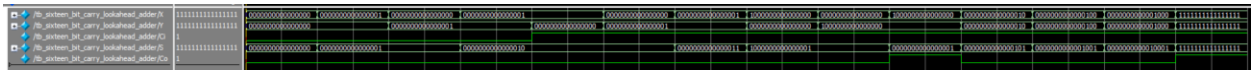


With 4 of these adders chained and the input bits properly distributed over them, a larger, 16-bit adder can be made with the added benefit of the lookahead logic in the 4-bit adders. This lookahead

logic allows for calculations of the output bits to be made in parallel with each other, contrary to normal adders which depend on propagation of the previous bit's adder results before the next can begin. By speeding up calculation within repeatedly generated modules, calculation can be done much faster at a large scale.

For the sixteen-bit adder, the carry out bit Co is the carry out of the MSB (bit 15), and sum of each place value is given on [15:0]S. The carry in bit Ci acts as the carry in value for the LSB place value.

Test Bench Results



To test the 16-bit adder's functionality, a test bench was made using different inputs of X, Y, and Ci. When 1 or 3 of these values is high for a given place value, its sum should be 1. If 2 or 3 of these values is high for a given place value, the carry out should be 1 (only the last carry out is an output, the rest are internal). The truth table below describes the output of S for X, Y, and Ci:

X	Y	Ci	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Given that the test bench outputs follow this table, the test was a success. Notably, Co only becomes a 1 when there is a carry out in the MSB, and not under any other conditions. The LSB was tested with Ci = 0 and Ci = 1 and performed within expectation.