DSD_HW2_Report

R13921072 何家祥

在 postsim 過後，要進行模擬時，雖然能通過 TB 的 pattern，但會出現 SDF error，因此模擬時的指令我是下 vcs RISCV_tb.v +define+SYN -full64 -R -debug_access+all +v2k +neg_tchk

也有修改.tcl 中的編譯方式，compile_ultra -no_autoungroup 使其能壓縮到更小面積的同時，該有模組名稱部會消失，可以讓 TB 驗證的時候提取。

ScreenShot of NOT latch :

```
Inferred memory devices in process
        in routine core line 167 in file
                '/home/raid7_2/user13/r3921072/DSD/hw2/verilog/core.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|   mem_addr_I_reg    | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```

```
Inferred memory devices in process
        in routine Register line 270 in file
                '/home/raid7_2/user13/r3921072/DSD/hw2/verilog/core.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|    registers_reg    | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```

```
Inferred memory devices in process
        in routine memory line 28 in file
                '/home/raid7_2/user13/r3921072/DSD/hw2/verilog/memory.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
|       mem_reg       | Flip-flop | 1024  |  Y  | N  | N  | N  | N  | N  | N  |
=================================================================================
```

ScreenShot of area :

```
Number of ports:                          532
Number of nets:                         10080
Number of cells:                         9535
Number of combinational cells:           6451
Number of sequential cells:              3073
Number of macros/black boxes:               0
Number of buf/inv:                       1905
Number of references:                       3

Combinational area:              72509.533382
Buf/Inv area:                    12676.183242
Noncombinational area:           32885.428080
Macro/Black Box area:                0.000000
Net Interconnect area:         1847264.121918

Total cell area:                105394.961462
Total area:                    1952659.083380
```

Performance :
area : 105394.961462
TB cycle time : 2.44
A*T : 257163.7