



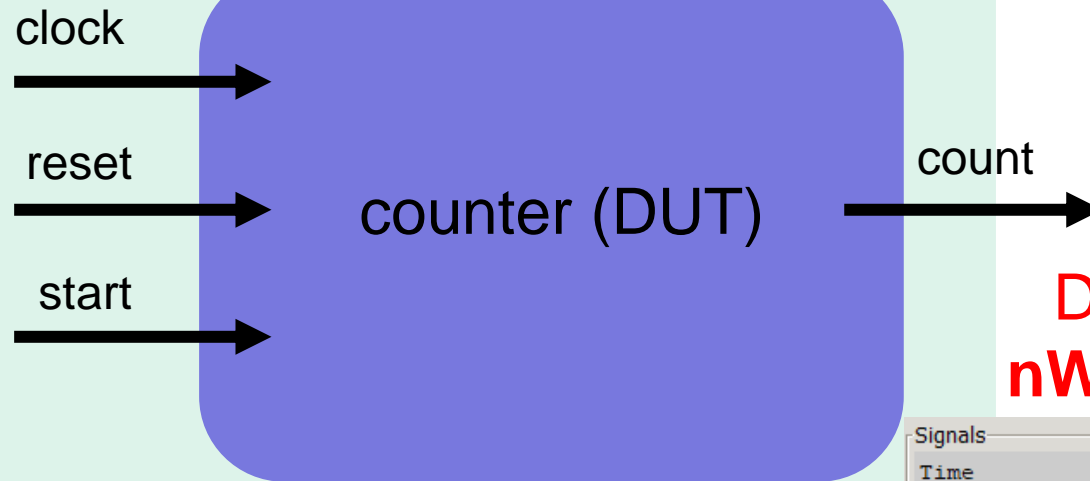
Verilog Debugging Tool - nWave

Speaker: 王景平



How to Debug

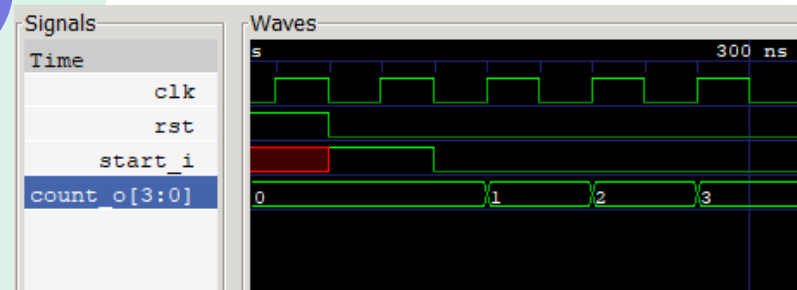
counter_tb (Testbench, tb)



Display in cmd

```
count = 0
count = 1
count = 2
count = 3
count = 4
count = 5
count = 6
count = 7
count = 8
```

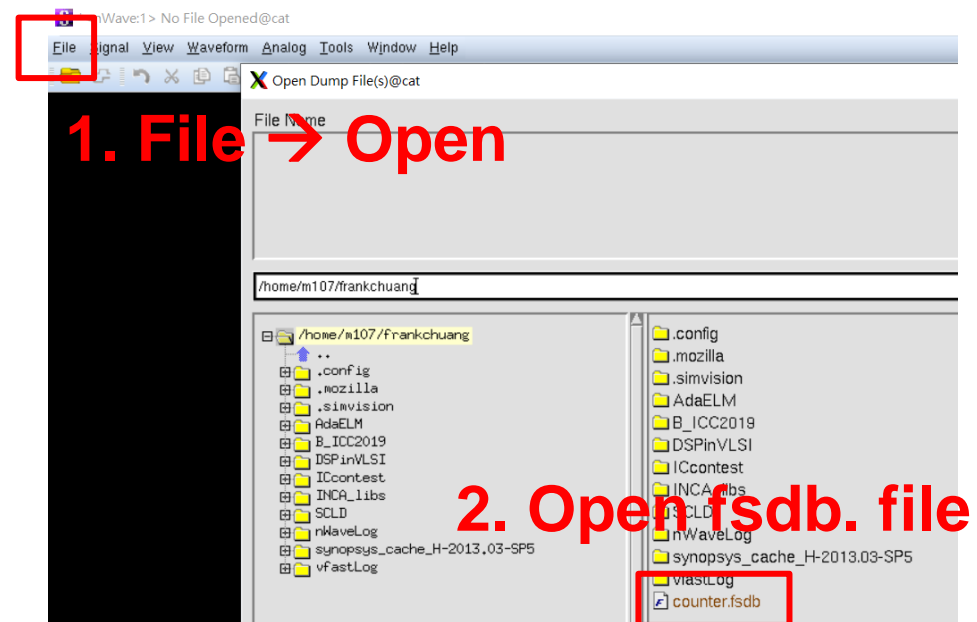
Display waveform in
nWave (most common)





nWave

- ❖ A waveform analysis tool for viewing **.fsdb* & **.vcd* waveform files
- ❖ **For school workstation, source license first**
 - ❖ `source /usr/cad/cadence/cshrc`
 - ❖ `source /usr/spring_soft/CIC/verdi.cshrc`
- ❖ **Invoke nWave**
 - ❖ `> nWave &`
- ❖ **Open waveform file**
 - ❖ `.fsdb` or `.vcd`





Select Signals to View

1

2

3

Signal Name	Signal Value
X[7:0]	reg_B[7:0]
alu_out[7:0]	reg_ins[3:0]
clk	reset
inputA[7:0]	sum[7:0]
inputB[7:0]	LOGIC_LOV
inputB_inv[7:0]	LOGIC_HIGH
instruction[3:0]	BLANK

4

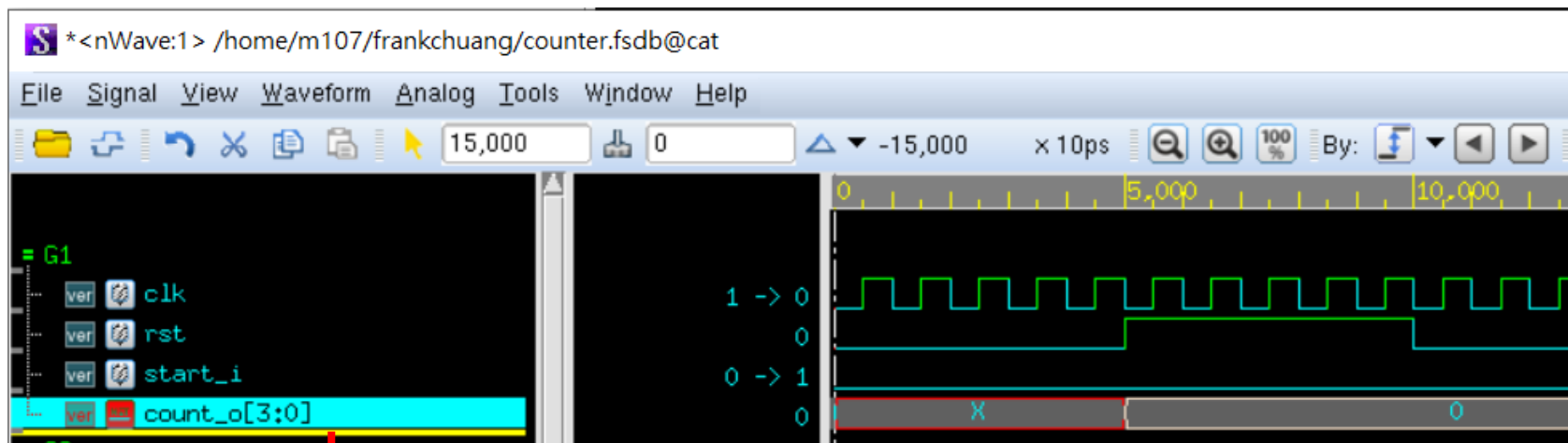
5

6

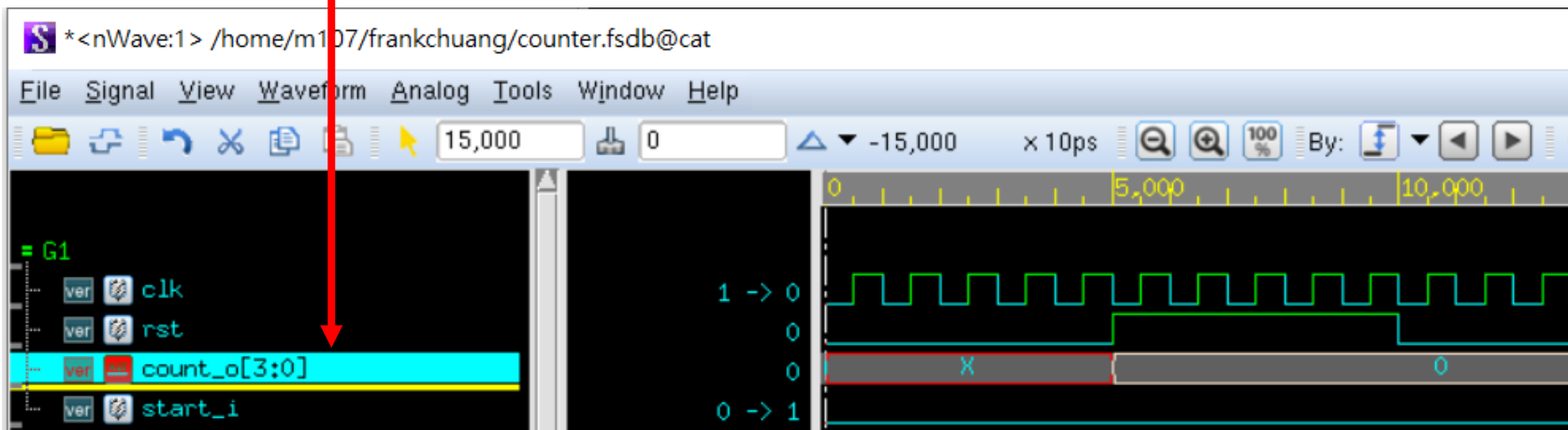
Signal Name	Signal Value
clk	reset
inputA[7:0]	sum[7:0]
inputB[7:0]	LOGIC_LOV
inputB_inv[7:0]	LOGIC_HIGH
instruction[3:0]	BLANK



Drag Selected Signals

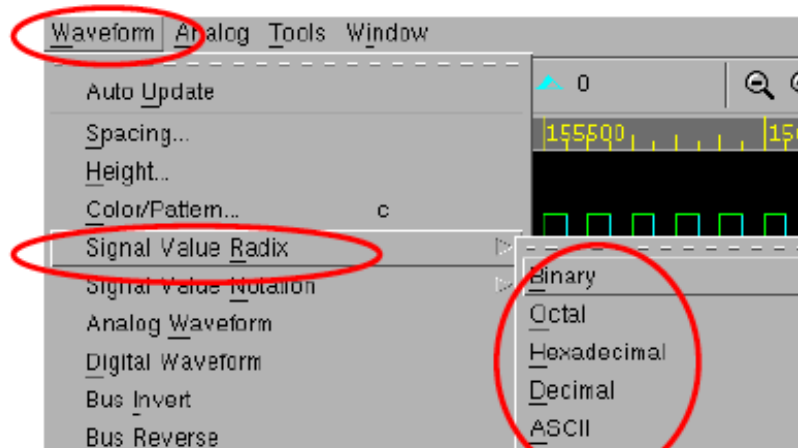
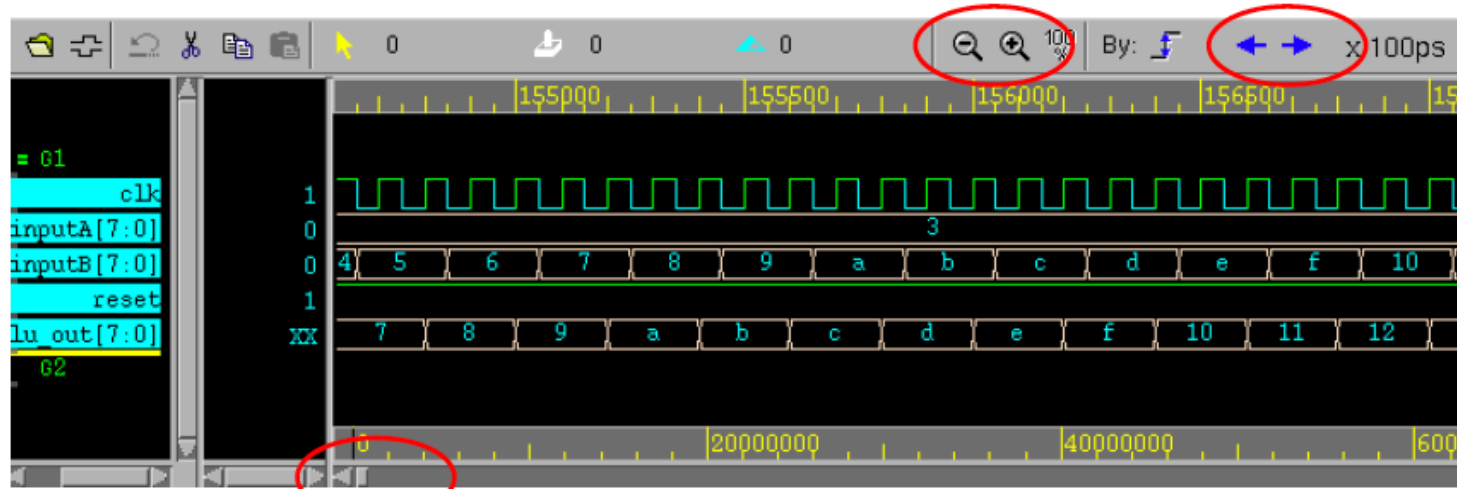


按住滑鼠中間滾輪拖移

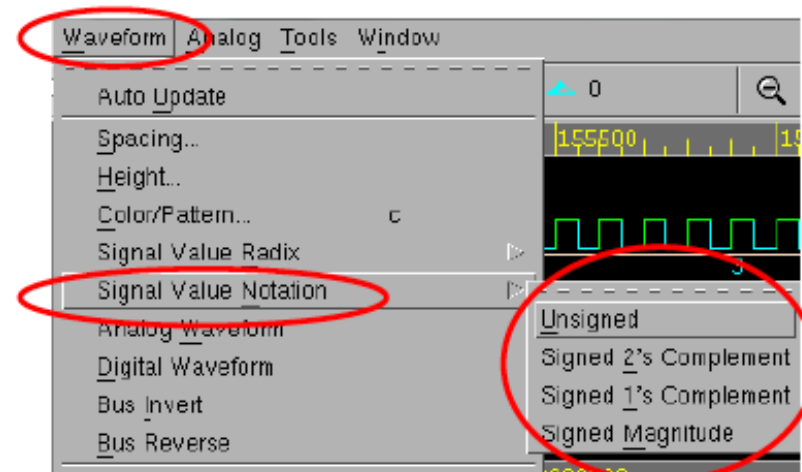




Shift windows Viewing Tools



Select Value Radix

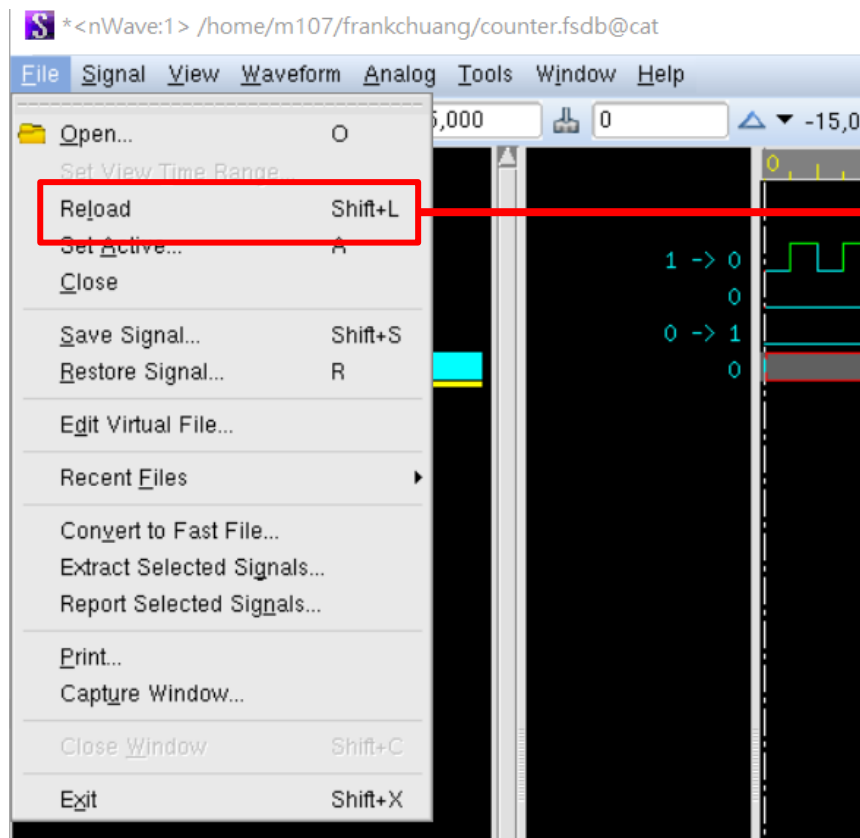


Select Value Notation



Reload New Waveform File (Shift+L)

- ❖ You don't need to re-open nWave to reload a new waveform file! → **Shift+L**



Shift+L