scientific reports

Check for updates

OPEN

A new positive output DC–DC buck–boost converter based on modified boost and ZETA converters

Majid Hosseinpour[1]✉, Milad Heydarvand[1] & Mahmoodreza Eskandarpour Azizkandi[2]

A new DC–DC buck–boost converter with a wide conversion ratio is presented in this paper. The proposed buck–boost converter consists of a combination of modified boost converter and ZETA converter, which has the advantages of both converters such as continuous input/output current and positive polarity of the output voltage. The combination of these two converters achieves semi-quadratic voltage gain and makes the proposed converter suitable for industrial and renewable energy applications. With a voltage gain higher than that of the ZETA converter and modified boost converter, the proposed converter also reduces input current stress due to its continuity. Two operating states are available for this converter in continuous conduction mode. This converter has two switches that operate simultaneously and can be easily controlled. The converter's output voltage ripple and output capacitor current stress are reduced as a result of continuous output current. Computational analysis and the introduced structure efficiency considering the influence of parasitic elements are presented in this paper. The small signal modelling and closed-loop control, as well as simulation and experimental results are also presented. This converter has also been compared with other similar and recently presented topologies. Finally, a 40–60 W, 20–76 V for boost mode and 10 V for buck mode prototype was implemented to verify the accuracy of the computational analysis.

Keywords Buck–boost converter, ZETA converter, Non-inverting, Voltage gain, Voltage and current stress

Climate change, global warming, and pollution from fossil fuels have made renewable energy sources like fuel cells, solar panels, and wind energy more appealing over recent decades [1]. Renewable energies are environmentally-friendly and have become competitive due to the increasing development of power electronics and can meet load demand using power electronic converters, especially DC–DC converters [2]. Many applications use DC–DC converters such as grid connections, light emitting diodes (LED), battery power systems, uninterrupted power supplies (UPS), and household appliances [3].

DC–DC converters are the main pillars of renewable energy equipment and are used to adjust their voltage and deliver to the DC-AC inverter and the grid [4]. These converters can be classified into isolated and non-isolated categories [5]. Despite the high voltage gain and low voltage stress on the switches, isolated converters have disadvantages such as high voltage spikes due to the transformer leakage inductance, large circuit volume and high manufacturing costs [6]. Several solutions exist to solve the spike problem, such as active or passive clamps. However, they complicate the circuit, as well as the way it is controlled [7]. In contrast, non-isolated converters are more commonly used because of their simple structure, small circuit volume, and low manufacturing costs [8]. The buck–boost converter is one of the non-isolated converters that can operate in a wide voltage conversion range and increase and decrease the input voltage [9]. SEPIC, ZETA, and CUK converters are conventional buck–boost converters [10]. Even though these converters have the advantages mentioned above, they also have drawbacks, such as discontinuous input current (conventional buck–boost and ZETA converters), negative output voltage polarity (conventional buck–boost and CUK converters), elevated voltage levels on switches, and reduced operational efficacy that limit their applications [11].

In order to surmount the limitations of traditional converters, various improved buck–boost structures have been proposed in recent years. References [12–15] present buck–boost converters with continuous input current and positive output voltage polarity, which are suitable for industrial applications and renewable energies, but do not

[1]Department of Electrical Engineering, University of Mohaghegh Ardabili, Ardabil, Iran. [2]Department of Electrical and Computer Engineering, NC State University, Raleigh, NC, USA. ✉email: hoseinpour.majid@uma.ac.ir

provide continuous output current. Reference [12] presents a semi-quadratic converter with a high voltage gain. Despite this, the control method of this converter is complex, and it has a large number of elements. Based on an active switched network, the converter presented in [13] has high voltage gain and low voltage stress on the switches and the diode. A single-switch buck–boost converter based on the SEPIC converter is presented in [14], which is easy to control due to its single-switch. Even though this converter has a large number of elements, the voltage gain is low. In reference [15], a converter based on SEPIC is presented, which the voltage stress of its switches is low.

The converters presented in [16–18] have continuous input and output currents and positive output voltage polarity. A converter with a quadratic voltage conversion ratio which is presented in [16] has a small number of elements, but a low voltage gain, and a relatively high voltage stress on the switches. The voltage strain experienced by the switch and diodes in the converter outlined in reference [18] exceeds that of the output voltage. In reference [19], an additional buck–boost converter exhibiting a broad conversion ratio and continuous input current is presented, suitable for industrial and renewable energy applications. However, the output voltage polarity of this converter is negative, and the output current exhibits intermittent behavior. In [20] and [21], buck–boost converters are presented with continuous output current and positive output voltage polarity. However, their input current is discontinuous. The converter presented in [20] is a single-switch buck–boost converter based on the ZETA converter, and its voltage conversion ratio is twice that of the ZETA converter. However, output voltage changes are not wide. In [21], another quadratic buck–boost converter is presented, which covers a wide range of conversion ratio.

A continuous input and output current converter is presented in [22] with a wide range of voltage conversion. However, the output voltage polarity of this converter is negative. The converters presented in [23] and [24] have positive output voltage polarity. Nevertheless, their input and output currents are discontinuous. The converter presented in [23] is a buck–boost converter using a quasi-Z impedance network, which has a higher conversion ratio and a lower duty cycle than the conventional buck–boost converter, which leads to increased efficiency. However, owing to the elevated gradient of the voltage gain curve, it is difficult to adjust the converter's voltage and control. In [24], a quadratic buck–boost converter is designed with fewer elements and consists of a pair of L-C networks and two switches that turn ON/OFF simultaneously. In reference [25], a buck–boost converter with discontinuous input/output current and negative output voltage polarity is presented. This converter is a semi-quadratic converter with a wide conversion ratio that uses a voltage multiplier cell (VMC) on the input side to increase the output voltage.

To overcome the aforementioned disadvantages of buck–boost converters, this paper presents a semi-quadratic buck–boost converter based on modified boost converter and ZETA converter, which has advantages such as continuous input and output currents and positive polarity of output voltage. Due to its semi-quadratic voltage gain, the introduced structure has a wide range of conversion ratio, and its simultaneous operation of the power switches makes its control easy. Also, the proposed converter has high efficiency and due to the importance of efficiency in its operation, the operation cost is also reduced and it is economical in terms of cost–benefit.

The rest of the paper is organized as follows. The structure of the proposed converter and the operation modes, CCM and DCM (Discontinuous Conduction Mode), are presented in section "Proposed converter and steady state analysis". Section "Proposed converter and steady state analysis" also describes the design parameters, as well as calculations of real voltage gain and efficiency considering the influence of parasitic parameters for converter performance. The comparison between the proposed converter and other similar converters is presented in section "Comparison of the proposed converter with similar converter", the small signal modeling of the proposed converter is presented in section "Small signal modeling of the proposed converter", the simulation and experimental results to verify the computational analysis are presented in section "Simulation and experimental results", and finally, the conclusion is presented in section "Conclusion".

Proposed converter and steady state analysis

The proposed buck–boost converter is shown in Fig. 1. This converter includes two switches (S_1, S_2), three diodes (D_1, D_2, D_3), three inductors (L_1, L_2, L_3), four capacitors (C_1, C_2, C_3, C_o) and a load (R_o) to achieve the high voltage gain. The switches of this converter are turned ON/OFF simultaneously. As seen in Fig. 1, this converter does not have common ground feature. Therefore, instead of being used in photovoltaics, this structure is used in cases such as switched-mode power supplies, batteries, portable electronic devices, and electric vehicles.

Due to the presence of inductors L_1 and L_3 at the input and output ports of the proposed converter, the input and output current are continuous. The operational states of the converter in continuous conduction mode

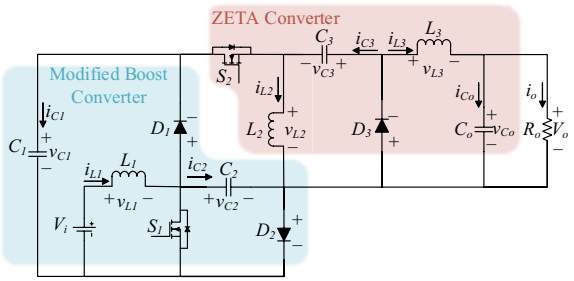


Fig. 1. The proposed buck–boost converter.

(CCM) are depicted in Fig. 2. The subsequent assumptions have been applied for simplifying the steady-state analysis.

1. The circuit Semiconductor elements such as switches and diodes are ideal.
2. The capacitors possess ample capacitance to maintain a constant voltage.
3. The input inductor is regarded as sufficiently large, resulting in the neglect of its current ripple.

The introduced topology key waveforms, which have the power switches gate pulses (V_{GS1}, $_{GS2}$), the inductors current (i_{L1}, i_{L2}, i_{L3}) and the capacitors current (i_{C1}, i_{C2}, i_{C3}, i_{Co}), are shown in Fig. 3. The operating states are also described below.

State1 [t_0, t_1]: During this mode, the power switches S_1 and S_2 are ON, and the diodes D_1, D_2, and D_3 are reverse biased. It can be seen from Fig. 2a that inductor L_1 is charged by the input source, and inductor L_2 is charged by capacitors C_1 and C_2. Additionally, the capacitors C_1, C_2, C_3, and C_o discharge within the inductor L_3 and the load R_o. The voltage across the inductors and the current through the capacitors are provided in Eqs. (1) and (2).

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_i \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = v_{C1} + v_{C2} \\ v_{L3} = L_3 \dfrac{di_{L3}}{dt} = v_{C1} + v_{C2} + v_{C3} - V_o \end{cases} \tag{1}$$

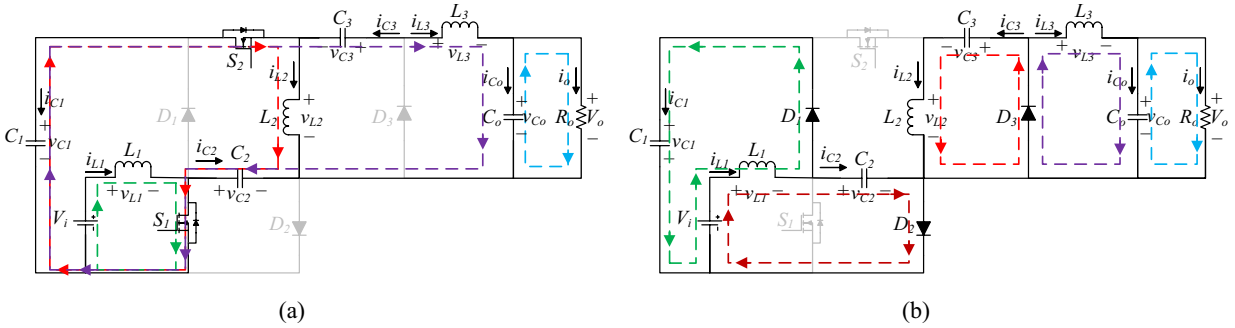


Fig. 2. Operation modes of the suggested converter: (**a**) state 1; (**b**) state 2.

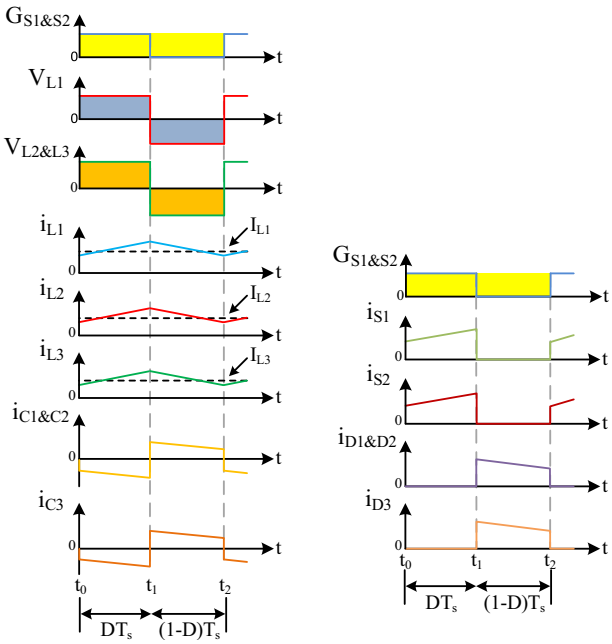


Fig. 3. Introduced converter key waveforms.

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -i_{L2} - i_{L3} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = -i_{L2} - i_{L3} \\ i_{C3} = C_3 \dfrac{dv_{C3}}{dt} = -i_{L3} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = i_{L3} - i_o \end{cases} \tag{2}$$

State2 [t_1, t_2]: As a result of this time interval, both main switches are OFF, and D_1, D_2 and D_3 are forward-biased. According to Fig. 2b, the capacitors C_1 and C_2 are charged by both the input source and the inductor L_1 through diodes D_1 and D_2, respectively. The energy accumulated in the inductor L_2 charges the capacitor C_3 through the diode D_3. Meanwhile, the inductor L_3 provides energy to both the capacitor C_o and the output load R_o. Furthermore, C_1 and C_2 have the same voltage. The voltage of the inductors and the current of the capacitors in this case are as follows.

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_i - v_{C1} \\ v_{L2} = L_2 \dfrac{di_{L2}}{dt} = -v_{C3} \\ v_{L3} = L_3 \dfrac{di_{L3}}{dt} = -V_o \\ v_{C1} = v_{C2} \end{cases} \tag{3}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = \dfrac{i_{L1}}{2} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = \dfrac{i_{L1}}{2} \\ i_{C3} = C_3 \dfrac{dv_{C3}}{dt} = i_{L2} \\ i_{Co} = C_o \dfrac{dv_{Co}}{dt} = i_{L3} - i_o \end{cases} \tag{4}$$

Ideal voltage gain

In this section, to determine the steady-state voltage gain, the volt-second balance principle is used for inductors L_1, L_2 and L_3 in a switching period. According to the volt-second balance, the average inductor voltage in a switching period under steady-state conditions should be zero.

By applying the volt-second balance principle on the inductors L_1, L_2 and L_3 in a switching period, the following results are obtained:

$$L_1: DV_i + (1-D)(V_i - v_{C1}) = 0 \tag{5}$$

$$L_2: D(v_{C1} + v_{C2}) + (1-D)(-v_{C3}) = 0 \tag{6}$$

$$L_3: D(v_{C1} + v_{C2} + v_{C3} - V_o) + (1-D)(-V_o) = 0 \tag{7}$$

By using the Eqs. (3) and (5), the voltage of capacitors C_1 and C_2 can be obtained as follows:

$$v_{C1} = v_{C2} = \frac{V_i}{1-D} \tag{8}$$

In addition, the voltage of capacitor C_3 can be calculated using the relations (6) and (8) as follows:

$$v_{C3} = \frac{2DV_i}{(1-D)^2} \tag{9}$$

By using the Eqs. (6) and (7), it is obtained:

$$v_{C3} = V_o \tag{10}$$

From (9) and (10), the output voltage is obtained as follows:

$$V_o = \frac{2DV_i}{(1-D)^2} \tag{11}$$

As a result, the voltage conversion ratio of the proposed converter is calculated as follows:

$$M_{ideal} = \frac{V_o}{V_i} = \frac{2D}{(1-D)^2} \tag{12}$$

The proposed converter functions in the boost mode when D exceeds 0.268, while it operates in the buck mode for D values less than 0.268. The border between the buck and boost modes is shown in Fig. 4.

DCM operation mode

Discontinuous Conduction Mode (DCM) has three modes. Modes 1 and 2 of DCM are similar to those of CCM. During the third mode, all switches and diodes are deactivated. Consequently, the voltage across the inductors is rendered to zero. The equivalent circuit representing the third mode of the DCM is illustrated in Fig. 5a. Furthermore, the waveforms depicting DCM operation modes are displayed in Fig. 5b. The mean current across the inductors equates to the mean current flowing through the diodes and the average output current.

In the Continuous Conduction Mode (CCM), the average current of the inductors must surpass half of the current ripple across the inductors ($I_L > 1/2\Delta i_L$). To achieve a standard inductor, the time constant $\tau_{L1,2,3}$ is defined as $\tau_{L1,2,3} = L_{1,2,3f.}/R$. Accordingly, inductors L_1, L_2 and L_3 have the boundary conditions presented in Eq. (13).

$$\begin{cases} \tau_{L1B} = \dfrac{(1-D)^4}{8D} \\ \tau_{L2B} = \dfrac{(1-D)^2}{2D} \\ \tau_{L3B} = \dfrac{1-D}{2} \\ \tau_{LtotalB} = \dfrac{(1-D)^4 + 4(1-D)^2 + 4D(1-D)}{8D} \end{cases} \tag{13}$$

According to Eq. (13), the correlation between the time constant τ_L being greater than τ_{LB} and the duty cycle D is depicted in Fig. 6 ($\tau_L > \tau_{LB}$). This implies that if τ_L surpasses τ_{LB}, the circuit operates in CCM; otherwise, it operates in DCM.

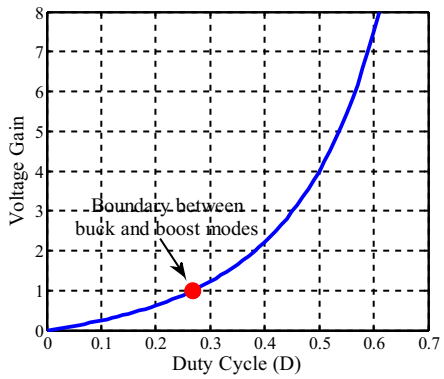
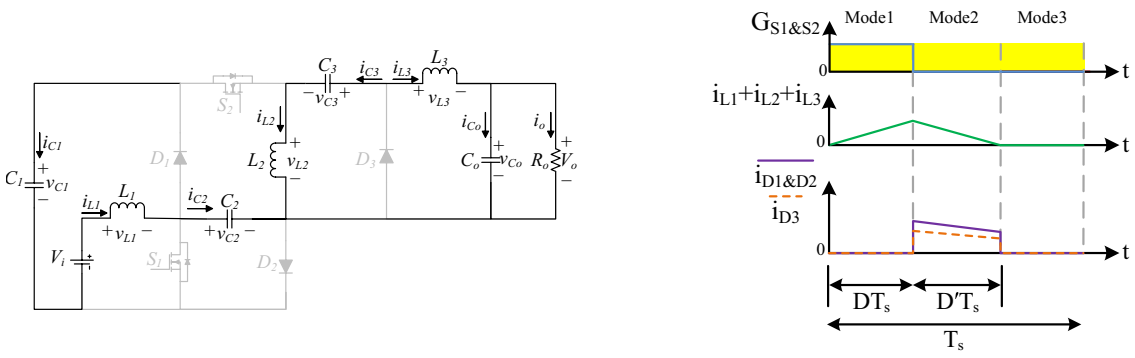


Fig. 4. The border between the buck and boost modes.



(a) (b)

Fig. 5. DCM operation mode: (**a**) equivalent circuit of the third mode of DCM; (**b**) operation waveforms for DCM.

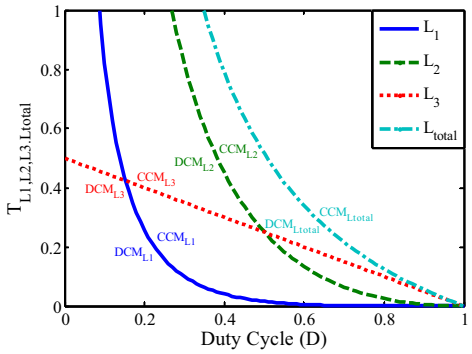


Fig. 6. Boundary conditions for the proposed converter.

Parameters design

Inductors design

During the on-state of the switches S_1 and S_2, the inductors' current increases linearly. It is assumed that the ripples in the inductor current of the proposed converter are equal to 40% of its average current. Equation (1) indicates that inductors L_1, L_2 and L_3 are in the following ranges based on the voltage relation of capacitors.

$$\begin{cases} L_1 \geq \dfrac{5(1-D)^4 V_o}{8Df_sI_o} \\ L_2 \geq \dfrac{5(1-D)^2 V_o}{2Df_sI_o} \\ L_3 \geq \dfrac{5(1-D)V_o}{2f_sI_o} \end{cases} \tag{14}$$

Inductors design

It is necessary to calculate the average current of the capacitors before designing the amount of capacitors. By applying the ampere-second balance principle on the C_1, C_2, C_3 and C_o capacitors and applying relations (2) and (4), the inductors average current is obtained as follows.

$$\begin{cases} I_{L1} = \dfrac{2DI_o}{(1-D)^2} \\ I_{L2} = \dfrac{DI_o}{1-D} \\ I_{L3} = I_o \end{cases} \tag{15}$$

By considering the permissible voltage ripple of 1% and combining Eq. (4) with the average current relations of the inductors, the range of the capacitors can be determined as follows. {#R11}

$$\begin{cases} C_1 = C_2 \geq \dfrac{2D^2}{1\%(1-D)^2R_of_s} \\ C_3 \geq \dfrac{D}{1\%R_of_s} \\ C_o \geq \dfrac{D}{1\%R_of_s} \end{cases} \tag{16}$$

Voltage/current stress of power switches and diodes

According to Fig. 2 and using Eqs. (8) and (9), the formula (17) provides the expression for calculating the voltage stress experienced by the switches and diodes in the suggested converter.

$$\begin{cases} V_{S1} = \dfrac{1}{(1-D)} V_i \\ V_{S2} = \dfrac{1+D}{(1-D)^2} V_i \\ V_{D1} = V_{D2} = \dfrac{1}{(1-D)} V_i \\ V_{D3} = \dfrac{2}{(1-D)^2} V_i \end{cases} \tag{17}$$

Also, the current stress of the switches and diodes according to Fig. 2 and using Eq. (15), is as follows:

$$\begin{cases} I_{S1,avg} = \dfrac{D(1+D)}{(1-D)^2} I_o \\ I_{S2,avg} = \dfrac{D}{(1-D)} I_o \\ I_{D1,avg} = I_{D2,avg} = \dfrac{D}{(1-D)} I_o \\ I_{D3,avg} = I_o \end{cases} \tag{18}$$

Real voltage gain and efficiency with parasitic parameters

This section analyzes the effect of parasitic parameters on output voltage and efficiency. Figure 7 depicts the circuit diagram of the proposed converter, accounting for the impact of parasitic parameters. The equivalent series resistances (ESR) of the inductors and capacitors are denoted as r_L and r_C, respectively. The on-state resistance of the switches and the internal resistance of the diodes are r_S and r_D, respectively, and V_D is the forward voltage drop of the diodes.

Real voltage gain

In practical conditions, the operational states of the proposed structure closely mirror its operation modes in CCM, taking into account the impact of parasitic parameters. Parasitic parameters include the on-state resistance of switches (r_S) equal to 0.05 Ω, internal resistance of diodes (r_D) equal to 0.15 Ω, capacitors and inductors *ESR* (r_C, r_L) equal to 0.02 Ω and 0.05 Ω, respectively, and the forward voltage drop (V_D) is equal to 0.6 V. The voltage of the inductors in the time interval of DT_s is as follows.

$$v_{L1} = V_i - r_L i_{L1} - r_S(i_{L1} + i_{L2} + i_{L3}) \tag{19}$$

$$v_{L2} = v_{C1} + v_{C2} - r_L i_{L2} - r_S(i_{L2} + i_{L3}) - r_C(i_{L2} + i_{L3}) - r_S(i_{L1} + i_{L2} + i_{L3}) - r_C(i_{L2} + i_{L3}) \tag{20}$$

$$v_{L3} = v_{C1} + v_{C2} + v_{C3} - V_o - (r_L + r_C) i_{L3} - r_S(i_{L2} + i_{L3}) - r_C(i_{L2} + i_{L3}) - r_S(i_{L1} + i_{L2} + i_{L3}) - r_C(i_{L2} + i_{L3}) \tag{21}$$

Similarly, in the (1-D)T_s time interval, the inductors' voltage is obtained as follows.

$$v_{L1} = V_i - v_{C1} - V_D - r_L i_{L1} - (r_C + r_D) i_{L1}/2 \tag{22}$$

$$v_{L2} = -v_{C3} - V_D - (r_L + r_C) i_{L2} - r_D(i_{L2} + i_{L3}) \tag{23}$$

$$v_{L3} = -V_o - V_D - r_L i_{L3} - r_D(i_{L2} + i_{L3}) \tag{24}$$

From Eq. (15) and Eqs. (19)–(24), the real voltage gain is obtained as follows:

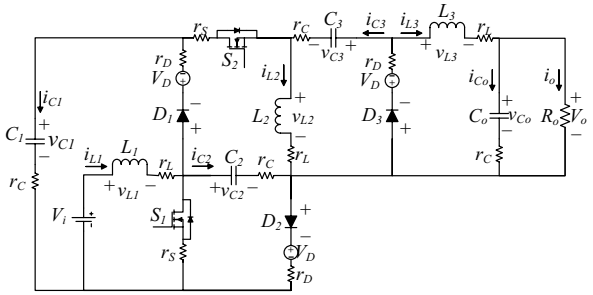


Fig. 7. The proposed buck–boost converter circuit with parasitic parameters.

$$G_{real} = \frac{G_{ideal} - \frac{1-D^2}{(1-D)^2}\left(\frac{V_D}{V_i}\right)}{1 + \frac{1}{R_o}(M_1 + M_2 + M_3 + M_4)} \tag{25}$$

The values of M_1, M_2, M_3 and M_4 are also presented as follows:

$$\begin{cases} M_1 = \dfrac{2D^3 + 2D}{(1-D)^4} r_S \\ M_2 = \dfrac{2D^4 - 6D^3 + 11D^2 - 4D + 1}{(1-D)^4} r_L \\ M_3 = \dfrac{D^3 - 2D^2 + 3D}{(1-D)^3} r_C \\ M_4 = \dfrac{3D^2 - 2D + 1}{(1-D)^3} r_D \end{cases} \tag{26}$$

The graphs of real voltage gain of the proposed converter versus duty cycle are presented in Fig. 8. As can be seen in Fig. 8, the real voltage gain varies with the r_L/R_o ratio. In this case, increasing r_L/R_o leads to a decrease in the real voltage gain.

Efficiency

In this section, efficiency calculations are analyzed based on the power losses of the proposed converter. The power losses include the power losses of the switches, diodes, inductors and capacitors. Switch losses are partitioned into two components: switching losses and conduction losses, elucidated as follows:

$$P_{Loss}^{Switch} = P_{Conduction}^{Switch} + P_{Switching}^{Switch} \tag{27}$$

$$\begin{cases} P_{Conduction}^{Switch} = R_{DS-on} I_{Switch,rms}^2 \\ P_{Switching}^{Switch} = \dfrac{1}{2} V_{DS-on} I_{Switch,avg} (t_r + t_f) f_s \end{cases} \tag{28}$$

where $R_{DS\text{-}on}$ is the on-state resistance of the switch, $I_{Switch,rms}$ is the root mean square (*RMS*) of the current passing through the switch, V_{DS} is the constant voltage of the switch, $I_{Switch,avg}$ is the average current passing through the switch, (t_r,t_f) are the rise and fall times of the switches respectively, and f_s is the switching frequency. The *RMS* values of switch currents are calculated as follows:

$$I_{S1,rms} = \sqrt{\frac{\int_0^{DT_s} (i_{L1} + i_{L2} + i_{L3})^2 dt}{T_s}} = \frac{\sqrt{D}(1+D)}{(1-D)^2} I_o \tag{29}$$

$$I_{S2,rms} = \sqrt{\frac{\int_0^{DT_s} (i_{L2} + i_{L3})^2 dt}{T_s}} = \frac{\sqrt{D}}{(1-D)} I_o \tag{30}$$

The converter diode losses can be expressed according to the following equation.

$$P_{Loss}^{Diode} = r_D I_{D,rms}^2 + V_D I_{D,avg} \tag{31}$$

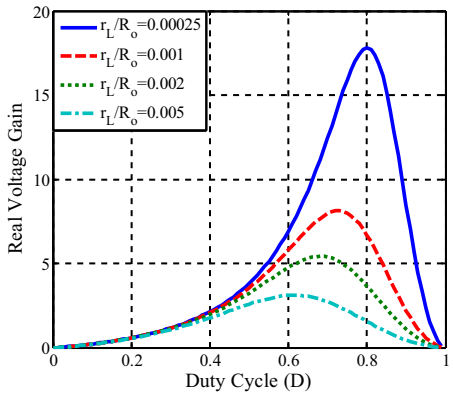


Fig. 8. Real voltage gain considering parasitic parameters.

Here, r_D represents the internal resistance of the diode, $I_{D,rms}$ signifies the *RMS* value of the current flowing through the diode, V_D denotes the forward voltage drop of the diode, and $I_{D,avg}$ represents the average current traversing the diode. The *RMS* values of diode currents are obtained as follows:

$$I_{D1,rms} = I_{D2,rms} = \sqrt{\frac{\int_{DT_s}^{T_s} (\frac{1}{2} i_{L1})^2 dt}{T_s}} = \frac{D}{\sqrt{(1-D)^3}} I_o \tag{32}$$

$$I_{D3,rms} = \sqrt{\frac{\int_{DT_s}^{T_s} (i_{L2} + i_{L3})^2 dt}{T_s}} = \frac{1}{\sqrt{1-D}} I_o \tag{33}$$

The winding resistance r_L leads to the copper loss of the inductor, which is calculated as follows:

$$P_{Loss}^{Inductor} = r_{L1} I_{L1,rms}^2 + r_{L2} I_{L2,rms}^2 + r_{L3} I_{L3,rms}^2 \tag{34}$$

where $I_{L1,rms}$, $I_{L2,rms}$ and $I_{L3,rms}$ are the *RMS* values of inductors current which are equal to the average current of inductors.

The parasitic resistance r_C results in capacitor losses calculated below.

$$P_{Loss}^{Capacitor} = r_{C1} I_{C1,rms}^2 + r_{C2} I_{C2,rms}^2 + r_{C3} I_{C3,rms}^2 + r_{Co} I_{Co,rms}^2 \tag{35}$$

The *RMS* values of the capacitors are calculated as follows:

$$I_{C1\&2,rms} = \sqrt{\frac{\int_0^{DT_s} (i_{L2} + i_{L3})^2 dt + \int_{DT_s}^{T_s} (\frac{1}{2} i_{L1})^2 dt}{T_s}} = \frac{\sqrt{D}}{\sqrt{(1-D)^3}} I_o \tag{36}$$

$$I_{C3,rms} = \sqrt{\frac{\int_0^{DT_s} i_{L3}^2 dt + \int_{DT_s}^{T_s} i_{L2}^2 dt}{T_s}} = \frac{\sqrt{D}}{\sqrt{1-D}} I_o \tag{37}$$

$$I_{Co,rms} = \sqrt{\frac{\int_0^{DT_s} (i_{L3} - i_o)^2 dt + \int_{DT_s}^{T_s} (i_{L3} - i_o)^2 dt}{T_s}} = 0 \tag{38}$$

The total losses can be determined by summing the aforementioned losses as follows.

$$P_{Loss}^{Total} = \sum (P_{Loss}^{Switch} + P_{Loss}^{Diode} + P_{Loss}^{Inductor} + P_{Loss}^{Capacitor}) \tag{39}$$

Finally, the converter efficiency is formulated in the following equation.

$$\eta = \frac{P_o}{P_o + P_{Loss}^{Total}} \times 100\% \tag{40}$$

Figure 9 shows the efficiency diagram of the proposed converter versus output power at the specified intervals in boost and buck modes. As can be seen, the boost mode efficiency is approximately 97%. Also, the efficiency in buck mode is more than 92%.

Figure 10 illustrates the comparison between the efficiency of the proposed converter and various other converters across different intervals of output power under identical conditions. Evidently, the proposed converter demonstrates superior efficiency compared to other converters at identical power levels. It should be noted that

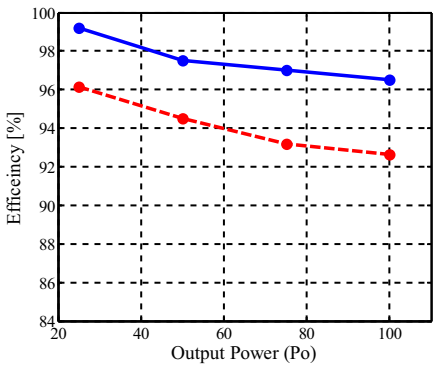


Fig. 9. Efficiency of the proposed converter versus output power in boost and buck modes.

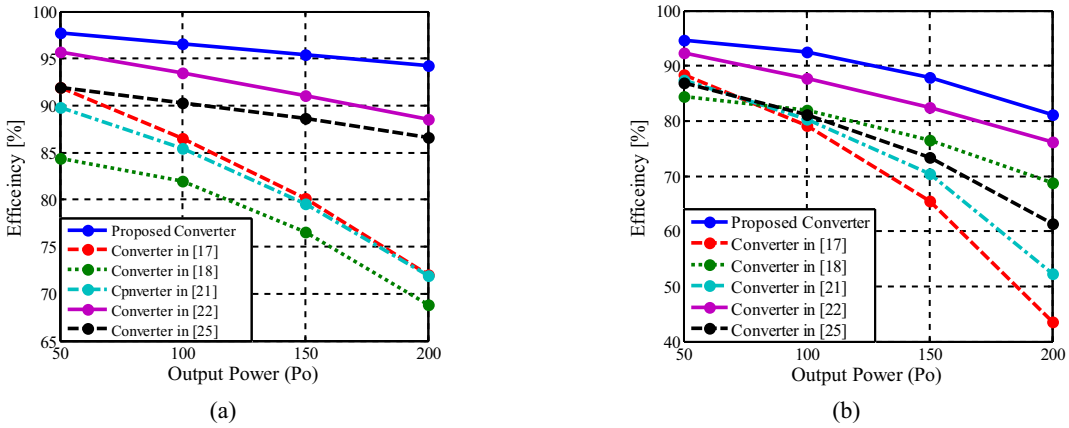


Fig. 10. Comparing the efficiency of the proposed converter with other converters: (**a**) boost mode; (**b**) buck mode.

the parasitic parameters used in the drawing of Figs. 9 and 10 include the on-state resistance of switches (r_S) equal to 0.05 Ω, internal resistance of diodes (r_D) equal to 0.15 Ω, capacitors and inductors *ESR* (r_C, r_L) equal to 0.02 Ω and 0.05 Ω, respectively, and the forward voltage drop (V_D) is equal to 0.6 V.

The pie chart of power loss distribution in boost and buck modes is shown in Fig. 11. The boost mode has a higher input current than the output current, while the buck mode has a lower input current than the output current. So, the efficiency in buck mode is lower than the efficiency in boost mode. As a result, buck mode loss is more than boost mode. Power losses of switches, diodes, capacitors and inductors are obtained by considering Eqs. (27) to (38).

In the boost mode, the output voltage increases compared to the input voltage, and the output current also decreases compared to the input current, in the same proportion. On the opposite point, in the buck mode, the output voltage decreases compared to the input voltage, and the output current also increases compared to the input current, in the same proportion. The placement of diode D_3 in the proposed circuit is close to the output load and it should pass more current in the buck mode. Since the diode D_3 passes the total current of the inductors L_2 and L_3 in state 2 of the equivalent circuit of the proposed converter, and according to the results of simulation and experiment, the sum of these two currents in the buck mode is about 2.5 times higher than the sum of these two currents in the boost mode. Therefore, the loss contribution of diode D_3 in the buck mode has achieved a significant amount.

Comparison of the proposed converter with similar converter

To assess the capabilities of the proposed converter, a comparative analysis was conducted, considering the number of elements, voltage gain, and voltage/current stress of switches and diodes. Specifically, efforts were made to select converters that closely resemble the proposed converter in terms of the total number of components and switches, ensuring a comprehensive and equitable evaluation. Also, a comparison between the proposed converter and other converters in terms of the common ground connection between the input and output ports has been made in Table 1.

Number of elements

The combination and number of elements utilized in structures is listed in Table 1. Despite having an equal number of elements, the proposed converter has a higher voltage gain than converters [18] and [21]. Furthermore, despite equality in the number of elements and voltage gain between the proposed converter and the converter [25], the proposed converter has a relatively low voltage/current stress on switches and diodes. In addition, converters [17,20,22,24] have fewer elements than the proposed converter, but they have a lower voltage gain. Also, the number of elements of converter 12 is more than the proposed converter. Therefore, its high voltage gain is logical.

Fig. 11. Pie chart of power loss distribution: (**a**) boost mode; (**b**) buck mode.

	Switches	Diodes	Capacitors	Inductors	Number of elements	Voltage stress of switches (V_S/V_i)	Voltage stress of diodes (V_D/V_i)	Current stress of switches (I_S/I_o)	Current stress of diodes (I_D/I_o)	Voltage gain	CG	CIC
[12]	2	3	5	4	14	$1/(1-D)$, $1/(1-D)^2$	$1/(1-D)$, $(2-D)/(1-D)^2$, $(2-D)/(1-D)^2$	$2/(1-D)^2$, $2/(1-D)$	$2D/(1-D)$, 1, 1	$2D(2-D)/(1-D)^2$	Yes	Yes
[17]	2	2	3	3	10	$1/(1-D)$, $D/(1-D)^2$	$1/(1-D)$, $D/(1-D)^2$	$D^2/(1-D)^2$, $D/(1-D)$	$D/(1-D)$, 1	$D^2/(1-D)^2$	Yes	Yes
[18]	1	5	3	3	12	$1/(1-D)^2$	$1/(1-D)$, $D/(1-D)^2$, $1/(1-D)^2$, $1/(1-D)$, $D/(1-D)^2$	$(D^3-D^2+D)/(1-D)^2$	$D^2/(1-D)$, $D^3/(1-D)^2$, D, D, $(1-D)$	$D^2/(1-D)^2$	Yes	Yes
[20]	1	2	4	3	10	$1/(1-D)$	$1/(1-D)$, $1/(1-D)$	$2/(1-D)$	$1/(1-D)$, $1/(1-D)$	$2D/(1-D)$	Yes	No
[21]	2	3	4	3	12	$1/(1-D)$, $D/(1-D)^2$	$1/(1-D)$, $1/(1-D)^2$, $D/(1-D)^2$	$(1+D)/(1-D)^2$, $(1+D)/(1-D)$	$(1+D)/(1-D)^2$, $D/(1-D)$, $D/(1-D)$	$D(1+D)/(1-D)^2$	Yes	No
[22]	2	2	3	3	10	$1/(1-D)$, $1/(1-D)^2$	$1/(1-D)$, $1/(1-D)^2$	$D/(1-D)^2$, $D/(1-D)$	$D/(1-D)$, 1	$D/(1-D)^2$	Yes	Yes
[24]	2	2	2	2	8	$1/(1-D)$, $D/(1-D)^2$	$1/(1-D)$, $D/(1-D)^2$	$D^3/(1-D)^4$, $D^2/(1-D)^3$	$D^3/(1-D)^4$, $D^2/(1-D)^3$	$D^2/(1-D)^2$	Yes	No
[25]	2	4	3	3	12	$2/(1-D)$, $2/(1-D)^2$	$1/(1-D)$, $1/(1-D)$, $2/(1-D)$, $2D/(1-D)^2$	$2D/(1-D)^2$, $1/(1-D)$	$2D/((1+D)(1-D)^2)$, $2D/((1+D)(1-D)^2)$, $(1+D)/(1-D)^2$, $1/(1-D)$	$2D/(1-D)^2$	Yes	No
Proposed	2	3	4	3	12	$1/(1-D)$, $(1+D)/(1-D)^2$	$1/(1-D)$, $1/(1-D)$, $2/(1-D)^2$	$(D(1+D))/(1-D)^2$, $D/(1-D)$	$D/(1-D)$, $D/(1-D)$, 1	$2D/(1-D)^2$	No	Yes

Table 1. Comparison between buck–boost converters characteristics. *CG* common ground, *CIC* continuous input current.

Voltage gain comparison

In addition to Table 1, Fig. 12 graphically represents the voltage gain of the comparative converters as a function of the duty cycle. It is obvious that the proposed converter and the converter [25] show a higher voltage gain than the alternative converters at varying duty cycle values except for the converter [12], as shown in Fig. 12. Considering that the converter [12] has more elements than the proposed converter, so the high voltage gain of the converter [12] is also reasonable compared to the proposed converter. In this figure, the voltage gain of converters [17,18,24] is the same. Even though the converters [18] and [21] have the same number of elements, their voltage gain is lower than the suggested topology. As mentioned earlier, despite having the same voltage gain as the proposed converter, the converter [25] has a relatively high voltage/current stress on switches and diodes compared to the proposed converter.

Voltage stress comparison of semiconductor devices

Figure 13 shows the relationship between voltage stress of the switches and duty cycle. The voltage stress experienced by switch S_1 in the proposed converter corresponds to the voltage stress encountered by switch S_1

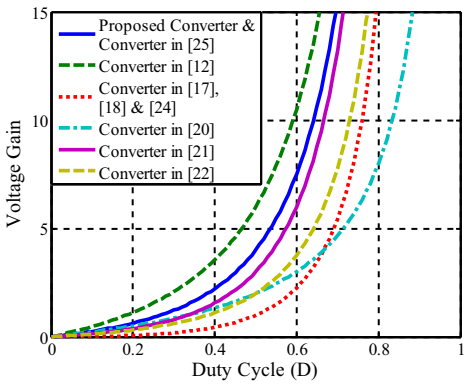


Fig. 12. Comparison of voltage gain of the converters versus duty cycle.

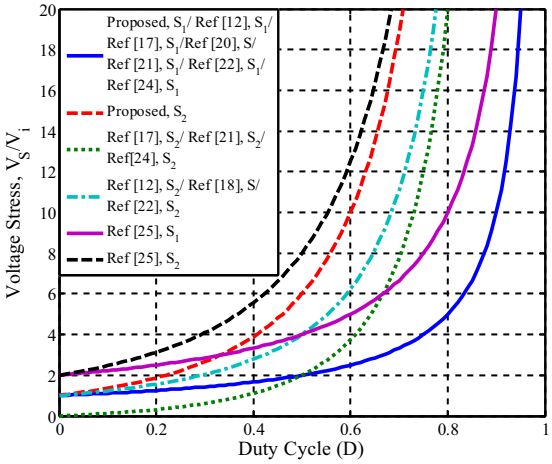


Fig. 13. Comparing the voltage stress of the switches of the converters versus duty cycle.

in converters [12,17,21,22,24] and switch S in converter [20]. Furthermore, the voltage stress of the switch S_2 in converters [17,21,24] are equivalent, While the voltage stress of the switch S_2 in converters [12] and [22] and the voltage stress of the switch S in the converter [18] are the same. As can be seen in Fig. 12, the switch S_1 of the proposed converter has a low voltage stress, and even though the switch S_2 of the proposed converter has a high voltage stress, it can be ignored due to the high voltage gain of the proposed converter except the converter [12]. Also, despite its voltage gain being equal to the proposed converter, the converter [25] has a high voltage stress of the switches.

Figure 14 shows the voltage stress of the diodes versus duty cycle. According to this figure, the voltage stress of the diodes D_1 and D_2 of the proposed converter is equal to the voltage stress of the diode D_1 of the converters [12,17,21,22,24], the diodes D_1 and D_4 of the converter [18], the diodes D_1 and D_2 of the converters [20] and [25]. Additionally, the voltage stress of the diode D_2 of the converter [17] is the same as that of the diodes D_2 and D_5 of the converter [18], the diode D_3 of the converter [21], and the diode D_2 of the converter [24]. The voltage stress of the diode D_3 of the converter [18] is also equal to the voltage stress of the diode D_2 of the converters [21] and [22]. Although the voltage stress of the diode D_3 of the proposed converter is high, it should be noted that the proposed converter has a relative superiority in terms of voltage gain and structural features compared to the other mentioned converters except the converter [12]. The voltage stress of the diodes D_1 and D_2 of the proposed converter is less or equal to the voltage stress of the diodes of other converters in a duty cycle greater than 50%.

Current stress comparison of semiconductor devices

Figure 15 shows the current stress of the switches of the proposed and compared converters. Observably, the current stress of the switch S_2 in the proposed converter matches the current stress of the switch S_2 in converters [17] and [22]. Moreover, the current stress of another switch in the proposed converter deviates from the current stress observed in the switches of the other compared converters. According to Fig. 15, the current stress of the switch S_2 in the proposed converter and switch S_2 of the converters [17] and [22] is better than the current stress of

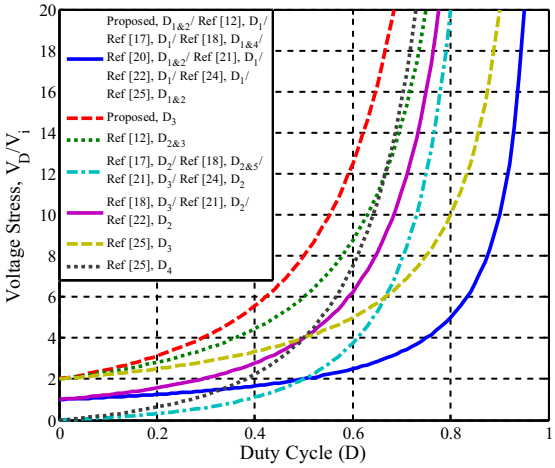


Fig. 14. Comparing the voltage stress of the diodes of converters versus duty cycle.

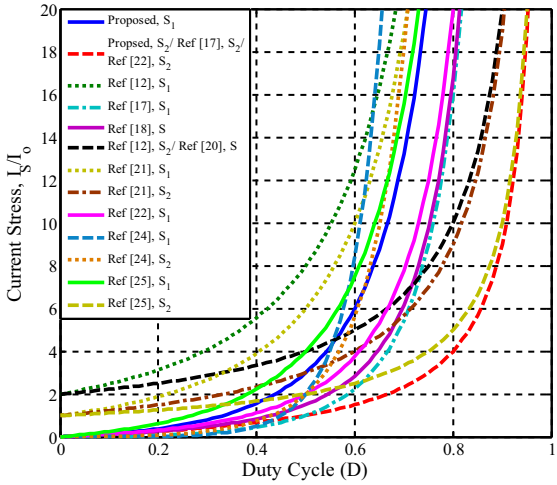


Fig. 15. Comparing the current stress of the switches of the converters versus duty cycle.

the other converters. The current stress of switch S_1 of the suggested topology is also within an acceptable range compared to the other converters according to Table 1.

In Fig. 16, the current stress of the diodes of the proposed converter is juxtaposed with that of the aforementioned converters. In this comparison, the current stress of the diodes D_1 and D_2 of the proposed converter is the same as the diode D_1 of the converter [17], the diodes D_1 and D_3 of the converter [21] and the diode D_1 of the converter [22]. Likewise, the current stress of the diode D_3 in the proposed converter matches the current stress observed in the diodes D_2 and D_3 of the converter [12] and the diode D_2 of the converters [17] and [22]. In the converter [18], the current stress of the diodes D_3 and D_4 is also equal. The current stress of the diodes D_1 and D_2 of the converter [20] is also equal to the current stress of the diode D_4 of the converters [25]. Additionally, the converter [21] diode D_1 current stress is the same as that of the diode D_3 of the converter [25]. The current stress of the diodes D_1 and D_2 of the converter [25] is also equal. Evidently, the current stress of the diodes of the proposed converter falls within an acceptable range in comparison to the other referenced converters.

Small signal modeling of the proposed converter

This section discusses the small signal modeling of the proposed converter. According to the small signal method, the state variables include the current of the inductors $i_{L1}(t)$, $i_{L2}(t)$ and $i_{L3}(t)$, the voltage of the capacitors $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$ and $v_{Co}(t)$, the duty cycle $d(t)$ and input voltage $v_i(t)$, consisting of two components: DC value (X) and disturbances ($\hat{x}$). Therefore, for the proposed converter, the equations are as follows:

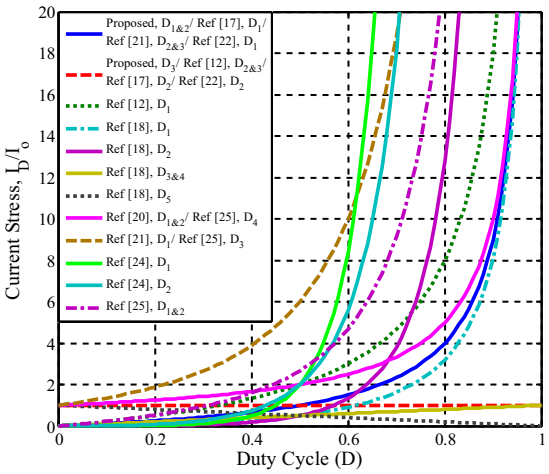


Fig. 16. Comparing the current stress of the diodes of the converters versus duty cycle.

$$\begin{cases} i_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ i_{L2}(t) = I_{L2} + \hat{i}_{L2}(t) \\ i_{L3}(t) = I_{L3} + \hat{i}_{L3}(t) \\ v_{C1}(t) = V_{C1} + \hat{v}_{C1}(t) \\ v_{C2}(t) = V_{C2} + \hat{v}_{C2}(t) \\ v_{C3}(t) = V_{C3} + \hat{v}_{C3}(t) \\ v_{Co}(t) = V_{Co} + \hat{v}_{Co}(t) \\ d(t) = D + \hat{d}(t) \\ v_i(t) = V_i + \hat{v}_i(t) \end{cases} \quad \text{with} \quad \begin{cases} \hat{i}_{L1}(t) \ll I_{L1} \\ \hat{i}_{L2}(t) \ll I_{L2} \\ \hat{i}_{L3}(t) \ll I_{L3} \\ \hat{v}_{C1}(t) \ll V_{C1} \\ \hat{v}_{C2}(t) \ll V_{C2} \\ \hat{v}_{C3}(t) \ll V_{C3} \\ \hat{v}_{Co}(t) \ll V_{Co} \\ \hat{d}(t) \ll D \\ \hat{v}_i(t) \ll V_i \end{cases} \tag{41}$$

By substituting Eq. (41) into Eqs. (1)–(4), the small-signal state equations are obtained as Eq. (42).

$$\begin{cases} L_1 \dfrac{d\hat{i}_{L1}(t)}{dt} = -(1-D)\hat{v}_{C1}(t) + \dfrac{V_i}{1-D}\hat{d}(t) + \hat{v}_i(t) \\ L_2 \dfrac{d\hat{i}_{L2}(t)}{dt} = D\hat{v}_{C1}(t) + D\hat{v}_{C2}(t) - (1-D)\hat{v}_{C3}(t) + \dfrac{2V_i}{(1-D)^2}\hat{d}(t) \\ L_3 \dfrac{d\hat{i}_{L3}(t)}{dt} = D\hat{v}_{C1}(t) + D\hat{v}_{C2}(t) + D\hat{v}_{C3}(t) - \hat{v}_{Co}(t) + \dfrac{2V_i}{(1-D)^2}\hat{d}(t) \\ C_1 \dfrac{d\hat{v}_{C1}(t)}{dt} = \dfrac{1-D}{2}\hat{i}_{L1}(t) - D\hat{i}_{L2}(t) - D\hat{i}_{L3}(t) - \dfrac{2DV_i}{R_o(1-D)^4}\hat{d}(t) \\ C_2 \dfrac{d\hat{v}_{C2}(t)}{dt} = \dfrac{1-D}{2}\hat{i}_{L1}(t) - D\hat{i}_{L2}(t) - D\hat{i}_{L3}(t) - \dfrac{2DV_i}{R_o(1-D)^4}\hat{d}(t) \\ C_3 \dfrac{d\hat{v}_{C3}(t)}{dt} = (1-D)\hat{i}_{L2}(t) - D\hat{i}_{L3}(t) - \dfrac{2DV_i}{R_o(1-D)^3}\hat{d}(t) \\ C_o \dfrac{d\hat{v}_{Co}(t)}{dt} = \hat{i}_{L3}(t) - \left(\dfrac{1}{R_o}\right)\hat{v}_{Co}(t) \end{cases} \tag{42}$$

Matrices A, B, C and D are obtained by simplifying Eq. (42) and comparing it with Eq. (43), in the form of Eqs. (44) to (47).

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{43}$$

$$A = \begin{bmatrix} 0 & 0 & 0 & -\left(\frac{1-D}{L_1}\right) & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{D}{L_2} & \frac{D}{L_2} & -\left(\frac{1-D}{L_2}\right) & 0 \\ 0 & 0 & 0 & \frac{D}{L_3} & \frac{D}{L_3} & \frac{D}{L_3} & -\frac{1}{L_3} \\ \frac{1-D}{2C_1} & -\frac{D}{C_1} & -\frac{D}{C_1} & 0 & 0 & 0 & 0 \\ \frac{1-D}{2C_2} & -\frac{D}{C_2} & -\frac{D}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-D}{C_3} & -\frac{D}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & 0 & -\left(\frac{1}{R_oC_o}\right) \end{bmatrix} \tag{44}$$

$$B = \begin{bmatrix} \frac{V_i}{L_1(1-D)} \\ \frac{2V_i}{L_2(1-D)^2} \\ \frac{2V_i}{L_3(1-D)^2} \\ -\frac{2DV_i}{R_oC_1(1-D)^4} \\ -\frac{2DV_i}{R_oC_2(1-D)^4} \\ -\frac{2DV_i}{R_oC_3(1-D)^3} \\ 0 \end{bmatrix} \tag{45}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{46}$$

$$D = [0] \tag{47}$$

By performing the Laplace transform on Eq. (43), the control-to-output transfer function of boost and buck modes is obtained as Eqs. (48) and (49).

$$G_{vd-boost}(s) = \frac{\widehat{v}_o(s)}{\widehat{d}(s)} = \frac{2.424e9s^4 - 2.629e11s^3 + 1.217e16s^2 - 3.627e17s + 7.826e21}{s^6 + 15000s^5 + 1.147e8s^4 + 5.224e11s^3 + 1.443e15s^2 + 2.247e18s + 1.517e21} \tag{48}$$

$$G_{vd-buck}(s) = \frac{\widehat{v}_o(s)}{\widehat{d}(s)} = \frac{9.47e8s^4 - 2.163e11s^3 + 9.413e15s^2 - 5.798e17s + 1.002e22}{s^6 + 12604s^5 + 7.36e7s^4 + 2.537e11s^3 + 5.257e14s^2 + 6.084e17s + 3.044e20} \tag{49}$$

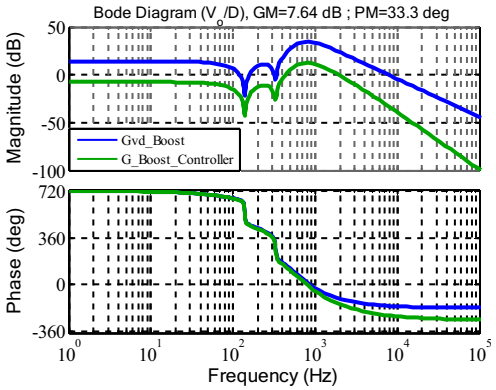
As can be seen in Eq. (50), the proposed controller includes a real pole ($a = 14{,}000$) and a coefficient equal to 1148. The Bode diagram with the presence of the compensator in both boost and buck modes is shown in Fig. 17.

$$G_C = \frac{K}{(s + a)} \tag{50}$$

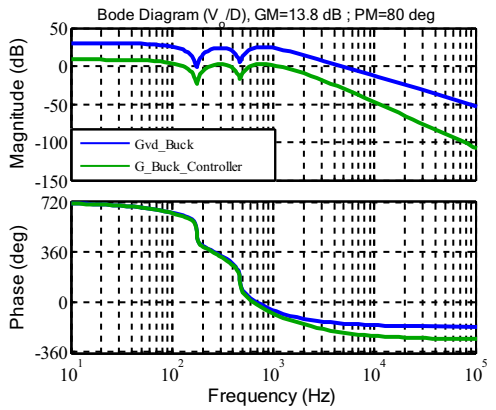
The Bode diagram based on theoretical calculations without compensator and with adding compensator is shown in Fig. 17. Figure 17a shows the Bode diagram in boost mode for duty cycle ($D = 0.5$) and load ($R = 97.82\ \Omega$). Also, Fig. 17b has drawn the Bode diagram in buck mode for ($D = 0.2$) and load ($R = 3.15\ \Omega$). From the figure, it is clear that both boost and buck modes in the mode without compensator, the values of gain margin (GM) and phase margin (PM) are not in the appropriate control range. As a result, the system under study does not have proper stability when a change in duty cycle occurs. Using MATLAB software SISOTOOL and considering the appropriate range of gain margin (at least 5 dB) and phase margin (between 30 and 80 degrees), the suitable controller is obtained as follows.

By using the controller, GM and PM in the boost mode are equal to 7.64 dB and 33.3 degrees, respectively. Similarly, the GM and PM of the buck mode are 13.8 dB and 80 degrees, respectively. It follows that the system under study is stable in spite of the disturbance of changes in duty cycle. Figure 18 shows the block diagram of the proposed converter control system considering the desired gain margin and phase margin.

The performance of the proposed converter in closed-loop conditions has been investigated in two scenarios including input voltage instantaneous change and output load sudden change. In the first scenario, the input DC voltage is reduced linearly from 30 to 10 V in the period of [0.3–0.5] seconds. In this situation, the output voltage



(a)



(b)

Fig. 17. Bode diagram of $G_{vd}(s)$: (**a**) boost mode; (**b**) buck mode.

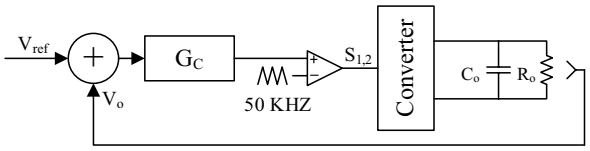
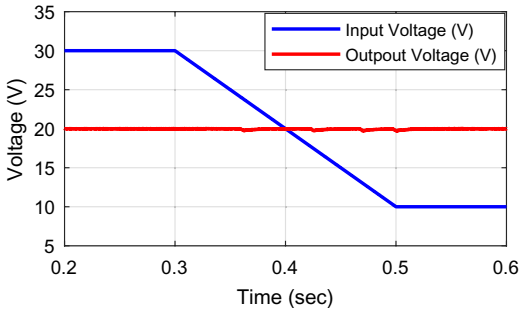


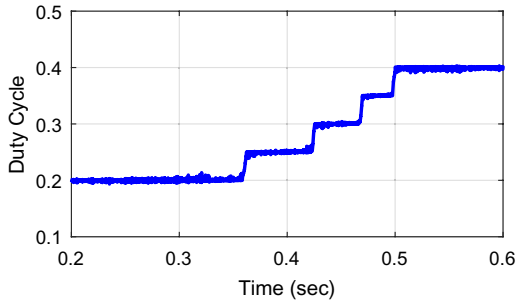
Fig. 18. Block diagram of the proposed converter control system.

reference value is set to 20 V and the goal is to stabilize the output voltage at 20 V. According to Fig. 19, the output voltage is well stabilized at 20 V and the proposed converter closed-loop system has worked correctly for a wide range of input voltage changes. In a time interval less than 0.4 s, the converter operates in the buck mode and for a time interval greater than 0.4 s, the converter operates in the boost mode. Therefore, the transition from buck to boost mode has been done without any problems. The duty cycle of the switches in this scenario is shown in Fig. 19b. The duty cycle has updated its value with steps of 0.05 when necessary. At the moment when this change in the duty cycle occurs, a negligible ripple is observed in the output voltage, which can be ignored. In Fig. 19c, the input and output current of the converter can be seen. Considering that the output load is constant and receives 3 A per 20 V output voltage, the input current should be increased by gradually decreasing the input voltage. According to this figure, the input current is gradually and continuously increased and the power balance between input and output is established.

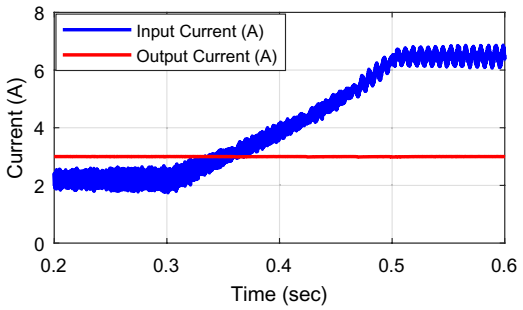
In the second scenario, the output load changes suddenly and then the performance of the closed loop control system is evaluated in this condition. In this scenario, the input voltage is 10 V and the closed-loop control sets the output voltage to 20 V. Therefore, the converter works in boost conditions. At 0.3 s, the output load resistance



(a)



(b)



(c)

Fig. 19. The closed-loop control performance of the proposed converter for changing the input voltage.

has decreased by 50%, which leads to a 50% increase in the output current from 2 to 3 A. At the moment of 0.4 s, the output resistance has increased by the same amount and the output load current decreases from 3 to 2 A. According to the results presented in Fig. 20, the closed-loop control system has worked correctly in this condition and the output voltage has been stabilized at 2 0 V. For this scenario, the waveform of the input and output current is shown in Fig. 20a, the duty cycle of the switches in Fig. 20b and the input and output voltage of the converter is shown in Fig. 20c.

Simulation and experimental results

Simulation results

Based on the parameters in Table 2, simulation has been conducted in Simulink MATLAB to verify the performance of the buck–boost converter. The simulation analysis of the proposed converter has been performed in two boost and buck modes in CCM mode, and the results for both modes are presented in Fig. 21. The evaluated output power for the boost and buck modes corresponds to 60 W and 40 W, respectively. Also, the power switches are controlled simultaneously on a duty cycle of 50% for boost mode and 20% for buck mode. Consequently, the outcomes were derived under practical circumstances, considering the impact of parasitic parameters. Therefore, the small difference between calculation and simulation results is negligible.

The output voltage and output current, the current of inductors, the voltage of capacitors, the voltage of diodes, the voltage of switches and the gate signals of switches are shown in Fig. 21. The input voltage of the converter in boost mode changes from 20 to 75.84 V with positive polarity, considering the duty cycle of 50%, which is equal to 80 V in the ideal state and based on theoretical calculations. The output current of the converter in boost mode is approximately equal to 0.79 A and is close to the ideal output current value equal to 0.83 A. It is worth mentioning that a difference of about 5% between the results of real conditions and ideal conditions

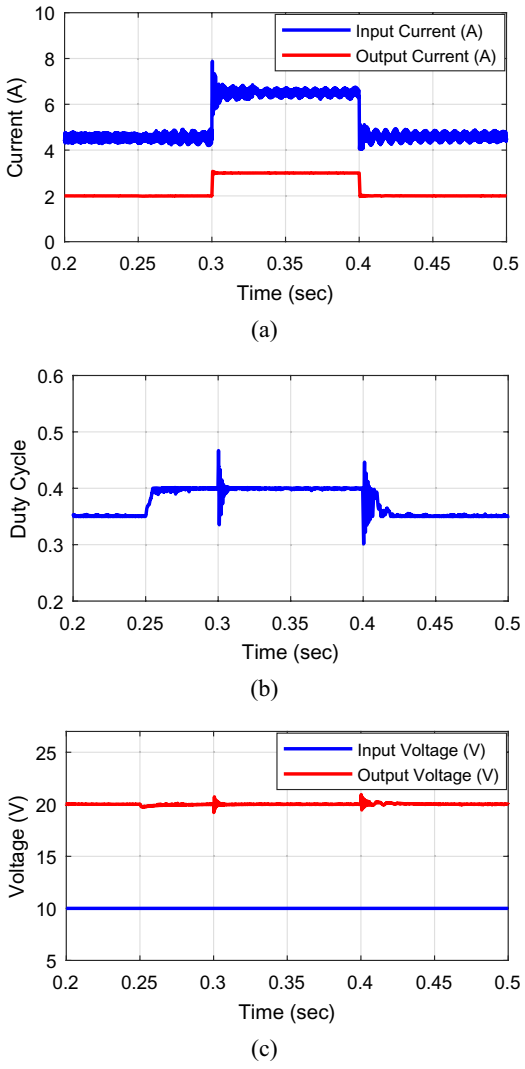


Fig. 20. The closed-loop control performance of the proposed converter for instantaneous change of the output load.

Buck mode	Boost mode	Parameters
20 V	20 V	Input voltage
12.5 V	80 V	Output voltage (ideal)
10.2 V	75.84 V	Output voltage (real)
40 W	60 W	Output power
50 KHz	50 KHz	Switching frequency
3.16 Ω	95.86 Ω	Output load
0.2	0.5	Duty cycle
IRFP260N	IRFP260N	MOSFETs
MBR20150CT	MBR20150CT	Diodes (D_1, D_2)
MUR1660CT	MUR1660CT	Diode (D_3)
200 µH	200 µH	Inductor (L_1)
2 mH	2 mH	Inductors (L_2, L_3)
220 µF	220 µF	Capacitors (C_1, C_2)
330 µF	330 µF	Capacitor (C_3)
150 µF	150 µF	Capacitor (C_o)

Table 2. Proposed converter parameters.

is common and if the elements with lower parasitic values are used in the converter, this difference will be less. According to Fig. 21a, the average current of inductors L_1, L_2, and L_3 is equal to 3.1 A, 0.8 A, and 0.8 A, respectively, which confirm the theoretical calculations made in Eq. (15). The voltage of capacitors C_1, C_2, C_3 and C_o from Fig. 21a, is equal to 38.6 V, 38.6 V, 75.84 V and 75.84 V, respectively, and these values correspond to Eqs. (8) to (10). Furthermore, according to Fig. 21a, the voltage of diodes D_1, D_2, and D_3 is equal to 40 V, 40 V, and 160 V, respectively, and these values also correspond to the voltage stress on diodes according to Table 1. The voltage of switches S_1 and S_2 in Fig. 21a is equal to 40 V and 120 V, respectively, which confirms the theoretical calculations compared to the voltage stress of switches in Table 1.

As indicated in Fig. 21b, the output voltage of the converter in the buck mode, considering a duty cycle of 20%, approximates 10.2 V, which closely aligns with the voltage in the ideal scenario, namely 12.5 V. The output current of the converter in buck mode according to Fig. 21b is equal to 3.92 A and in the ideal state it is equal to 3.95 A, which the closeness of these values shows the correctness of the theoretical calculations. The average current of inductors L_1, L_2 and L_3 in Fig. 21b is equal to 2.5 A, 0.98 A and 3.94 A, respectively, which confirms the correctness of theoretical calculations compared to Eq. (15). The voltage of capacitors C_1, C_2, C_3 and C_o in Fig. 21b is equal to 23.9 V, 23.9 V, 10.35 V and 10.21 V, respectively, which corresponds to Eqs. (8)–(10). The voltage of diodes D_1, D_2 and D_3 is equal to 24 V, 24 V and 60 V according to Fig. 21b, which also corresponds to the voltage stress of diodes according to Table 1. Moreover, the voltage of switches S_1 and S_2 is shown in Fig. 21b is almost equal to 25 V and 36 V, which is confirmed by the theoretical calculations compared to the voltage stress of switches in Table 1.

Experimental results

As can be seen in Fig. 22, to validate the precision of the simulation outcomes and the theoretical computations, a laboratory prototype was constructed. The results of the experimental prototype of the proposed converter are shown in Figs. 23 and 24. These figures exhibit the waveforms of currents and voltages across various components of the proposed converter within the laboratory setting, showcasing both the boost and buck modes. In Fig. 23, the results for the boost mode at duty cycle 50% are presented. Figure 23 shows the buck mode for some converter waveforms at duty cycle 20%. Figures 25 and 26 also show the output voltage and current in two boost and buck modes, respectively. The parasitic parameters of the equipment used in the practical circuit are similar to those introduced in Sect. (2.5.A).

The average current of inductors L_1, L_2 and L_3 in Fig. 23 is equal to 3.1 A, 0.8 A and 0.8 A, respectively, which corresponds to Eq. (15). The voltage of capacitors C_1, C_2 and C_3 in Fig. 23 is equal to 38 V, 35 V and 75 V, respectively, which is also consistent with Eqs. (8) to (10). The voltage of diodes D_1 and D_2 in Fig. 23 is equal to 38 V and 39 V, respectively, which corresponds to the voltage stress of diodes in Table 1. The voltage of switches S_1 and S_2 in Fig. 23 is equal to 40 V and 114 V, respectively, which corresponds to the voltage stress of switches in Table 1.

The average current of inductors L_1, L_2, and L_3 in Fig. 24 is equal to 2.5 A, 1 A, and 4 A, respectively, which confirms the correctness of the calculations compared to Eq. (15). The voltage of capacitors C_1, C_2, and C_3 in Fig. 24 is equal to 24 V, 24 V, and 10.1 V, respectively, and comparing it with Eqs. (8)–(10), confirms the correctness of the theoretical calculations. The voltage of diodes D_1 and D_2 in Fig. 24 is equal to 24 V and 26 V, respectively, which corresponds to the voltage of diodes in Table 1. The voltage of switches S_1 and S_2 in Fig. 24 is equal to 27 V and 36 V, respectively, which is consistent with the voltage stress of switches in Table 1.

The output voltage and output current depicted in Fig. 25, under the boost mode, correspond to 76 V and 0.78 A, respectively, aligning with the theoretical calculations in the ideal condition. Similarly, the output voltage and output current showcased in Fig. 26, during the buck mode, are recorded as 10 V and 3.9 A, respectively, harmonizing with the theoretical computations under ideal circumstances.

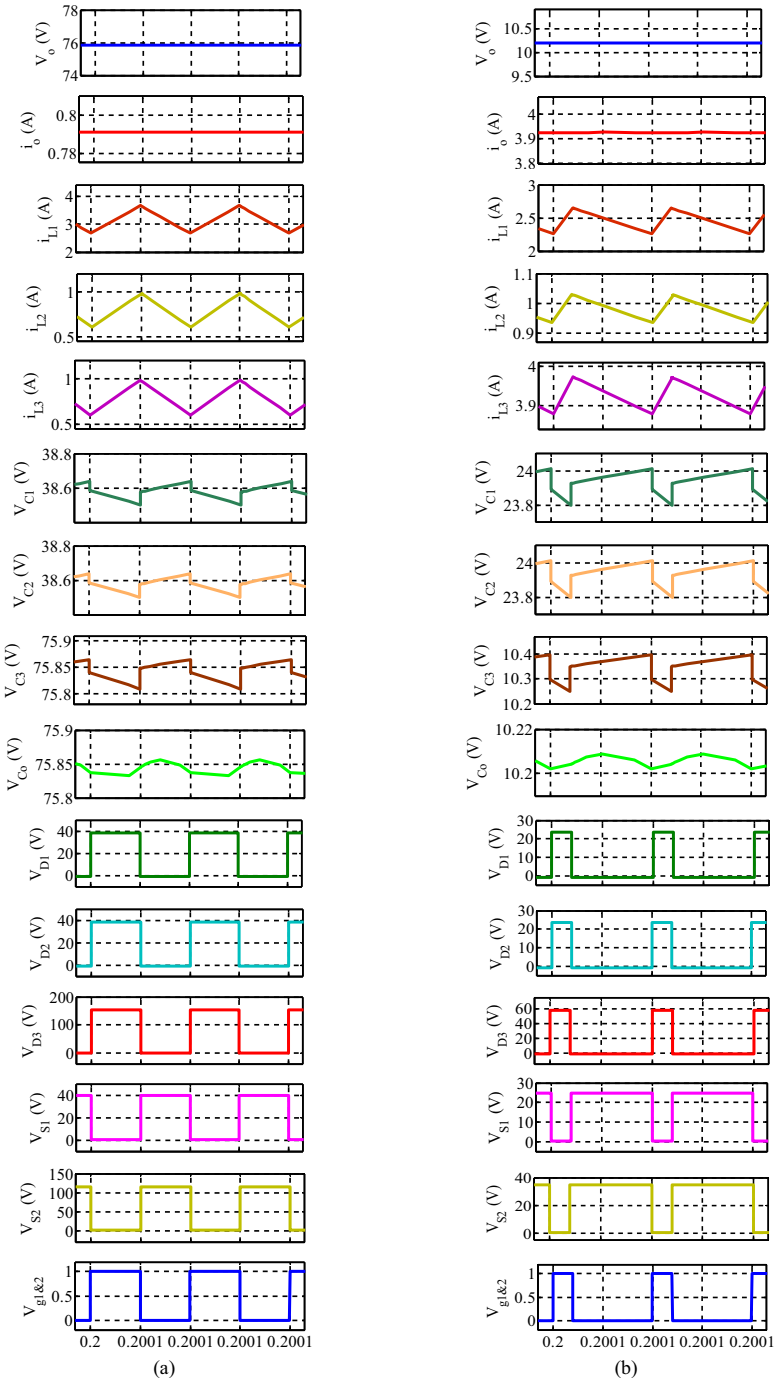


Fig. 21. The waveforms of the simulation results of the proposed converter: (**a**) boost mode; (**b**) buck mode.

Conclusion

This paper presents a non-inverting DC–DC buck–boost converter based on a modified boost converter and ZETA converter, which has the advantages of both converters such as continuous input/output current and positive polarity of the output voltage. The voltage conversion ratio of this topology is semi-quadratic and encompasses an extensive range of conversion ratios. The continuous output current of this converter renders it suitable for applications in renewable energy systems and industrial settings. The simultaneous operation of the switches in the converter results in a straightforward control mechanism. The continuity of input and output currents leads to a reduction in input current and output voltage ripples. Comparison of the ideal voltage gain of the converter with other similar models underscores the superiority of the proposed converter. The voltage/current stress of the switches and diodes as well as the introduced topology efficiency and its comparison with other structures are presented. The comparison results show the superiority of the suggested converter over other topologies in most cases. The small signal modeling and closed-loop control were also presented. The simulation results

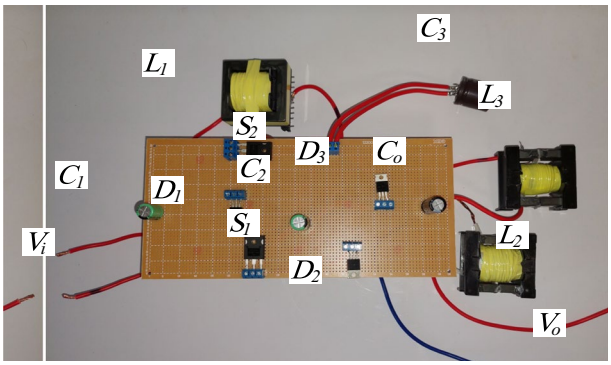


Fig. 22. Prototype of the proposed converter.

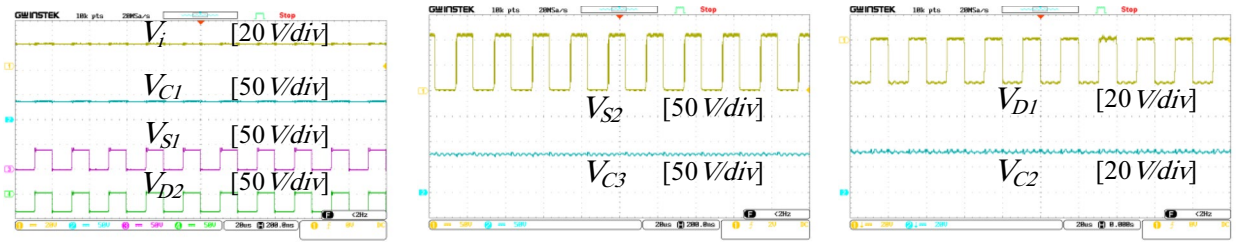


Fig. 23. Experimental results: boost mode.

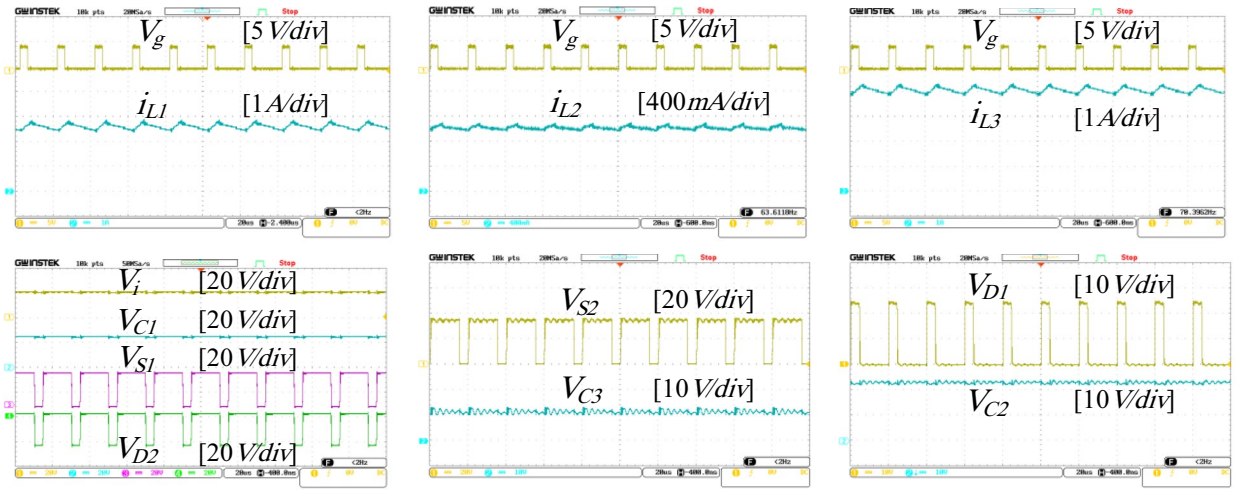


Fig. 24. Experimental results: buck mode.

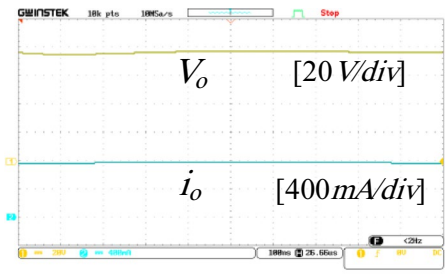


Fig. 25. Experimental results: output voltage/current in boost mode.

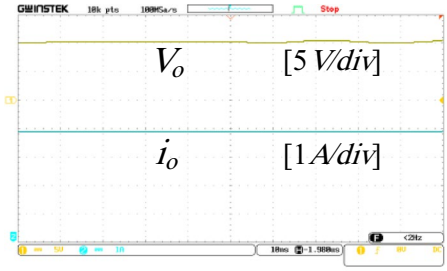


Fig. 26. Experimental results: output voltage/current in buck mode.

in two boost and buck modes using the Simulink environment of MATLAB software confirm the theoretical calculations. Finally, a 40 ~ 60W, 20 to 76 V for boost mode and 10 V for buck mode prototype are implemented in the laboratory to verify the simulation results and the relationships obtained from the theoretical analysis.

Data availability

All data generated and analyzed during the current study are available from the corresponding author upon reasonable request.

Received: 12 May 2024; Accepted: 29 August 2024
Published online: 05 September 2024

References

1. Kumar, M. A. B. & Krishnasamy, V. A single-switch continuous input current buck–boost converter with noninverted output voltage. *IEEE Trans. Power Electron.* **38**(2), 2181–2190 (2023).
2. Selvam, S., Sannasy, M. & Sridharan, M. Analysis and design of two-switch enhanced gain SEPIC converter. *IEEE Trans. Ind. Appl.* **59**(3), 3552–3561 (2023).
3. Hosseinpour, M., Seifi, E., Seifi, A. & Shahparasti, M. Design and analysis of an interleaved step-up DC–DC converter with enhanced characteristics. *Sci. Rep.* **14**(1), 14413 (2024).
4. Gholizadeh, H. & Ben-Brahim, L. A new non-isolated high-gain single-switch DC–DC converter topology with a continuous input current. *Electronics* **11**(18), 2900 (2022).
5. Zhao, J., Chen, D. & Jiang, J. Transformerless high step-up DC–DC converter with low voltage stress for fuel cells. *IEEE Access* **9**, 10228–10238 (2021).
6. Zheng, Y. & Smedley, K. M. Analysis and design of a single-switch high step-up coupled-inductor boost converter. *IEEE Trans. Power Electron.* **35**(1), 535–545 (2020).
7. Dastgiri, A., Hosseinpour, M., Sedaghati, F. & Mousavi-Aghdam, S. R. A high step-up DC–DC converter with active switched LC-network and voltage-lift circuit: Topology, operating principle, and implementation. *Int. J. Circuit Theory Appl.* **50**(1), 226–248 (2022).
8. Hosseinpour, M., Ahmadi, M., Seifi, A. & Mousavi-Aghdam, S. R. A new transformerless semi-quadratic buck–boost converter based on combination of Cuk and traditional buck–boost converters. *Int. J. Circuit Theory Appl.* **50**(11), 3926–3948 (2022).
9. Hasanpour, S., Mostaan, A., Baghramian, A. & Mojallali, H. Analysis, modeling, and implementation of a new transformerless semi-quadratic Buck–boost DC/DC converter. *Int. J. Circuit Theory Appl.* **47**(6), 862–883 (2019).
10. Hosseinpour, M., Ahmadi, M., Seifi, A. & Hosseini, S. H. A new transformerless buck-boost converter with improved voltage gain and continuous input current. *IET Power Electron.* **17**(4), 534–550 (2024).
11. Rosas-Caro, J. C., Valdez-Resendiz, J. E., Mayo-Maldonado, J. C., Alejo-Reyes, A. & Valderrabano-Gonzalez, A. Quadratic buck–boost converter with positive output voltage and minimum ripple point design. *IET Power Electron.* **11**(7), 1306–1313 (2018).
12. Yari, K., Shahalami, S. H. & Mojallali, H. A novel nonisolated buck–boost converter with continuous input current and semiquadratic voltage gain. *IEEE J. Emerg. Sel. Top. Power Electron.* **9**(5), 6124–6138 (2021).
13. Sadaf, S., Al-Emadi, N., Maroti, P. K. & Iqbal, A. A new high gain active switched network-based boost converter for DC microgrid application. *IEEE Access* **9**, 68253–68265 (2021).
14. Banaei, M. R. & Sani, S. G. Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current. *IEEE Trans. Power Electron.* **33**(12), 10317–10325 (2018).
15. Ansari, S. A. & Moghani, J. S. A novel high voltage gain noncoupled inductor SEPIC converter. *IEEE Trans. Ind. Electron.* **66**(9), 7099–7108 (2019).
16. Veerachary, M. & Khuntia, M. R. Design and analysis of two-switch-based enhanced gain buck–boost converters. *IEEE Trans. Ind. Electron.* **69**(4), 3577–3587 (2021).
17. Gholizadeh, H., Gorji, S. A. & Sera, D. A quadratic buck–boost converter with continuous input and output currents. *IEEE Access* **11**, 22376–22393 (2023).
18. Zhang, N., Zhang, G., See, K. W. & Zhang, B. A single-switch quadratic buck–boost converter with continuous input port current and continuous output port current. *IEEE Trans. Power Electron.* **33**(5), 4157–4166 (2018).
19 Sarikhani, A., Allahverdinejad, B. & Hamzeh, M. A nonisolated buck–boost DC–DC converter with continuous input current for photovoltaic applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **9**(1), 804–811 (2021).
20. Banaei, M. R. & Bonab, H. A. F. A high efficiency nonisolated buck–boost converter based on ZETA converter. *IEEE Trans. Ind. Electron.* **67**(3), 1991–1998 (2020).
21. García-Vite, P. M. *et al.* Quadratic buck–boost converter with reduced input current ripple and wide conversion range. *IET Power Electron.* **12**(15), 3977–3986 (2019).
22. Okati, M., Eslami, M., Jafari Shahbazzadeh, M. & Shareef, H. A new transformerless quadratic buck–boost converter with high-voltage gain ratio and continuous input/output current port. *IET Power Electron.* **15**(13), 1280–1294 (2022).
23. Lahooti Eshkevari, A., Mosallanejad, A. & Sepasian, M. Improving step-up gain and efficiency in non-inverting buck-boost dc-dc converter using quasi-Z impedance network. *IET Power Electron.* **15**(2), 109–122 (2022).
24. Loera-Palomo, R., Morales-Saldaña, J. A., Rivero, M., Álvarez-Macías, C. & Hernández-Jacobo, C. A. Noncascading quadratic buck–boost converter for photovoltaic applications. *Micromachines* **12**(8), 984 (2021).

25. Malick, I. H., Zaid, M., Ahmad, J., Varesi, K. & Lin, C. H. Implementation and reliability analysis of a new non-isolated quadratic buck–boost converter using improved Markov modelling. *IET Renew. Power Gener.* **17**(11), 2733–2749 (2023).

Author contributions

All authors reviewed the manuscript. M.H. designed and performed all the experiments, data analysis, documentation and supervision. M.H. performed the experiment, data analysis, and documentation. M.E.A. performed the data analysis and supervision.

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to M.H.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.