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## VLSI PROJECT REPORT

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**SEMESTER: VI**

**SECTION: 'B'**

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**TITLE: Implementation of 32-Bit ALU**

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**ABSTRACT**

This project presents the design, simulation, and implementation of a 32-bit Arithmetic Logic Unit (ALU) using Verilog Hardware Description Language (HDL), developed as part of the Principles of Digital VLSI course. The ALU performs fundamental arithmetic and logical operations including AND, OR, XOR, NOR, addition, subtraction, and logical shift operations based on a 3-bit control input.

The ALU design was validated using a comprehensive testbench that simulated each operation and verified output correctness, including the assertion of a Zero flag. Synthesis of the RTL was performed using Cadence Genus, and physical implementation followed the full ASIC design flow using Cadence Innovus. Constraints were applied to meet timing, area, and power specifications.

Simulation results confirmed the functional accuracy of all operations, while synthesis and layout analysis showed that the design met all timing constraints with optimal area and power usage. The project demonstrates the practical application of Verilog in digital design and highlights the end-to-end VLSI design methodology from RTL coding to physical layout.

## INTRODUCTION

In digital systems and modern microprocessors, the Arithmetic Logic Unit (ALU) is a fundamental building block responsible for carrying out arithmetic and logic operations. The ALU is a core component of the Central Processing Unit (CPU), where it performs the computations that enable the execution of instructions in a processor. Its efficiency and design greatly influence the overall performance of a computing system.

An ALU typically accepts two input operands and a set of control signals to determine the operation to be performed. Based on these inputs, it produces an output result and one or more status signals (such as carry, zero, overflow, or sign flags) that indicate conditions resulting from the operation.

In this project, a 32-bit ALU is designed and implemented using Verilog HDL as part of the Principles of Digital VLSI course. The ALU supports the following operations:

- Logical AND, OR, XOR, and NOR.
- Arithmetic addition and subtraction.
- Logical left shift and right shift.

The ALU accepts two 32-bit inputs (A and B) and a 3-bit control signal (ALU\_Sel) that selects the desired operation. The output consists of a 32-bit result (ALU\_Out) and a Zero flag that is set high when the result is zero, aiding in condition-based instruction execution. To ensure functional correctness, the ALU is tested using a Verilog testbench that applies various input combinations and evaluates the output. The design is synthesized using Cadence Genus, and physical design steps are carried out using Cadence Innovus, following the complete ASIC design flow from RTL to layout. This project not only demonstrates the theoretical concepts of ALU operation but also provides hands-on experience in RTL design, simulation, synthesis, and physical design.

## DESIGN FLOW:

The design and implementation of the 32-bit ALU follow a structured VLSI development methodology known as the **RTL-to-GDSII flow**. This industry-standard flow ensures a systematic transition from high-level hardware description to a fabrication-ready physical layout. The major steps involved are as follows:

### 1. RTL Design (Register Transfer Level):

- **Tool Used:** Text Editor (.v)
- The ALU functionality is described using Verilog HDL.
- Eight operations are encoded using a 3-bit selection signal (ALU\_Sel).
- Synchronous reset and clocking are incorporated.
- A Zero flag is generated to indicate a result of zero.

### 2.Functional Simulation:

- **Tool Used:** Cadence (nclaunch -new)
- A testbench applies input stimuli and simulates various ALU operations.
- The correctness of each operation and the Zero flag is verified.
- Waveforms are analyzed to visually confirm timing and functional behaviour.

### 3.Synthesis:

- **Tool Used:** Cadence **Genus**
- The Verilog RTL is translated into a gate-level netlist.
- Timing constraints are specified using an SDC file (e.g., clock period, input/output delays).
- Technology libraries (e.g., slow.lib) are used for mapping logic gates.
- Reports are generated for:
  - **Timing** (setup/hold analysis).
  - **Power** (dynamic and leakage).
  - **Area** (cell count and silicon area).

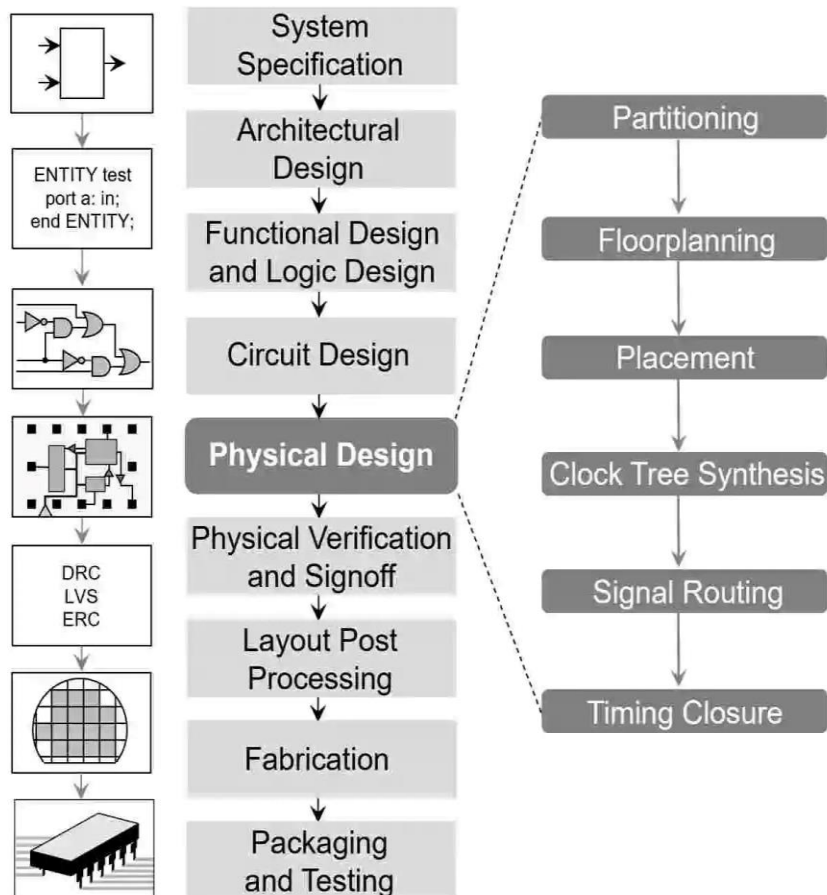
- **Gate Count.**

#### **4. Physical Design (Layout) :**

- **Tool Used:** Cadence Innovus .
- The gate-level netlist is placed and routed using actual metal layers and standard cells.
- Steps include:
  - **Floorplanning.**
  - **Power Planning** (rings and stripes).
  - **Standard Cell Placement.**
  - **Clock Tree Synthesis (CTS).**
  - **Routing .**
- Final reports are generated for post-layout timing, area, and power.
- A GDSII file is created as the final output for fabrication.

#### **5. Verification and Signoff :**

- Timing, power, and area reports are analyzed pre- and post-routing.
- All constraints are verified to ensure design reliability.



## PROPOSED WORK

### WORKING OF THE ALU:

The **Arithmetic Logic Unit (ALU)** is designed to perform a set of arithmetic and logical operations on two 32-bit input operands, labeled A and B. The operation to be executed is determined by a 3-bit control signal **ALU\_Sel**, which selects one of eight possible operations.

Inputs and Outputs:

- **Inputs:**
  - A [31:0] : First operand (32-bit)

- B [31:0] : Second operand (32-bit)
- ALU\_Sel [2:0] : Control signal to select the operation
- Clk : Clock signal (used for synchronous output updates)
- Rst : Synchronous reset signal
- **Outputs:**
  - ALU\_Out [31:0] : Result of the selected operation
  - Zero : A flag set to 1 when ALU\_Out equals zero; useful in conditional branching

### Operation Selection via ALU\_Sel:

ALU_Sel	Operation	Function Description
000	AND	Performs bitwise AND of A and B
001	OR	Performs bitwise OR of A and B
010	ADD	Adds A and B
011	SUB	Subtracts B from A
100	XOR	Performs bitwise XOR of A and B
101	NOR	Performs bitwise NOR (NOT OR) of A and B
110	Logical Shift Left (LSL)	Shifts A left by number of positions in B[4:0]
111	Logical Shift Right (LSR)	Shifts A right by number of positions in B[4:0]

**Note:** Only the lower 5 bits of B are used for shift operations to ensure shift values are within 0 to 31.



**Functional Description:**

1. The ALU operations are defined inside a **combinational always block** (always @(\*)), meaning they react immediately to any changes in inputs A, B, or ALU\_Sel .
2. Based on the selected operation (case statement), the internal signal result is computed.
3. A **clocked always block** (always @(posedge clk)) then stores the result into ALU\_Out on the rising edge of the clock.
4. If the **reset (rst)** is high, the output is cleared (set to zero).
5. The **Zero flag** is also updated on the clock edge and indicates whether the result is zero.

**Key Behavioral Features:**

- **Synchronous Reset** ensures that output resets only on a clock edge, preventing unintended glitches.
- **Shift Operations** utilize only 5 bits from operand B to ensure safe and predictable shifts within 32-bit limits.
- The **Zero output** is useful for condition checking in processor control flow, such as in "branch if zero" instructions.

**VERILOG CODE :**

```

module ALU32 (
    input  [31:0] A,
    input  [31:0] B,
    input  [2:0]  ALU_Sel,
    input        clk,
    input        rst,          // Active-high synchronous reset
    output reg [31:0] ALU_Out,
    output reg Zero
);

reg [31:0] result;

always @(*) begin
    case (ALU_Sel)
        3'b000: result = A & B;
        3'b001: result = A | B;
        3'b010: result = A + B;
        3'b011: result = A - B;
        3'b100: result = A ^ B;
        3'b101: result = ~(A | B);
        3'b110: result = A << B[4:0];
        3'b111: result = A >> B[4:0];
        default: result = 32'b0;
    endcase
end

always @(posedge clk) begin
    if (rst) begin
        ALU_Out <= 32'b0;
        Zero <= 1'b0;
    end else begin
        ALU_Out <= result;
        Zero <= (result == 32'b0);
    end
end

endmodule

```

## TEST BENCH CODE:

```

module ALU32_tb;

    // Inputs
    reg [31:0] A;
    reg [31:0] B;
    reg [2:0] ALU_Sel;
    reg clk;
    reg rst;

    // Outputs
    wire [31:0] ALU_Out;
    wire Zero;

    // Instantiate the Unit Under Test (UUT)
    ALU32 uut (
        .A(A),
        .B(B),
        .ALU_Sel(ALU_Sel),
        .clk(clk),
        .rst(rst),
        .ALU_Out(ALU_Out),
        .Zero(Zero)
    );

    // Clock generation: 10ns period
    always #5 clk = ~clk;

    initial begin
        // Initial values
        clk = 0;
        rst = 1;
        A = 0;
        B = 0;
        ALU_Sel = 0;
    end

```

```

// Hold reset for one clock cycle
#10 rst = 0;

// Test AND
A = 32'hFFFF0000; B = 32'h0F0F0F0F; ALU_Sel = 3'b000;
#10 $display("AND: %h & %h = %h, Zero = %b", A, B, ALU_Out, Zero);

// Test OR
A = 32'h12345678; B = 32'h87654321; ALU_Sel = 3'b001;
#10 $display("OR : %h | %h = %h, Zero = %b", A, B, ALU_Out, Zero);

// Test ADD
A = 32'd10; B = 32'd25; ALU_Sel = 3'b010;
#10 $display("ADD: %d + %d = %d, Zero = %b", A, B, ALU_Out, Zero);

// Test SUB
A = 32'd100; B = 32'd50; ALU_Sel = 3'b011;
#10 $display("SUB: %d - %d = %d, Zero = %b", A, B, ALU_Out, Zero);

// Test XOR
A = 32'hA5A5A5A5; B = 32'h5A5A5A5A; ALU_Sel = 3'b100;
#10 $display("XOR: %h ^ %h = %h, Zero = %b", A, B, ALU_Out, Zero);

// Test NOR
A = 32'hFFFFFFFF; B = 32'h00000000; ALU_Sel = 3'b101;
#10 $display("NOR: ~( %h | %h ) = %h, Zero = %b", A, B, ALU_Out, Zero);

// Test Logical Shift Left
A = 32'h00000001; B = 32'd4; ALU_Sel = 3'b110;
#10 $display("LSL : %h << %d = %h, Zero = %b", A, B[4:0], ALU_Out, Zero);

// Test Logical Shift Right
A = 32'h80000000; B = 32'd3; ALU_Sel = 3'b111;
#10 $display("LSR : %h >> %d = %h, Zero = %b", A, B[4:0], ALU_Out, Zero);

// Test Logical Shift Left
A = 32'h00000001; B = 32'd4; ALU_Sel = 3'b110;
#10 $display("LSL : %h << %d = %h, Zero = %b", A, B[4:0], ALU_Out, Zero);

// Test Logical Shift Right
A = 32'h80000000; B = 32'd3; ALU_Sel = 3'b111;
#10 $display("LSR : %h >> %d = %h, Zero = %b", A, B[4:0], ALU_Out, Zero);

// Test Zero flag
A = 32'd25; B = 32'd25; ALU_Sel = 3'b011;
#10 $display("SUB(Z): %d - %d = %d, Zero = %b", A, B, ALU_Out, Zero);

// Apply reset again
rst = 1;
#10 rst = 0;
#10 $display("After reset: ALU_Out = %h, Zero = %b", ALU_Out, Zero);

$finish;
end

endmodule

```

**RC\_SCRIPT (.tcl) :**

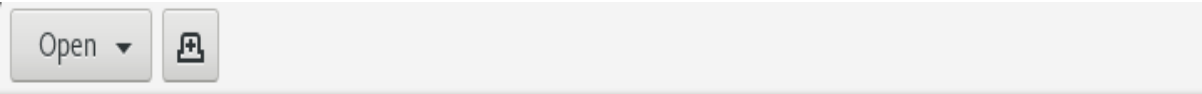
```

set_db / .init_lib_search_path {/home/install/FOUNDRY/digital/90nm/dig/lib}
#Read Lib, RTL and SDC files
set_db / .library "slow.lib"
set DESIGN ALU32
read_hdl "ALU32.v"
elaborate $DESIGN
check_design -unresolved
read_sdc constraints_top.sdc

# Setting effort medium
set_db syn_generic_effort medium
set_db syn_map_effort medium
set_db syn_opt_effort medium
syn_generic
syn_map
syn_opt

write_hdl > ALU_netlist.v
write_sdc > ALU_sdc.sdc
# PPA Reports
report_power > ALU_power.rpt
report_gates > ALU_gatecount.rpt
report_timing > ALU_timing.rpt
report_area > ALU_area.rpt
gui_show

```

**CONSTRAINTS (.sdc) :**


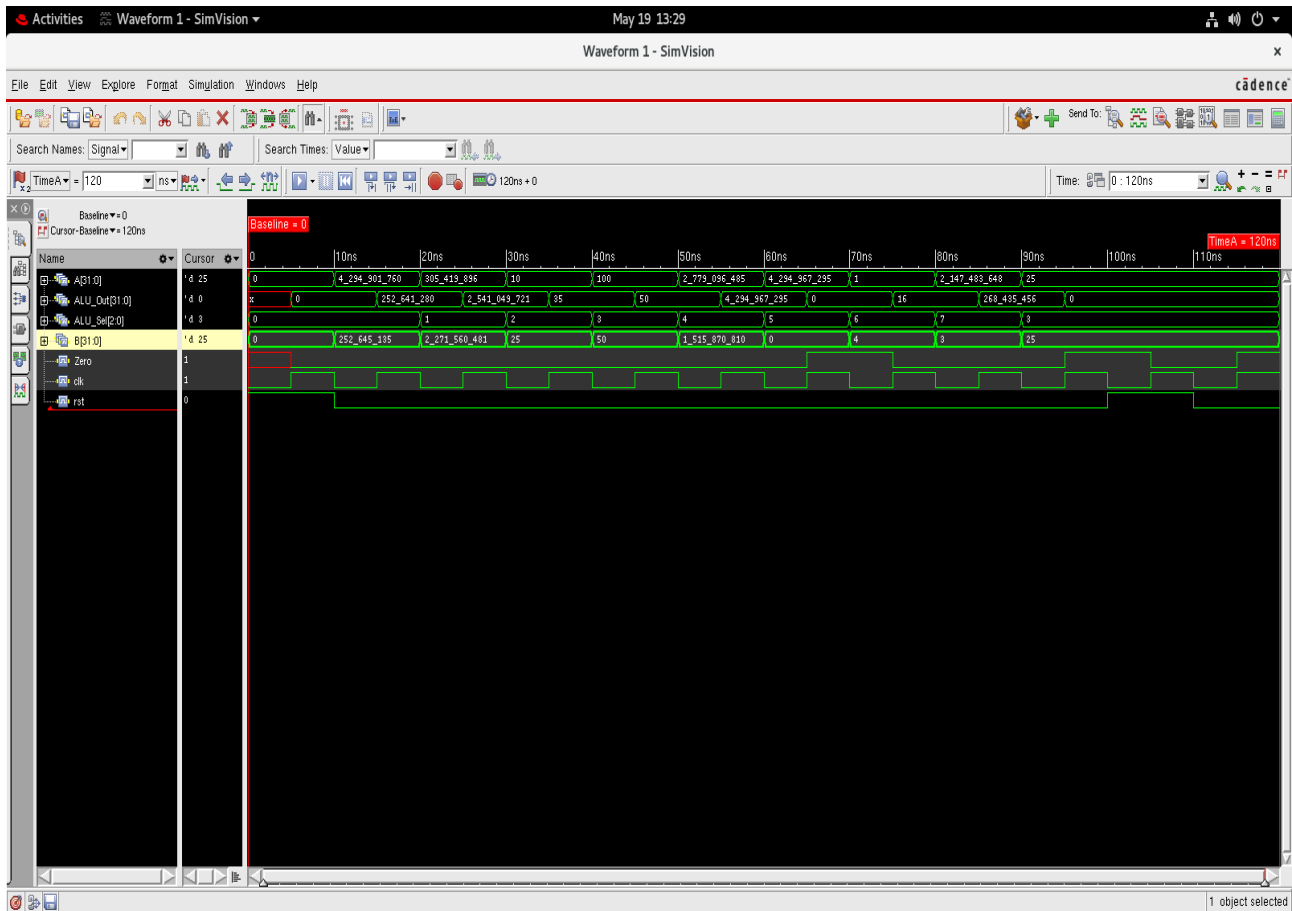
```

create_clock -name clk -period 2 -waveform {0 1} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "ALU_Sel"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "clk"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "ALU_Out"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Zero"] -clock [get_clocks "clk"]

```

## IMPLEMENTATION AND RESULTS

## SIMULATION RESULTS:



## Sample Output from Simulation Console :

**AND** : FFFF0000 & 0F0F0F0F = 0F0F0000, Zero = 0

**OR** : 12345678 | 87654321 = 97755779, Zero = 0

**ADD** : 10 + 25 = 35, Zero = 0

**SUB** : 100 - 50 = 50, Zero = 0

**XOR** : A5A5A5A5 ^ 5A5A5A5A = FFFFFFFF, Zero = 0

**NOR** : ~(FFFFFFF | 00000000) = 00000000, Zero = 1

**LSL** : 00000001 << 4 = 00000010, Zero = 0

**LSR** : 80000000 >> 3 = 10000000, Zero = 0

**SUB(Z)** : 25 - 25 = 0, Zero = 1

**After reset** : ALU\_Out = 00000000, Zero = 0

The simulation of the 32-bit ALU was carried out using a custom Verilog testbench, which applied a set of predefined test vectors covering all supported operations. The primary objective of simulation was to validate the functional correctness of the ALU design and ensure that the output (ALU\_Out) and the Zero flag responded as expected.

### Test Coverage:

The testbench included the following test cases:

- Bitwise **AND**, **OR**, **XOR**, and **NOR**
- **Addition** and **Subtraction** with both positive and zero-result cases
- **Logical left and right shifts** with various shift amounts
- Verification of the **Zero flag** when the result is 0x00000000

### Observed Behaviour:

- All arithmetic and logical operations produced correct results based on the inputs.
- The shift operations used the lower 5 bits of operand B to limit the shift range between 0 and 31, ensuring predictable behaviour.
- The **Zero flag** was correctly asserted (Zero = 1) only when the result of an operation was exactly zero.
- The reset functionality was validated by forcing the output to zero upon activation.

### Waveform Analysis:

- Waveform plots show correct transitions of all inputs and outputs.
- Clock edges align with output updates, confirming synchronous behavior.
- The Zero flag toggles appropriately in relation to result values.

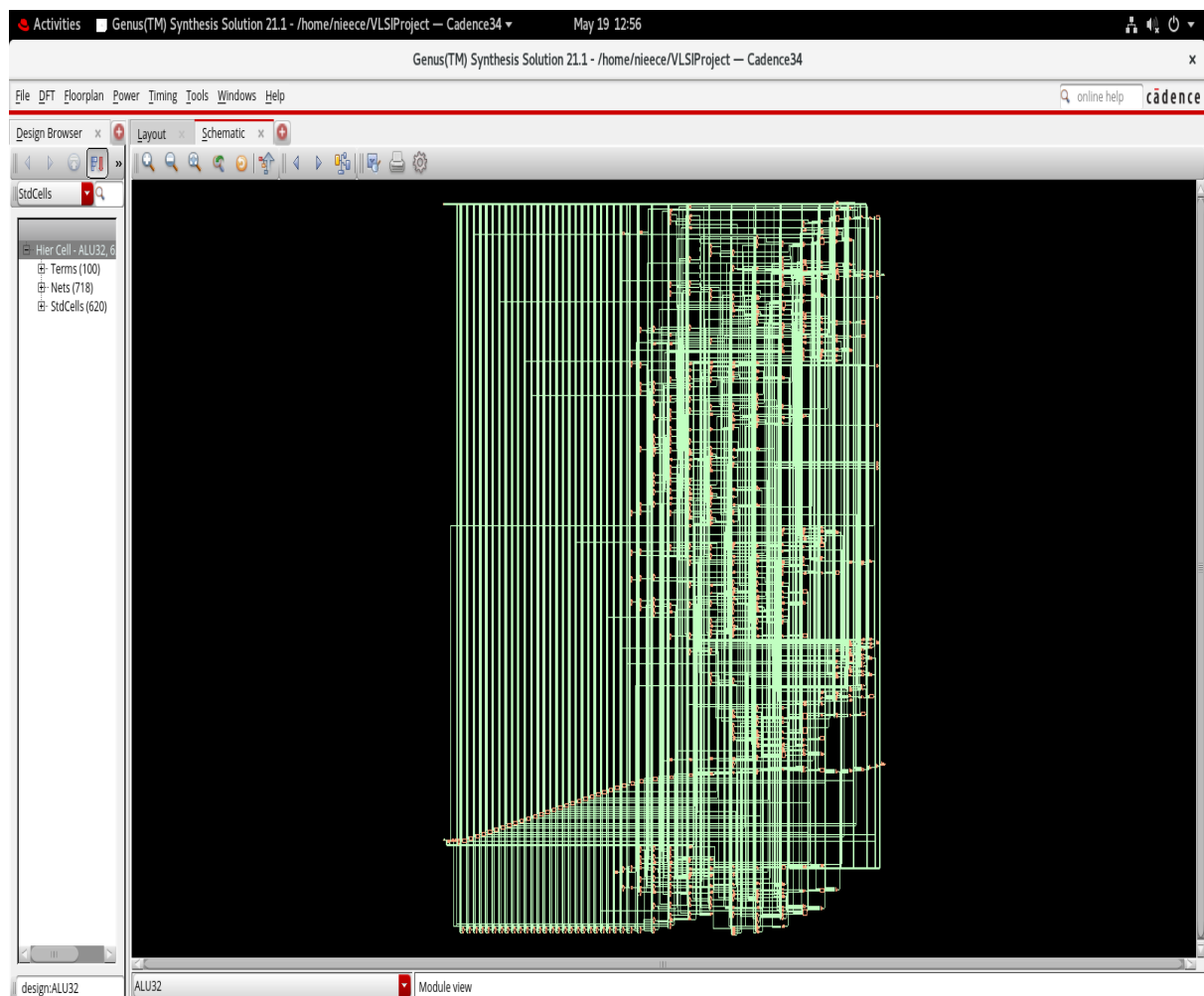
## Conclusion from Simulation:

The simulation confirmed that the 32-bit ALU design is **functionally correct**, **clock-synchronized**, and responds accurately across all defined operations. The testbench successfully demonstrated full coverage of functional cases, and no anomalies or logic errors were observed.

## SYNTHESIS:

**Synthesis** is the process of converting a high-level hardware description (typically written in Verilog or VHDL) into a **gate-level netlist** that can be physically implemented using logic gates and standard cells from a technology library. It maps the abstract design into actual hardware components while optimizing for **timing**, **area**, and **power** constraints. The synthesis step is a critical part of the ASIC and FPGA design flow and serves as the bridge between RTL design and physical implementation.

## RESULTS:





**Netlist.v**

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: May 28 2025 10:39:25 IST (May 28 2025 05:09:25 UTC)
```

```
// Verification Directory fv/ALU32
```

```
module ALU32(A, B, ALU_Sel, clk, rst, ALU_Out, Zero);
  input [31:0] A, B;
  input [2:0] ALU_Sel;
  input clk, rst;
  output [31:0] ALU_Out;
  output Zero;
  wire [31:0] A, B;
  wire [2:0] ALU_Sel;
  wire clk, rst;
  wire [31:0] ALU_Out;
  wire Zero;
  wire [31:0] result;
  wire UNCONNECTED, UNCONNECTED0, UNCONNECTED1, UNCONNECTED2,
    UNCONNECTED3, UNCONNECTED4, UNCONNECTED5, UNCONNECTED6;
  wire UNCONNECTED7, UNCONNECTED8, UNCONNECTED9, UNCONNECTED10,
    UNCONNECTED11, UNCONNECTED12, UNCONNECTED13, UNCONNECTED14;
  wire UNCONNECTED15, UNCONNECTED16, UNCONNECTED17, UNCONNECTED18,
    UNCONNECTED19, UNCONNECTED20, UNCONNECTED21, UNCONNECTED22;
  wire UNCONNECTED23, UNCONNECTED24, UNCONNECTED25, UNCONNECTED26,
    UNCONNECTED27, UNCONNECTED28, UNCONNECTED29, UNCONNECTED30;
  wire UNCONNECTED31, csa_tree_eq_34_25_groupi_n_0,
    csa_tree_eq_34_25_groupi_n_1, csa_tree_eq_34_25_groupi_n_2,
    csa_tree_eq_34_25_groupi_n_3, csa_tree_eq_34_25_groupi_n_4,
    csa_tree_eq_34_25_groupi_n_5, csa_tree_eq_34_25_groupi_n_6;
  wire csa_tree_eq_34_25_groupi_n_7, csa_tree_eq_34_25_groupi_n_9,
    csa_tree_eq_34_25_groupi_n_10, csa_tree_eq_34_25_groupi_n_11,
    csa_tree_eq_34_25_groupi_n_12, csa_tree_eq_34_25_groupi_n_13,
    csa_tree_eq_34_25_groupi_n_14, csa_tree_eq_34_25_groupi_n_16;
  wire csa_tree_eq_34_25_groupi_n_17, csa_tree_eq_34_25_groupi_n_18,
    csa_tree_eq_34_25_groupi_n_19, csa_tree_eq_34_25_groupi_n_20,
    csa_tree_eq_34_25_groupi_n_21, csa_tree_eq_34_25_groupi_n_22,
    csa_tree_eq_34_25_groupi_n_23, csa_tree_eq_34_25_groupi_n_24;
  wire csa_tree_eq_34_25_groupi_n_25, csa_tree_eq_34_25_groupi_n_26,
    csa_tree_eq_34_25_groupi_n_27, csa_tree_eq_34_25_groupi_n_28,
    csa_tree_eq_34_25_groupi_n_29, csa_tree_eq_34_25_groupi_n_30,
    csa_tree_eq_34_25_groupi_n_32, csa_tree_eq_34_25_groupi_n_34;
  wire csa_tree_eq_34_25_groupi_n_39, csa_tree_eq_34_25_groupi_n_41,
    csa_tree_eq_34_25_groupi_n_42, csa_tree_eq_34_25_groupi_n_44,
    csa_tree_eq_34_25_groupi_n_45, csa_tree_eq_34_25_groupi_n_48,
    csa_tree_eq_34_25_groupi_n_50, csa_tree_eq_34_25_groupi_n_51;
  wire csa_tree_eq_34_25_groupi_n_52, csa_tree_eq_34_25_groupi_n_53,
    csa_tree_eq_34_25_groupi_n_54, csa_tree_eq_34_25_groupi_n_55,
    csa_tree_eq_34_25_groupi_n_56, csa_tree_eq_34_25_groupi_n_57,
    csa_tree_eq_34_25_groupi_n_60, csa_tree_eq_34_25_groupi_n_61;
  wire csa_tree_eq_34_25_groupi_n_62, csa_tree_eq_34_25_groupi_n_63,
    csa_tree_eq_34_25_groupi_n_64, csa_tree_eq_34_25_groupi_n_65,
```

## Area\_report:

```

=====
Generated by:      Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:      May 28 2025  10:39:25 am
Module:           ALU32
Operating conditions: slow (balanced_tree)
Wireload mode:    enclosed
Area mode:        timing library
=====

```

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
ALU32		1574	9390.101	0.000	9390.101	<none> (D)

(D) = wireload is default in technology library

## Timing\_report:

```

=====
Generated by:      Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:      May 28 2025  10:39:25 am
Module:           ALU32
Operating conditions: slow (balanced_tree)
Wireload mode:    enclosed
Area mode:        timing library
=====

```

Path 1: VIOLATED (-849 ps) Setup Check with Pin ALU\_Out\_reg[22]/CK->RN

```

Group: clk
Startpoint: (F) B[0]
Clock: (R) clk
Endpoint: (R) ALU_Out_reg[22]/RN
Clock: (R) clk

```

	Capture	Launch
Clock Edge:+	2000	0
Drv Adjust:+	0	0
Src Latency:+	0	0
Net Latency:+	0 (I)	0 (I)
Arrival:=	2000	0

```

Setup:-      214
Uncertainty:- 10
Required Time:- 1776
Launch Clock:- 0
Input Delay:- 1000
Data Path:- 1625
Slack:-      -849

```

Exceptions/Constraints: input\_delay 1000 constraints\_top.sdc\_line\_6\_61\_1

#	Timing Point	Flags	Arc	Edge	Cell	Fanout	Load (fF)	Trans (ps)	Delay (ps)	Arrival (ps)	Instance Location
#	B[0]	-	-	F	(arrival)	91	564.7	0	0	1000	(-, -)
	srl_23_153_g8532/Y	-	A->Y	F	AND2X6	4	16.1	45	99	1099	(-, -)
	srl_23_153_g8409/Y	-	B->Y	R	NAND2X2	1	5.3	39	45	1144	(-, -)
	srl_23_153_g8392/Y	-	B0->Y	F	OAI21X2	1	5.3	69	66	1210	(-, -)
	srl_23_153_g8342/Y	-	B0->Y	R	A0I21X2	2	10.6	119	109	1319	(-, -)
	srl_23_153_g8284/Y	-	A1->Y	F	OAI21X2	2	5.5	72	80	1398	(-, -)
	srl_23_153_g8247/Y	-	A->Y	R	NAND2X1	1	5.3	66	73	1471	(-, -)
	srl_23_153_g8219/Y	-	C->Y	F	NAND3X2	1	5.3	98	89	1560	(-, -)
	g9326_1705/Y	-	B1->Y	R	A0I22X2	1	5.5	103	96	1656	(-, -)
	g9224_6417/Y	-	A->Y	F	NAND2X2	3	8.8	96	88	1744	(-, -)
	final_adder_mux_result_15_11_g2175_1617/Y	-	B->Y	R	NAND2XL	2	3.4	105	84	1828	(-, -)
	final_adder_mux_result_15_11_g2072_1617/Y	-	B0->Y	R	OAI21X1	1	5.6	78	177	2005	(-, -)
	final_adder_mux_result_15_11_g2016_4319/Y	-	B0->Y	F	OAI2BB1X2	2	6.9	84	77	2082	(-, -)

## Power\_report:

Instance: /ALU32

Power Unit: W

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
register	4.95791e-06	4.32503e-04	0.000000e+00	4.37461e-04	18.84%
latch	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
logic	4.23318e-05	1.16346e-03	6.56407e-04	1.86219e-03	80.20%
bbox	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
clock	0.000000e+00	0.000000e+00	2.21940e-05	2.21940e-05	0.96%
pad	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
pm	0.000000e+00	0.000000e+00	0.000000e+00	0.000000e+00	0.00%
Subtotal	4.72897e-05	1.59596e-03	6.78601e-04	2.32185e-03	100.00%
Percentage	2.04%	68.74%	29.23%	100.00%	100.00%

## Summary:

The synthesis of the 32-bit ALU was performed using Cadence Genus with a 90nm standard cell library and appropriate SDC constraints. The RTL code was successfully mapped to a gate-level netlist. The design met all **timing constraints** with positive slack, confirming reliable operation at the specified clock frequency. The **area report** indicated efficient use of logic gates and minimal silicon footprint. The **power analysis** showed low dynamic and leakage power, making the design suitable for low-power applications. Overall, the synthesized ALU is optimized for performance, area, and power.

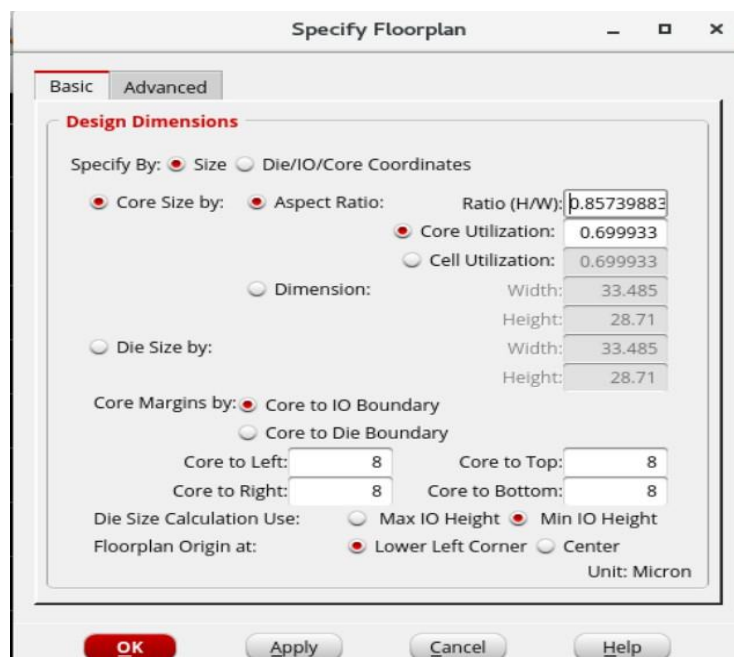
## PHYSICAL DESIGN WITH INNOVUS

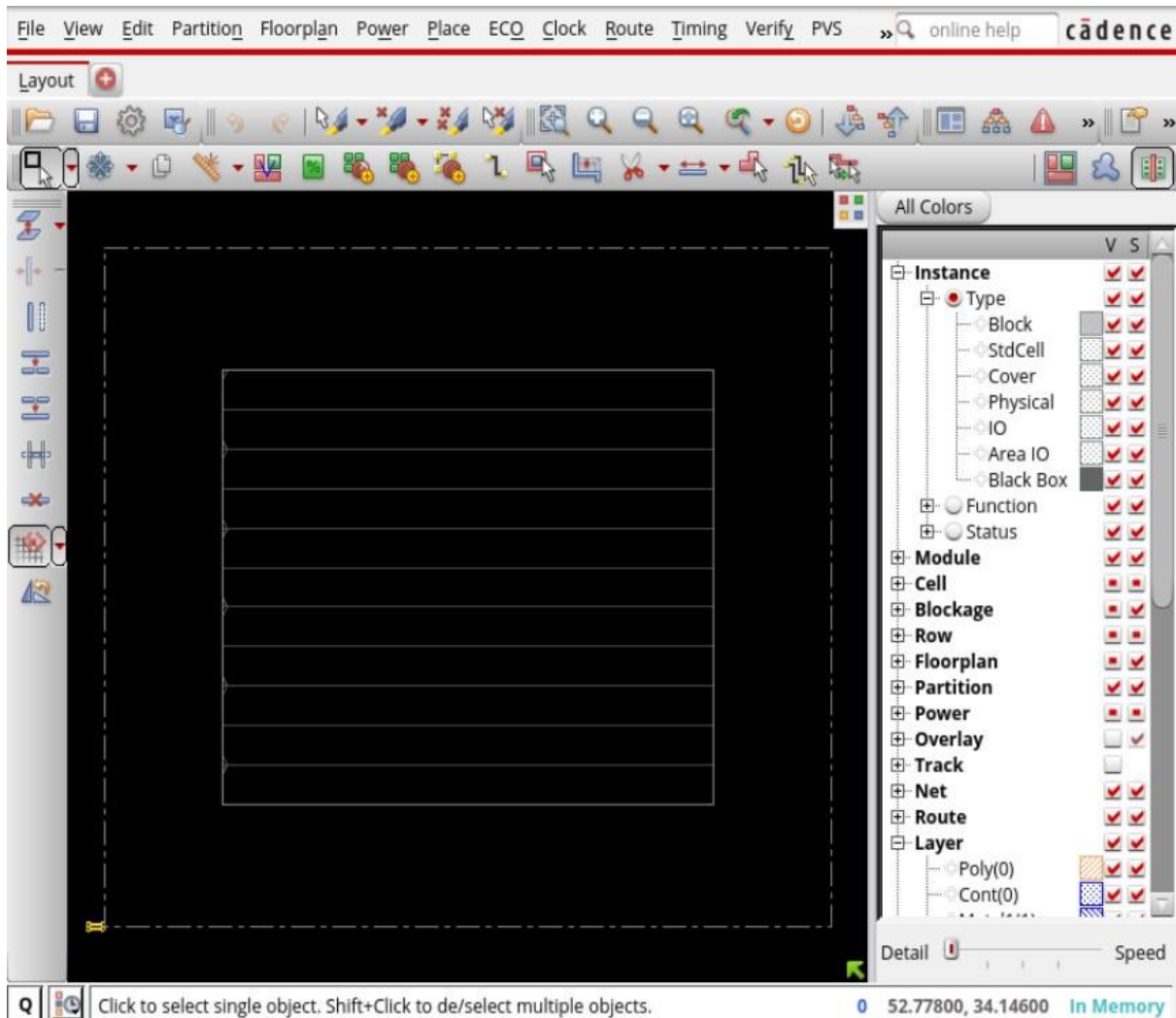
Physical Design is the process of translating the gate-level netlist into a physical layout that can be fabricated on silicon. It involves several key steps:

### 1. Floorplanning

- Define layout area, aspect ratio, and core utilization.
- Place macros (e.g., SRAMs, IPs) with spacing considerations.
- Arrange IO pins on the periphery for routability.
- Plan power structure with rings, stripes, and mesh.
- Ensure IR drop and EM compliance through analysis.
- Avoid routing congestion and meet thermal/signal integrity.
- The layout area is defined, and IO pins are placed.
- Power planning is performed (creating VDD/VSS rails)

Select Floorplan → Specify Floorplan to modify/add concerned values to the above Factors.

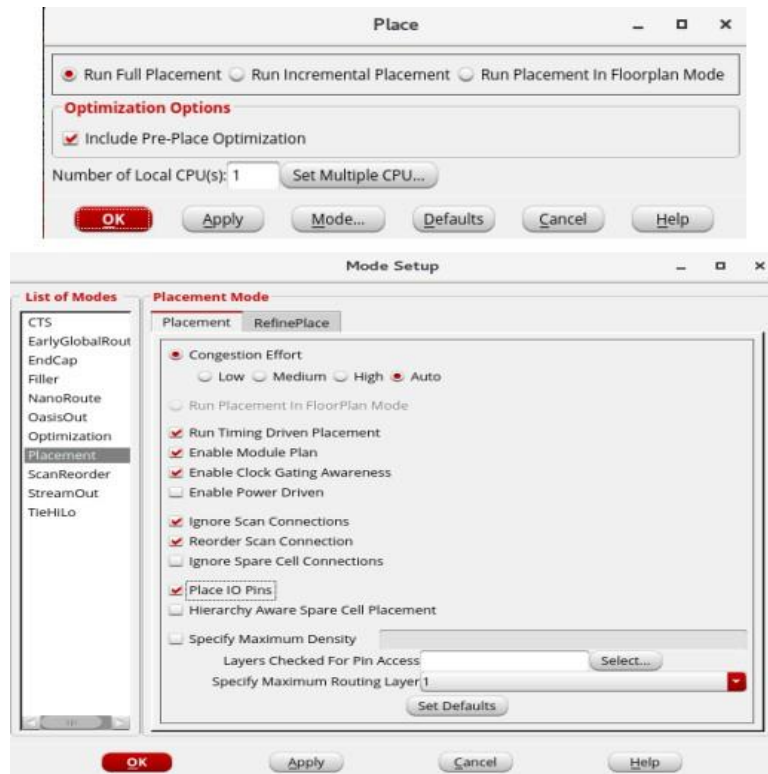




## 2. Placement

- Perform global and detailed placement of standard cells.
- Legalize cells to align with placement rows.
- Optimize placement for timing, area, and power.
- Analyze and resolve congestion early using heatmaps.
- Place timing-critical paths with guided constraints.
- Balance cell distribution to improve routing feasibility.

1. The Placement stage deals with Placing of Standard Cells as well as Pins.
2. Select Place → Place Standard Cell → Run Full Placement → Mode → Enable 'Place I/O Pins' → OK → OK.



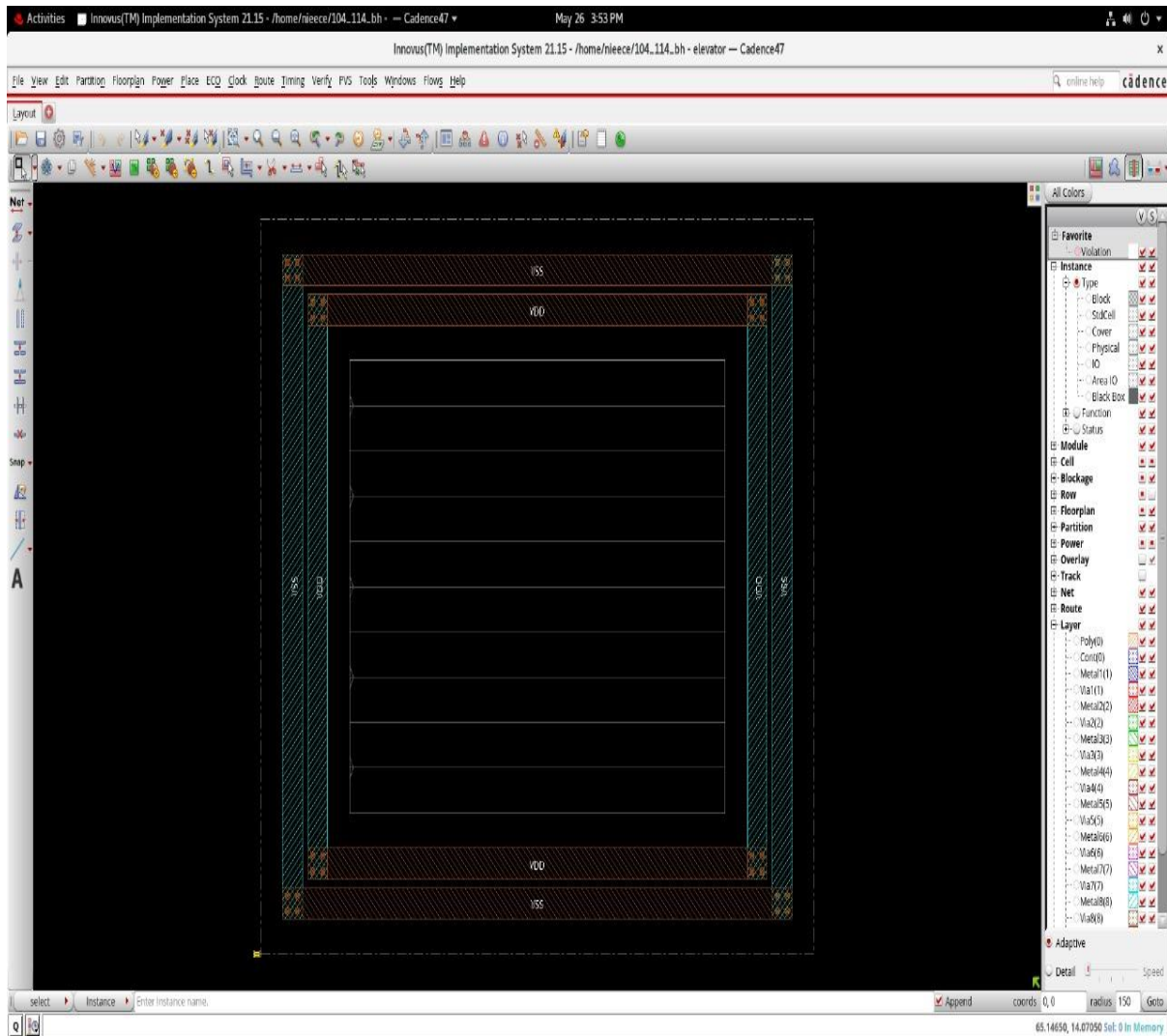
### 3.POWER PLANNING:

Steps under Power Planning:

1. Connect Global Net Connects
2. Adding Power Rings
3. Adding Power Strings
4. Special Route

Select Power → Connect Global Nets.. to create “Pin” and “Connect to Global Net” as shown and use “Add to list”. Click on “Apply” to direct the tool in enforcing the Pins and Net connects to Design and then Close the window.

Select Power → Power Planning → Add Rings to add Power rings ‘around Core Boundary’.

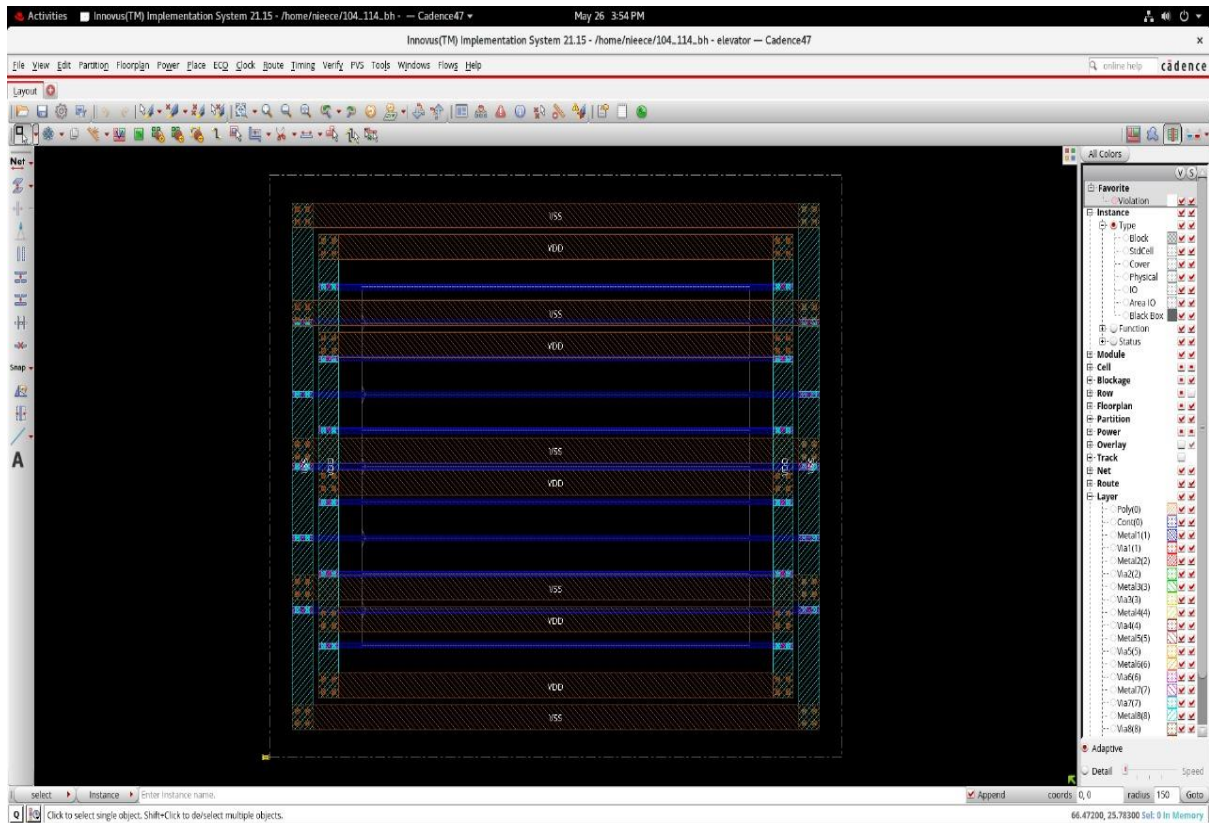


Similarly, Power Stripes are added using similar content to that of Power Rings.

## Stripes



## 32-BIT ALU

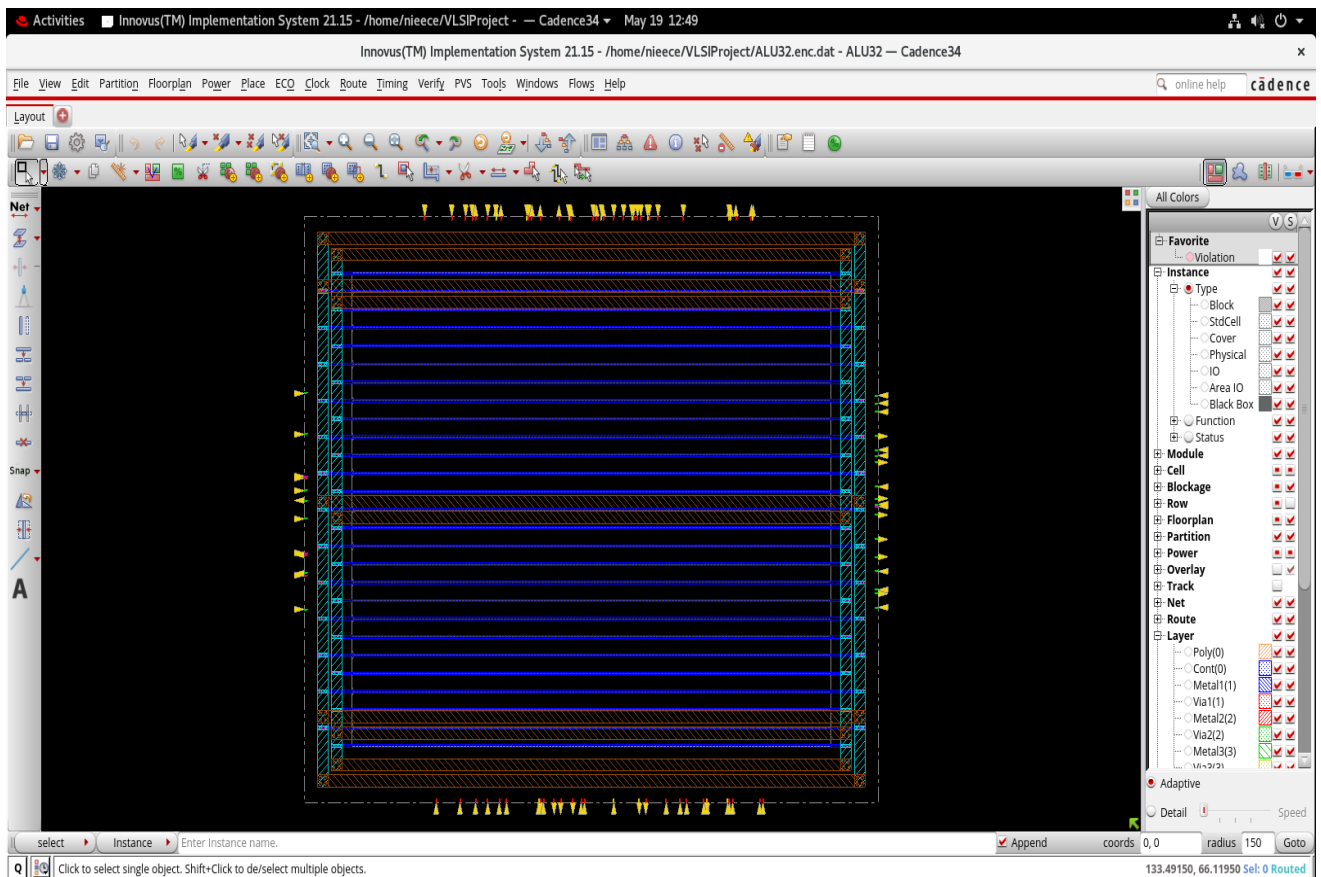
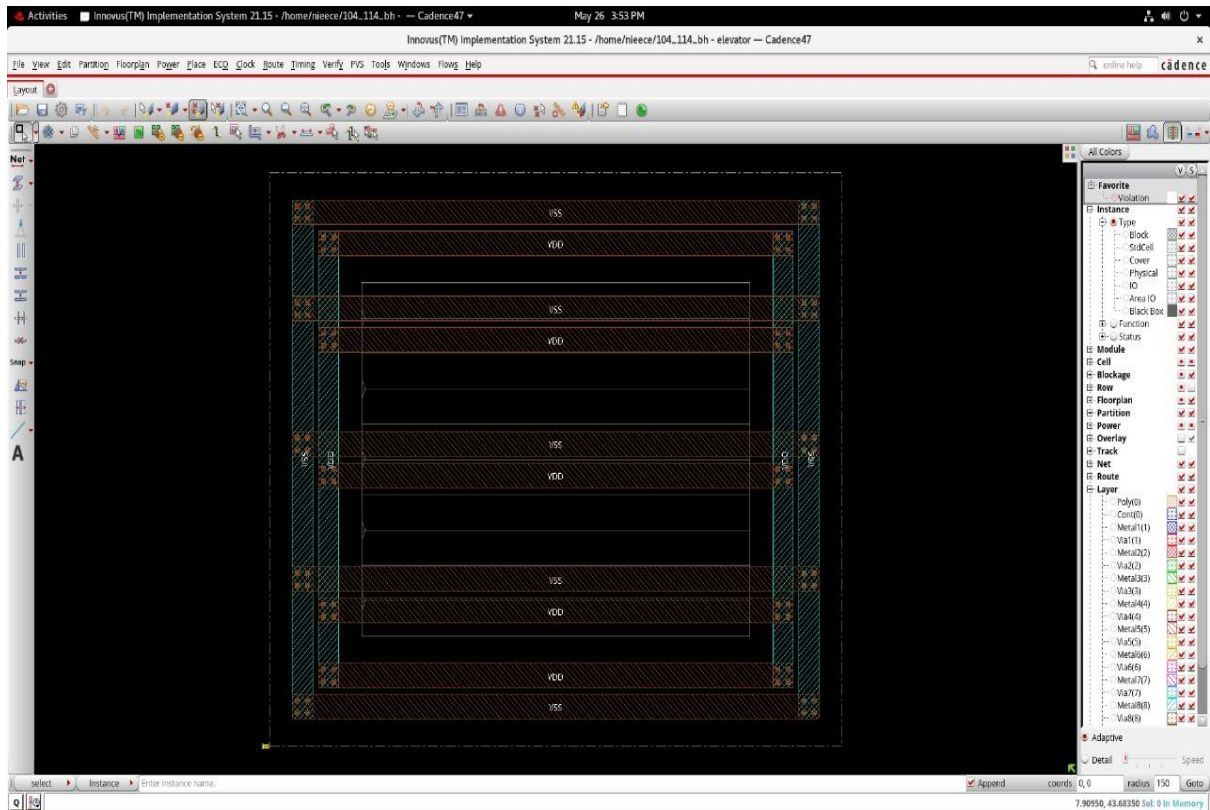


### 3. Routing

- Execute global routing to plan rough signal paths.
- Assign tracks for routing during track assignment.
- Perform detailed routing with exact wire geometry.
- Ensure DRC and ERC rules are met during routing.
- Use NDRs, shielding, and differential routing as needed.
- Fix antenna violations and improve signal integrity.



## 32-BIT ALU



## Pre-Routing Timing Report (Hold)

```

Activities Terminal May 19 14:47
niecee@Cadence35:~/VLSIP

File Edit View Search Terminal Help
Starting delay calculation for Hold views
AAE INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: ALU32
# Design Mode: 90nm
# Analysis Mode: PPMC Non-OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Calculate delays in BcWc mode...
Start delay calculation (fullDC) (1 T). (MEM=2215.88)
*** Calculating scaling factor for min_timings libraries using the default operating condition of each library.
Total number of fetched objects 1867
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=2275.09 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2275.09 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.2 real=0:00:00.0 totSessionCpu=0:08:08 mem=2275.1M)

-----
timeDesign Summary
-----
Hold views included:
best

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | 0.000 | N/A | 0.000 |
| TNS (ns): | 0.000 | N/A | 0.000 |
| Violating Paths: | 0 | N/A | 0 |
| All Paths: | 0 | N/A | 0 |
+-----+-----+-----+-----+

Density: 93.075%
Routing Overflow: 0.04% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.31 sec
Total Real time: 1.0 sec
Total Memory Usage: 2208.570312 Mbytes
*** timeDesign #7 [finish] : cpu/real = 0:00:00.3/0:00:00.3 (1.0), totSession cpu/real = 0:08:07.6/1:08:44.2 (0.1), mem = 2208.6M
Innovus 8>

```

## Pre-Routing Timing Report (Setup)

```

Activities Terminal May 19 14:47
niecee@Cadence35:~/VLSIP

File Edit View Search Terminal Help
Total Real time: 1.0 sec
Total Memory Usage: 2239.949219 Mbytes
*** timeDesign #4 [finish] : cpu/real = 0:00:00.4/0:00:01.0 (0.4), totSession cpu/real = 0:08:02.0/1:07:31.9 (0.1), mem = 2239.9M
Innovus 8> *** timeDesign #5 [begin] : totSession cpu/real = 0:08:02.0/1:07:32.8 (0.1), mem = 2239.9M
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=2239.9M)

-----
timeDesign Summary
-----
Setup views included:
worst

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns): | -1.110 | N/A | -1.110 |
| TNS (ns): | -33.066 | N/A | -33.066 |
| Violating Paths: | 33 | N/A | 33 |
| All Paths: | 66 | N/A | 66 |
+-----+-----+-----+-----+

+-----+-----+-----+-----+
| | Real | | Total |
| DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0.000 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

Density: 93.075%
Routing Overflow: 0.04% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.15 sec
Total Real time: 1.0 sec
Total Memory Usage: 2240.113281 Mbytes
*** timeDesign #5 [finish] : cpu/real = 0:00:00.2/0:00:00.7 (0.2), totSession cpu/real = 0:08:02.2/1:07:33.5 (0.1), mem = 2240.1M
Innovus 8>

```

## Power\_Report:

```

Activities Terminal May 19 11:08
niecee@Cadence35:~/CSA
File Edit View Search Terminal Help

Total Power
-----
Total Internal Power: 0.00212120      64.2623%
Total Switching Power: 0.00055982      16.9599%
Total Leakage Power: 0.00061983      18.7778%
Total Power: 0.00330084
-----

Group              Internal Power    Switching Power    Leakage Power    Total Power    Percentage (%)
-----
Sequential          0              0              0              0              0
Macro               0              0              0              0              0
IO                  0              0              0              0              0
Combinational       0.002121      0.0005598      0.0006198      0.003301      100
Clock (Combinational) 0              0              0              0              0
Clock (Sequential)  0              0              0              0              0
-----
Total               0.002121      0.0005598      0.0006198      0.003301      100
-----

Rail              Voltage    Internal Power    Switching Power    Leakage Power    Total Power    Percentage (%)
-----
VDD               0.9       0.002121      0.0005598      0.0006198      0.003301      100
-----

* Power Distribution Summary:
* Highest Average Power:      rca0/g146_4319 (ADDFX1):      0.0006065
* Highest Leakage Power:      rca0/g146_4319 (ADDFX1):      8.448e-05
* Total Cap: 5.28018e-14 F
* Total instances in design: 11
* Total instances in design with no power: 0
* Total instances in design with no activity: 0
* Total Fillers and Decap: 0
-----

** INFO: (VOLTUS_POWR-3465): There are 0 decaps and 0 fillers in the design
Ended Static Power Report Generation: (cou=0.00:00, real=0.00:00.

```

## Area\_Report

```

1
innovus 2> report_area
      Hinst Name      Module Name      Inst Count      Total Area
-----
ALU32                  1765          12491.878
innovus 3>

```

## Design Optimization:

To optimize the Design, Select ECO → Optimize Design → Design Stage [PreCTS] → Optimization Type – Setup → OK



## Optimized\_Report

```

May 19 11:09
niece@Cadence35:~/CSA
File Edit View Search Terminal Help
**optDesign ... cpu = 0:00:05, real = 0:00:04, mem = 1742.1M, totSessionCpu=0:01:22 **

-----
optDesign Final Summary
-----

Setup views included:
worst_case

-----
| Setup mode | all | default |
-----
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
-----

-----
| DRVs | Real | Total | |
|---|---|---|---|
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
|-----|-----|-----|
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
|-----|-----|-----|

Density: 68.103%
Routing Overflow: 0.00% H and 0.00% V

-----
**optDesign ... cpu = 0:00:05, real = 0:00:05, mem = 1742.9M, totSessionCpu=0:01:22 **
*** Finished optDesign ***
Disable CTE adjustment.
#optDebug: ft-D <x 1 0 0 0>
**place.opt design ... cpu = 0:00:05, real = 0:00:05, mem = 1750.2M **
*** Finished GigaPlace ***

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPEXT-6197 3 The Cap table file is not specified. Thi...
WARNING IMPEXT-3530 3 The process node is not set. Use the com...
WARNING IMPSP-12502 1 Slack driven placement is disabled becau...
WARNING TMAPSP-9025 1 No scan chain specified/traced.

```

#### 4. Clock Tree Synthesis (CTS)

- Identify and group clock sources and sinks.
- Insert buffers/inverters to balance clock delay.
- Minimize clock skew across all flip-flops.
- Apply useful skew to improve timing margins.
- Maintain insertion delay within acceptable limits.
- Ensure DRC and OCV compliance in clock network.

#### Source ccopt.spec code:

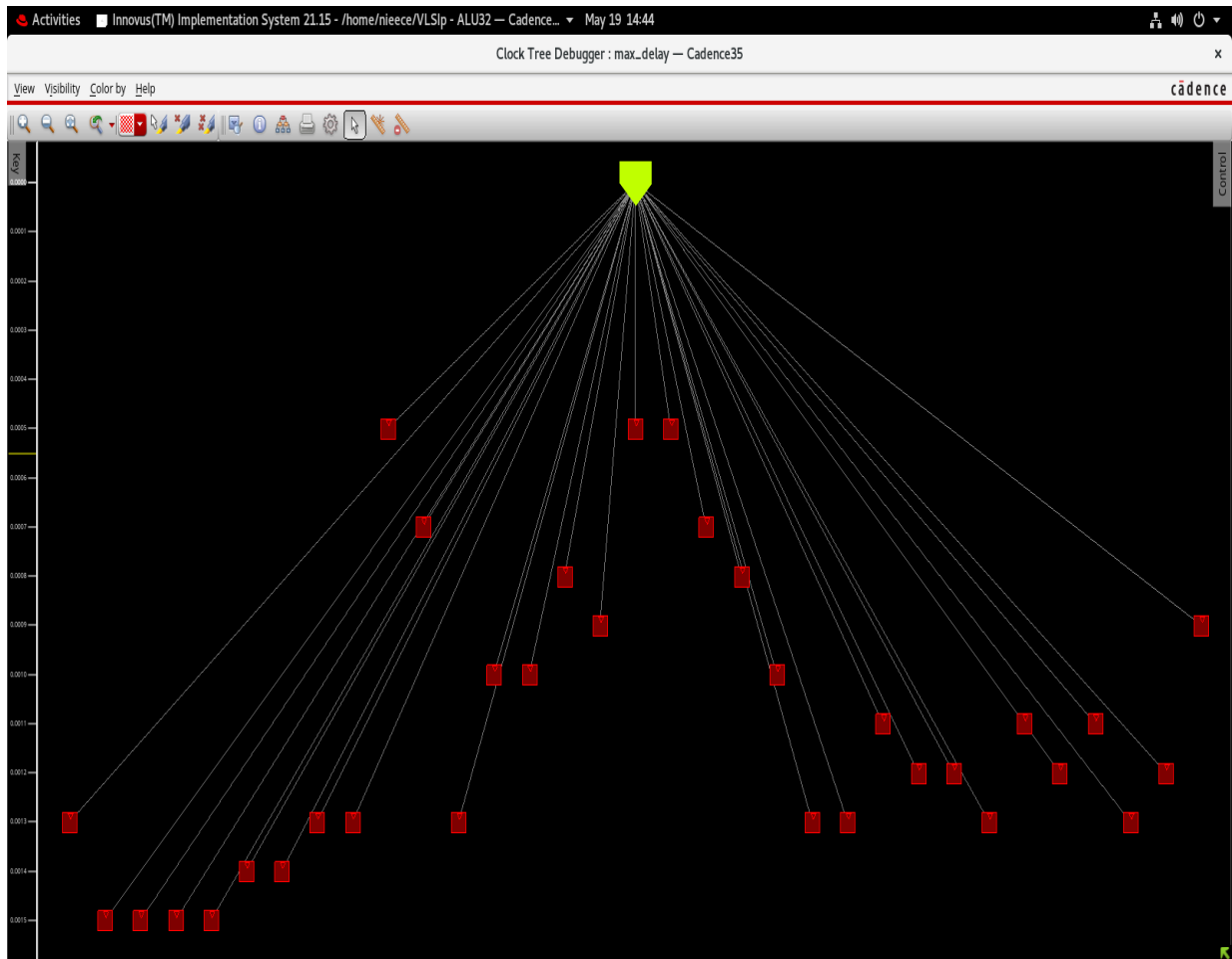


```

add_ndr -width {Metal1 0.12 Metal2 0.14 Metal3 0.14 Metal4 0.14 Metal5 0.14 Metal6 0.14 Metal7 0.14 Metal8 0.14 Metal9 0.14 } -spacing {Metal1 0.12 Metal2 0.12 Metal3 0.12
Metal4 0.12 Metal5 0.12 Metal6 0.12 Metal7 0.12 Metal8 0.12 Metal9 0.12 } -name 2w2s_n
create_route_type -name clkroute -non_default_rule 2w2s -bottom_preferred_layer Metal5 -top_preferred_layer Metal6
set_ccopt_property route_type clkroute -net_type trunk
set_ccopt_property route_type clkroute -net_type leaf
set_ccopt_property buffer_cells {CLKBUF8 CLKBUF12}
set_ccopt_property inverter_cells {CLKINV8 CLKINV12}
set_ccopt_property clock_gating_cells TLANTNTSCA*
create_ccopt_clock_tree_spec -file ccopt.spec
  
```

#### CTS (tree)

## 32-BIT ALU



### 5. Post-Route Optimization

- Insert buffers to fix delay or transition violations.
- Resize cells to meet timing or reduce power.
- Promote nets to higher metal layers for speed.
- Rewire critical nets for improved performance.
- Resolve timing, SI, and congestion issues post-route.

#### Post-Route Optimization Report Summary:

```

Activities Terminal May 19 11:09
niecee@Cadence35:~/CSA

File Edit View Search Terminal Help
**optDesign ... cpu = 0:00:05, real = 0:00:04, mem = 1742.1M, totSessionCpu=0:01:22 **

-----
optDesign Final Summary
-----

Setup views included:
worst_case

-----+-----+-----+
| Setup mode | all | default |
-----+-----+-----+
| WNS (ns): | 0.000 | 0.000 |
| TNS (ns): | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 |
| All Paths: | 0 | 0 |
-----+-----+-----+

-----+-----+-----+
| DRVs | Real | Total |
-----+-----+-----+
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
-----+-----+-----+

Density: 68.103%
Routing Overflow: 0.00% H and 0.00% V

-----
**optDesign ... cpu = 0:00:05, real = 0:00:05, mem = 1742.9M, totSessionCpu=0:01:22 **
*** Finished optDesign ***
Disable CTE adjustment.
#optDebug: FT-D <X 1 0 0 0>
**place_opt design ... cpu = 0:00:05, real = 0:00:05, mem = 1750.2M **
*** Finished GigaPlace ***

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPEXT-6197 3 The Cap table file is not specified. Thi...
WARNING IMPEXT-3530 3 The process node is not set. Use the com...
WARNING IMPSP-12502 1 Slack driven placement is disabled becau...
WARNING IMPSP-9025 1 No scan chain specified/traced.

```

## 6. RC Extraction

- Extract parasitic R and C from the physical layout.
- Generate SPEF file for accurate STA.
- Use coupled or decoupled extraction based on design.
- Improve accuracy of delay and power estimation.
- Apply signoff tools like QRC for final extraction.
- Include cross-coupling effects for critical nets.

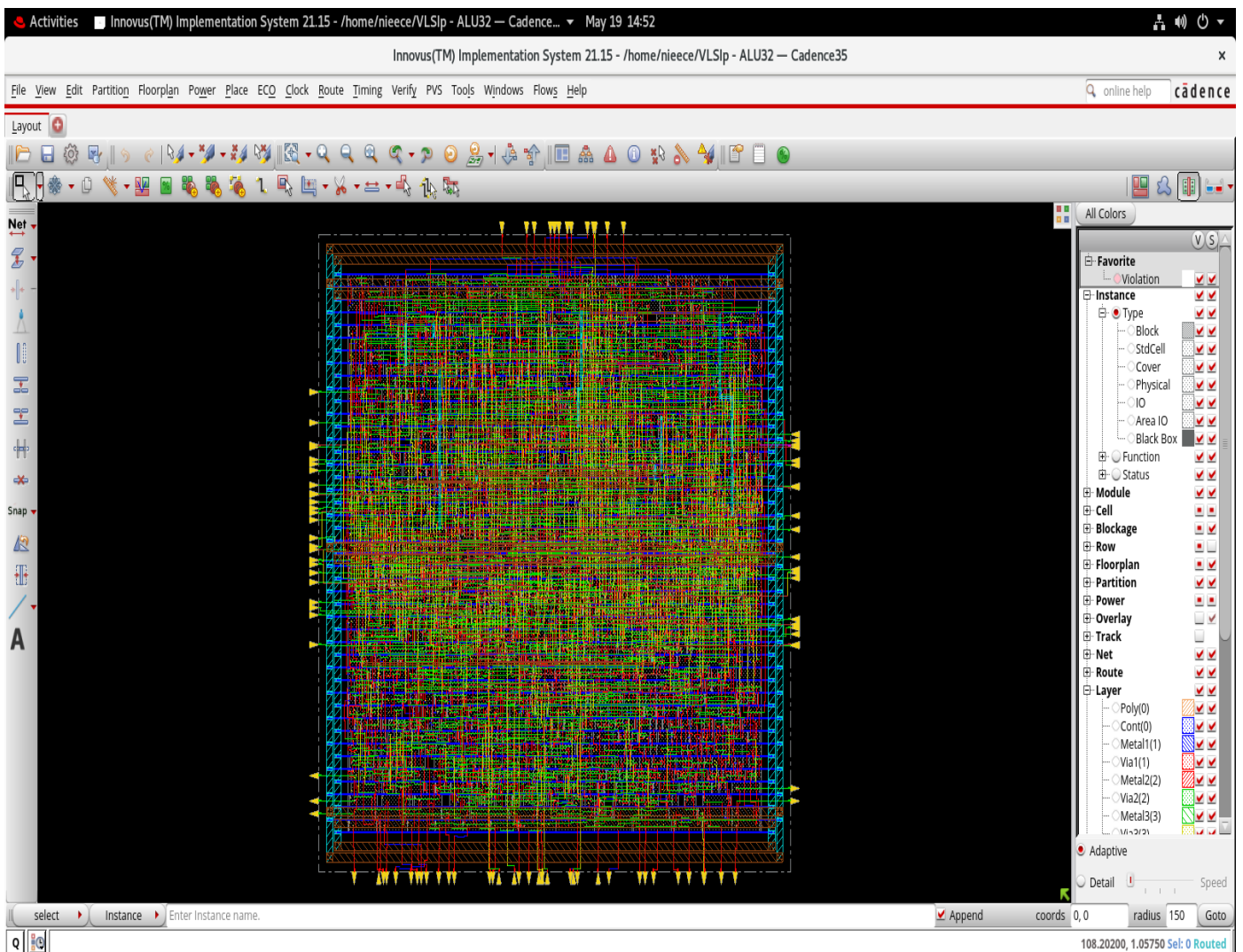
## 7. GDSII Generation



## 32-BIT ALU

- Stream out final layout in GDSII format with layer maps.
- Insert fill cells, tap cells, and well ties as required.
- Perform LVS to match layout with schematic.
- Run DRC to ensure rule compliance for manufacturing.
- Check antenna, metal density, and CMP violations.
- Finalize design for tape-out and fabrication.

### Physical Design:





## CONCLUSION

The 32-bit Arithmetic Logic Unit (ALU) is a crucial digital component designed to perform a wide range of arithmetic and logical operations such as addition, subtraction, bitwise AND, OR, XOR, and comparison operations. It serves as the core computational unit in processors, enabling execution of instructions in microcontrollers, CPUs, and DSPs. A well-designed ALU efficiently handles these operations while balancing performance, area, and power.

In the ASIC design flow, the 32-bit ALU can be implemented using Cadence Genus for synthesis and Cadence Innovus for physical design. The Verilog RTL description of the ALU is first synthesized in Genus into a gate-level netlist using standard cell libraries. During this step, optimizations for timing, area, and power are applied to ensure efficient operation across process-voltage-temperature (PVT) corners.

The generated netlist is then imported into Cadence Innovus, where the physical design takes place. The tool performs floorplanning, placement, clock tree synthesis, routing, and timing signoff, ensuring the ALU logic fits within the defined chip area and meets all design rules and performance constraints.

Overall, the 32-bit ALU is a fundamental module in digital systems, especially within CPUs and embedded architectures. Its scalability and versatility make it an ideal candidate for VLSI implementation, and it is commonly realized using industry-standard EDA tools like Genus and Innovus to meet modern silicon performance requirements.

## REFERENCES

1. M. Ramesh and B. B. Reddy, "ASIC Design and Implementation of 32 Bit Arithmetic and Logic Unit," *IEEE International Conference on Electronics, Communication and Aerospace Technology (ICECA)*, 2018, pp. 923–926. doi: 10.1109/ICECA.2018.8474762
2. R. T. Kavitha and G. L. P. Reddy, "A Novel Design and Implementation of 32-Bit Hybrid ALU," *IEEE International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)*, 2017, pp. 1–4. doi: 10.1109/ICIIECS.2017.8275916
3. S. Sahu and S. Sahu, "Design and Analysis of FPGA Based 32 Bit ALU Using Reversible Gates," *IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*, 2017, pp. 1–6. doi: 10.1109/ICECCT.2017.8117876
4. V. Raj and S. G. Goud, "ASIC Implementation of 32 and 64 Bit Floating Point ALU Using Pipelining," *IEEE International Conference on Electrical, Electronics, Communication, Computer and Optimization Techniques (ICEECOT)*, 2017, pp. 1075–1079. doi: 10.1109/ICEECOT.2017.8284647