## Compiler Construction

Chapter 7: Code Shape

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## Code shape



#### Translation choices

- Runtime speed
- Memory requirement
- Register optimization

For example, how should we translate the **switch** statement in C?

- A series of if-else
- Array access
- Hashing



	Source Code	Low-Le	evel, Three-Addre	ss Code
Code	x + y + z	$\begin{array}{l} r_1 \;\leftarrow\; r_x + r_y \\ r_2 \;\leftarrow\; r_1 + r_z \end{array}$	$\begin{array}{l} r_1 \;\leftarrow\; r_x + r_z \\ r_2 \;\leftarrow\; r_1 + r_y \end{array}$	$ r_1 \leftarrow r_y + r_z \\ r_2 \leftarrow r_1 + r_x $
Tree	x y z	+ r <sub>z</sub>	+ r <sub>y</sub>	r <sub>y</sub> r <sub>z</sub>

**FIGURE 7.1** Alternate Code Shapes for x + y + z.

How should we translate x+y+z into 3-address codes?

• 
$$r1 = rx + rz$$
;  $r2 = r1 + ry$ ;

What if the expression is x+2+3?



### Arithmetic operators



- Base-offset for variables
- Immediate for constants
- Function call
- Automatic type conversion
- Assignment



Given an activation record with the base address in r\_arp, we may load variable a into a temporary register r\_a by

loadI @a 
$$\rightarrow$$
 r\_1 loadAO r\_arp, r\_1  $\rightarrow$  r\_a

#### Arithmetic operators



```
expr(node) {
     int result, t1, t2;
     switch(type(node)) {
          case x, ÷, +, -:
               t1 ← expr(LeftChild(node));
               t2 ← expr(RightChild(node));
               result ← NextRegister();
                                                                    (b) Abstract Syntax Tree for
               emit(op(node), t1, t2, result);
                                                                              a - bxc
               break:
          case NAME:
               entry ← STLookup (node);
               result ← ValueIntoRea(entry);
                                                                   loadI
                                                                               0a
                                                                                           \Rightarrow r<sub>1</sub>
               break:
                                                                   loadA0
                                                                               rarn, r1
                                                                                           \Rightarrow r_2
          case NUMBER:
                                                                   loadI
                                                                               ØЬ
                                                                                           ⇒ r<sub>3</sub>
               num ← NumberFromNode(node):
                                                                    loadA0
                                                                               rarp, r3
                                                                                           \Rightarrow r<sub>4</sub>
               result ← NumberIntoReg(num);
                                                                   loadI
                                                                               @c
                                                                                           \Rightarrow r_5
               break:
                                                                   loadA0
                                                                               r_{arp}, r_5
                                                                                           \Rightarrow r<sub>6</sub>
                                                                   mu1t
                                                                               r_4, r_6
     return result;
                                                                                           ⇒ r<sub>7</sub>
                                                                   sub
                                                                               r2. r7
                                                                                           \Rightarrow r<sub>8</sub>
             (a) Treewalk Code Generator
                                                                          (c) Naive Code
```

■ FIGURE 7.2 Simple Treewalk Code Generator for Expressions.

## Other concerns in arithmetic operations



Commutativity, associativity, and number systems

- Common subexpression help improving the code quality
- However, floating-point operations should NOT be re-ordered

Function calls in an expression

- If the return value is put in a register,
- The change in evaluation order may have side effects to the call

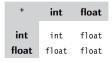
Solution: activation record

# Other concerns in arithmetic operations



#### Mixed-type expressions

• The compiler must insert the conversion code



Conversion Table for +

## Assignment operator



- Evaluate the right-hand side of the assignment to a value
- Evaluate the left-hand side of the assignment to a location
- Store the right-hand side value into the left-hand side location
- R-value: an expression is evaluated to a value
- L-value: an expression is evaluated to a location

# Reducing demand for registers



```
loadI
                                                             loadI
                           \Rightarrow r_1
                                                                                        \Rightarrow r<sub>1</sub>
loadA0
              r_{arn}, r_1 \Rightarrow r_2
                                                             loadA0
                                                                           r_{arn}, r_1 \Rightarrow r_1
loadI
                                                             loadI
loadA0
                                                             loadA0
             r_{arp}, r_3 \Rightarrow r_4
                                                                           r_{arp}, r_2 \Rightarrow r_2
I had I
                                                             loadI
                           \Rightarrow r<sub>5</sub>
loadA0
                                                             loadA0
             r_{arp}, r_5 \Rightarrow r_6
                                                                           r_{arp}, r_3 \Rightarrow r_3
mult
              r_4, r_6 \Rightarrow r_7
                                                             mult
                                                                           r_2, r_3 \Rightarrow r_2
sub
             r_2, r_7 \Rightarrow r_8
                                                             sub
                                                                           r_1, r_2 \Rightarrow r_2
(a) Code from Fig. 7.2(c)
                                                        (b) Code After Register Allocation
loadI
                           \Rightarrow r_1
                                                             loadI
                                                                                        \Rightarrow r<sub>1</sub>
loadA0
             r_{arn}, r_1 \Rightarrow r_2
                                                             loadA0
                                                                           r_{arn}, r_1 \Rightarrow r_1
loadI
                                                             loadI
                           \Rightarrow r<sub>3</sub>
                                                                                        \Rightarrow r_2
loadA0
             r_{arp}, r_3 \Rightarrow r_4
                                                             loadA0
                                                                           r_{arn}, r_2 \Rightarrow r_2
mult
                                                             mult
             r_2, r_4 \Rightarrow r_5
                                                                           r_1, r_2 \Rightarrow r_1
loadI
                                                             loadI
             @a
                           \Rightarrow r_6
                                                                                        \Rightarrow r_2
loadA0
              r_{arp}, r_6 \Rightarrow r_7
                                                             1oadA0
                                                                           r_{arp}, r_2 \Rightarrow r_2
sub
              r_7, r_5 \Rightarrow r_8
                                                             sub
                                                                           r_2, r_1 \Rightarrow r_1
  (c) Evaluate b x c First
                                                        (d) Code After Register Allocation
```

■ FIGURE 7.3 Rewriting a - b x c to Reduce Demand for Registers.

## Accessing parameter values



#### Call-by-value

• Similar to local variable, using AR

#### Call-by-reference

- Save the address (pointer) into the AR. The retrieval needs 2 dereferencing steps
- Passing parameter d

```
loadI @d -> r1
loadAO r_arp, r_1 -> r_2
load r_2 -> r3
```

#### Access methods for values



- Variables stored in a register
- Variables stored in memory: base + offset
- Local variables: r\_arp + offset
- Local variables of surrounding scopes: level information e.g. from access links/global display
- Static and global variables: addresses based on labels e.g. loadI <label> -> r\_i
- Variables passed as parameters
- Variables stored in the heap
- Access methods for aggregates e.g. objects, structs, vectors, strings

#### Structure



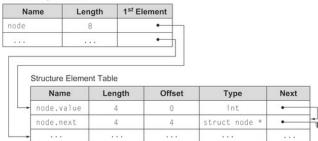
- C's struct
- Pascal's **record**
- Object's record

#### Structure layouts



#### Linkedlist

#### Structure Layout Table



## Structure layout



```
struct example {
  int fee;
  double fie;
  int foe;
  double fum;
};
```

0	4	8 12	16	20	24	28	
	fee	 fie	1	oe ·		fum	

#### Elements in Declaration Order

0	4	8	12	16	1	6
	fie		fum	f	ee	foe

Elements Ordered by Alignment

### Object reference

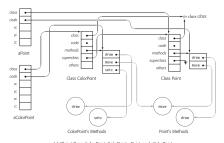






(a) Class Definitions

(b) Corresponding Scope Tables



(c) Object Records for Point, ColorPoint, aPoint, and aColorPoint

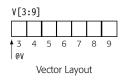
■ FIGURE 6.3 Object Layout, Linking, and Inheritance.



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#### Vector addressing





```
      subI
      r_i 3
      r_1 // (i - lower bound)

      multI
      r_1 4
      r_2 // x element length (4)

      add
      r_0v
      r_2
      r_3 // address of v[i]

      load
      r_3
      r_v[i] // get the value of v[i]
```

ullet The false zero of a vector v is the address where v[0] would be

The location of v[i] is  $(i - low) \times w$  where

- low is the lower bound
- w is the element length
- Then, v[0] = v low \* w



# Storing and accessing arrays



Base and offset calculation

**Example**: accessing a [4] whose element in a requires 4 bytes

1 1	r 0- 0		0	# 1	
load	[ @a_0		r_a0	# base	
mult	I r_i,	4	r_2	# offset size	
addI	r_a0,	r_2	r_3	# add offset	
load	r_3		r_ai		

However, the the first index is not 0, we need to adjust the offset calculation

### Multiplication to addition



If the offset size  $\mathbf{w}$  in  $\mathbf{r}_i * \mathbf{w}$  is a power of two, we can use  $\mathbf{shift}$  operation instead

- Fewer processing cycle
- ullet E.g., lshiftI r\_i 2 -> r\_2 is equivalent with r\_i \* 4

## String representation





# String assignment



#### a[1] = b[2];

Generated codes depend on the target machine instruction set

```
loadl @b -> r_b
cloadl r_b, 2 -> r_2
loadl @a -> r_a
cstoreAl r_2 -> r_a, 1
```

Or

```
loadI 0x0000FF00 ⇒ rc2 // mask for 2nd char
loadI 0xFF00FFFF ⇒ rc124 // mask for chars 1, 2, & 4
loadI
         @b
                   ⇒ r@h // address of b
load
                    \Rightarrow r<sub>1</sub> // get 1st word of b
         rah
         r_1.r_{C2} \Rightarrow r_2 // mask away others
and
lshiftI r_2.8 \Rightarrow r_3 // move it over 1 byte
loadI
         @a
                 ⇒ r@a // address of a
load
         rea
                  ⇒ r4 // get 1st word of a
and
         r4, rc124 ⇒ r5 // mask away 2nd char
         r_3, r_5 \Rightarrow r_6 // put in new 2nd char
or
                  ⇒ r@a // put it back in a
store
         r6
```

## String assignment



```
loadI
                                         ⇒ r@b
                      loadAI r@b.-4 ⇒ r1
                                                       // get b's length
                      loadI
                                         ⇒ rea
                      loadAI r_{@a}, -4 \Rightarrow r_2
                                                      // get a's length
                      cmp_LT r_2, r_1 \Rightarrow r_3 // will b fit in a?
                      cbr
                                 r_3 \rightarrow L_{SOV}, L_1
                                                      // raise overflow
                  L<sub>1</sub>: loadI 0
                                         ⇒ r<sub>4</sub>
                                                      // counter
                      cmp_LT r_4, r_1 \Rightarrow r_5
                                                      // more to copy?
a = b:
                      cbr
                                 r_5 \rightarrow L_2, L_3
                  L<sub>2</sub>: cloadAO r_{\text{mb}}, r_4 \Rightarrow r_6 // get char from b
                      cstoreAO r_6 \Rightarrow r_{@a}, r_4 // put it in a
                                                      // increment offset
                      addI
                                r_4.1 \Rightarrow r_4
                      cmp_LT r_4, r_1 \Rightarrow r_7
                                                      // more to copy?
                      cbr r_7 \rightarrow L_2, L_3
                  L3: storeAI r_1 \Rightarrow r_{\Theta_0}, -4 // set length
```

## String assignment



```
loadI
                                             @b \Rightarrow r_{@b}
                                                               // get pointers
                                   loadI
                                             @a
                                                      ⇒ r@a
                                             NULL \Rightarrow r<sub>1</sub> // terminator
                                   loadI
t_1 = a;
                                   cload
                                             r_{\text{@b}} \Rightarrow r_2 // get next char
t_2 = b:
                                                      \Rightarrow r<sub>@a</sub> // store it
                             L1: cstore r2
do {
                                   addI
                                             r_{\text{Mb}}, 1 \Rightarrow r_{\text{Mb}} // bump pointers
  *t_1++ = *t_2++;
                                   addI
                                             r_{@a}, 1 \Rightarrow r_{@a}
} while (*t2 != '\0')
                                   cload
                                             r_{\text{@b}} \Rightarrow r_2 // get next char
                                   cmp_NE r_1, r_2 \Rightarrow r_4
                                   cbr
                                             r_4 \rightarrow L_1, L_2
                                                                   // next statement
                              L2: nop
```

# Other string operations



- String concatenation
- String length

# Array storage layout



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#### Row-major and column-major choices

٨	1,1	1,2	1,3	1,4
Α	2,1	2,2	2,3	2,4

1,1	1,2	1,3	1,4	2,1	2,2	2,3	2,4
O 4	1 8	3 1	2 1	6 2	0 2	4 2 @A[2	8 ,3]

#### Let

- low1 be the first index of the first dimension
- low2 be the first index of the second dimension
- high1 be the first dimension's upper bound
- high\_2 be the second dimension's upper bound
- len\_k = high\_k low\_k + 1 be the size of dimension k
- w be the size of each element

The location of A[i,j] is

$$A + (i - low_1) * len_2 * w + (j - low_2) * w$$



#### We can simplify

#### into

```
A + i * len_2 * w - low_1 * len_2 * w + j * w - low_2 * w

= A + (i * len_2 * w) + (j * w) - (low_1 * len_2 * 2 - low_2 * w)

= A + (i * len_2 * w) + (j * w) + A_0

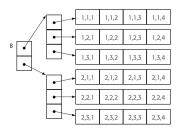
= A_0 + (i * len_2 + j) * w
```

#### If i, j are $in r_i$ , $r_j$ then

# High dimensional array



#### Indirection address



■ FIGURE 7.4 Indirection Vectors in Row-Major Order for B[1:2,1:3,1:4].

#### To access B[i,j,k]

```
loadI B_0 -> r_B0 // false zero
multI r_i 4 -> r_1 // pointer size = 4
loadA0 r_B0 r_1 -> r_2 // Address of B[i]
multI r_j 4 -> r_3 // pointer size = 4
loadA0 r_2 r_3 -> r_4 // Address of B[i,j]
muliT r_k 4 -> r_5 // w = 4
loadA0 r_4 r_5 -> r_b // B[i,j,k]
```

#### Dope vectors



#### A descriptor for an actual parameter array

```
program main;
begin;
declare x(1:100,1:10,2:50),
    y(1:10,1:10,15:35) float;
call fee(x);
call fee(y);
end main;
procedure fee(A)
declare A(*,*,*) float;
...
end fee;
```

Α	
A	0у <sub>0</sub>
	1
	10
	1
	10
	15
	35

(a) PL/I Code That Passes Whole Arrays (b) Dope Vector for the First Call Site

 $0x_0$ 

(c) Dope Vector for the Second Call Site

■ FIGURE 7.5 Dope Vectors.

### Range check



A program that access an out-of-bound element is not well formed. Naive range checking

```
for i in 1 .. n
    for j in 1 .. m
    if low_1 <= i <= high_1 and low_2 <= j <= high_2 then
        access a[i,j]
    else
        throw OutOfBoundException</pre>
```

#### Optimized version

```
if low_1 <= 1 <= and n <= high_1 and low_2 <= 1 and m <= high_2 then
    for i in 1 .. m
        access a[i,j]
else
    throw OutOfBoundException</pre>
```

We can move the range check out of the two loops