Operating Systems

Tutorial

Week 1

TOC

Submission & git

Quick Lecture Recap

Assignment 1 Primer & C Programming

References

Intro

- Problems with sheet 0?
- Did someone install Arch Linux?
- Did you test your C toolchain?
- Other issues?

Section 1

Submission & git

Submission

- Submissions by everybody on her/his own
- Teamwork is allowed, copy-pasting is not allowed!
- If you plagiarize, you get no points.
- use the folder to submit (note to self: show it)

Settings

- Once: Go to settings → visibility and set
  Project Visibility → Private
- Once: Add the base repository as upstream:

```
git remote add upstream
↪   git@gitlab.inf.uni-konstanz.de:matthias.rupp/betriebssysteme.git
```

basic git commands I

- List all associated remotes `git remote -v`
- Update from the base repository:

```
git fetch upstream
git merge upstream/master
git commit -am "merge updates"
git push
```

- Update from your own repository `git pull`
- Submit you work:

```
git add <folders and files>
git commit -m "<message>"
git push
```

basic git commands II

- Undo a commit without changing the files locally
  `git reset --soft HEAD~1`
- Reset your repository to the state of the latest commit
  `git reset --hard HEAD~1`
- Squashing 3 commits together `git rebase -i HEAD~3` and then select squash on all but the most recent commit.
- Show the differences between the last two commits
  `git diff HEAD HEAD~1`
- Show the log of commits `git log`
- Search text in files under version control `git grep`
- substitute commit hash instead of HEAD

basic git commands III

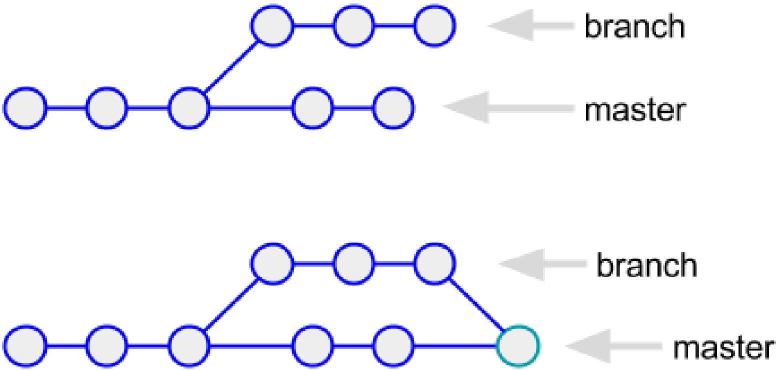


Figure: Git branching workflow [1]

basic git commands IV

- List existing branches `git branch -v`
- Switch branches `git checkout <branch>`
- Create and switch to a new branch
  `git checkout -b <branch name>`
- Delete branch locally `git branch -d <branch name>`
- Delete branch from remote
  `git push origin --delete <branch>`

basic git commands V

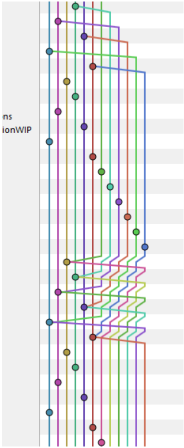


Figure: "I fucked up Git so bad it turned into Guitar Hero." [2]

Section 2

Quick Lecture Recap

Definition

"An operating system comprises computer programs that administrate the resources of a computer and make them available via interfaces." *Wikipedia*

Figure: The defintion given by Wikipedia. [3]

Overview

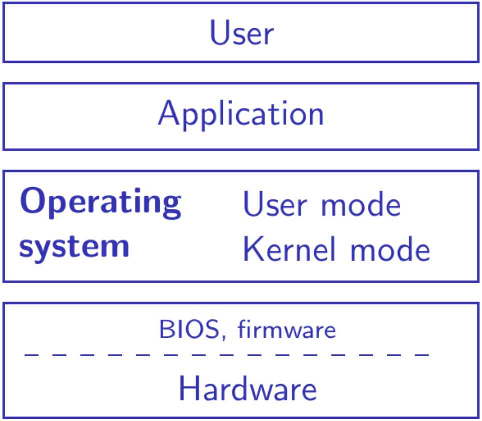


Figure: High level view on an OS. [4]

High-level Requirements

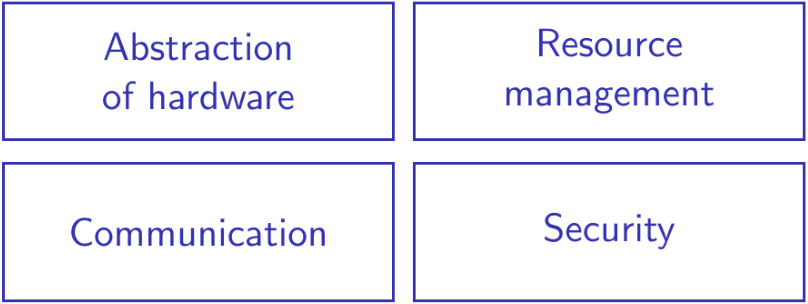


Figure: High-level requirements of an operating system. [4]

Topics

Introduction			
Virtualization	**Concurrency**	**Input/output**	**Security**
processes threads scheduling memory virtualization	theory deadlocks solutions	devices drivers mass storage file systems multimedia	cryptography threats counter measures
Closure			

Figure: Conceptual schedule of the course. [4]

Operating System Types

Custom OSes

- Robotics (e.g. for Mars Rovers)
- Automated Manufacturing
- Gaming Consoles (e.g. Playstation)

Mobile

- Android 76 %
- iOS 22 %

Tablet

- iOS 73 %
- Android 27 %

Desktop

- Windows 80 %
- OS X 15 %
- Linux 2 %

Server

- Cloud: Linux 90 %
- Supercomputers: Linux ~100 %
- Web servers: Linux 70–97 %
- Internet of Things: Linux 72 %
- Business: mostly Windows

Figure: Market share of broadband OS use cases. [4]

Computing Architectures

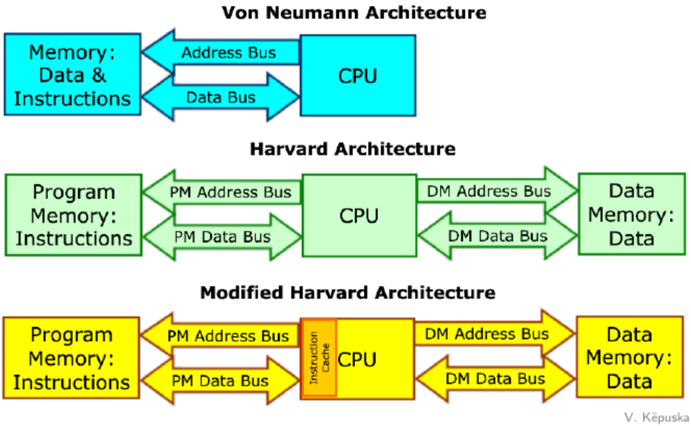


Figure: Von Neumann and Harvard architectures. [4]

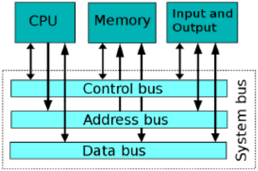
Bus Systems

What is a bus?

- Communication system
- Transfers data between computer(s) and/or component(s)
- Hardware, protocols
- Parallel vs. serial vs. network

Examples

- Serial ATA (SATA 3: 6 Gb/s)
- Universal Serial Bus (USB 4: 40 Gb/s)
- PCI express (PCIe 6: 64 Gb/s)
- InfiniBand (NDR: 100 Gb/s/link)



W. Nowicki (Wikipedia)

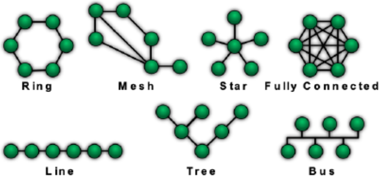


Figure: Bus system and topology examples. [4]

Chipset & Motherboard I

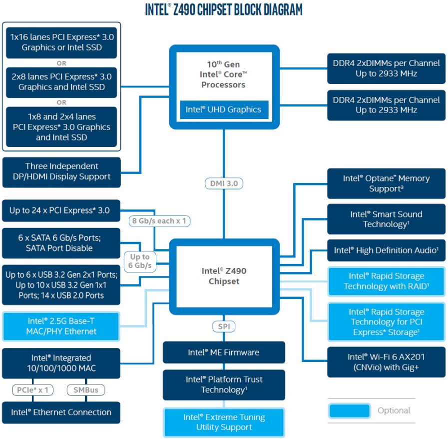


Figure: High Level Diagram of an Intel chipset. [5]

Chipset & Motherboard II

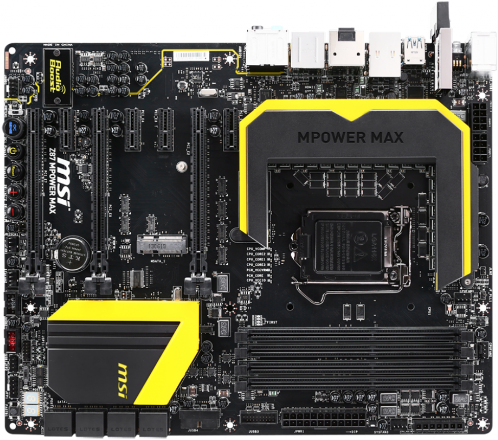


Figure: A modern moderboard (MSI Z87 MPOWER MAX. [6]

Processors I

- Exist different processor architectures e.g. x64_86, arm, PowerPC, ...
- MMU $\equiv$ IMC

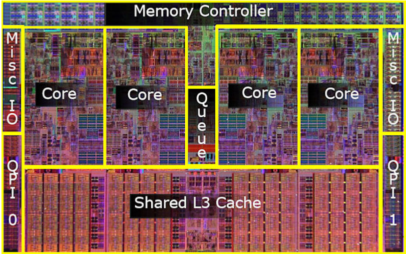


Figure: Picture of an i7. [7]

Processors II

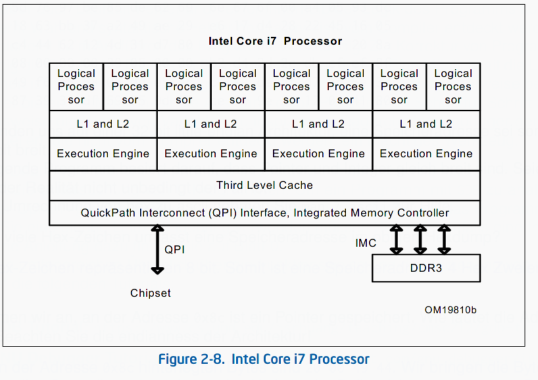


Figure: High Level Diagram of an Intel i7 processor. [5]

Processors III

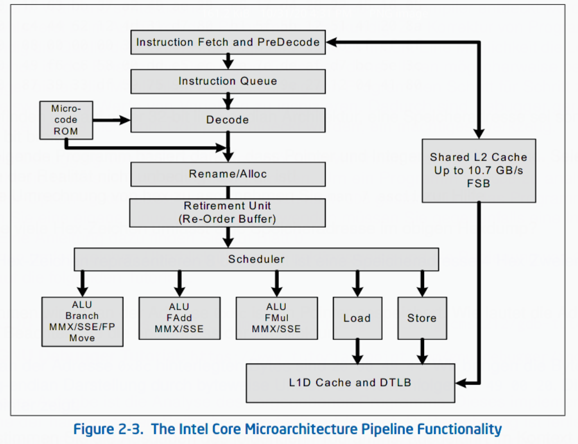


Figure: High Level Diagram of an Intel execution engine. [5]

Processors IV

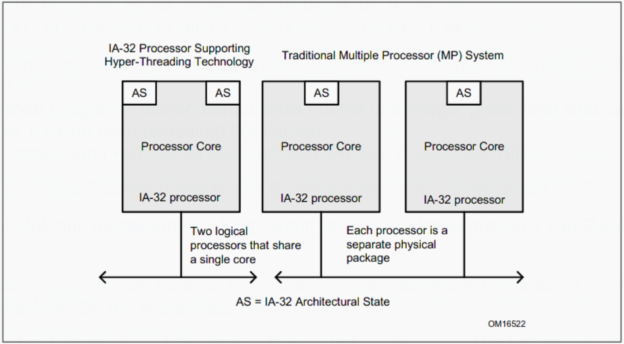


Figure 2-5. Comparison of an IA-32 Processor Supporting Hyper-Threading Technology and a Traditional Dual Processor System

Figure: Intel's Hyperthreadding compared to actual cores. [5]

Processors V

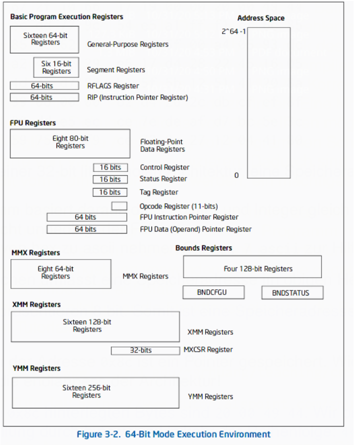


Figure: Registers on an x64 CPU. [5]

Random Access Memory I

- Most common: Double Data Rate Synchronous Dynamic Random Access Memory
- Current market technology: DDR4-SDRAM
- Bus/IO clock defines data rate (w/o prefetch):

$$\text{IO frequency } \cdot 2 \text{ DDR } \cdot 64 \text{ (bus width) } \cdot \frac{1}{8} \text{ (bits per byte)}$$

$$= \text{ effective data rate in bytes per seconds}$$

- 8-time prefetch enables theoretically 8 times the data rate (if all prefetches hit).

Random Access Memory II

- Realistically the latencies set the actual memory performance:
  1. Column Acess Strobe (CAS) — latency: How many cycles to serve data.
  2. row to column access time (tRCD): memory cell is read via row and column signals. Constant delay between signals is tRCD.
  3. precharge delay (tPR): Time to deliver necessary voltage for access
  4. Row active time (tRAS): Theoretically CAS + tRP + safety delay; amount of cycles to access cell after previous op.

Random Access Memory III

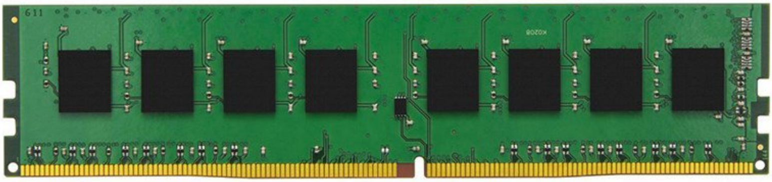


Figure: Picture of a DDR4-SDRAM unit. [8]

GPUs I

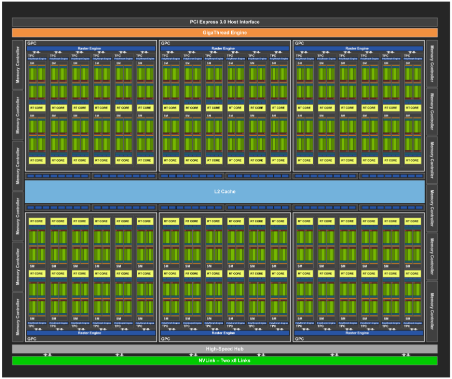


Figure: High level overview of the Nvidia Turing Architecture (here RTX 2080). [9]

GPUs II

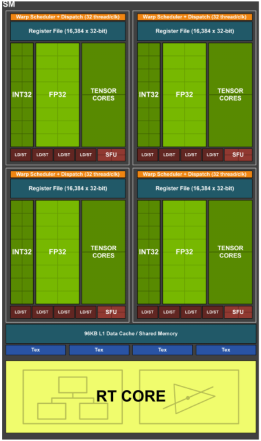


Figure: High level view on a single streaming multiprocessor. [9]

IO devices I

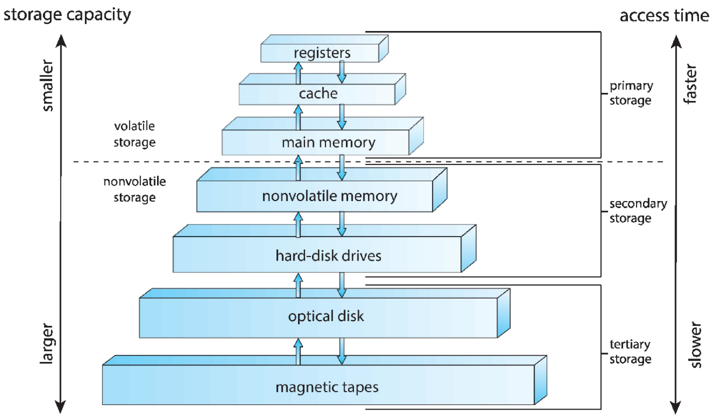


Figure: The Storage hierarchy implemented today. [10]

IO devices II

Level	1	2	3	4	5
Name	registers	cache	main memory	solid-state disk	magnetic disk
Typical size	< 1 KB	< 16MB	< 64GB	< 1 TB	< 10 TB
Implementation technology	custom memory with multiple ports CMOS	on-chip or off-chip CMOS SRAM	CMOS SRAM	flash memory	magnetic disk
Access time (ns)	0.25-0.5	0.5-25	80-250	25,000-50,000	5,000,000
Bandwidth (MB/sec)	20,000-100,000	5,000-10,000	1,000-5,000	500	20-150
Managed by	compiler	hardware	operating system	operating system	operating system
Backed by	cache	main memory	disk	disk	disk or tape

Movement between levels of storage hierarchy can be explicit or implicit

Figure: Details on costs and speed. [10]

IO devices III

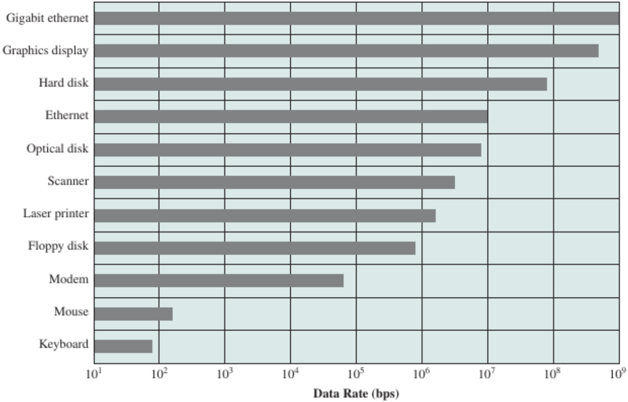


Figure 11.1 **Typical I/O Device Data Rates**

Figure: Rates of different IO devices. [10]

IO devices IV

- Character devices deal with streams of data
- Block devices deal with fixed block data
- Network devices are special [11] (don't show up in `/dev/`, ...)

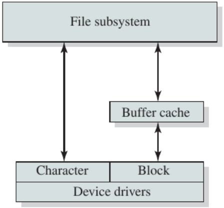


Figure 11.12 **UNIX I/O Structure**

Figure: The types of devices, as modeled in the UNIX standard. [10]

Up next

- Questions so far?
- Assignment sheet 1
- `C`

References I

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