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ABSTRACT

This thesis work details the designing process of two stage operational amplifier with indirect feedback compensation and with Miller compensation technique. The main objective of this thesis is to study the advantages of indirect feedback compensation in comparison with Miller compensation and how this technique can be applied to meet certain design specifications. The operational amplifiers are design with gpdk045nm CMOS technology process ideally for temperature range of - 40° C and 125° C. The two stage op-amp is designed to have a DC gain of about 60 dB and 60° Phase Margin. The proposed two stage op amp produces high gain Design and simulations results are verified using CADENCE tool. The proposed two stage op amp produces high gain Design and simulations results are verified using CADENCE tool. The indirect feedback compensation design showed similar simulation results as the Miller compensation technique; nevertheless, it showed a reduce in the compensation capacitor size, meaning a smaller design area, and an improvement in the phase margin from LHP zero. Also, the proposed design showed a higher unity gain frequency.

The ability of the method adopted, to use the smaller compensation capacitor, C_c , which improves the slew rate, also beneficial for the area of compensation circuit.

CHAPTER 1

INTRODUCTION

1.1 Background And Conceptual Principle

CMOS operational amplifiers are one of the most fundamental, versatile and integral building blocks of many analog and mixed-signal circuits and system. They are used in a wide range of applications such as comparators, differentiators, dc bias applications and many other applications. IC designers tend to design systems with a single dominated pole behaviour because these are easily analysed and can tolerate negative feedback without stability issues.

CMOS technology has been constantly scaling down establishing some challenges when designing operational amplifiers and others integrated circuits. Multiple stage amplifiers can be implemented to achieve higher gains circuit designs regardless of the limitations of the power supply voltage and other performance aspects that affect single stage amplifiers.

However, multiple stage amplifiers are generally complex to compensate. Two-stage operational amplifiers are the most common used multistage amplifier because it can provide high gain and high output swing.

1.2 ABOUT THE COMPANY

KNK TECHNOLOGIES PVT. LTD

KNK(Komol and Kumari) Technologies is established in Imphal, Manipur with a vision of creating skilled Human Resources in VLSI and Embedded Design domains Knk School of VLSI and Embedded design, the Education initiative arm of KnK Technologies strive to work as a platform for Engineering graduates in Manipur and Eastern region of India,providing them an opportunity to enter and excel the world of VLSI design and the ESDM industry.

The aim of Knk is to create an ESDM ecosystem in the state of Manipur and Eastern region of India in the next few years. To achieve this mission, KnK School of VLSI and Embedded Design train engineering graduates in various aspects of VLSI Design like Circuit Design and Simulation ,Custom Layout, Standard Cell Layout etc .After completing the training modules offered by KnKSVED, an engineer would have got complete exposure to the IC design and development flow.

All the course offered by KnK School of VLSI and Embedded Design have been prepared considering various factors .Extent of VLSI domain exposure one gets in regular B.Tech and M.Tech Courses Gap between the exposure of fresh B.Tech and M.Tech graduates and skill required to work in the VLSI industry

Our effort is to bridge this gap by offering Specialized Job Oriented Courses and guiding our trainers to be industry ready and excel in their jobs in the industry .Our trainers will be trained using Industry, Standard EDA Tools and will work on design projects as part of the courses.

The courses and curriculum offered by KnKSVED are well thought of, and defined considering the skill level required to enter the VLSI design industry and perform World Class design in the ever demanding ESDM sector of today. Backed by industry experts, with close to 20 years in the ESDM and VLSI Design industry, KnK Technologies is certain that you will get the best opportunity to be employed at KnK Technologies or any other Design company. KnK Technologies will provide all required support to its trainers to get a job in the VLSI industry on successful completion of KnKSVED's training modules.

1.3 CMOS Technology

CMOS (Complimentary Metal-Oxide Semiconductor) is a predominant technology for manufacturing integrated circuits. This dominance of CMOS Technology in the fabrication of Integrated Circuits or ICs will continue for decades to come.

Generally, the CMOS Technology is associated with VLSI or Very Large-Scale Integrated Circuit, where a few millions or even billions of transistors (MOSFETs to be specific) are integrated into a single chip or die. The reasons for the dominant use of CMOS Technology in the fabrication of VLSI chips are reliability, low power consumption, considerably low cost and most importantly scalability.

Opamps are the most commonly used devices in electronic circuits. CMOS opamps have been the core component of various analog and mixed circuits and systems. Their applications are wide. They are used in Filters, Differentiators, Integrators, Digital-Analog convertors and Comparators. The challenge faced in CMOS technology is mainly about scaling these devices to decrease their size and power consumption. Opamps are of two types namely inverting Opamp and non-inverting Opamp with two inputs and single output.

The main prospect in this report is to design, Layout and simulate using gpdk 45nm technology. The modulation made here leads to better efficiency and operating frequency. The problem lies in design and implementation of two stage CMOS Opamp keeping various parameters into consideration which are constraints. In this paper the specification which becomes the target is the (W/L) ratio which indirectly relates to gain. In designing of high gain capacitive load, circuit need to be compensated to confirm the stability and a well behaved time response .

After the simulation, in ordered to optimize the better performance most of the transistors size still needed to be modified. The advantages of two stage op-amp have good gain, high output swing, low noise and good bandwidth over folded cascode. And it needs compensation, low PSRR value compared to folded cascode. To ensure the closed loop stability, Miller compensation is the simplest approach. Opamp presented in schematic has been designed with ≥ 60 dB DC gain, 30MHz UGB and $\pm 1.8V$ power supply.

1.4 Operational Amplifiers

We can define as a “high-gain differential amplifier”. By *high* we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5 . Since op-amps are usually employed to implement feedback system, their open loop gain is chosen according to the precision required of the closed loop circuit.

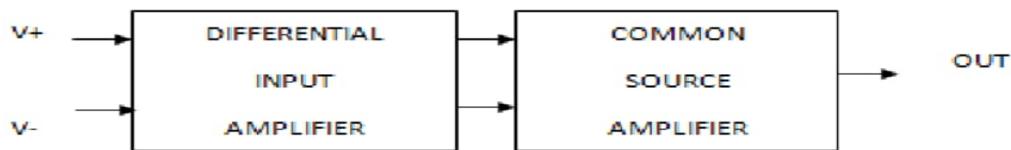


Figure 1.1 : Typical two-stage op-amp.

Fig. 1.1, is referred to as a “two-stage” op amp. The first stage usually consists of a high-gain differential amplifier. This stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain.

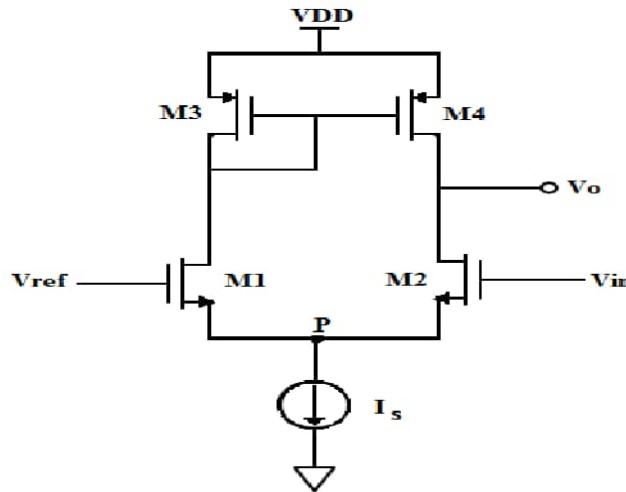
A typical CMOS differential amplifier stage is shown in Fig. 1.2. Differential amplifiers are often desired as the first stage in an op amp due to their differential input to single ended output conversation and high gain. PMOS input devices are used more because of its improved slew rate and reduced $1/f$ noise . PMOS input devices also provides reduced power supply rejection due to the current mirror’s low sensitivity to change in power supply voltage.

For the CMOS differential input stage, the gain and bandwidth are calculated as

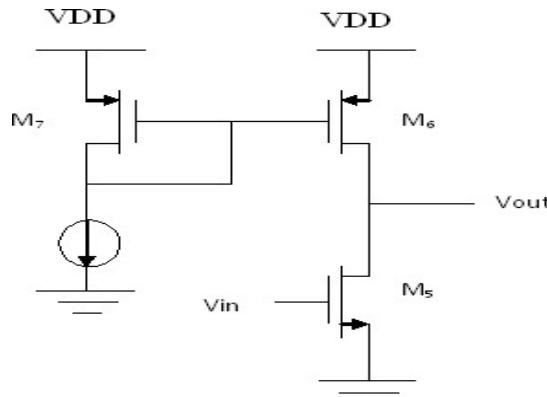
$$A_1 = g_{m1} (r_{ds2} || r_{ds4}) \dots \text{(i)}$$

$$\text{And } \omega_1 = \frac{1}{C_{out}(r_{ds2}||r_{ds4})} \dots \text{(ii)}$$

respectively.

**Figure 1.2 : CMOS differential input stage.**

The second stage implementation of a common source amplifier shown in Fig. 1.3. Similar to the first stage, Higher gains are often desirable for this stage when using Miller compensation techniques, although higher gains leads to lower bandwidth and the designer has to decide between these tradeoffs based on the specifications of the system.

**Figure 1.3 : Common source amplifier stage.**

For the circuit in common source, the gain and bandwidth are calculated as

$$A_2 = -g_{m5} (r_{ds5} || r_{ds6}) \dots \text{(iii)}$$

And $\omega_1 = \frac{1}{C_{out}(r_{ds5}||r_{ds6})} \dots \text{(iv)}$

respectively.

1.5 Thesis Organization

The thesis is divided into five chapters and its outline is described as given below.

Chapter 1: Introduction

Brief overview of issues related to modern CMOS Opamp and outline of the thesis.

Chapter 2: Literature Review

This chapter starts with the operational amplifier overview and describing the various parameters.

Chapter 3: Design Process of Two Stage Operational Amplifier

This chapter discusses the various calculation steps taken to design the final design and the equations followed to implement the design.

Chapter 4 : Simulation Results and Layout

This chapter contains various simulations results of the final circuit, Layout and LVS report.

Chapter 5 : Conclusion and future scope for work

This Chapter which is the concluding chapter, the design has been analyzed for further improvements which are possible.

CHAPTER 2

LITERATURE REVIEW

2.1 OVERVIEW OF TWO STAGE OPAMP

The designed CMOS operational amplifier circuit consists of two subsections, namely differential gain stage and second gain stage.

A . Circuit Operation :

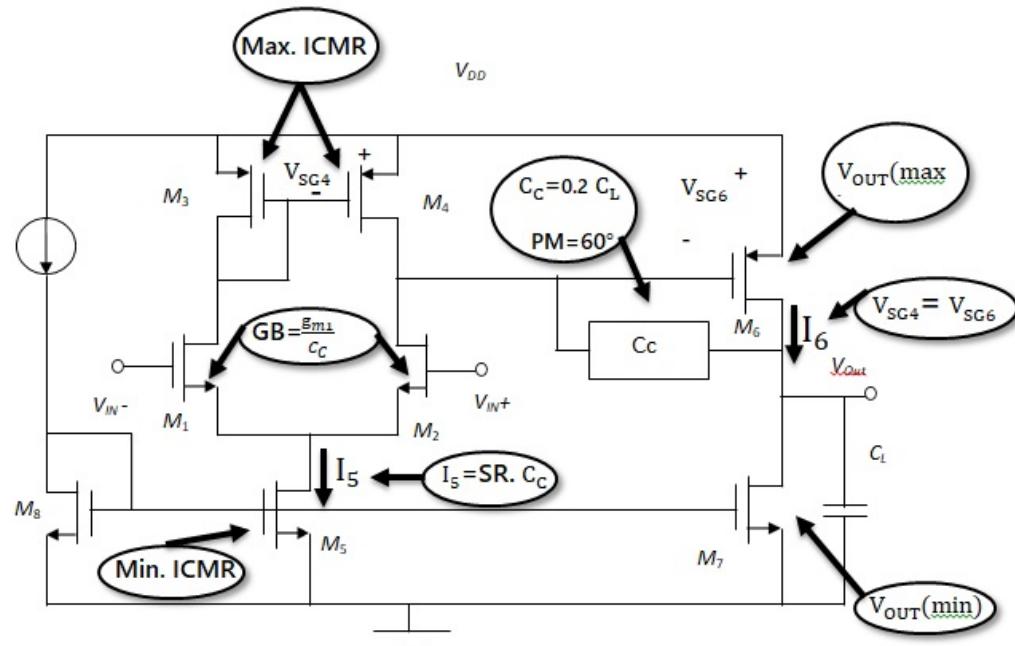


Figure 2.1: Two-stage op-amp

B. Differential Gain Stage

The differential gain stage consists of M1, M2, M3 and M4 form the first stage of the operational amplifier. Transistors M1 and M2 are standard NMOS which form the basic input stage of the differential amplifier. The gate of M1 and M2 are the inverting and non-inverting inputs with respect to transistors.

The two main resistances that contribute to the output resistance are that of the input transistors and also the output resistance of the active load transistors, M3 and M4. The gain of the two stage operational amplifier is the Transconductance of M2 times the total output resistance at the drain of M2.

A differential input signal applied across the two input terminals that will be amplified according to the gain of the differential stage. In this circuit have advantages by using the current mirror active load transistors M3 and M4. The use of active load devices gives a very large output resistance. The current mirror topology helps to conversion of the input signal from differential to single-ended. And load helps with common mode rejection ratio.

The current from M1 is mirrored by transistors M3 and M4 as shown and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage will give the single-ended output voltage. And also which constitutes the input of the second gain stage.

C. Second Gain Stage

This stage consists of transistors M6 and M7, as the name indicates, is to provide additional gain in the amplifier. Output from the drain of M2 and amplifies it through M6 which is called as common source configuration.

Similar to the differential gain stage, this stage employs an active device M7, to serve as the resistance for M6. Gain of this stage can be determined by the Transconductance of M6 times the effective load resistance comprised of the output resistance of the M6 and M7. Where M6 acts as the load, M7 acts as the driver.

2.2 Op-amp Parameters

There are various parameters to be considered while designing any circuit. The parameters that are to be considered when designing an Op-Amp are described below.

➤ **Gain :**

The most important factor in designing an Op-Amp circuit is the required gain from the circuit. In this circuit, we expect a gain of ≥ 60 dB. In order to achieve such higher gains, we use multiple stage CMOS Op-Amp. For this project we use 2 stage op-amp with differential amplifier at the first stage and a common source amplifier at 2nd stage

➤ **Unity Gain Frequency :**

The frequency at which the Gain of the circuit becomes ‘1’ or 0 dB is termed as Unity Gain Frequency. In this project, we need Unity Gain Frequency to be greater than or equal to 30 MHz.

➤ **Phase Margin :**

For Amplifiers, Phase Margin is the difference between phase measured in degrees for an output signal and 180 degrees. Phase margin should be ≥ 45 degrees.

➤ **Offset :**

The input offset voltage is the differential voltage that is required between the input terminals of differential amplifier to make output voltage equal to zero.

➤ **Slew rate :**

It is maximum rate of change of output with respect to unit time. In this project, we expect slew rate to be greater than or equal to 20 V/us.

➤ **PSRR :**

PSRR is the ability to reject noise or ripple occurring at the input side due to change in input offset voltage with respect to the change in power supply voltage .

$\text{PSRR} = 20 \log(\text{Power Supply Variation}) / (\text{Input Offset Voltage Variation}) [\text{dB}]$.

Generally, PSRR is frequency dependent, and decreases as the frequency increases.

➤ **CMRR :**

The Op-amp Common Mode Rejection Ratio(CMRR) is the ratio of the common mode gain to differential-mode gain. The function of the CMRR is to reduce the noise on the transmission lines.

➤ **ICMR :**

The Input Common-mode Voltage Range generally indicates the range of input voltage within which an IC operates normally. When the input voltage is outside the Input Common-mode Voltage Range, the offset voltage is rapidly increased beyond the normal operation region. It is to check the range of the voltage where the opamp will be in saturation.

2.3 Operational Amplifier Compensation

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90° assuming the gain bandwidth is ten times higher than the single pole. However, due to low dc gain of single stage amplifier, op amps requires at least two or more gain stages which results in multiple pole system. The poles contribute to the negative phase shift and may cause the phase margin become zero before reaching unity gain frequency. This negative phase margin is responsible for the system to oscillate. The process of altering the amplifier circuit to increase the phase margin and which ensures stability of closed loop circuit is known as “compensation”.

2.4 Miller Compensation And Addition Of Nulling Resistor

Miller Compensation is a technique for stabilizing op-amps by means of a capacitance C_C connected in negative- feedback fashion across one of the internal gain stages, typically the second stage. The right-half plane zero causes the Miller compensation to deteriorate. Methods for eliminating the influence of the RHP zero are :

- Nulling resistor
- Increasing the magnitude of the output pole

The PSRR of the two stage op-amp is poor because of the Miller capacitance ,however, methods exist to eliminate this problem.

CHAPTER 3

DESIGN PROCESS OF TWO STAGE OPERATIONAL AMPLIFIER

3.1 Design Specification

The following specifications will be used to design a two-stage operational amplifier.

Sl. No.	Parameter	Value
1	Technology	gpdk045n
2	Power Supply (Vdd)	1.8V
3	Load Capacitance (CL)	2pF
4	DC Gain(Av)	60dB
5	Phase Margin (PM)	> = 45 Degree
6	Slew rate (SR)	>= 20 V/ μ s
7	GBW	> = 30 MHz
8	ICMR	0.8 – 1.2
9	Power Dissipation, $P_{Diss.}$	2mW

Table 3.1. Required Design Specifications.

3.2 PROCEDURE

The circuit contains two stages.

The first is formed by the differential pair M1-M2 with its current mirror load M3-M4. Differential pair is biased using the current source M5. The transistor M5 is fed by a reference current mirror IRef.

The second stage is comprised of transistor M6 with its current source load M7. The second stage is used to improve the gain significantly. The two stage Op-Amp is expected to produce a gain greater than 1000. In order to design the Op-Amp with the specifications mentioned above, the first step is to estimate the value of IRef.

The next step is to calculate the (W/L) ratios of the transistors in the circuit based on the Reference Current. Finally, we estimate the value of the compensation Capacitor required to provide the negative feedback.

In order to avoid systematic output dc offset voltage, we need to choose the (W/L) ratios of transistors carefully.

3.3 SCHEMATIC

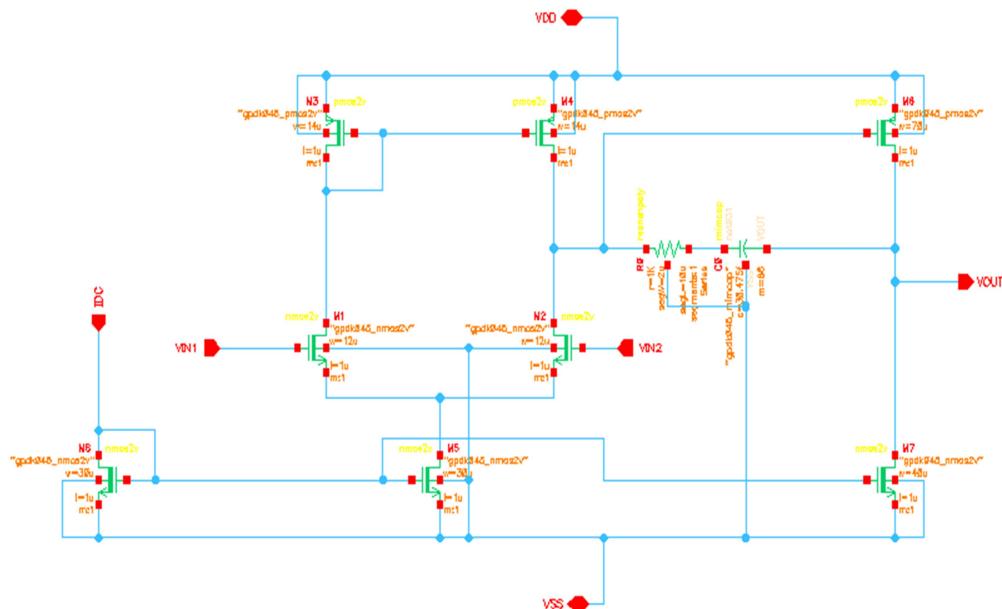


Figure 3.1 : Schematic diagram of two stage operational amplifier

3.4 SYMBOL

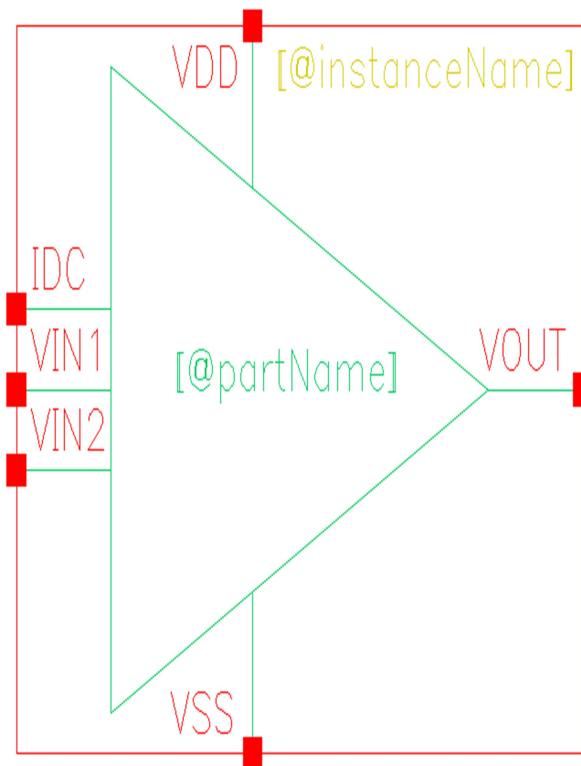


Figure 3.2 : Symbol of Two Stage Op-amp.

3.5 DESIGN STEPS

Choose the smallest the device length that will keep the channel modulation parameter constant and give a good matching for a current mirror. So assuming the channel length is to be $1\mu\text{m}$.

3.5.1 Design of Compensation Capacitor

From the desired phase margin, choose the maximum value for C_C that is, for a 60° phase margin choose

$$\frac{10 g_{m1}}{C_L} \geq 2.2 \frac{g_{m1}}{C_C}$$

$$C_C > 0.22 \times C_L = 2\text{pF}$$

This assume that the RHP zero z is placed at or beyond ten times GB (Gain Bandwidth).

That is $z \geq 10GB$.

Where, Gain bandwidth $\text{GB} = \frac{g_{m1}}{C_C}$

3.5.2 Design of I5

To determine the minimum value for the “tail current”.

We have,

$$\text{SR} = \frac{I_5}{C_C}$$

$$I_5 = \text{SR} \cdot C_C = 20\mu\text{A}$$

3.5.3 Design of gm1 for M1

$$g_{m1} = \text{GB} \cdot C_C \cdot 2\pi = 150.79 \mu \approx 150 \mu$$

3.5.4 Design for M1 and M2

We know that,

$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)} I_D$$

Therefore, the aspect ratio (W/L)₁ is shown below :

$$M_1 = (W/L)_1 = \frac{g_m 1^2}{2\mu_n C_{ox} I_5} = 3.75 \approx 4$$

Where $\mu_n \cdot C_{ox} = 300\mu = \beta_{eff}$ (NMOS transistor)

3.5.5 Design for M3 and M4

Form the maximum input voltage relation,

$$\text{Positive ICMR } V_{in}(\max) = V_{DD} - \sqrt{\frac{15}{\beta_3}} - |V_{T3}|(\max) + V_{T1}(\min)$$

$$M_3 = (W/L)_3 = \frac{2 I_5}{K_p [V_{DD} - V_{in}(\max) - V_{tn} + V_{tp}]^2} \\ = 14$$

Where $K_p = \mu_p \cdot C_{ox} \cdot (W/L)_p = \beta_{eff}$ (P for PMOS transistor)

- $\mu_p \cdot C_{ox} = 300\mu$
- $V_{in}(\max) = \text{Max. ICMR}$
- $V_{tn} = V_{T3}(\max) \quad \& \quad V_{tp} = V_{T1}(\max)$

3.5.6 Design for M5 and M8

Enough information is now available to calculate the saturation voltage of transistor M5.

Using the negative ICMR equation, calculate V_{DS5} using the following relationship,

$$\begin{aligned} V_{dsat5} &\geq V_{in}(\min) - V_{gs1} \\ &\geq \text{Min. ICMR} - \sqrt{\frac{2I_5}{\beta_1}} - V_{tn} \\ &\geq 1.2V \end{aligned}$$

Where ,

$$\begin{aligned} V_{tn} &= V_{T1}(\max) \\ \beta_1 &= \mu_n \cdot C_{ox} \cdot (W/L)_1 \\ &= \beta_{eff} \quad (\text{for NMOS transistor M1}) \end{aligned}$$

With V_{DSat5} determined,

$(W/L)_5$ can be extracted using the relation given below :

$$I_5 = \frac{\mu_n \cdot C_{ox}}{2} \left(\frac{W}{L} \right)_5 (V_{dsat5})^2$$

Therefore,

$$M_5 = (W/L)_5 = \frac{2I_5}{K_n(V_{ds5})^2} = 10$$

Where $K_n = \mu_n \cdot C_{ox} \cdot (W/L)_5 = \beta_{eff}$ (for NMOS transistor M5)

3.5.7 Design of g_{m6} for M_6

By placing the zero z_1 at or beyond ten times GB or by letting the second pole(p2) be equal to 2.2 times GB.

$$\text{i.e. } z_1 > 10GB$$

$$\frac{g_{m6}}{C_C} > 10 \left(\frac{g_{m1}}{C_c} \right)$$

$$\begin{aligned} g_{m6} &= 10 g_{m1} \\ &= 1500 \mu \end{aligned}$$

Where, Gain bandwidth $\mathbf{GB} = \frac{g_{m1}}{C_c}$

3.5.8 Design of M_6 and I_6

To achieve proper mirroring of the first-stage current mirror load of (M_3 and M_4), this requires that $V_{SG4} = V_{SG6}$.

If $V_{SG4} = V_{SG6}$,then we can write the following relationships

$$\left(\frac{W_6}{L_4}\right) / \left(\frac{W_4}{L_4}\right) = \left(\frac{I_6}{I_4}\right) = \left(\frac{g_{m6}}{g_{m4}}\right)$$

$$Gm4 = \sqrt{\mu_p \cdot C_{ox}} \left(\frac{W}{L}\right)_4 \times 2I_4 = 129.61\mu \approx 130\mu$$

$$\text{Therefore, } \left(\frac{W_6}{L_4}\right) / \left(\frac{W_4}{L_4}\right) = \left(\frac{g_{m6}}{g_{m4}}\right)$$

$$M_6 = M_4 \left(\frac{g_{m6}}{g_{m4}}\right) = 161.538\mu \approx 162\mu$$

Knowing $gm6$ and M_6 will define the dc current using the following equation :

$$I_6 = \frac{g^2 m_6}{(2)(K'_6)(S_6)} = \left(\frac{W_6}{L_4}\right) / \left(\frac{W_4}{L_4}\right) \times I_4 = 115.7\mu \approx 116\mu$$

$$\text{Where, } I_4 = \frac{I_5}{2}$$

3.5.9 Design of M₇

To achieve the desire current ratios between I₅ and I₆

If V_{SG5} = V_{SG7}, then we can write the following relationships

$$\left(\frac{M7}{M5}\right) = \left(\frac{I7}{I5}\right)$$

Therefore,

$$M7 = M5 \left(\frac{I6}{I5}\right) = 57.5 \mu \approx 58 \mu$$

3.5.10 DESIGN CHOICE OF TWO STAGE OPAMP :

Values of transistors and aspect ratio of the design is given below :

Transistor	Aspect Ratio(W/L)	
	<i>W Values(in um)</i>	<i>L Values(in um)</i>
M1	4	1
M2	4	1
M3	14	1
M4	14	1
M5	10	1
M8	10	1
M6	162	1
M7	58	1

Table 3.2. Transistor design choice of the Op-amp.

3.5.11 DESIGN ASPECT RATION AFTER OF TUNING :

Table 3.3 states the size of each transistor used in two-stage operational amplifier.

Transistor	Aspect Ratio(W/L)	
	<i>W Values(in um)</i>	<i>L Values(in um)</i>
M1	12	1
M2	12	1
M3	14	1
M4	14	1
M5	30	1
M8	30	1
M6	70	1
M7	40	1

Table 3.3. Transistor Sizing of the Op-amp.

CHAPTER 4

SIMULATION RESULTS AND LAYOUT

4.1 PRE-SIMULATION

4.1.1 DC Analysis :

To check the values of various parameters(V_{gs} , I_d , V_{ds} , V_{th})

and check the region of a transistor (i.e saturation region).

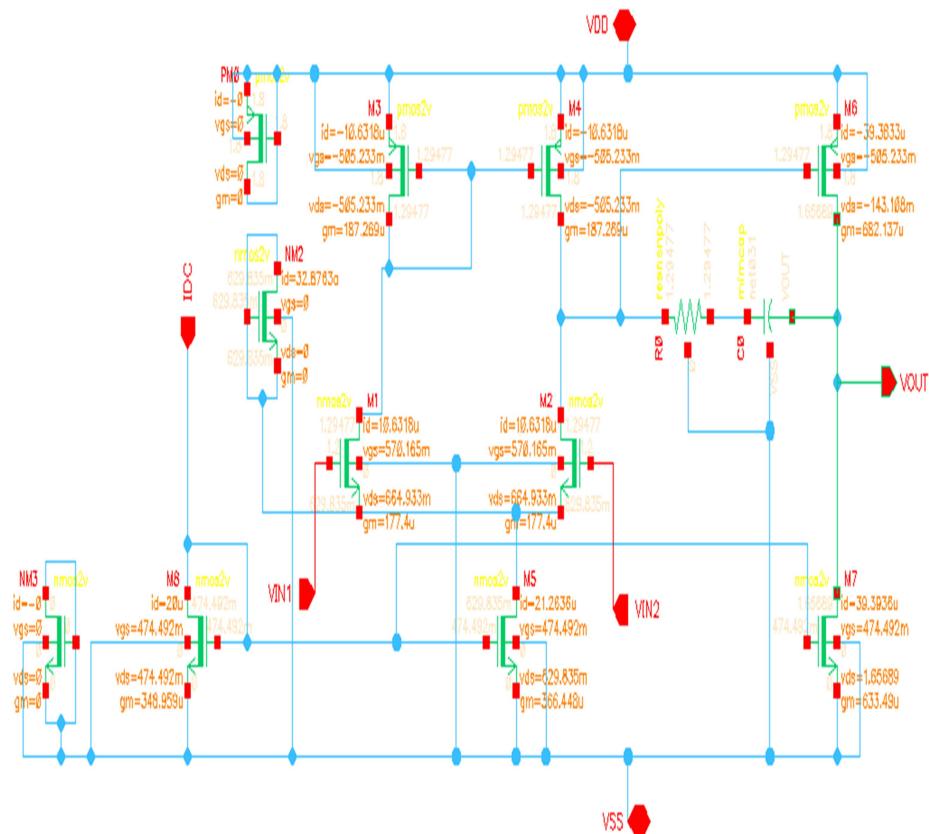


Figure 4.1 Schematic of DC analysis

4.1.2 Transient Analysis :

To check the input and output waveform of the circuit.

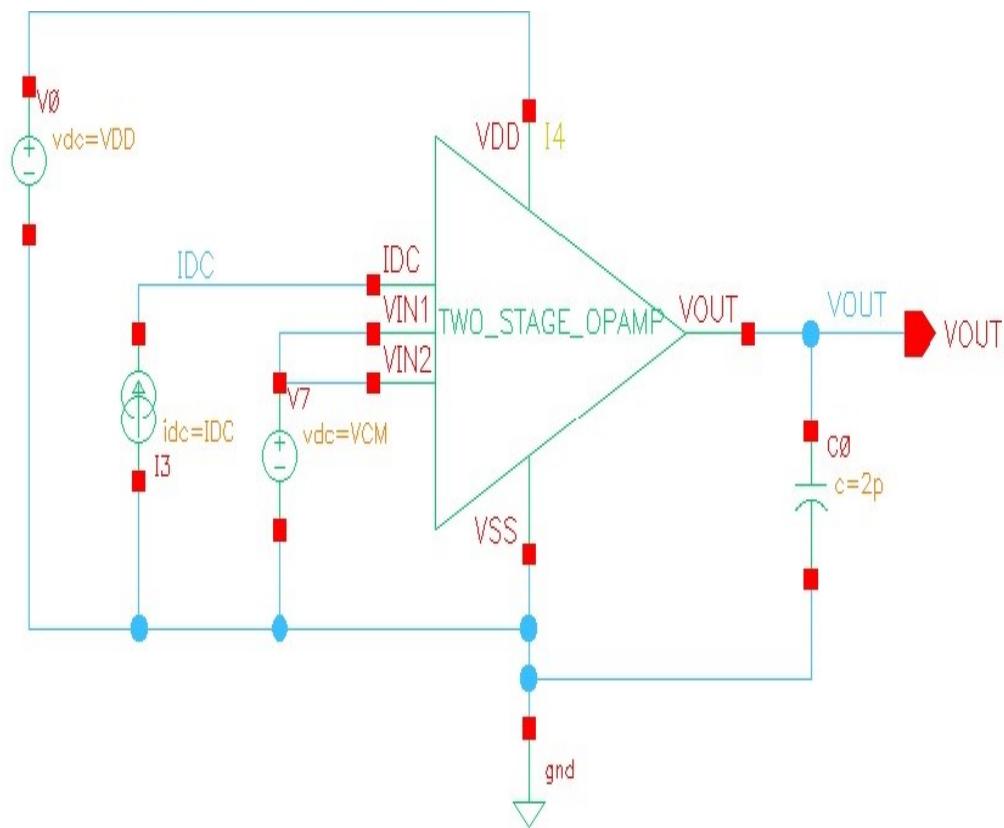


Figure 4.2 : Testbench of transient analysis.

Waveform of Transient Responds :

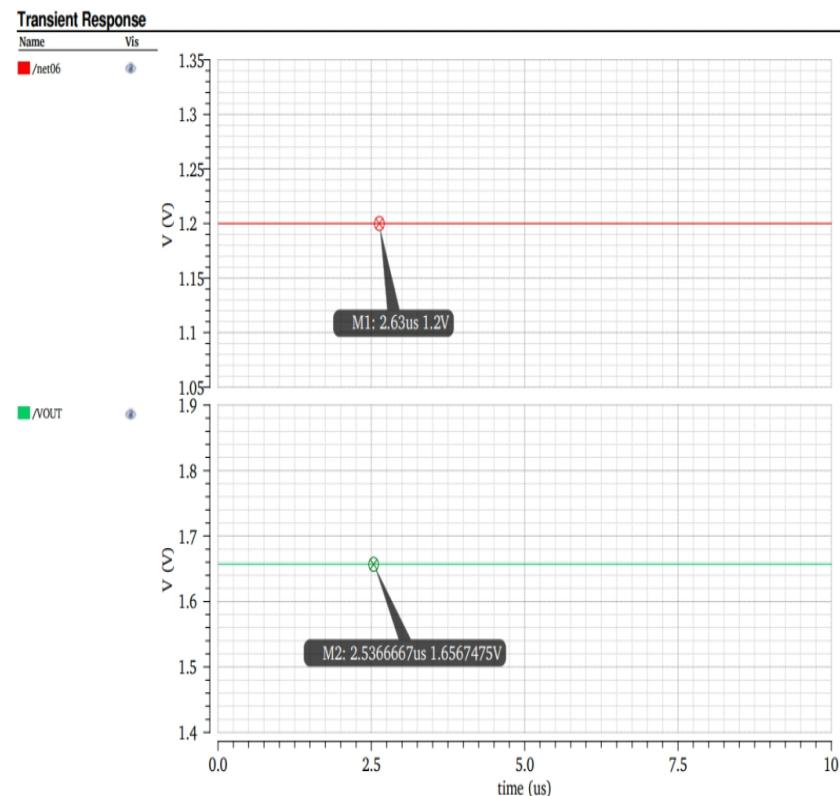


Figure 4.3 Waveform of Transient Responds .

4.1.3 Stability Analysis :

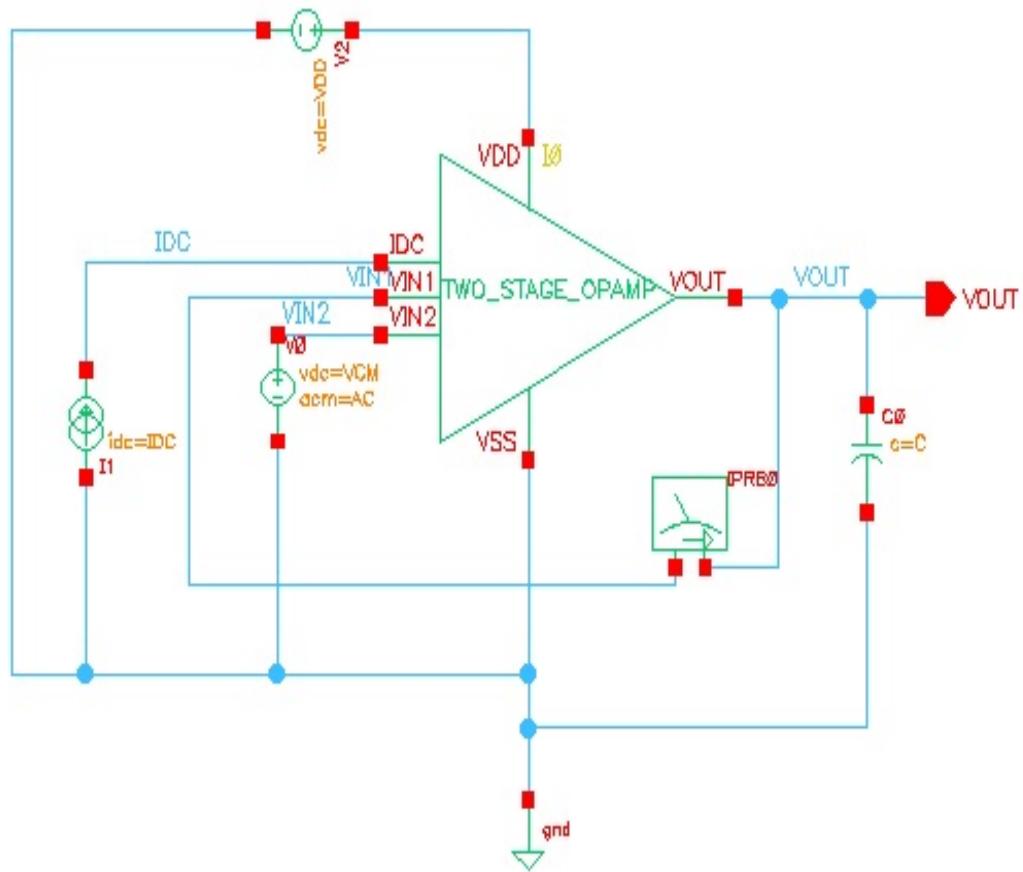
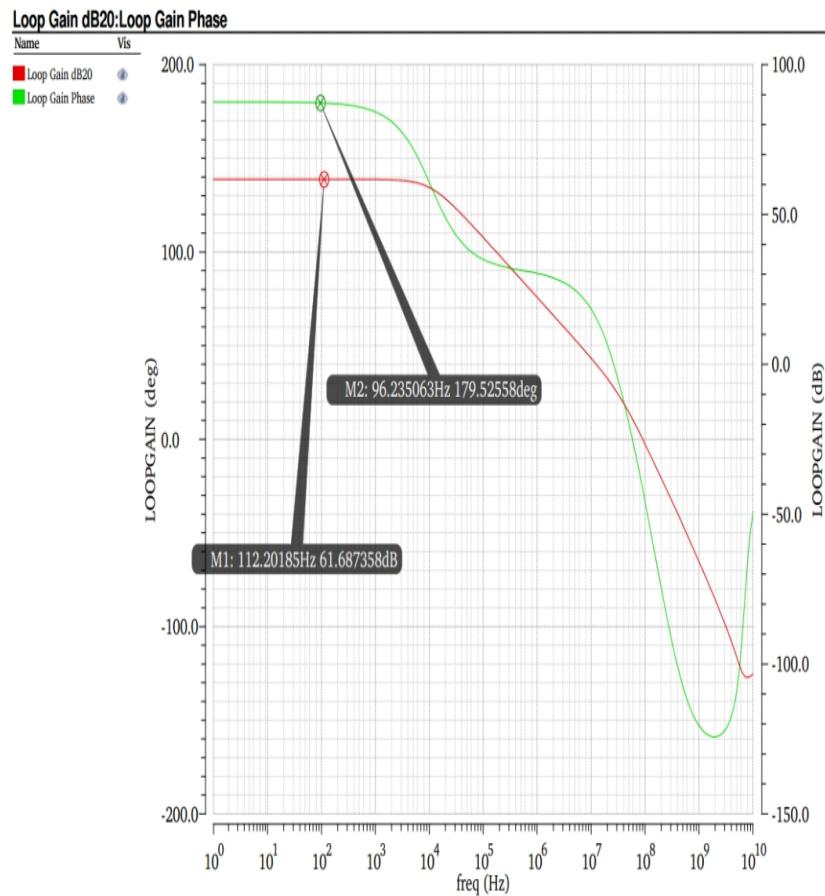
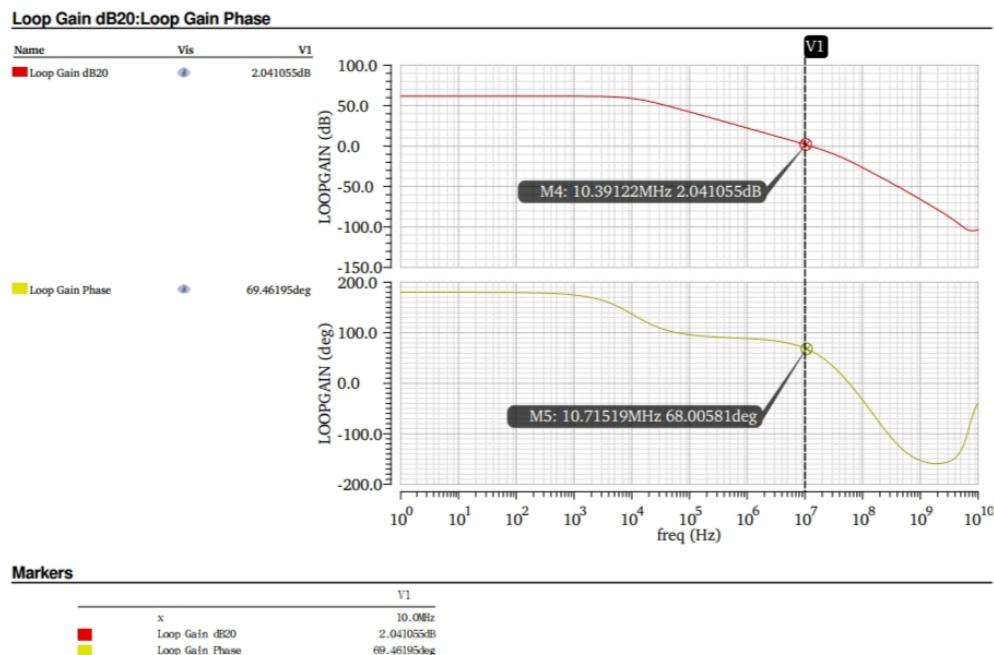


Figure 4.4 : Testbench of Stability analysis.

Waveform :**Figure 4.5 : Frequency Responds of Stability analysis.**

UGB waveform :**Figure 4.6 : UGB frequency responds.**

4.1.4 AC Analysis :

To plot Loop Gain and Phase Margin and to calculate the value.

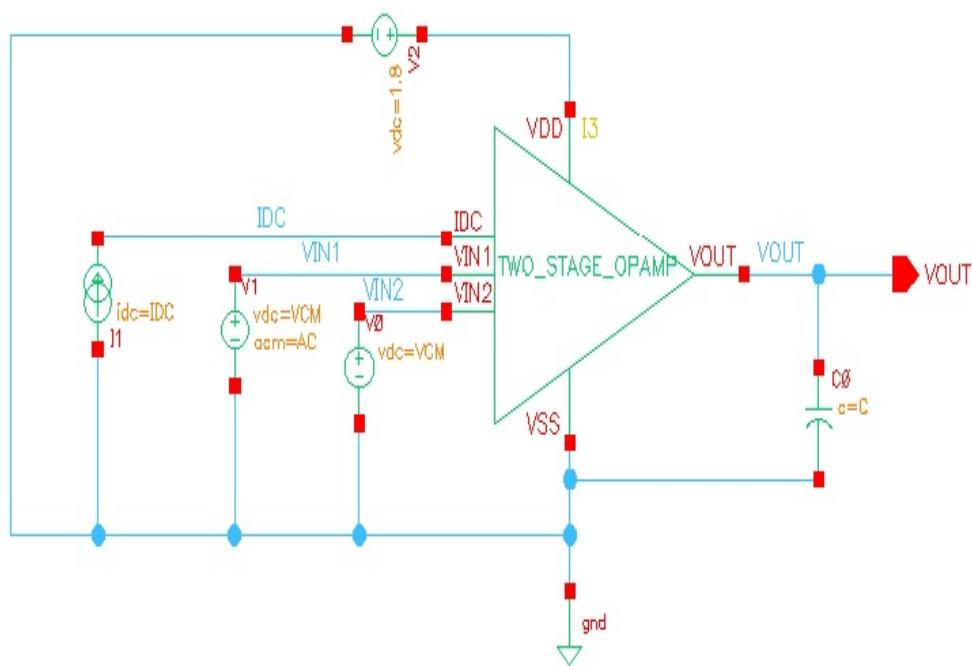


Figure 4.7 : Testbench of AC Analysis.

Waveform of AC Analysis :

```
dB20((VF("/VOUT" "/home/asha/simulation/AC_ANALYSIS/spectre/schematic") / VF("/VIN1"
"/home/asha/simulation/AC_ANALYSIS/spectre/schematic")));phaseDegUnwrapped((VF("/VOUT"
"/home/asha/simulation/AC_ANALYSIS/spectre/schematic") / VF("/VIN1"
"/home/asha/simulation/AC_ANALYSIS/spectre/schematic")))
```

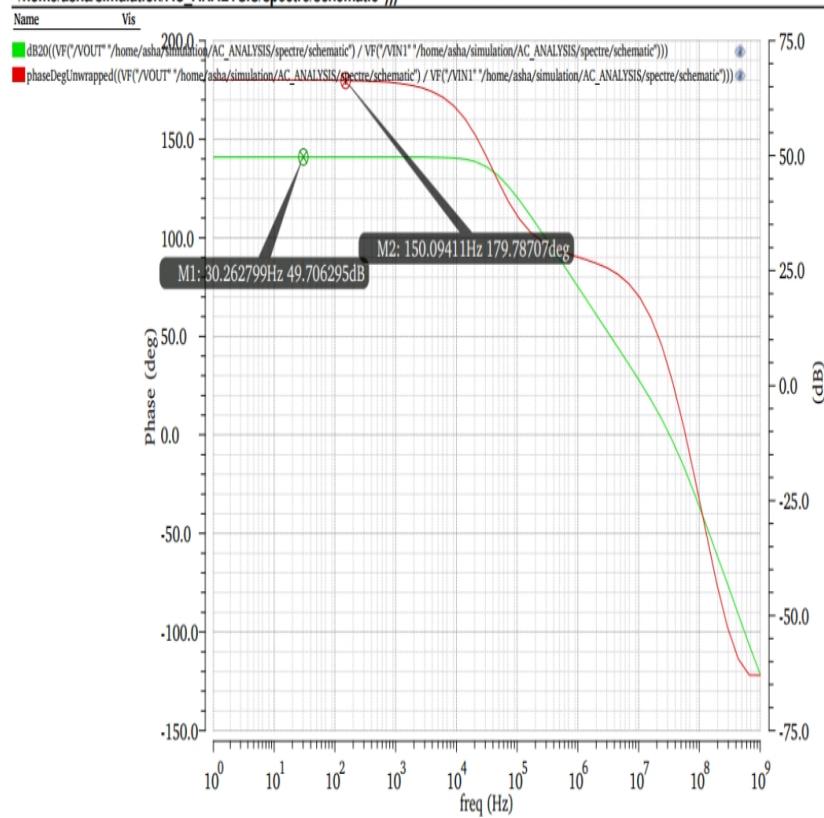
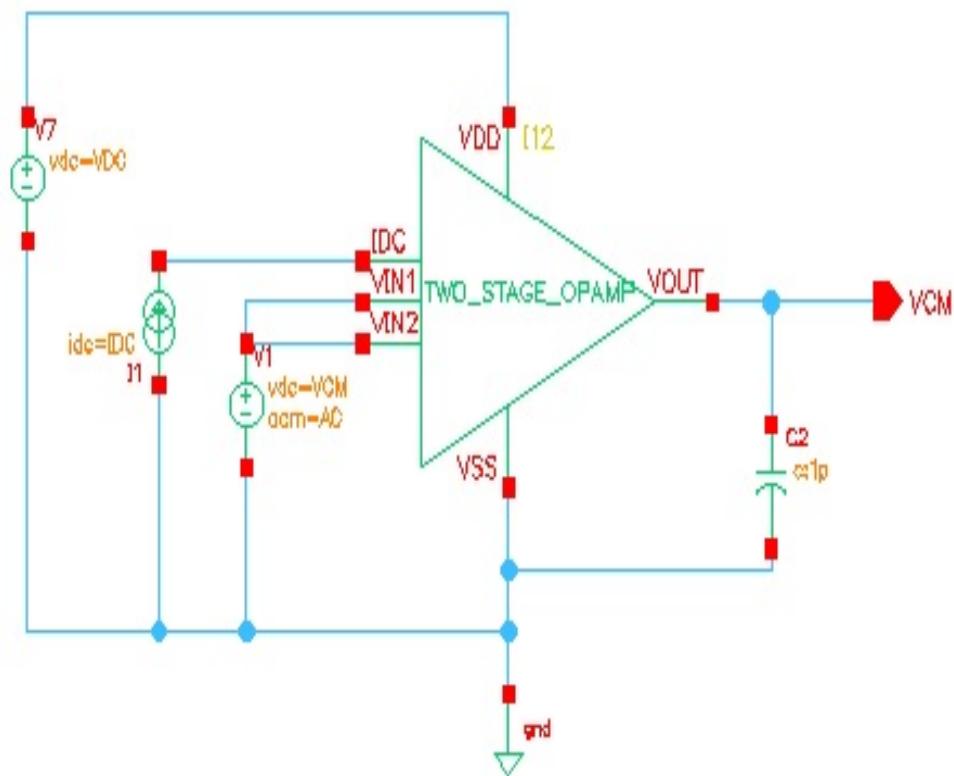


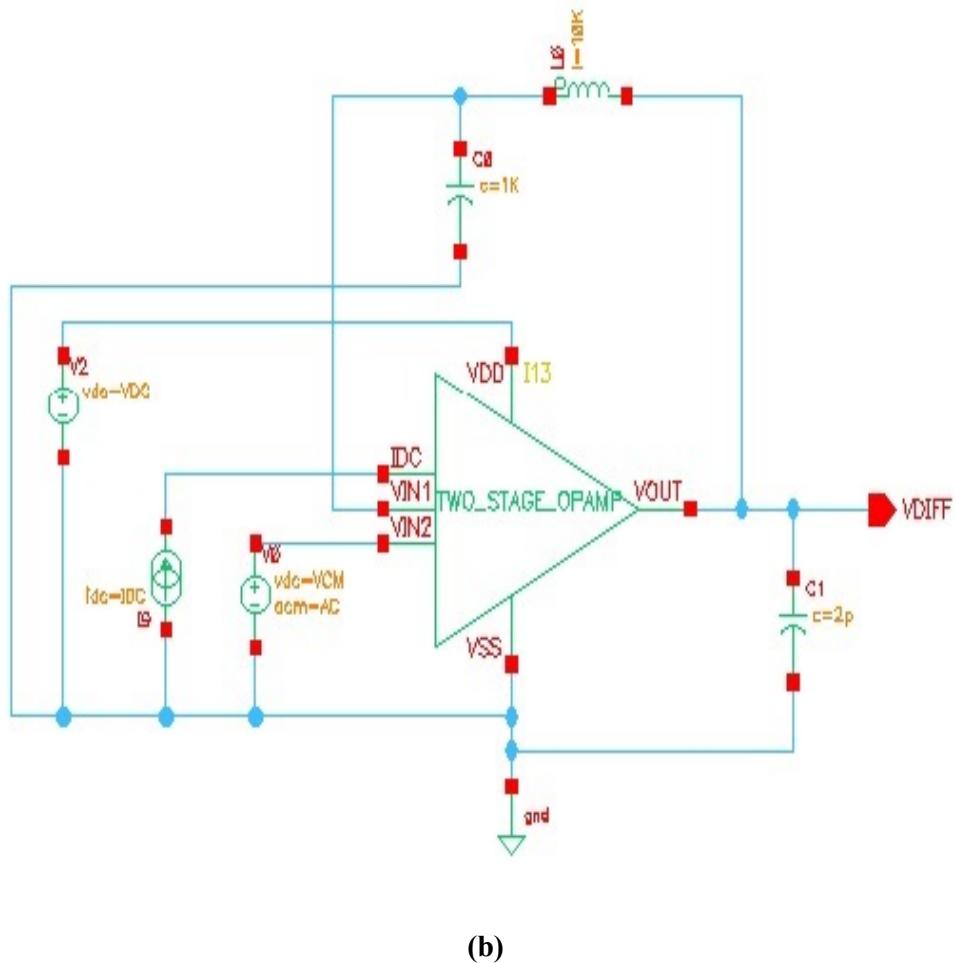
Figure 4.8 : Frequency responds of AC Analysis.

4.1.5 CMRR :

The Ability of an operational amplifier to reject common mode signal present between the inverting and non-inverting inputs.

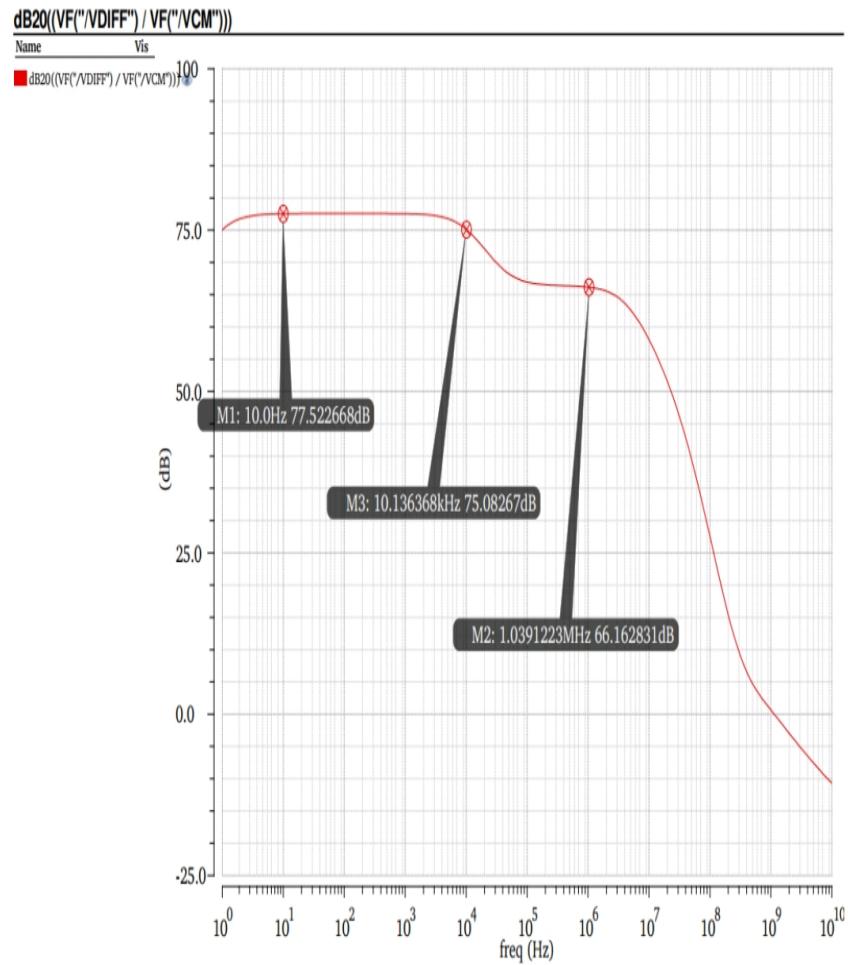


(a)



(b)

Figure 4.9(a & b) : Testbench of CMRR

Waveform of CMRR :**Figure 4.10 : Frequency responds of CMRR.**

4.1.6 ICMR :

To check the range of voltage where the op amp will be in saturation.

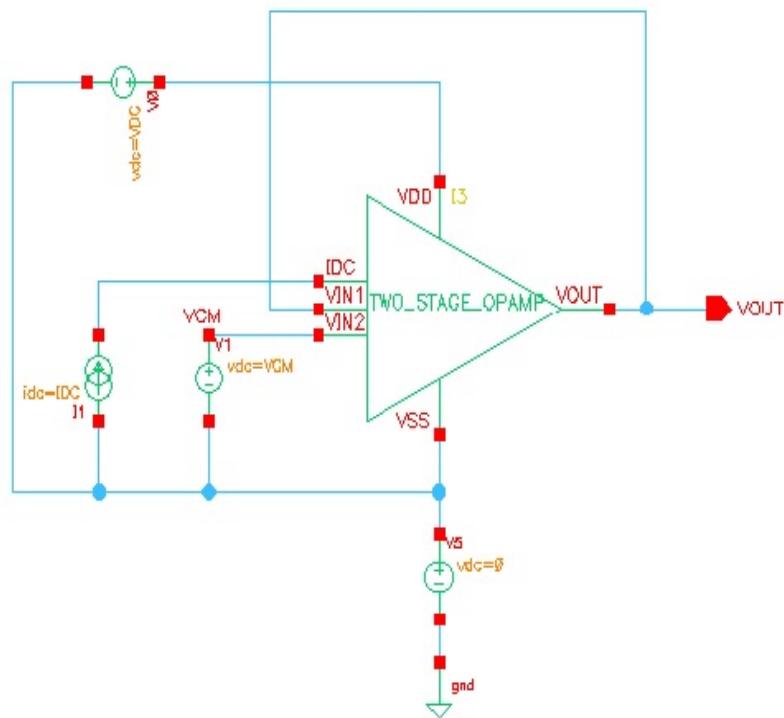


Figure 4.11 : Testbench of ICMR Analysis.

Waveform of ICMR Analysis.:

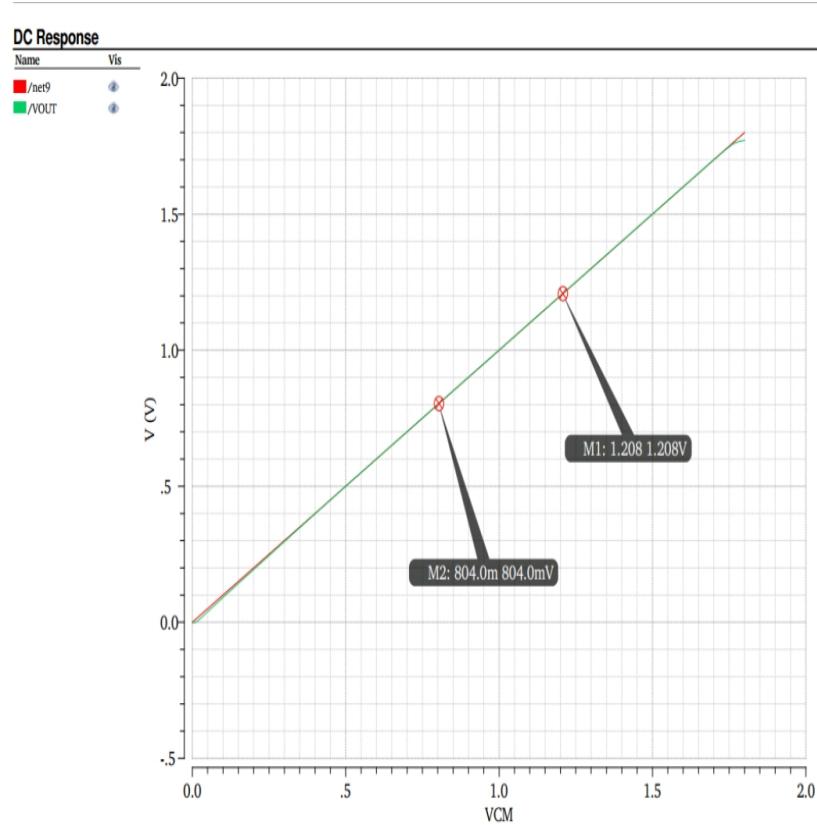


Figure 4.12 : VCM of ICMR Analysis.

4.1.7 PSRR :

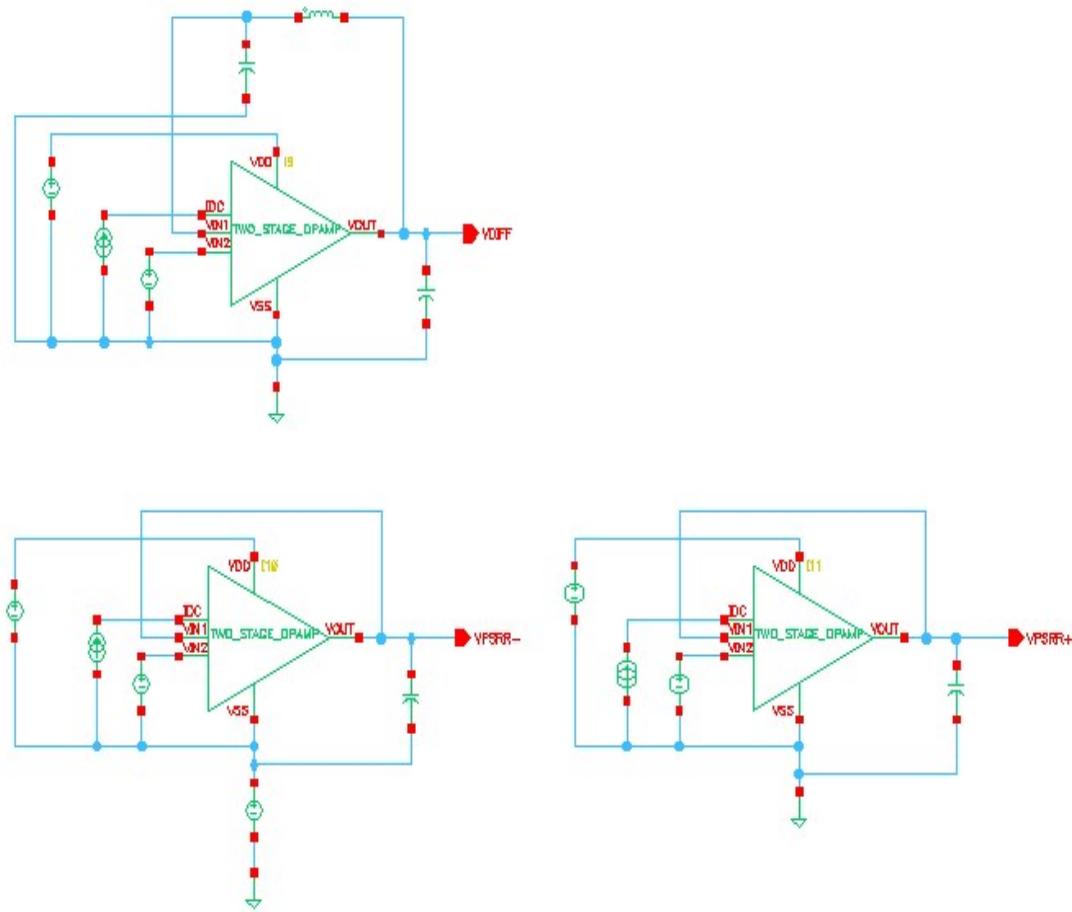
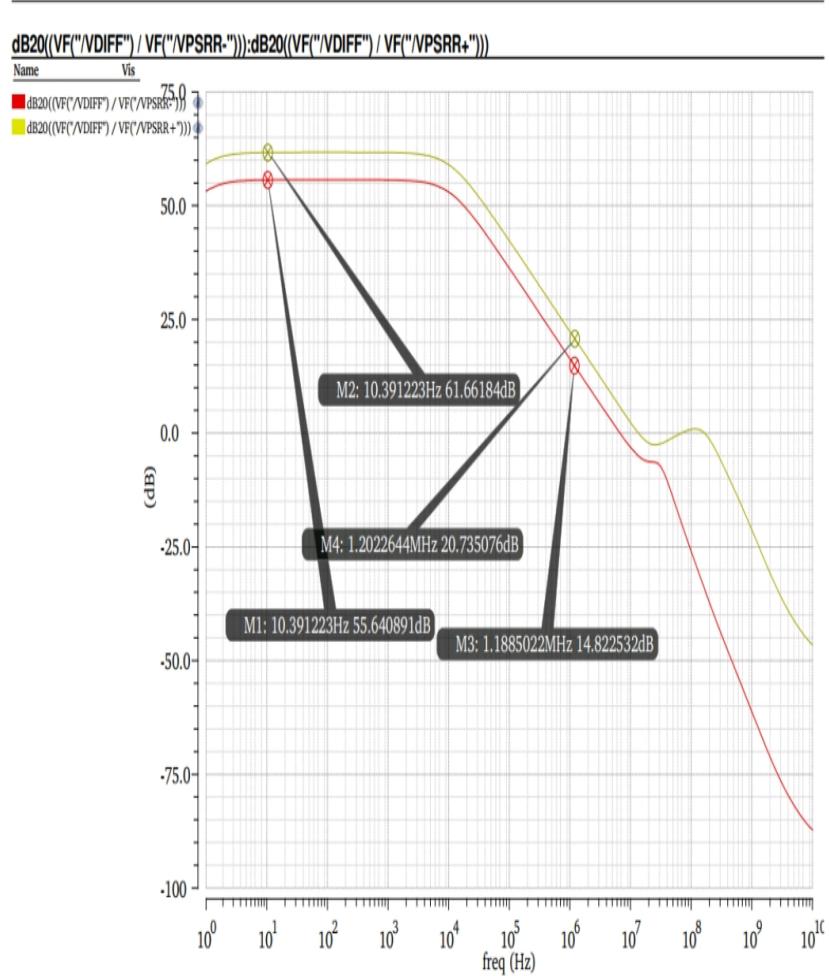


Figure 4.13 : Testbench of PSRR Analysis.

Waveform of PSRR Analysis :**Figure 4.14 : Waveform of PSRR Analysis.**

4.1.8 Slew Rate :

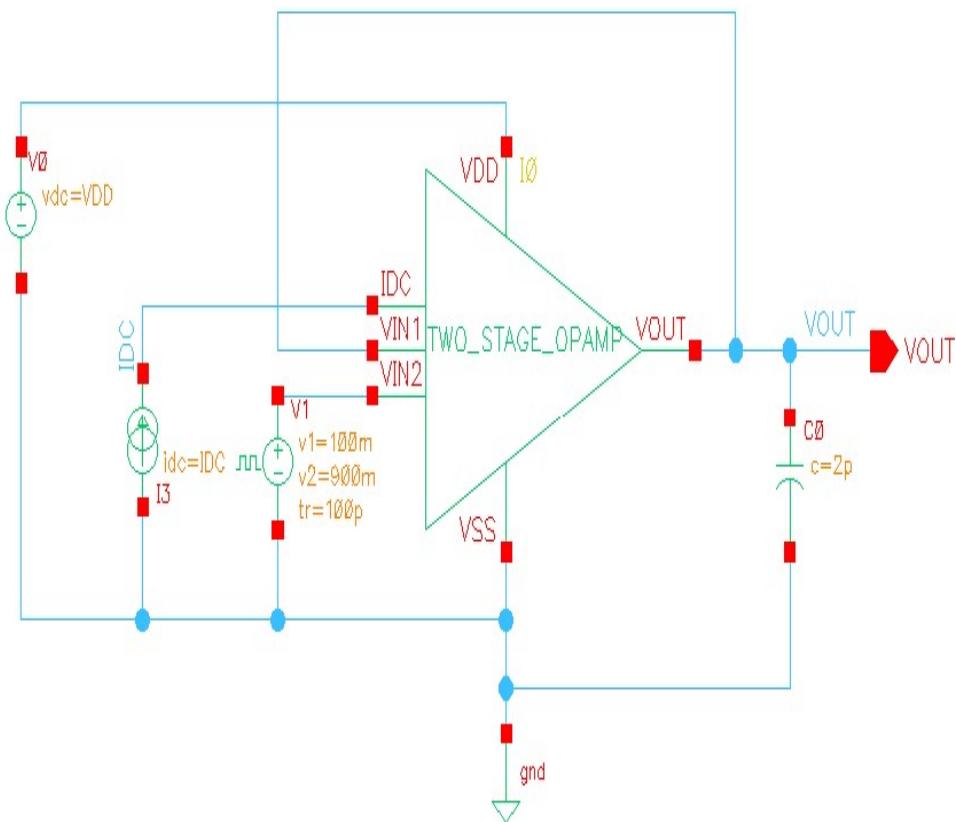


Figure 4.15 : Testbench of Slew Rate.

4.1.9 Offset Analysis :

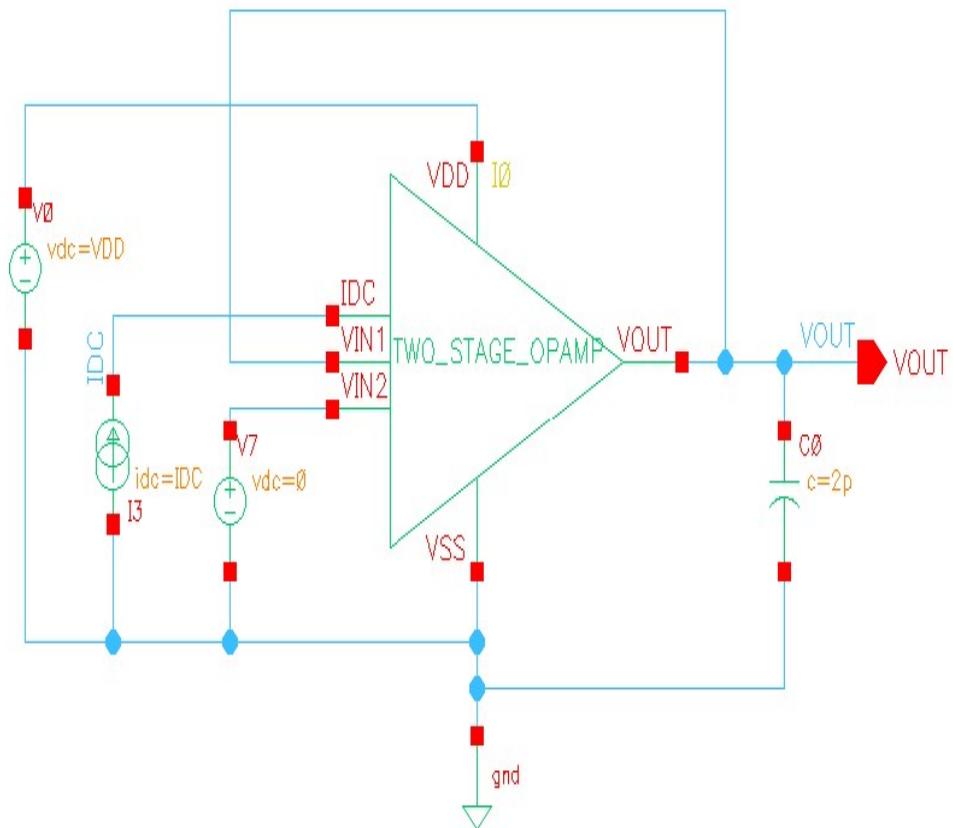
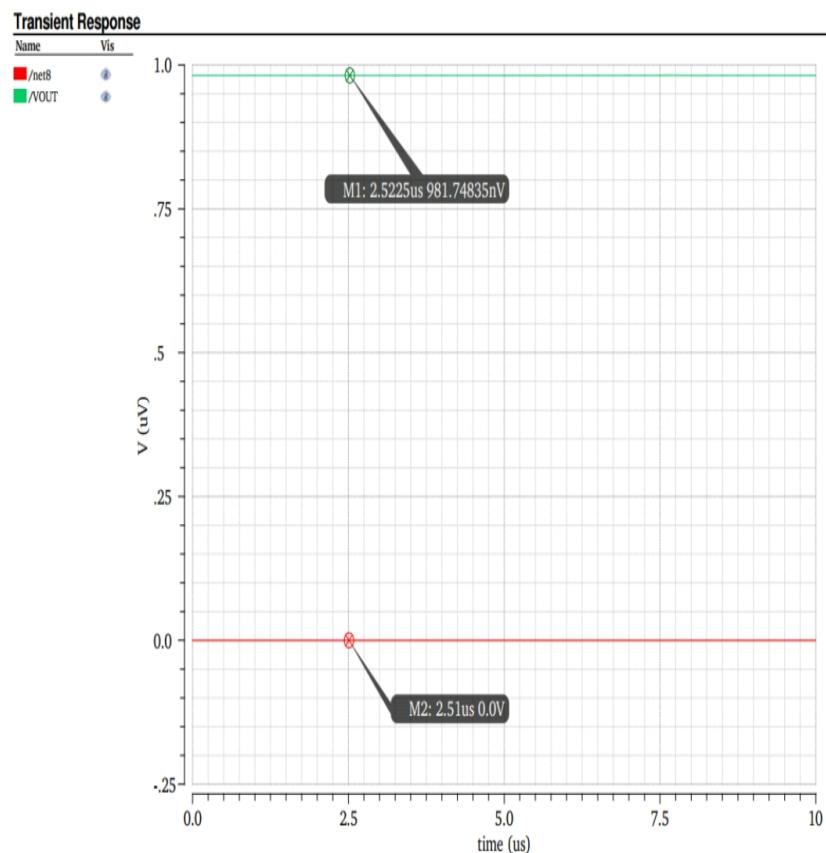


Figure 4.16 : Test bench of Offset Analysis.

Waveform of Offset Analysis :**Figure 4.17 : Waveform responds of Offset Analysis.**

4.1.10 Power Consumption :

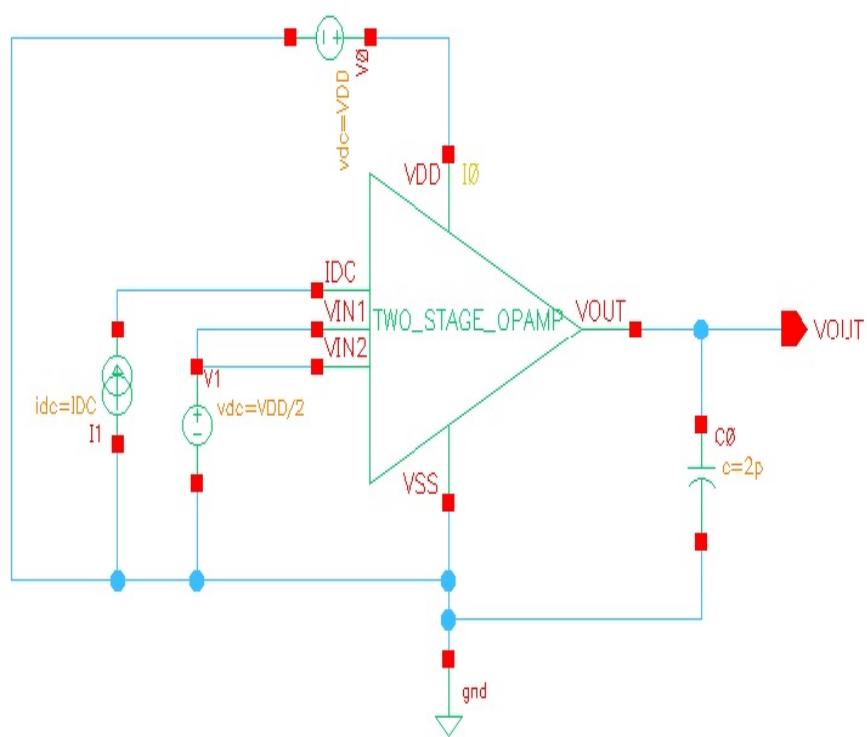
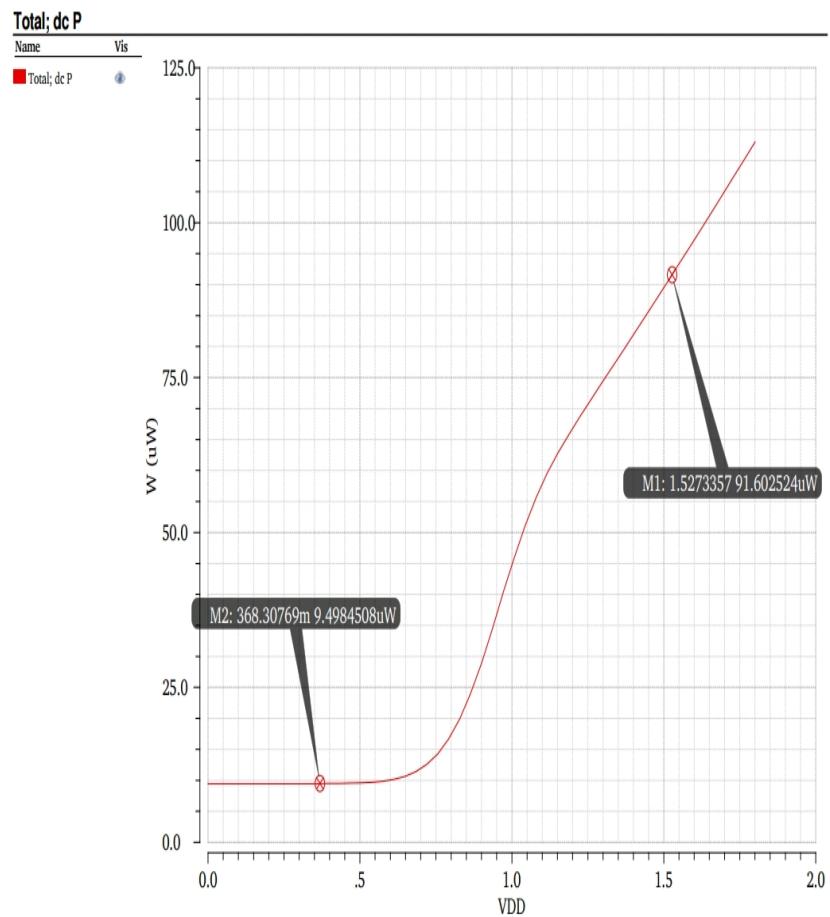


Figure 4.18 : Test bench of Power Consumption.

Waveform of Power Consumption :**Figure 4.19: Waveform of Power Consumption.**

4.2 Pre - Layout Simulation

Parameter	VC M	V D D	gdk0 45.scs	gdk045_mi mcap.scs	tempe rature	Out put	LOOP_ GAIN	Pha se Ma rgin	Gai n Ma rgin	Phase Margi n Frequ ency	Gain Margi n Frequ ency
Nomi nal	1. 2	1. 8	tt	tt_mim	27	Nom inal	61.69	64. 65	18. 18	1.24E +07	5.82E +07
						Min	57.74	54. 59	13. 78	8.40E +06	3.57E +07
						Max	63.16	72. 92	24. 3	1.68E +07	8.93E +07
CO_1 3	1. 2	1. 62	fs	ff_mim	125	CO_ 13	57.74	63. 4	16. 53	1.01E +07	4.33E +07
CO_1 4	1. 2	1. 98	fs	ff_mim	-40	CO_ 14	63.01	71. 2	23. 86	1.25E +07	8.87E +07
CO_1 5	1. 2	1. 98	fs	ff_mim	125	CO_ 15	62.53	62. 71	16. 36	1.04E +07	4.34E +07
CO_1 6	1. 2	1. 62	sf	ff_mim	-40	CO_ 16	60.9	72. 9	23. 33	1.01E +07	7.39E +07
CO_1 7	1. 2	1. 62	sf	ff_mim	125	CO_ 17	60.39	64. 88	16. 72	8.73E +06	3.92E +07
CO_1 8	1. 2	1. 98	sf	ff_mim	-40	CO_ 18	61.75	72. 92	23. 36	1.00E +07	7.40E +07
CO_1 9	1. 2	1. 98	sf	ff_mim	125	CO_ 19	61.55	64. 69	16. 65	8.77E +06	3.91E +07
CO_2 0	1. 2	1. 62	sf	ff_mim	-40	CO_ 20	60.41	72. 07	24. 18	1.19E +07	8.85E +07
CO_2 1	1. 2	1. 62	sf	ff_mim	125	CO_ 21	58.7	64. 19	16. 81	9.80E +06	4.32E +07
CO_2 2	1. 2	1. 98	sf	ff_mim	-40	CO_ 22	62.82	71. 99	24. 3	1.20E +07	8.93E +07
CO_2 3	1. 2	1. 98	sf	ff_mim	125	CO_ 23	62.47	63. 68	16. 69	9.98E +06	4.33E +07
CO_2 4	1. 2	1. 62	ss	ff_mim	-40	CO_ 24	61.18	71. 71	21. 85	9.71E +06	6.45E +07
CO_2 5	1. 2	1. 62	ss	ff_mim	125	CO_ 25	60.64	63. 69	15. 96	8.40E +06	3.57E +07
CO_2 6	1. 2	1. 98	ss	ff_mim	-40	CO_ 26	62.12	71. 74	21. 9	9.71E +06	6.47E +07
CO_2 7	1. 2	1. 98	ss	ff_mim	125	CO_ 27	62.01	63. 5	15. 9	8.46E +06	3.57E +07
CO_2 8	1. 2	1. 62	ss	ff_mim	-40	CO_ 28	60.43	70. 57	22. 23	1.16E +07	7.50E +07
CO_2 9	1. 2	1. 62	ss	ff_mim	125	CO_ 29	58.4	62. 8	15. 92	9.43E +06	3.90E +07
CO_3 0	1. 2	1. 98	ss	ff_mim	-40	CO_ 30	63.16	70. 49	22. 32	1.17E +07	7.58E +07

Table 4 .1 : Pre Layout Simulation table

4.2.1 Pre – Simulation Result

Sl. No.	Parameter	Value
1	Power Supply (Vdd)	1.8V
2	Load Capacitance (CL)	2pF
3	DC Gain(Av)	61.6
4	Phase Margin (PM)	64.65
6	CMRR	96.61
7	PSRR(-)	-53.16
	PSRR(+)	59.18
8	Power Consumption	9.58 μ

Table 4.2 : Pre – Simulation Result table

4.3 LAYOUT

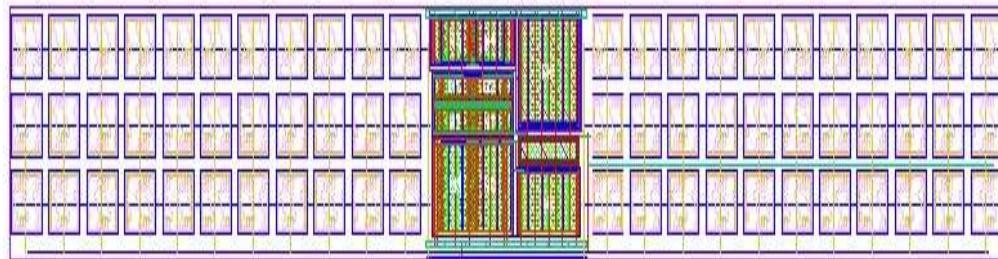


Figure 4.20 : Layout of two stage opamp

4.4 EXTRACTED LAYOUT

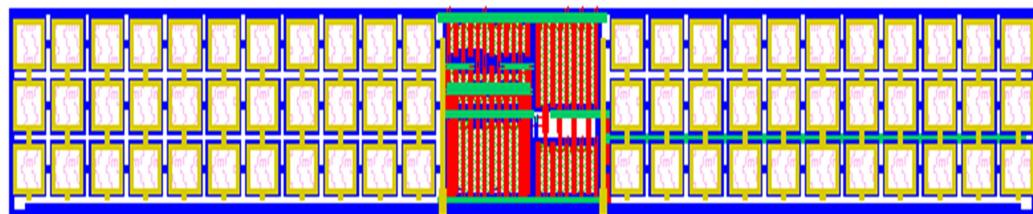


Figure 4 .21 : Extracted view of layout for Post Simulation.

4.5 PHYSICAL VERIFICATION

4.5.1 DRC verification



Figure 4. 22 : DRC Physical Verification

4.5.2 LVS Verification

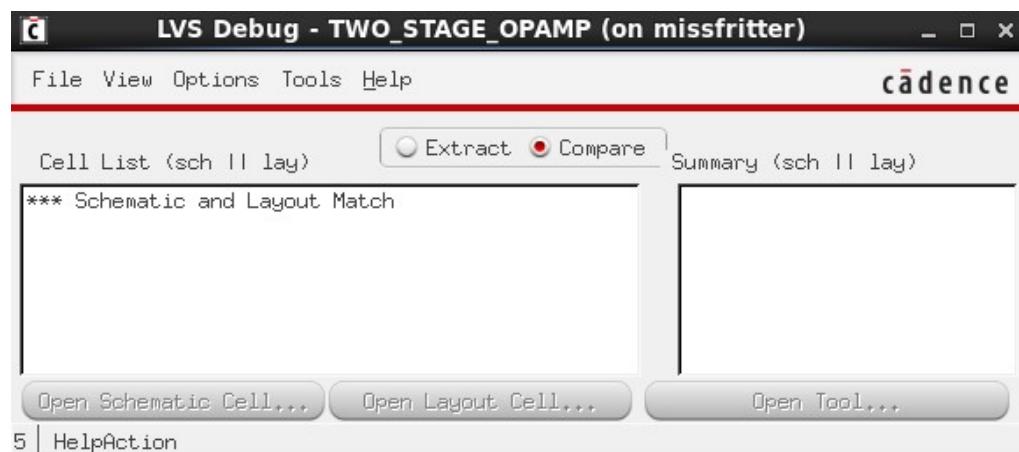


Figure 4.23: Physical verification of LVS

4.6 POST SIMULATION

4.6.1 Post- Layout Simulation

Parameter	VCM	VDD	gpd k04 5.sc s	gdk04 5_mimc ap.scs	Temp eratu re	Output	LOOP _GAI N	Phase margi n	Gain margin	Phase margin frequency	Gain margin frequency
Nominal	1.2	1.62	tt	tt_mim	27	Nominal	61.75	82.7	23.5	23.22e6	144.8e6
FIELD7						min	59.82	60.6	21.51	12.16e6	103.8e6
FIELD8						max	65.42	96.54	28.44	35.19e6	192.1e6
CO_5	1.2	1.62	ff	ff_mim	125	CO_5	59.82	61.26	26.18	18.71e6	122e6
CO_6	1.2	1.98	ff	ff_mim	-40	CO_6	64.77	72.96	26.24	25.88e6	192.1e6
CO_7	600e-3	1.98	ff	ff_mim	125	CO_7	63.39	60.6	26.49	19.17e6	125.4e6
CO_8	600e-3	1.62	fs	ff_mim	-40	CO_8	62.36	96.34	23.95	13.3e6	146.6e6
CO_9	600e-3	1.62	fs	ff_mim	125	CO_9	61.29	85.31	25.28	14.35e6	116.4e6
CO_10	600e-3	1.98	fs	ff_mim	-40	CO_10	63.11	96.54	24.06	18.36e6	148.5e6
CO_11	1.2	1.98	fs	ff_mim	125	CO_12	62.11	85.29	25.38	14.43e6	117.6e6
CO_12	1.2	1.62	fs	ff_mim	-40	CO_13	62.31	85.48	21.51	34.09e6	158.3e6
CO_13	1.2	1.62	fs	ff_mim	125	CO_14	59.96	84.66	23.56	19.31e6	123.9e6
CO_14	1.2	1.98	fs	ff_mim	-40	CO_15	65.26	84.54	21.66	35.19e6	161.4e6
CO_15	600e-3	1.98	fs	ff_mim	125	CO_16	64.28	83.79	23.6	20.26e6	126.2e6
CO_16	600e-3	1.62	sf	ff_mim	-40	CO_16	61.95	96.22	24.63	15.24e6	140.5e6
CO_17	600e-3	1.62	sf	ff_mim	125	CO_17	60.77	85.2	25.93	13.12e6	115.2e6
CO_18	600e-3	1.98	sf	ff_mim	-40	CO_18	62.64	96.41	24.76	15.45e6	143.3e6
CO_19	600e-3	1.98	sf	ff_mim	125	CO_19	61.4	85.2	26.05	13.19e6	116.6e6
CO_20	1.2	1.62	sf	ff_mim	-40	CO_20	62.51	88.48	22.09	31.08e6	159.3e6
CO_21	1.2	1.62	sf	ff_mim	125	CO_21	60.46	84.81	24.09	18.16e6	124.3e6
CO_22	1.2	1.98	sf	ff_mim	-40	CO_22	64.86	88.09	22.31	31.83e6	162.8e6
CO_23	1.2	1.98	sf	ff_mim	125	CO_23	63.74	84.38	24.27	18.79e6	127.3e6
CO_24	600e-3	1.62	ss	ff_mim	-40	CO_24	62.31	94.43	25.05	12.84e6	128.5e6
CO_25	600e-3	1.62	ss	ff_mim	125	CO_25	61.53	83.65	26.23	12.16e6	108.9e6
CO_26	600e-3	1.98	ss	ff_mim	-40	CO_26	63.04	94.59	25.11	13.15e6	131.2e6
CO_27	600e-3	1.98	ss	ff_mim	125	CO_27	62.3	83.61	26.34	12.26e6	110.3e6
CO_28	1.2	1.62	ss	ff_mim	-40	CO_28	62.77	89.48	22.42	27.87e6	154.2e6
CO_29	1.2	1.62	ss	ff_mim	125	CO_29	60.67	83.49	24.44	16.89e6	119.8e6
CO_30	1.2	1.98	ss	ff_mim	-40	CO_30	65.42	89.04	22.62	28.59e6	157.4e6

Table 4.3 : Post Layout simulation table.

4.6.2 Post-Simulation result :

Sl. No.	Parameter	Value
1	Power Supply (Vdd)	1.62V
2	Load Capacitance (CL)	2pF
3	Loop Gain	61.75
4	Phase Margin (PM)	82.7
5	Voltage Common Mode (VCM)	1.2
6	CMRR	96.61
7	PSRR(-)	-52.92
	PSRR(+)	58.94
8	Power Consumption	9.58 μ

Table 4.4 : Table of Post – Simulation Result

5.1 Conclusion and Future Scope for work

This paper present design, layout and simulation of a two stage CMOS op-amp. The simulation result shows that the designed operational amplifier has successfully satisfied all the given specifications. By using CADENCE tool results are verified for the different parameters. The two stage op-amp operates in saturation mode . The designed and implemented two stage operational amplifier achieved the targeted gain.

As the required Gain and Phase Margin of the design is obtained, the design is ready for use as a fundamental part for various electronic devices.

Overall, I would describe my internship as a positive and instructive experiment. The completion of this internship give me so much knowledge about analog simulation, design and layout. I also get to know how the real design and layout is carried out in industries.

This internship provides me the minimum knowledge required to work for bigger projects as a design or layout Engineer in VLSI design and layout domain. For future aspect, I can pursue my career as a design or layout engineer in VLSI domain.

5.2 References

1. CMOS Analog Circuit Design by Phillip E Allen Douglas R . Holberg Third edition.
2. Design of Analog CMOS Integrated Circuits by Behzad Razavi Second Edition
3. CMOS Circuit Design , Layout and Simulation by R Jacob Baker IEEE Press Series on Microelectronics System Third Edition