REVISION	PAGE	REVISION DESCRIPTION	APPROVAL	DATE
A	All	Released to production	CEV	22Jan02
A.1	all 5,7 11 11 - 16 13,34 34	Added part numbers NA162SD07CA/DA-### and NA202SD16CA/DA-### Added side views and end views for -##2 and -##3 part numbers in Sec. 3.2.2 and 3.2.4 Supply voltage was 6.5V Max. in Sec. 3.5 Added Supply voltage, Supply current, and Timing specifications for 3.3V version in Sec. 3.5 - 3.7 Added Note 2 to Sec 3.7.2 and 8.0 Added 3.3V (C and D), Slimline (-##3 and -##3), and Motorola M68 parallel interface without read function (-3##) options to part number tree in Sec. 9.0	CEV	05Jun06
A.2	18 all all	Added (M68 mode only) and (M68 or I80 modes) to Sec. 4.1 for clarification Part number NA402SD10AB/BB-### was NA402SD10AA/BA-### (ECO 09-002) Part number NA204SD02AB/BB-### was NA204SD02AA/BA-### (ECO 09-003)	CEV	29Jan10

This specification applies to the following product part numbers:

PART NUMBER
NA16SD08AA/BA-###
NA162SD07AA/BA/CA/DA-###
NA202MD15AA/BA-###
NA202SD16AA/BA/CA/DA-###
NA204SD02AB/BB-###
NA242SD04AA/BA-###
NA402SD10AB/BB-###

Futaba®

Futaba Corporation of America Schaumburg, IL

DRAWING TITLE: PRODUCT SPECIFICATION

PART NUMBER: LCD EMULATORS

DESIGNED BY:	SYSTEMS ENGINEERING APPROVAL:	CUSTOMER NAME / PART NUMBER:	
Futaba	Charles Voegeli	STANDARD PRODUCT	
CHECKED BY:	QUALITY ASSURANCE APPROVAL:	FILE NAME:	
Systems Engineering	John Kowalewski	LCD_Emulators_revA.2_29Jan10.doc	
CUSTOMER APPROVAL:	DIRECTOR OF ENGINEERING APPROVAL:	DATE PRINTED:	SHEET:
N/A	Gary R. Wires	29Jan10	1 OF 34

1.0 GENERAL DESCRIPTION

The Futaba LCD Emulator vacuum fluorescent display (VFD) modules consist of a multiple character by multiple or single line 5x8 dot matrix display, DC-DC/AC converter, and controller/driver circuitry. The modules are designed to be directly compatible with industry standard liquid crystal display (LCD) modules that utilize the Hitachi HD44780U LCD controller/driver. The modules can be configured for a Motorola M68-type parallel interface, an Intel I80-type parallel interface, or a synchronous serial interface. A character generator ROM with 240 5x8 characters is provided along with RAM for the user to program an additional 8 characters. The luminance level of the VFD can be varied by setting two bits in the function set instruction, which are "don't care" bits for LCD modules. Additional options include English-Katakana or English-European character font, with or without a connector, and internal or external reset function.

A primary advantage of these modules over industry standard LCD modules is that they have a dual-port RAM that allows data and instructions to be sent to them continuously. Thus, the busy flag is always 0 and the host never has to read the busy flag bit to determine if the modules are busy. Due to this feature, the execution times for each instruction are not specified.

2.0 APPLICABLE DOCUMENTS

1) Futaba Vacuum Fluorescent Display Specifications (see table below)

LCD Emulator Part Number	Futaba VFD Specification
NA16SD08AA/BA-###	16-SD-08GNK
NA162SD07AA/BA/CA/DA-###	162-SD-07GN
NA202MD15AA/BA-###	202-MD-15GNK
NA202SD16AA/BA/CA/DA-###	202-SD-16GN
NA204SD02AB/BB-###	204-SD-02GN
NA242SD04AA/BA-###	242-SD-04GN
NA402SD10AB/BB-###	402-SD-10G

2) Futaba America Engineering Standard FAES 801, Printed Circuit Board Markings

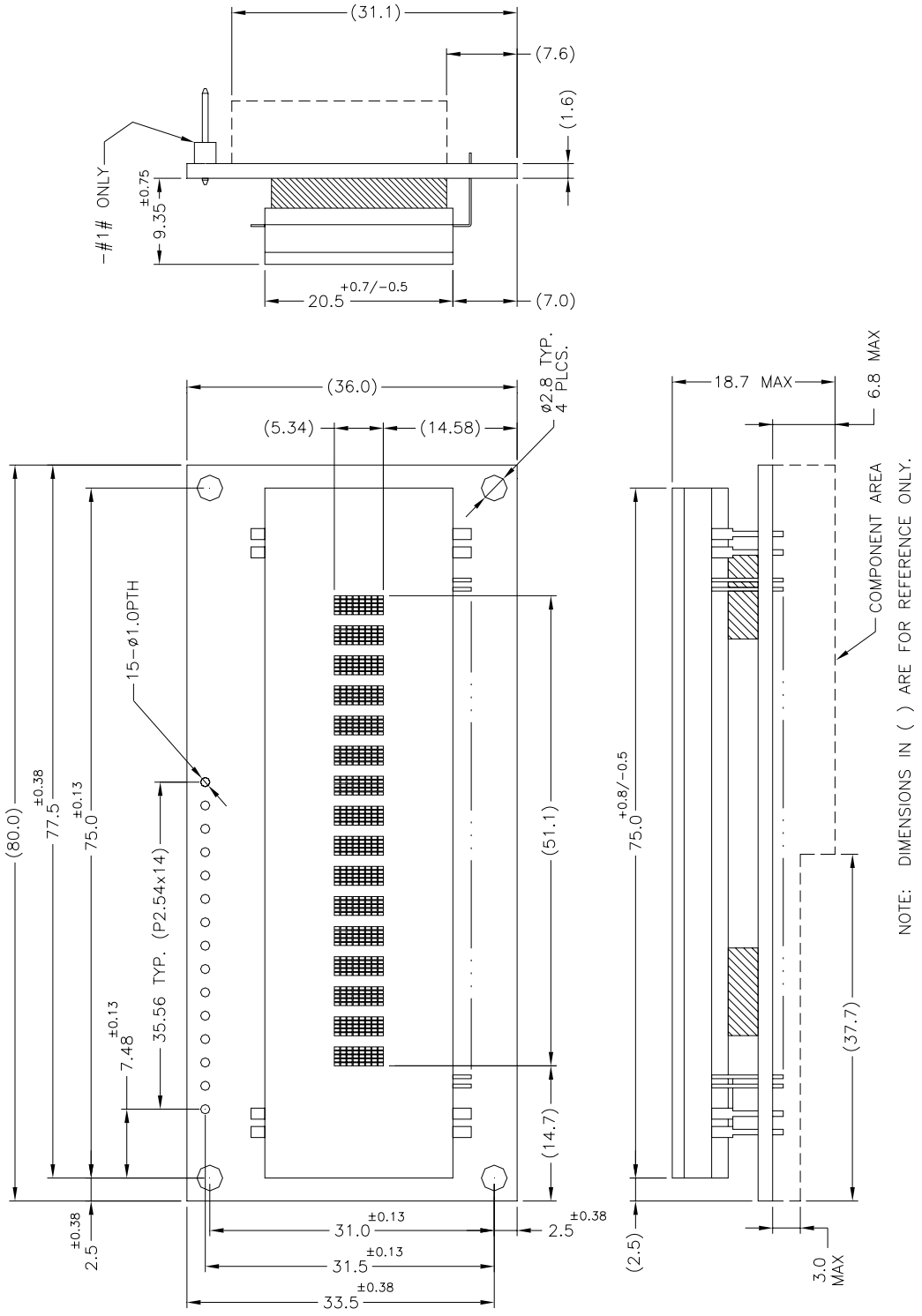
3.0 SPECIFICATIONS

3.1 GENERAL SPECIFICATIONS

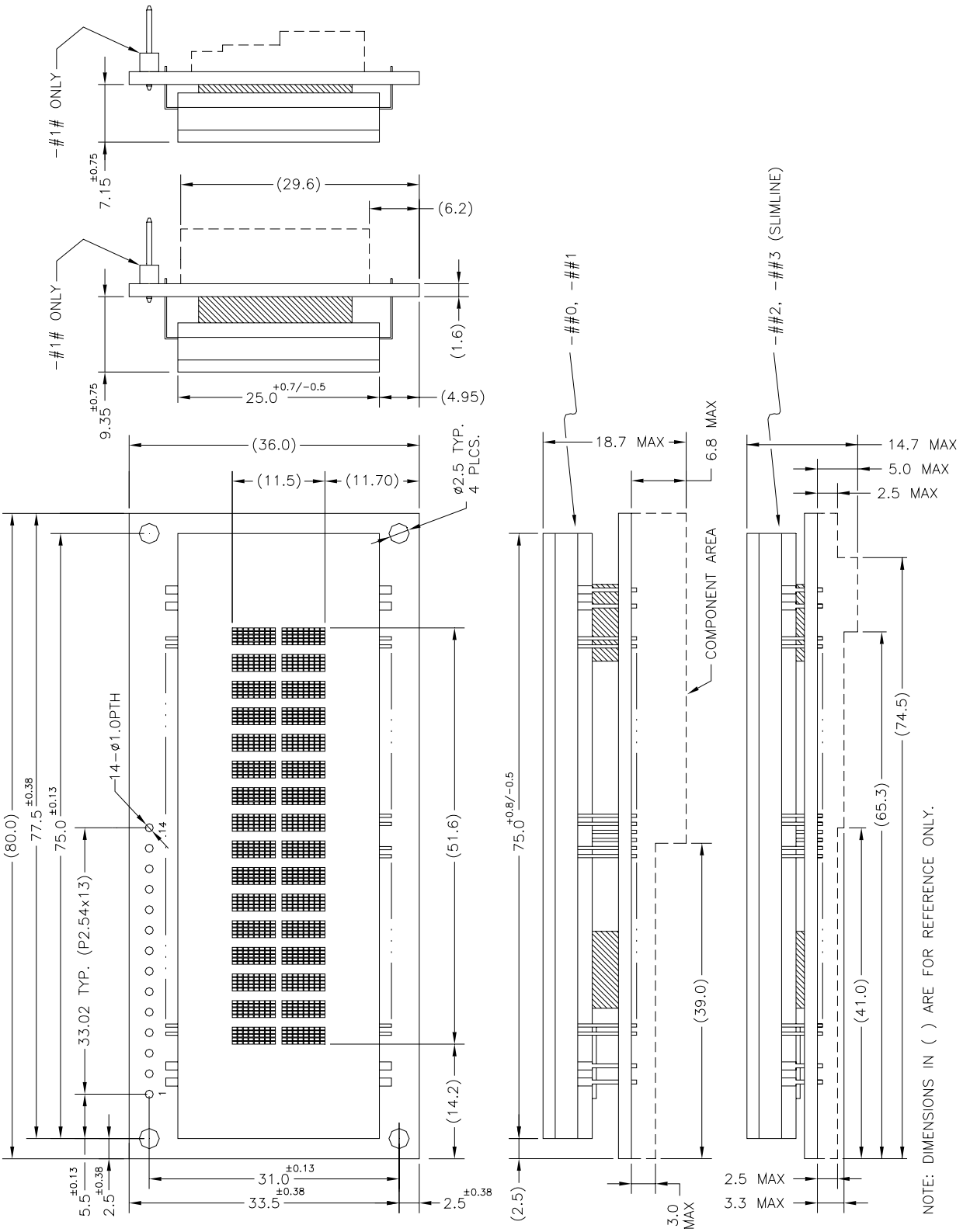
Item		NA16SD08AA/BA-###	NA162SD07AA/BA/CA/DA-###	NA202MD15AA/BA-###	NA202SD16AA/BA/CA/DA-###	NA204SD02AB/BB-###	NA242SD04AA/BA-###	NA402SD10AB/BB-###
Number of characters (char x line)		16 x 1	16 x 2	20 x 2	20 x 2	20 x 4	24 x 2	40 x 2
Character configuration		5 x 8 dot matrix						
Character height (mm)		5.34	5.34	8.86	5.34	4.84	5.34	5.34
Character width (mm)		2.05	2.10	3.90	2.35	2.35	2.17	2.15
Character pitch (mm)		3.27	3.30	5.15	3.60	3.75	3.57	3.40
Line pitch (mm)		NA	6.16	9.64	6.16	8.71	6.16	6.16
Dot size (mm)	width	0.33	0.34	0.70	0.39	0.39	0.35	0.35
	height	0.58	0.58	1.02	0.58	0.52	0.58	0.58
Dot pitch (mm)	width	0.43	0.44	0.80	0.49	0.49	0.45	0.45
	height	0.68	0.68	1.12	0.68	0.62	0.68	0.68
Peak wavelength of illumination		Green (505 nm) x = 0.235, y = 0.405						
Luminance (cd/m^2 / fL)	min.	350 / 102						
	typ.	500 / 146						

3.2 MECHANICAL DRAWINGS

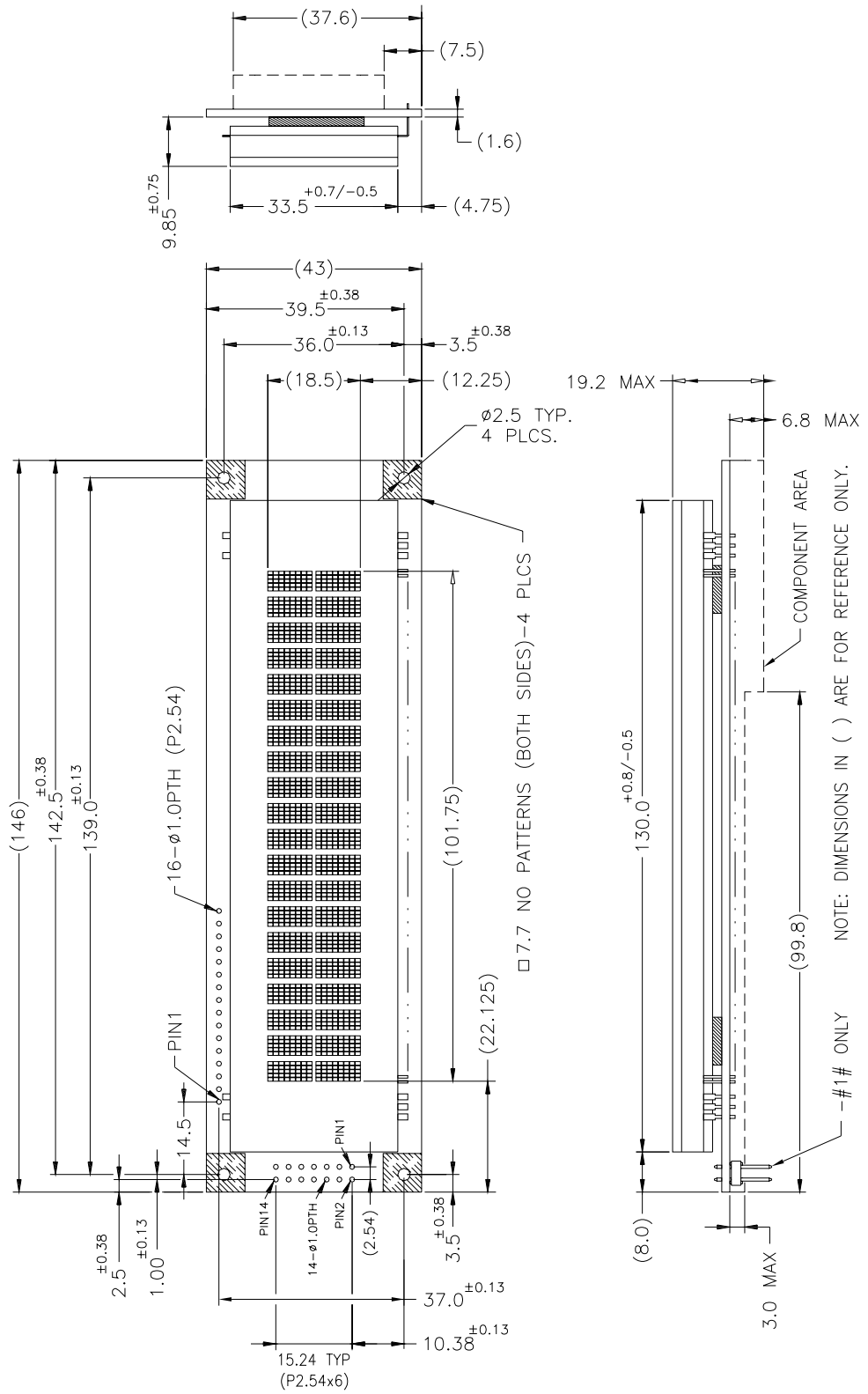
3.2.1 NA16SD08AA/BA-###



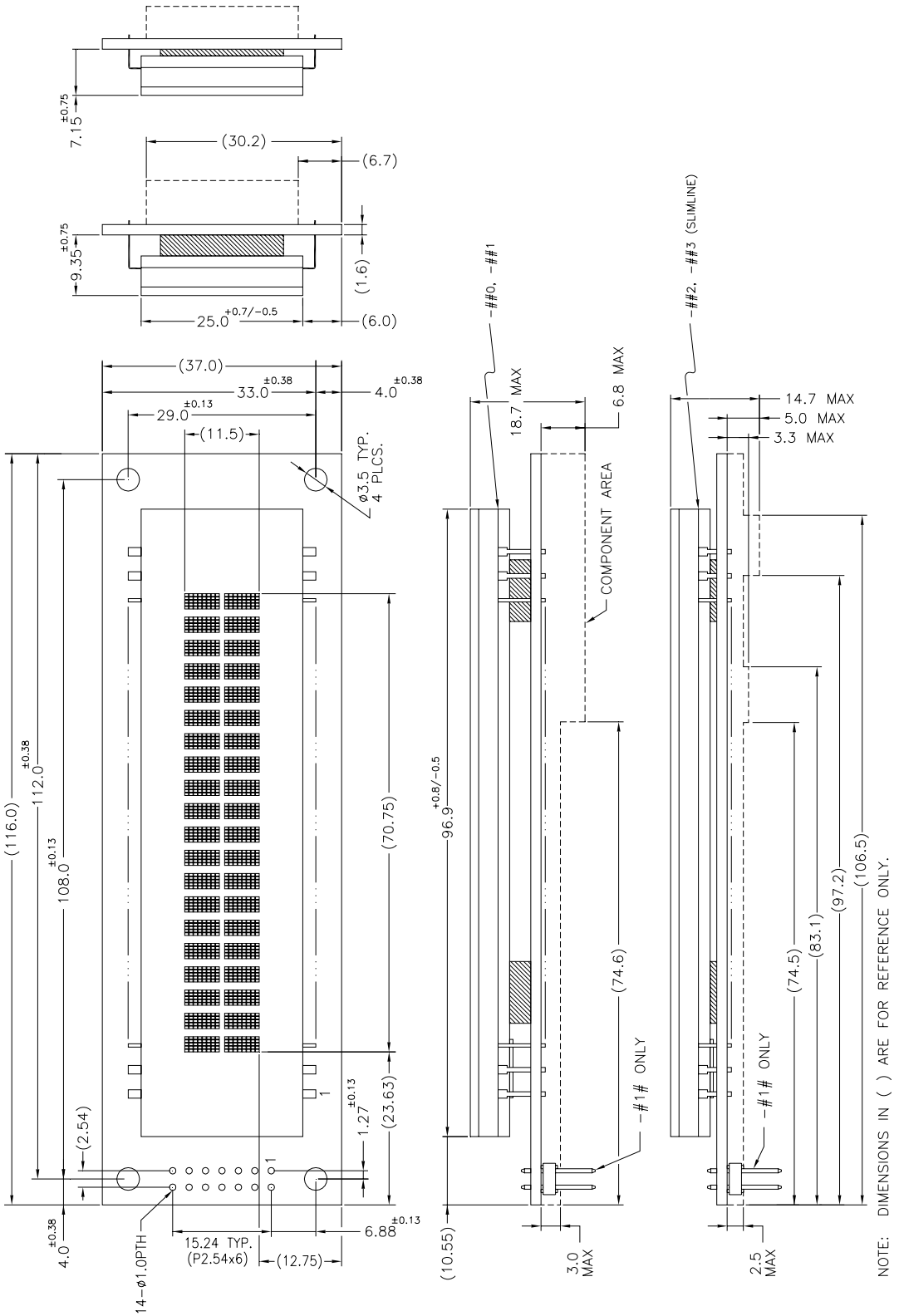
3.2.2 NA162SD07AA/BA/CA/DA-###



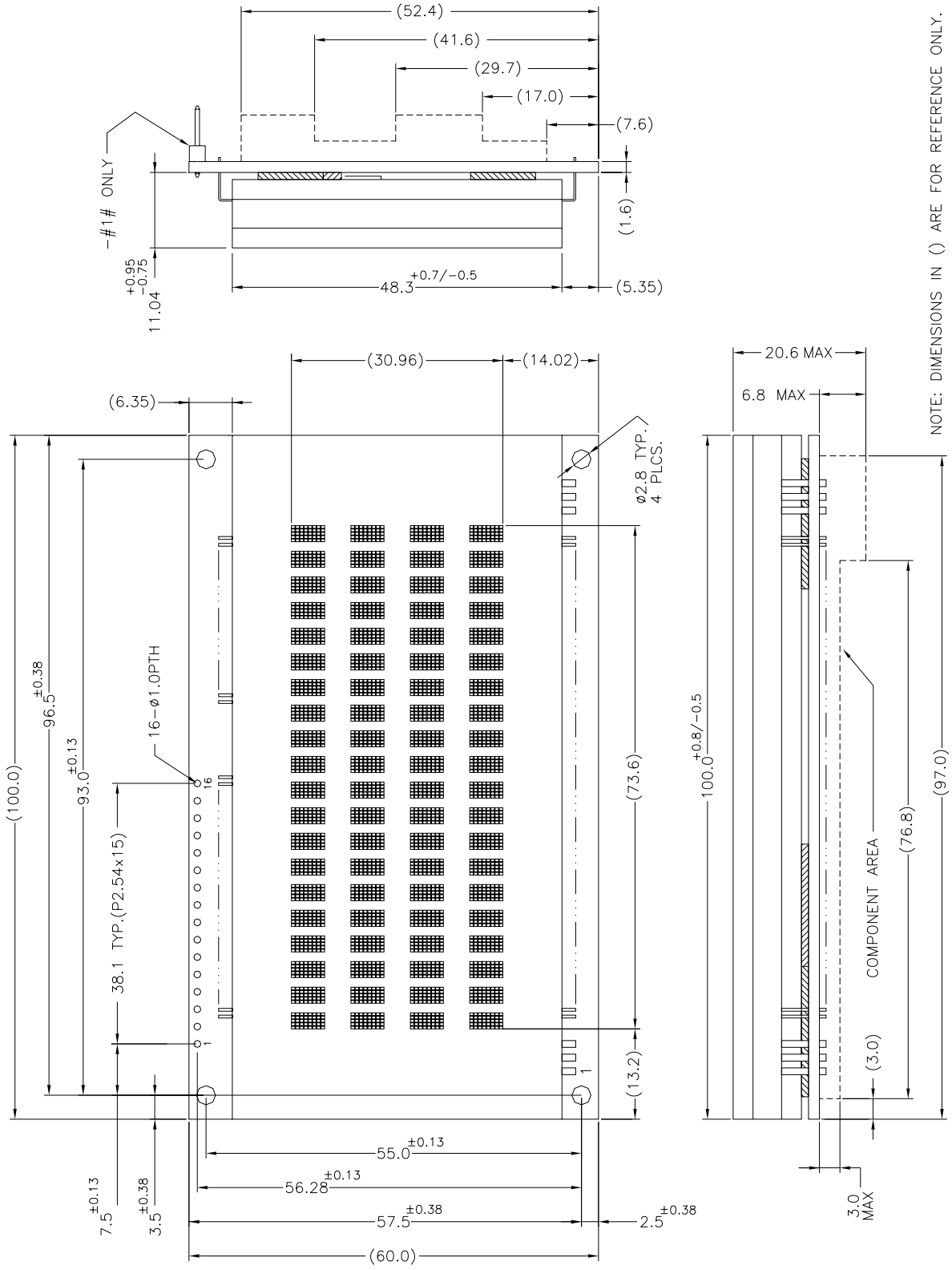
3.2.3 NA202MD15AA/BA-###



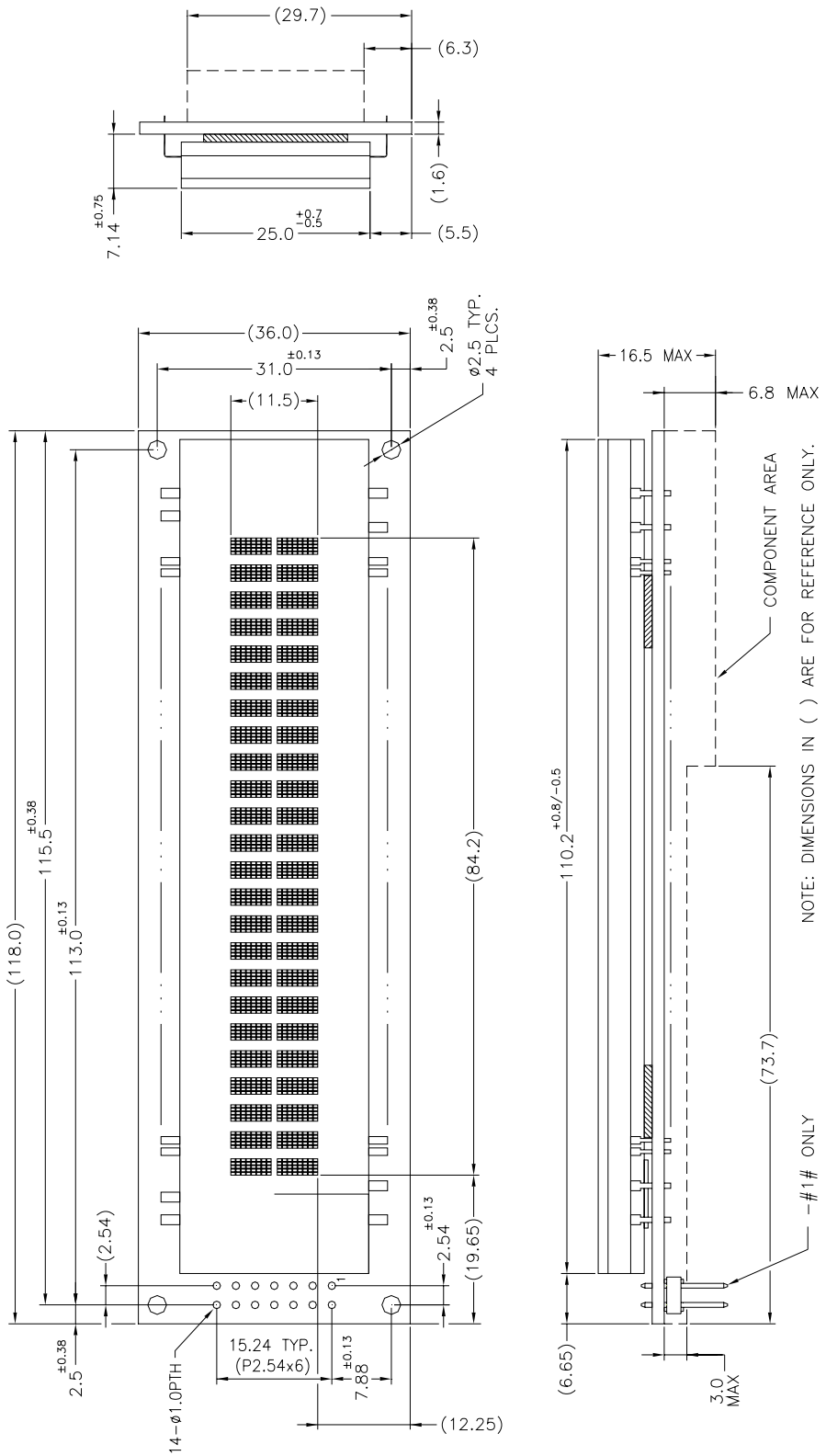
3.2.4 NA202SD16AA/BA/CA/DA-###



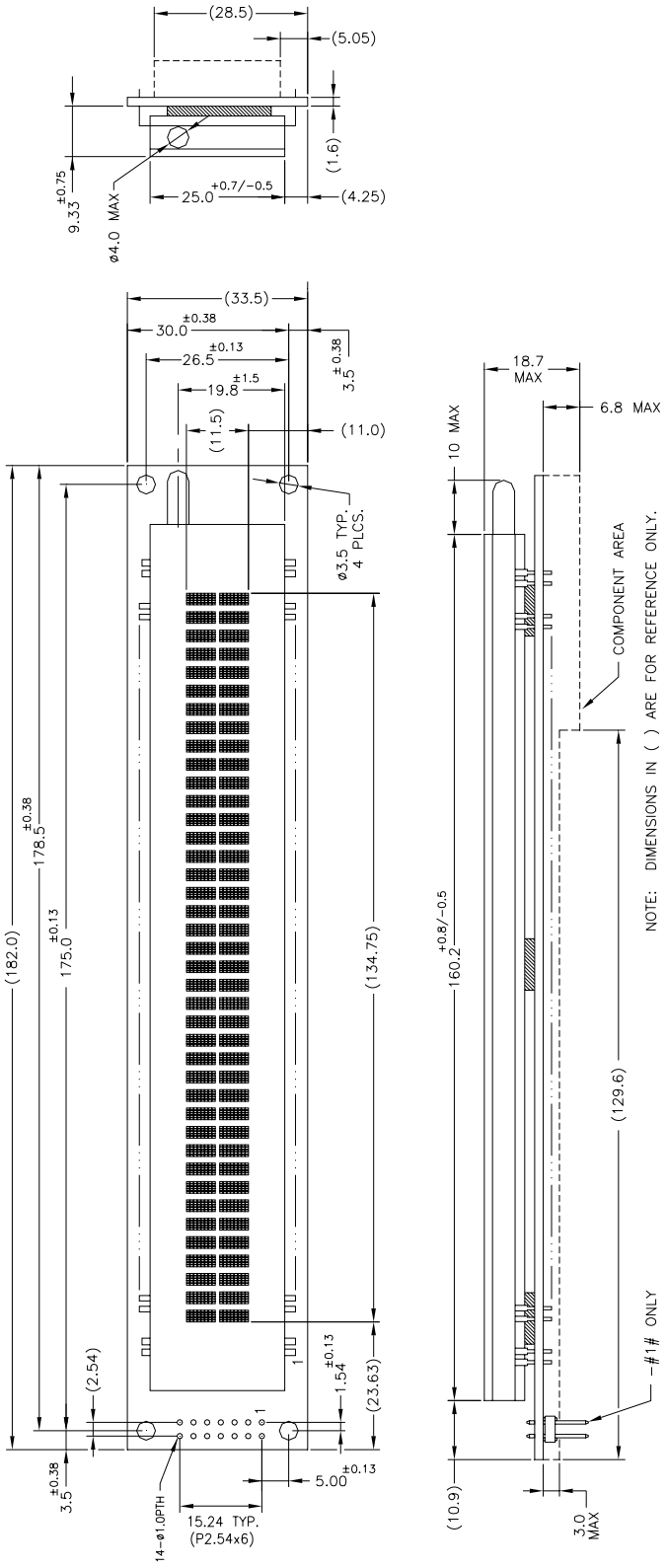
3.2.5 NA204SD02AB/BB-###



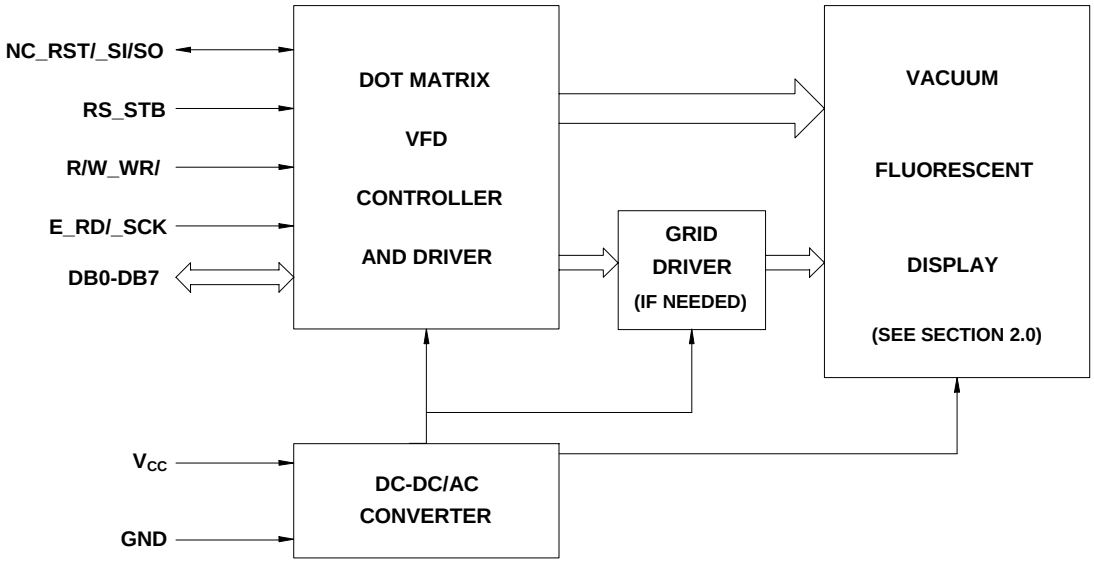
3.2.6 NA242SD04AA/BA-###



3.2.7 NA402SD10AB/BB-###



3.3 SYSTEM BLOCK DIAGRAM



3.4 ENVIRONMENTAL SPECIFICATIONS

Item	Symbol	Min.	Max.	Unit	Comment
Operating temperature	Topr	-40	+85	^{o}C	
Storage temperature	Tstg	-55	+85	^{o}C	
Operating humidity	Hopr	20	85	%RH	Without condensation
Storage humidity	Hstg	20	90	%RH	Without condensation
Vibration	--	--	4	G	Total amplitude: 1.5mm Freq: 10 - 55 Hz sine wave Sweep time: 1 min./cycle Duration: 2 hrs./axis (X,Y,Z)
Shock	--	--	40	G	Duration: 11ms Waveform: half sine wave 3 times/axis (X,Y,Z,-X,-Y,-Z)

3.5 ABSOLUTE MAXIMUM SPECIFICATIONS

Item		Symbol	Min.	Max.	Unit
Supply voltage	5.0V version	V_{CC}	-0.3	6.0	V
	3.3V version		-0.3	3.96	
Input signal voltage		V_{IN}	-0.3	V_{CC}+0.3	V

3.6 DC ELECTRICAL SPECIFICATIONS

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	5.0V version	V_{CC}	4.5	5.0	5.5	V
	3.3V version		2.97	3.3	3.63	
Supply current	NA16SD08AA/BA-###	I_{CC}	-	65	95	mA
	NA162SD07AA/BA-###		-	120	170	
	NA162SD07CA/DA-###		-	185	260	
	NA202MD15AA/BA-###		-	310	440	
	NA202SD16AA/BA-###		-	140	190	
	NA202SD16CA/DA-###		-	215	290	
	NA204SD02AB/BB-###		-	300	400	
	NA242SD04AA/BA-###		-	155	215	
	NA402SD10AB/BB-###		-	220	300	
High-level input voltage (see Note) (E,R/W,RD/,SCK,RST/)		V_{IH1}	0.8*V_{CC}	-	V_{CC}	V
Low-level input voltage (see Note) (E,R/W,RD/,SCK,RST/)		V_{IL1}	0.0	-	0.2*V_{CC}	V
High-level input voltage (see Note) (all inputs except E,R/W,RD/,SCK,RST/)		V_{IH2}	0.7*V_{CC}	-	V_{CC}	V
Low-level input voltage (see Note) (all inputs except E,R/W,RD/,SCK,RST/)		V_{IL2}	0.0	-	0.3*V_{CC}	V
High-level output voltage (I_{OH} = -0.1mA)		V_{OH}	V_{CC}-0.5	-	-	V
Low-level output voltage (I_{OL} = 0.1mA)		V_{OL}	-	-	0.5	V
Input current (see Note)		I_I	-500	-	1.0	uA

Note: A 10K ohm pull-up resistor is provided on each input for TTL compatibility.

3.7 AC ELECTRICAL SPECIFICATIONS

3.7.1 RESET TIMING

(See Figures 1 and 2)

Item	Symbol	Min.	Max.	Unit
V_{CC} rise time	t_{RVCC}	-	10	ms
V_{CC} off time	t_{OFF}	1	-	ms
Delay time after power-up reset	t_{IRSTD}	100	-	us
Delay time after external reset	t_{ERSTD}	100	-	us
RST/ pulse width low	t_{RSTL}	500	-	ns
Input signal fall time	t_f	-	15	ns
Input signal rise time	t_r	-	15	ns

Note: All timing is specified using 20% and 80% of V_{CC} as the reference points.

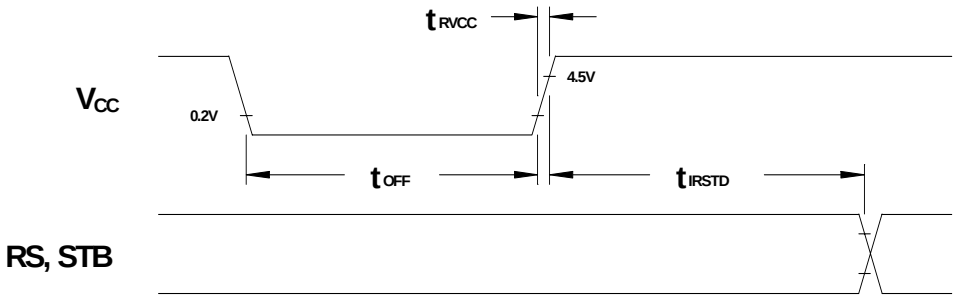


Figure 1. Power-up Internal Reset Timing

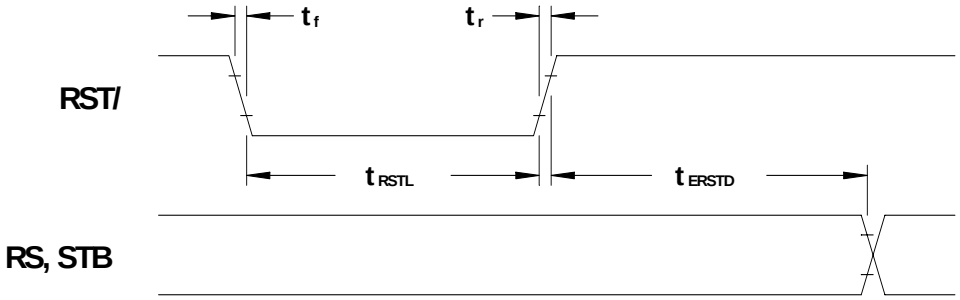


Figure 2. External Reset Timing

3.7.2 MOTOROLA M68-TYPE PARALLEL INTERFACE TIMING

(See Figures 3 and 4)

Item	Symbol	3.3V version		5.0V version		Unit
		Min.	Max.	Min.	Max.	
RS, R/W setup time	t_{AS}	60	-	20	-	ns
RS, R/W hold time	t_{AH}	30	-	10	-	ns
Input signal rise time	t_r	-	15	-	15	ns
Input signal fall time	t_f	-	15	-	15	ns
E pulse width high	PW_{EH}	450	-	230	-	ns
E pulse width low	PW_{EL}	450	-	230	-	ns
Write data setup time	t_{DS}	195	-	80	-	ns
Write data hold time	t_{DH}	10	-	10	-	ns
E cycle time	t_{CYCE}	1000	-	500	-	ns
Read data delay time (Note 2)	t_{DD}	-	360	-	160	ns
Read data hold time (Note 2)	t_{DHR}	5	-	5	-	ns

Note 1: All timing is specified using 20% and 80% of V_{CC} as the reference points.
Note 2: Read function not guaranteed on -3## part numbers.

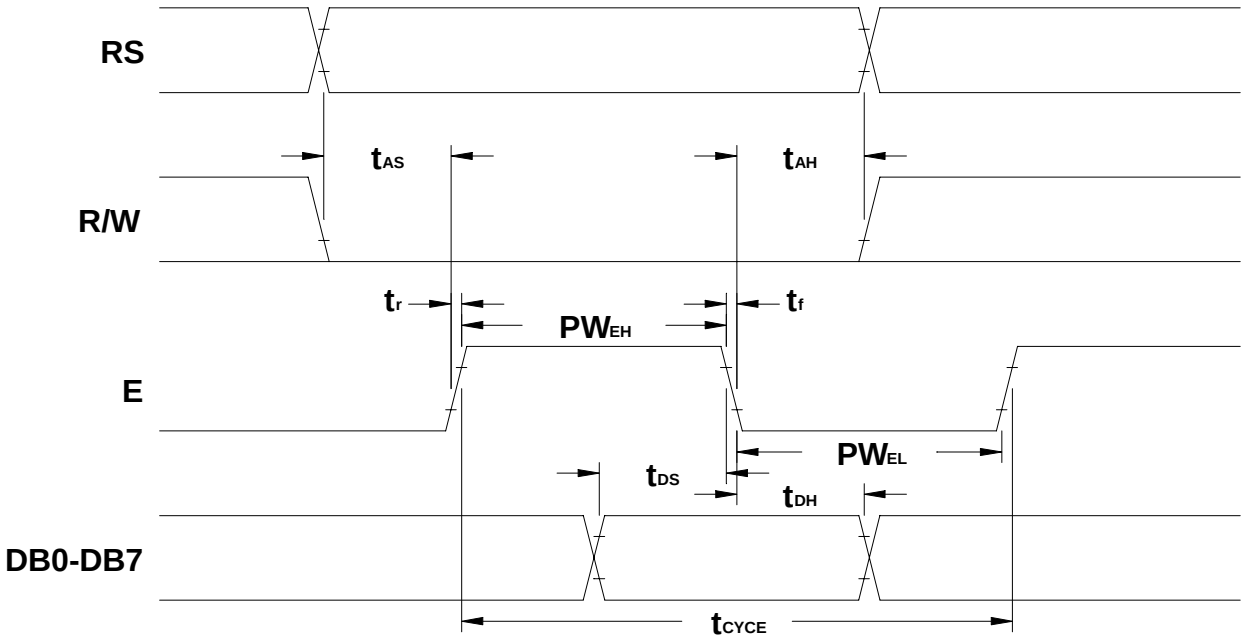


Figure 3. Motorola M68-Type Parallel Interface Write Cycle Timing

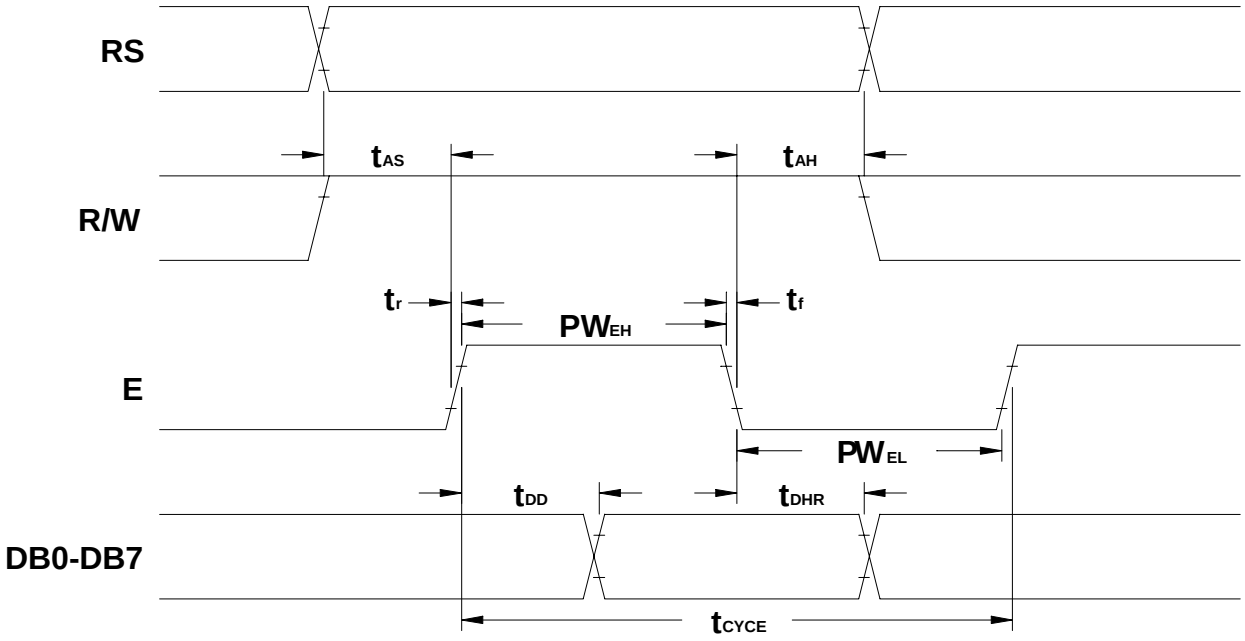


Figure 4. Motorola M68-Type Parallel Interface Read Cycle Timing

3.7.3 INTEL I80-TYPE PARALLEL INTERFACE TIMING

(See Figures 5 and 6)

Item	Symbol	3.3V version		5.0V version		Unit
		Min.	Max.	Min.	Max.	
RS setup time	t_{RSS}	30	-	10	-	ns
RS hold time	t_{RSH}	20	-	10	-	ns
Input signal fall time	t_f	-	15	-	15	ns
Input signal rise time	t_r	-	15	-	15	ns
WR/ pulse width low	t_{WRL}	50	-	30	-	ns
WR/ pulse width high	t_{WRH}	200	-	100	-	ns
Write data setup time	t_{DSi}	60	-	30	-	ns
Write data hold time	t_{DHi}	20	-	10	-	ns
WR/ cycle time	t_{CYCWR}	600	-	200	-	ns
RD/ cycle time	t_{CYCRD}	600	-	200	-	ns
RD/ pulse width low	t_{RDL}	200	-	70	-	ns
RD/ pulse width high	t_{RDH}	200	-	100	-	ns
Read data delay time	t_{DDi}	-	140	-	70	ns
Read data hold time	t_{DHRi}	5	-	5	-	ns

Note: All timing is specified using 20% and 80% of V_{CC} as the reference points.

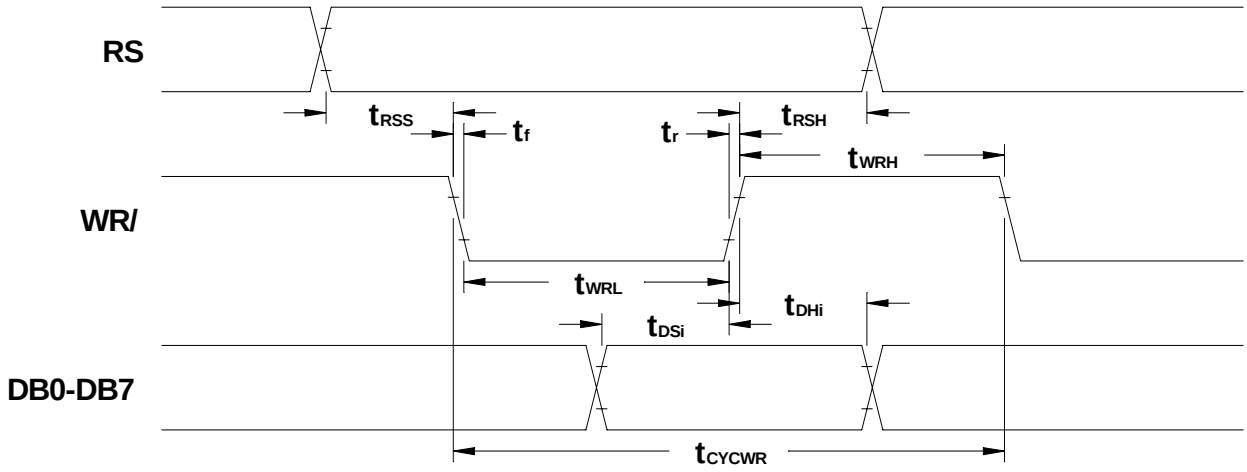


Figure 5. Intel I80-Type Parallel Interface Write Cycle Timing

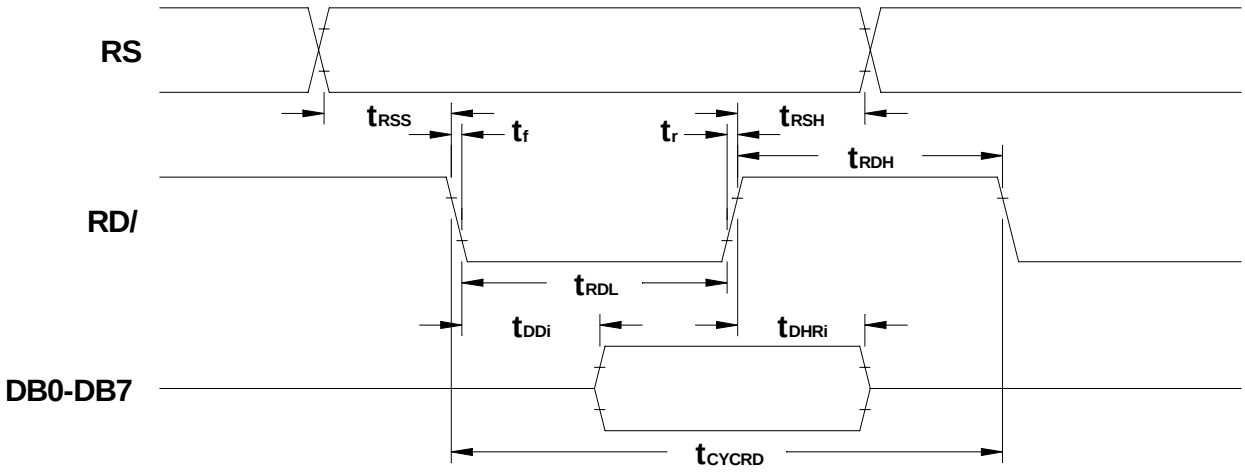


Figure 6. Intel I80-Type Parallel Interface Read Cycle Timing

3.7.4 SYNCHRONOUS SERIAL INTERFACE TIMING

(See Figures 7, 8 and 12)

Item	Symbol	3.3V version		5.0V version		Unit
		Min.	Max.	Min.	Max.	
STB setup time	t_{STBS}	150	-	100	-	ns
STB hold time	t_{STBH}	750	-	500	-	ns
Input signal fall time	t_f	-	15	-	15	ns
Input signal rise time	t_r	-	15	-	15	ns
STB pulse width high	t_{WSTB}	750	-	500	-	ns
SCK pulse width high	t_{SCKH}	300	-	200	-	ns
SCK pulse width low	t_{SCKL}	300	-	200	-	ns
SI data setup time	t_{DSs}	150	-	100	-	ns
SI data hold time	t_{DHs}	150	-	100	-	ns
SCK cycle time	t_{CYCSCK}	1000	-	500	-	ns
SCK wait time between bytes	t_{WAIT}	1	-	1	-	us
SO data delay time	t_{DDs}	-	300	-	150	ns
SO data hold time	t_{DHRs}	5	-	5	-	ns

Note: All timing is specified using 20% and 80% of V_{CC} as the reference points.

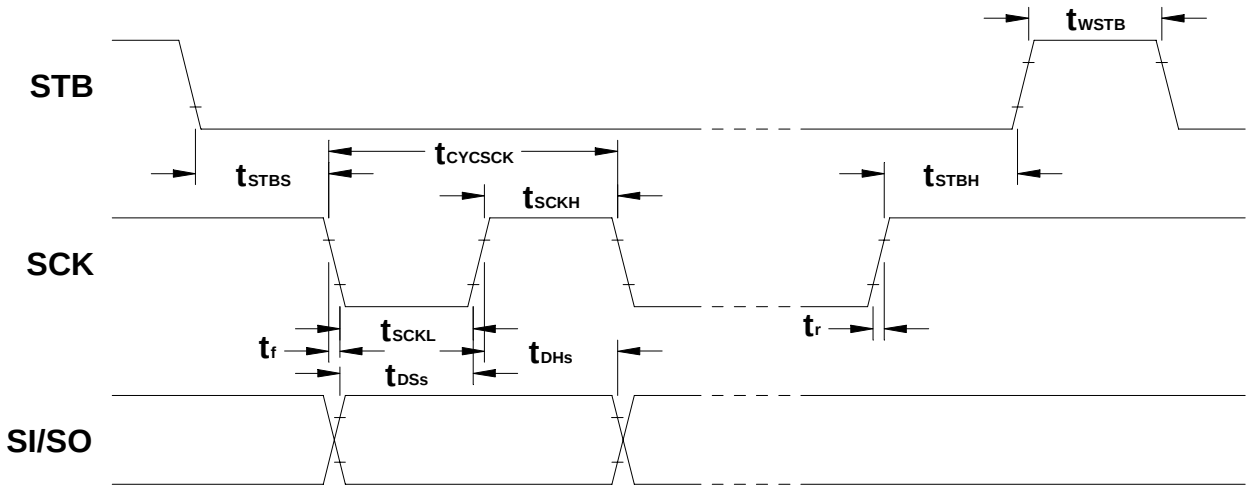


Figure 7. Synchronous Serial Interface Write Cycle Timing

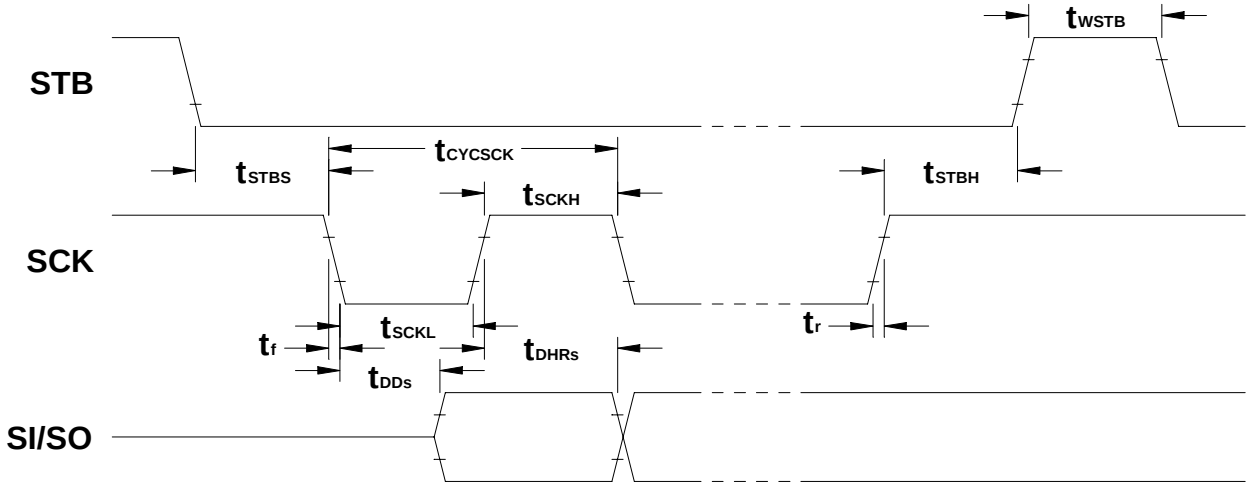


Figure 8. Synchronous Serial Interface Read Cycle Timing

4.0 MODES OF OPERATION

The following modes of operation are selectable via jumpers (see section 8.0 Jumper Settings).

4.1 PARALLEL INTERFACE MODES

In the parallel interface mode, 8-bit instructions and data are sent between the host and the modules using either 4-bit nibbles (M68 mode only) or 8-bit bytes (M68 or I80 modes). Nibbles are transmitted high nibble first on DB4-DB7 (DB0-DB3 are ignored) whereas bytes are transmitted on DB0-DB7. The Register Select (RS) control signal is used to identify DB0-DB7 as an instruction (low) or data (high).

4.1.1 MOTOROLA M68-TYPE MODE

This mode uses the Read/Write (R/W) and Enable (E) control signals to transfer information. Instructions/data are written to the modules on the falling edge of E when R/W is low and are read from the modules after the rising edge of E when R/W is high.

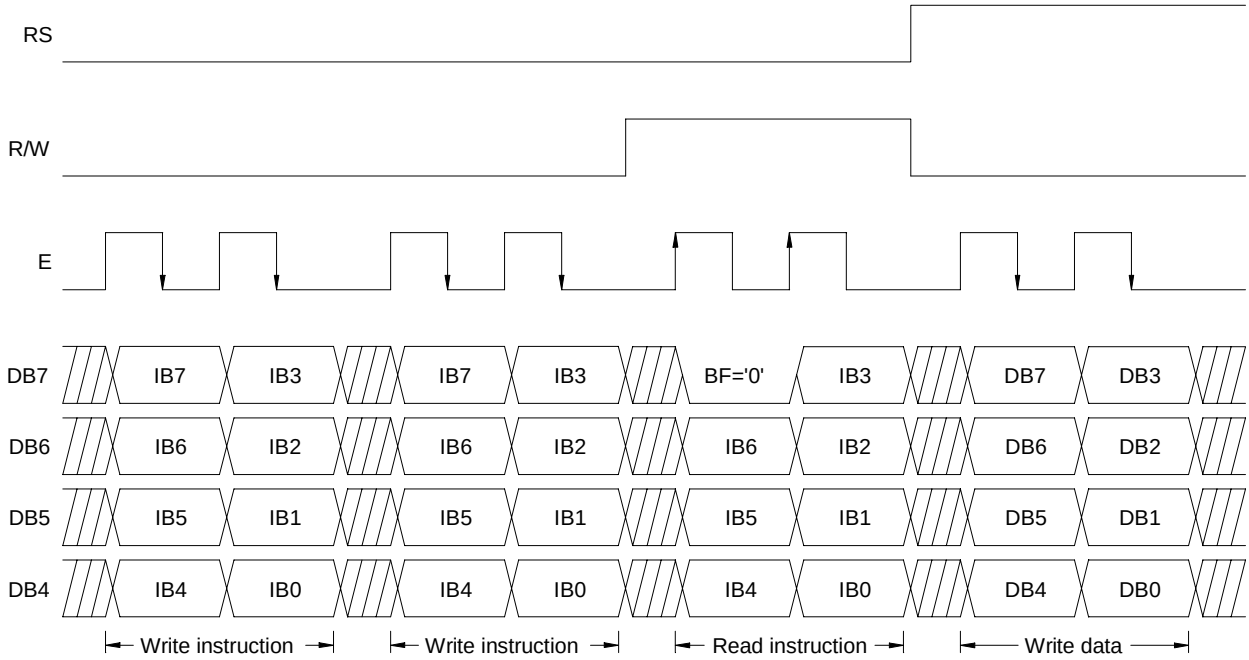


Figure 9. Typical 4-Bit Parallel Interface Sequence Using M68-Type Mode

4.1.2 INTEL I80-TYPE MODE

This mode uses the Read (RD/) and Write (WR/) control signals to transfer information. Instructions/data are written to the modules on the rising edge of WR/ and are read from the modules after the falling edge of RD/. When reading from the DDRAM a dummy read must be executed after the AC has been set.

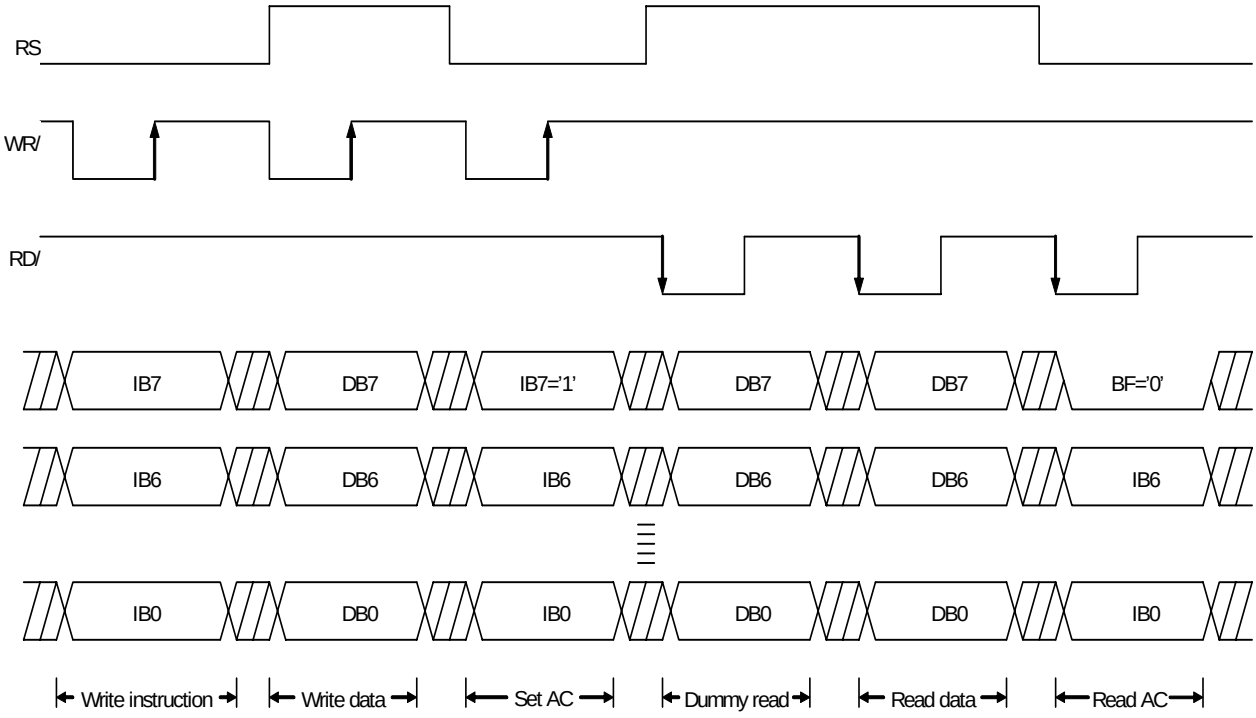


Figure 10. Typical 8-Bit Parallel Interface Sequence Using I80-Type Mode

4.2 SYNCHRONOUS SERIAL INTERFACE MODE

In the synchronous serial interface mode, instructions and data are sent between the host and the modules using 8-bit bytes. Two bytes are required per read/write cycle and are transmitted MSB first. The start byte contains 5 high bits, the Read/Write (R/W) control bit, the Register Select (RS) control bit, and a low bit. The following byte contains the instruction/data bits. The R/W bit determines whether the cycle is a read (high) or a write (low) cycle. The RS bit is used to identify the second byte as an instruction (low) or data (high).

This mode uses the Strobe (STB) control signal, Serial Clock (SCK) input, and Serial I/O (SI/SO) line to transfer information. In a write cycle, bits are clocked into the modules on the rising edge of SCK. In a read cycle, bits in the start byte are clocked into the modules on the rising edge of SCK. After the minimum wait time, each bit in the instruction/data byte can be read from the modules after each falling edge of SCK. The AC must be set at the beginning of a valid read cycle. Each read/write cycle begins on the falling edge of STB and ends on the rising edge. To be a valid read/write cycle, the STB must go high at the end of the cycle.

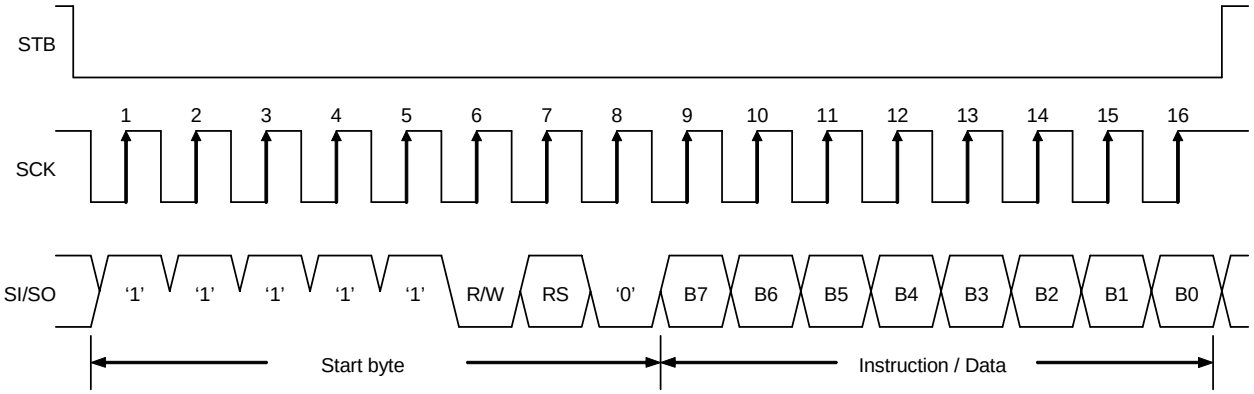


Figure 11. Typical Synchronous Serial Interface Write Cycle

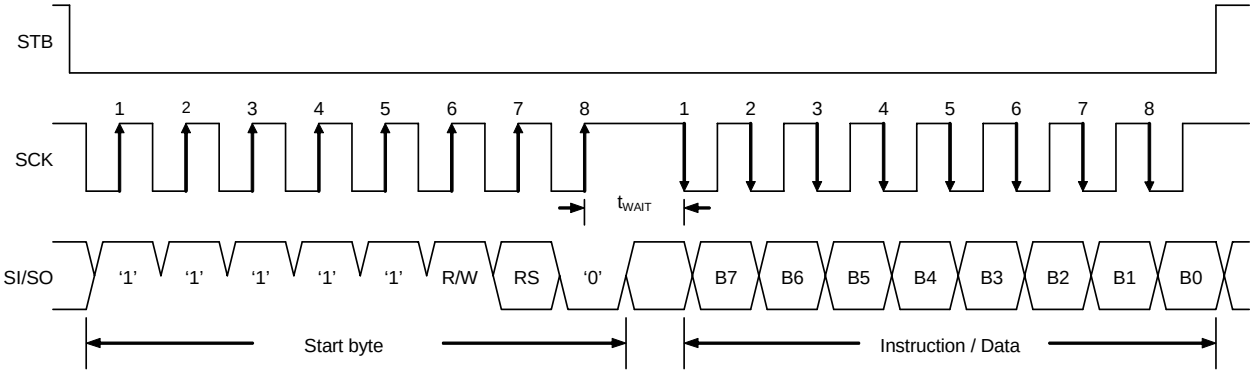


Figure 12. Typical Synchronous Serial Interface Read Cycle

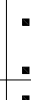
4.3 RESET MODES

The modules are reset automatically at power-up by an internal R-C circuit. However, an external reset mode can also be selected when using one of the parallel interface modes (this option is not available when using the synchronous serial interface mode). This mode allows the modules to be reset by setting the Reset (RST/) input low.

5.0 CHARACTER FONT TABLES

5.1 ENGLISH / KATAKANA CHARACTER FONT (OPTIONS A AND C)

5.2 ENGLISH / EUROPEAN CHARACTER FONT (OPTIONS B AND D)

UPPER NIBBLE / LOWER NIBBLE	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)																
0001	CG RAM (2)																
0010	CG RAM (3)																
0011	CG RAM (4)																
0100	CG RAM (5)																
0101	CG RAM (6)																
0110	CG RAM (7)																
0111	CG RAM (8)																
1000	CG RAM (1)																
1001	CG RAM (2)																
1010	CG RAM (3)																
1011	CG RAM (4)																
1100	CG RAM (5)																
1101	CG RAM (6)																
1110	CG RAM (7)																
1111	CG RAM (8)																

6.0 FUNCTIONAL DESCRIPTION

6.1 ADDRESS COUNTER (AC)

6.1.1 SINGLE LINE DISPLAYS

The AC stores the address of the data being written to and read from DDRAM or CGRAM. The AC increments by 1 (overflows from 4FH to 00H) or decrements by 1 (underflows from 00H to 4FH) after each DDRAM access. The AC increments by 1 (overflows from 3FH to 00H) or decrements by 1 (underflows from 00H to 3FH) after each CGRAM access. When addressing DDRAM, the value in the AC also represents the cursor position.

6.1.2 MULTIPLE LINE DISPLAYS

The AC stores the address of the data being written to and read from DDRAM or CGRAM. The AC increments by 1 (overflows from 27H to 40H and from 67H to 00H) or decrements by 1 (underflows from 40H to 27H and from 00H to 67H) after each DDRAM access. The AC increments by 1 (overflows from 3FH to 00H) or decrements by 1 (underflows from 00H to 3FH) after each CGRAM access. When addressing DDRAM, the value in the AC also represents the cursor position.

6.2 DISPLAY DATA RAM (DDRAM)

6.2.1 SINGLE LINE DISPLAYS

The DDRAM stores the character code of each character being displayed on the VFD. Valid DDRAM addresses are 00H to 4FH. DDRAM not being used for display characters can be used as general purpose RAM. The tables below show the relationship between the DDRAM address and the character position on the VFD before and after a display shift (with the number of display lines set to 1).

6.2.2 MULTIPLE LINE DISPLAYS

The DDRAM stores the character code of each character being displayed on the VFD. Valid DDRAM addresses are 00H to 27H and 40H to 67H. DDRAM not being used for display characters can be used as general purpose RAM. The tables below show the relationship between the DDRAM address and the character position on the VFD before and after a display shift (with the number of display lines set to 2).

6.3 DISPLAY SHIFT DETAIL

6.3.1 NA16SD08AA/BA-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

Relationship after a display shift to the left:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

6.3.2 NA162SD07AA/BA/CA/DA-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Relationship after a display shift to the left:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

6.3.3 NA202MD15AA/BA-### AND NA202SD16AA/BA/CA/DA-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

Relationship after a display shift to the left:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52

6.3.4 NA204SD02AB/BB-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
4	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

Relationship after a display shift to the left:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54
3	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	00
4	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	40

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52
3	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26
4	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66

6.3.5 NA242SD04AA/BA-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57

Relationship after a display shift to the left:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56

6.3.6 NA402SD10AB/BB-###

Relationship before a display shift (non-shifted):

	1	2	3	4	5	6	7	8	9					32	33	34	35	36	37	38	39	40
1	00	01	02	03	04	05	06	07	08	-	-	-	-	1F	20	21	22	23	24	25	26	27
2	40	41	42	43	44	45	46	47	48	-	-	-	-	5F	60	61	62	63	64	65	66	67

Relationship after a display shift to the left:

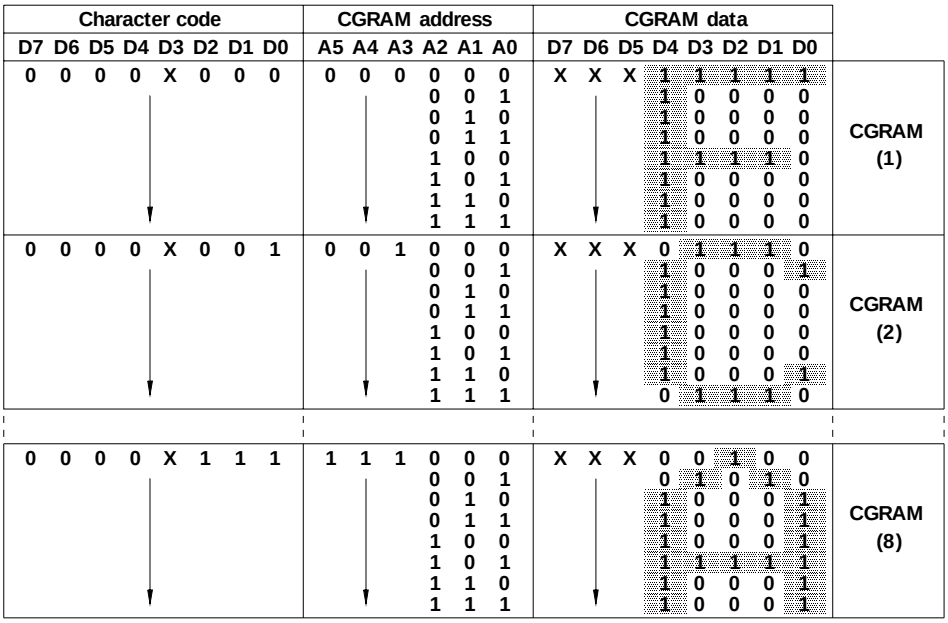
	1	2	3	4	5	6	7	8	9					32	33	34	35	36	37	38	39	40
1	01	02	03	04	05	06	07	08	09	-	-	-	-	20	21	22	23	24	25	26	27	00
2	41	42	43	44	45	46	47	48	49	-	-	-	-	60	61	62	63	64	65	66	67	40

Relationship after a display shift to the right:

	1	2	3	4	5	6	7	8	9					32	33	34	35	36	37	38	39	40
1	27	00	01	02	03	04	05	06	07	-	-	-	-	1E	1F	20	21	22	23	24	25	26
2	67	40	41	42	43	44	45	46	47	-	-	-	-	5E	5F	60	61	62	63	64	65	66

6.4 CHARACTER GENERATOR RAM (CGRAM)

The CGRAM stores the pixel information (1 = pixel on, 0 = pixel off) for the eight user-definable 5x8 characters. Valid CGRAM addresses are 00H to 3FH. CGRAM not being used to define characters can be used as general purpose RAM (lower 5 bits only). Character codes 00H to 07H (or 08H to 0FH) are assigned to the user-definable characters (see section 5.0 Character Font Tables). The table below shows the relationship between the character codes, CGRAM addresses, and CGRAM data for each user-definable character.



x = don't care

6.5 INSTRUCTIONS

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear display	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	x
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	x	x
Function set	0	0	0	0	1	DL	N	x	BR1	BR0
CGRAM address set	0	0	0	1	CGRAM address					
DDRAM address set	0	0	1	DDRAM address						
Address counter read	0	1	BF=0	AC contents						
DDRAM or CGRAM write	1	0	Write data							
DDRAM or CGRAM read	1	1	Read data							

x = don’t care

6.5.1 CLEAR DISPLAY

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction clears the display (without affecting the contents of CGRAM) by performing the following:

1) Fills all DDRAM locations with character code 20H (character code for a space).
2) Sets the AC to DDRAM address 00H (i.e. sets cursor position to 00H).
3) Returns the display to the non-shifted position.
4) Sets the I/D bit to 1.

6.5.2 CURSOR HOME

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

x = don't care

This instruction returns the cursor to the home position (without affecting the contents of DDRAM or CGRAM) by performing the following:

1) Sets the AC to DDRAM address 00H (i.e. sets cursor position to 00H).
2) Returns the display to the non-shifted position.

6.5.3 ENTRY MODE SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

This instruction selects whether the AC (cursor position) increments or decrements after each DDRAM or CGRAM access and determines the direction the information on the display shifts after each DDRAM write. The instruction also enables or disables display shifts after each DDRAM write (information on the display does not shift after a DDRAM read or CGRAM access). DDRAM, CGRAM, and AC contents are not affected by this instruction.

I/D = 0: The AC decrements after each DDRAM or CGRAM access. If S = 1, the information on the display shifts to the right by one character position after each DDRAM write.

I/D = 1: The AC increments after each DDRAM or CGRAM access. If S = 1, the information on the display shifts to the left by one character position after each DDRAM write.

S = 0: The display shift function is disabled.

S = 1: The display shift function is enabled.

6.5.4 DISPLAY ON/OFF CONTROL

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

This instruction selects whether the display and cursor are on or off and selects whether or not the character at the current cursor position blinks. DDRAM, CGRAM, and AC contents are not affected by this instruction.

D = 0: The display is off (display blank).
D = 1: The display is on (contents of DDRAM displayed).

C = 0: The cursor is off.
C = 1: The cursor is on (8^{th} row of pixels).

B = 0: The blinking character function is disabled.
B = 1: The blinking character function is enabled (a character with all pixels on will alternate with the character displayed at the current cursor position at about a 1Hz rate with a 50% duty cycle).

6.5.5 CURSOR/DISPLAY SHIFT

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	x	x

x = don't care

This instruction increments or decrements the AC (cursor position) and shifts the information on the display one character position to the left or right without accessing DDRAM or CGRAM. DDRAM and CGRAM contents are not affected by this instruction. If the AC was addressing CGRAM prior to this instruction, the AC will be addressing DDRAM after this instruction. However, if the AC was addressing DDRAM prior to this instruction, the AC will still be addressing DDRAM after this instruction.

S/C	R/L	AC contents (cursor position)	Information on the display
0	0	Decrements by one	No change
0	1	Increments by one	No change
1	0	Decrements by one	Shifts one character position to the left
1	1	Increments by one	Shifts one character position to the right

6.5.6 FUNCTION SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	x	BR1	BR0

x = don't care

This instruction sets the width of the data bus for the parallel interface modes, the number of display lines, and the luminance level (brightness) of the VFD. It must be the first command sent after any reset. DDRAM, CGRAM, and AC contents are not affected by this instruction.

DL = 0: Sets the data bus width for the parallel interface modes to 4-bit (DB7-DB4).
DL = 1: Sets the data bus width for the parallel interface modes to 8-bit (DB7-DB0).

N = 0: Sets the number of display lines to 1 (this setting is not recommended for multiple line displays).
N = 1: Sets the number of display lines to 2 (this setting is not recommended for single line displays).

BR1,BR0 = 0,0: Sets the luminance level to 100%.
0,1: Sets the luminance level to 75%.
1,0: Sets the luminance level to 50%.
1,1: Sets the luminance level to 25%.

6.5.7 CGRAM ADDRESS SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	CGRAM address					

This instruction places the 6-bit CGRAM address specified by DB5-DB0 into the AC (cursor position). Subsequent data writes (reads) will be to (from) CGRAM. DDRAM and CGRAM contents are not affected by this instruction.

6.5.8 DDRAM ADDRESS SET

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	DDRAM address						

This instruction places the 7-bit DDRAM address specified by DB6-DB0 into the AC (cursor position). Subsequent data writes (reads) will be to (from) DDRAM. DDRAM and CGRAM contents are not affected by this instruction.

6.5.9 ADDRESS COUNTER READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF=0	AC contents						

This instruction reads the current 7-bit address from the AC on DB6-DB0 and the busy flag (BF) bit (always 0) on DB7. DDRAM, CGRAM, and AC contents are not affected by this instruction. Because the BF is always 0, the host never has to read the BF bit to determine if the modules are busy before sending data or instructions. Therefore, data and instructions can be sent to the modules continuously according to the E, WR/, and SCK cycle times specified in section 3.7 AC Timing Specifications. Due to this feature, the execution times for each instruction are not specified.

6.5.10 DDRAM OR CGRAM WRITE

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

This instruction writes the 8-bit data byte on DB7-DB0 into the DDRAM or CGRAM location addressed by the AC. The most recent DDRAM or CGRAM Address Set instruction determines whether the write is to DDRAM or CGRAM. This instruction also increments or decrements the AC and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction.

6.5.11 DDRAM OR CGRAM READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

This instruction reads the 8-bit data byte from the DDRAM or CGRAM location addressed by the AC on DB7-DB0. The most recent DDRAM or CGRAM Address Set instruction determines whether the read is from DDRAM or CGRAM. This instruction also increments or decrements the AC and shifts the display according to the I/D and S bits set by the Entry Mode Set instruction. Before sending this instruction, a DDRAM or CGRAM Address Set instruction should be executed to set the AC to the desired DDRAM or CGRAM address to be read.

6.6 RESET CONDITIONS

After either a power-up reset or an external reset, the modules initialize to the following conditions:

1) All DDRAM locations are set to 20H (character code for a space).
2) The AC is set to DDRAM address 00H (i.e. sets cursor position to 00H).
3) The relationship between DDRAM addresses and character positions on the VFD is set to the non-shifted position.
4) Entry Mode Set instruction bits:
   - I/D = 1: The AC increments after each DDRAM or CGRAM access.
   - S = 0: The display shift function is disabled.
5) Display On/Off Control instruction bits:
   - D = 0: The display is off (display blank).
   - C = 0: The cursor is off.
   - B = 0: The blinking character function is disabled.
6) Function Set instruction bits:
   - DL = 1: Sets the data bus width for the parallel interface modes to 8-bit (DB7-DB0).
   - N = 1(0): Number of display lines set to 2 for multiple line displays (number of display lines set to 1 for single line displays).
   - BR1,BR0 = 0,0: Sets the luminance level to 100%.

Note that the function set command must be the first instruction sent to the module after any reset.

6.6.1 INITIALIZATION

The modules can be initialized by using instructions if the modules are not reset according to the reset timing detailed in Section 3.7.1 (Reset Timing). After any reset, the function set command must be the first instruction sent to the module.

7.0 CONNECTOR INTERFACE

Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)	Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)
1	GND	GND	GND	2	V_{CC}	V_{CC}	V_{CC}
3	SI/SO	NC or RST/	NC or RST/	4	STB	RS	RS
5	NC	WR/	R/W	6	SCK	RD/	E
7	NC	DB0	DB0	8	NC	DB1	DB1
9	NC	DB2	DB2	10	NC	DB3	DB3
11	NC	DB4	DB4	12	NC	DB5	DB5
13	NC	DB6	DB6	14	NC	DB7	DB7
15*	NC	NC	NC	16*	NC	NC	NC

NC = No Connection
*If applicable.

7.1 CONNECTOR CONFIGURATION

Product Number	Connector (if applicable)	Configuration
NA16SD08AA/BA-#1#	Amp P/N 1-103747-5 or equivalent	1 x 15
NA162SD07AA/BA/CA/DA-#1#	Amp P/N 1-103747-4 or equivalent	1 x 14
*NA202MD15AA/BA-#1#	Berg P/N 67997-114 or equivalent	2 x 7
NA202SD16AA/BA/CA/DA-#1#	Berg P/N 67997-114 or equivalent	2 x 7
NA204SD02AB/BB-#1#	Amp P/N 1-103747-6 or equivalent	1 x 16
NA242SD04AA/BA-#1#	Berg P/N 67997-114 or equivalent	2 x 7
NA402SD10AB/BB-#1#	Berg P/N 67997-114 or equivalent	2 x 7

*Also has holes that accept a 1 x 16 connector, Amp P/N 1-103747-6 or equivalent.

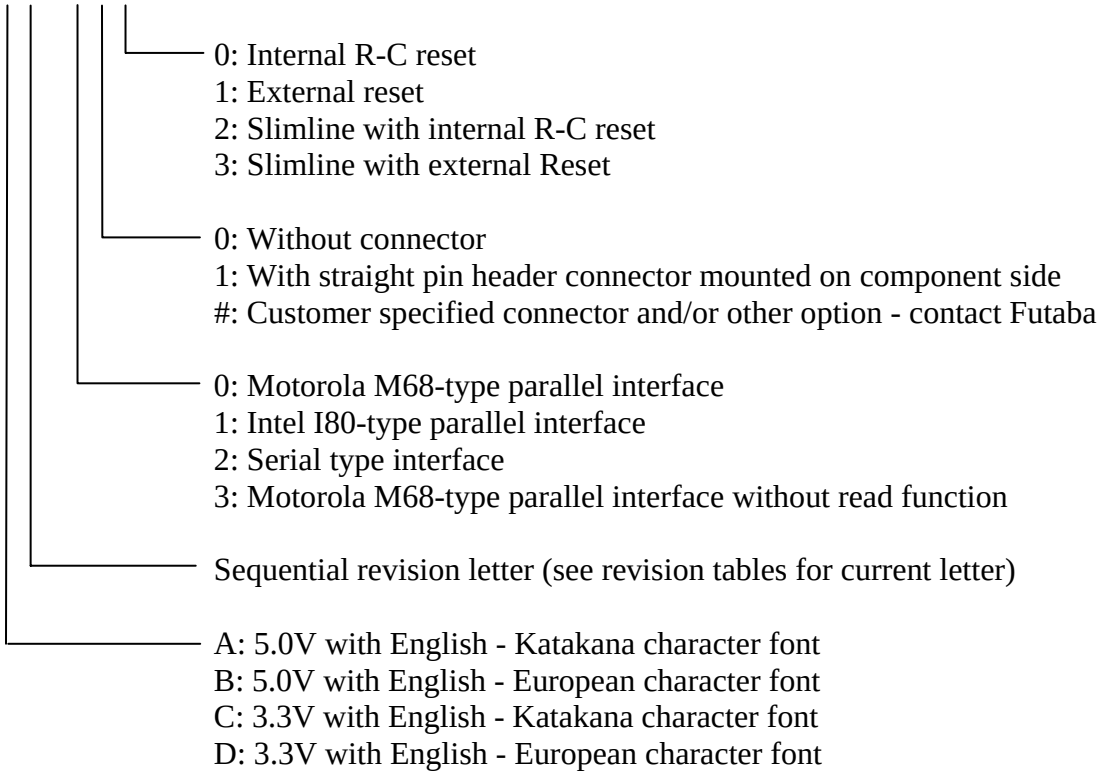
8.0 JUMPER SETTINGS

Mode	JP2	JP3	JP4	JP5	JP6	JP7
Parallel (Motorola) (Note 2)	(Note 1)	open	shorted	open	shorted	open
Parallel (Intel)	(Note 1)	open	shorted	open	open	shorted
Serial	open	shorted	open	shorted	shorted	open

Note 1: JP2 shorted (open) enables (disables) external reset mode.
Note 2: Read function not guaranteed on -3## part numbers.

9.0 PART NUMBER OPTIONS

NA202SD16AA - 0 0 0*



This example defines a 5.0V, 20 x 2 LCD Emulator display with English - Katakana character font, revision letter A, Motorola M68-type interface, no connector, without external reset.

*Default configuration is –000. Other options may be pre-configured by Futaba for large orders.