BRAC UNIVERSITY
CSE460
VLSI DESIGN
Assignment - 1

Name: **ID:** **Section:**

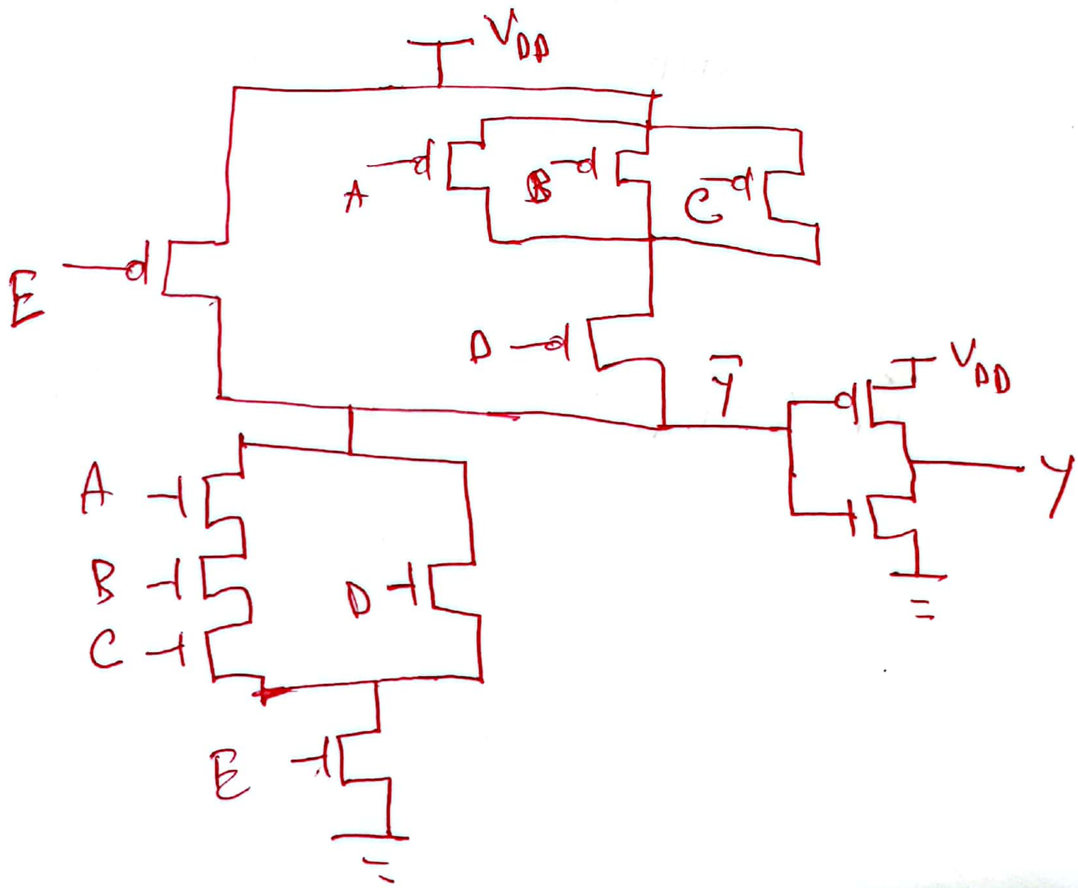
Question 1:[10 Marks]

Design a CMOS implementation of the following functions:

(a) Y = ((A . B . C) + D) . E

(b) Y = (A + (B . C)) . (D + E)

(a)



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Question 1:[10 Marks]

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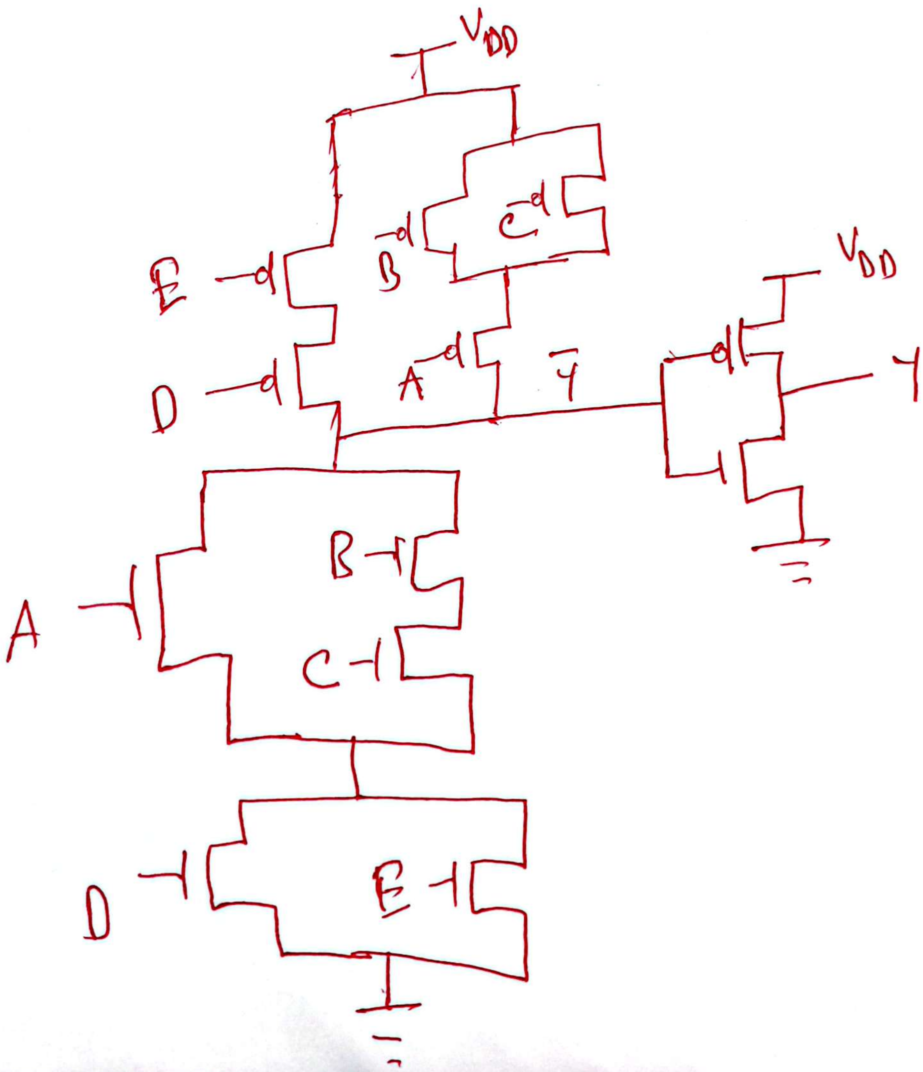
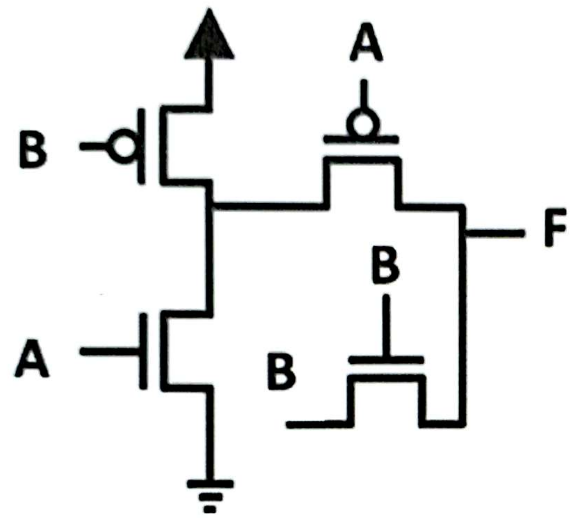


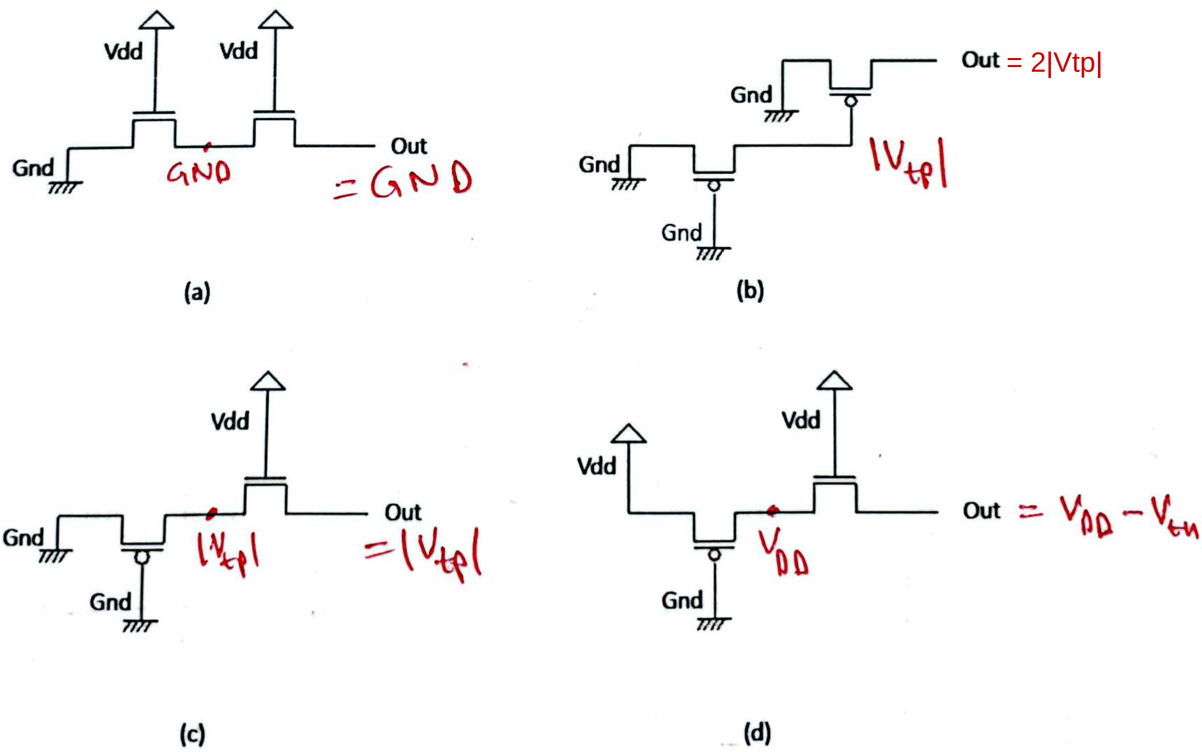
Question 2:[10 Marks]

Complete the truth table from the given circuit. Floating state or Z is also a possible answer.



A	B	F
0	0	1
0	1	1
1	0	Z
1	1	1

Question 3:[10 Marks]



Find the value of Out for each of the above pass transistor circuits.

Question 4:[20 Marks]

Consider you need to design a temperature control system for your classroom at BRAC University. Your system has 1 Output **D**, and 3 inputs **A**, **B**, and **C** that come directly from three different sensors installed in the room. When a certain threshold of the temperature is crossed, each sensor gives a logical **HIGH** output. Your logic circuit should turn on the AC (**D = 1**) when the **majority** of inputs are **HIGH**.

(a) Convert the problem statement into a Truth Table and write the simplified Boolean expression.
(b) Implement the logic with a CMOS implementation.
(c) How many transistors are required in the CMOS implementation?
(d) Can you implement the logic with only NAND gates? If so, show the implementation.

(a)

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$D = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + ABC + A\bar{B}C + ABC + AB\bar{C} + ABC$$

$$= (\bar{A} + A)BC + AC(\bar{B} + B) + AB(\bar{C} + C)$$

$$= BC + AC + AB$$

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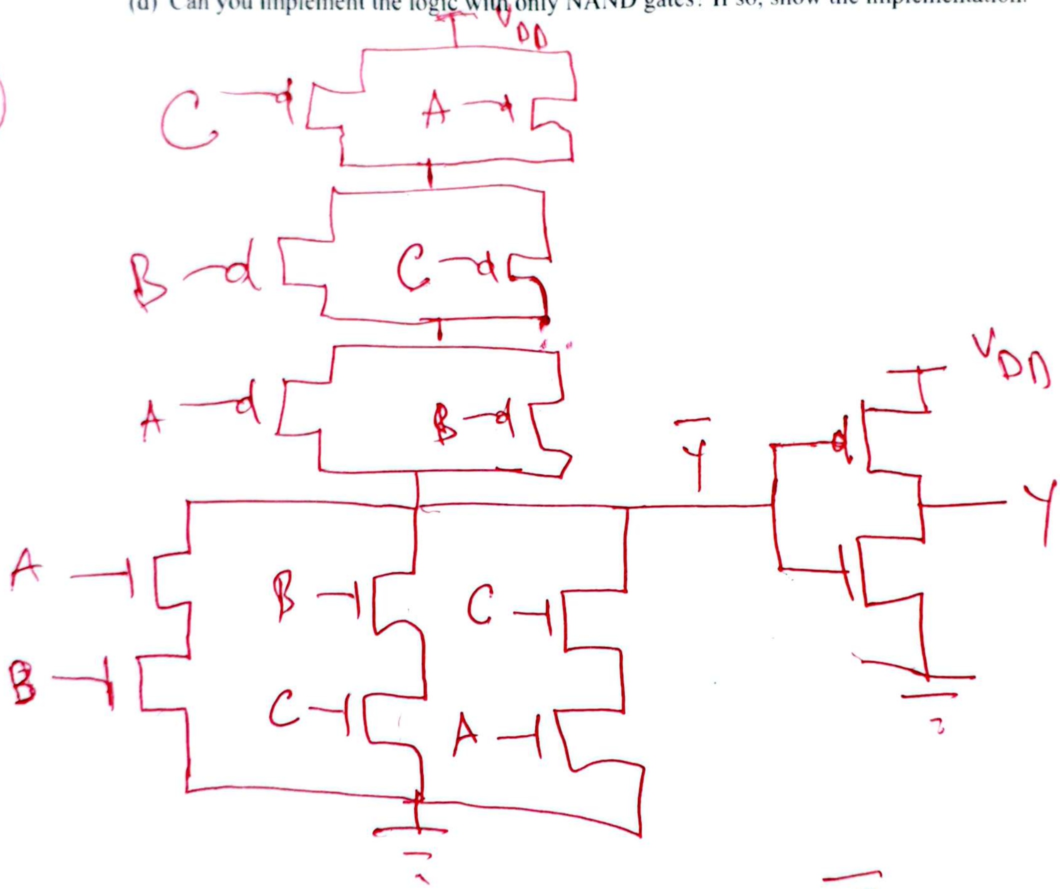
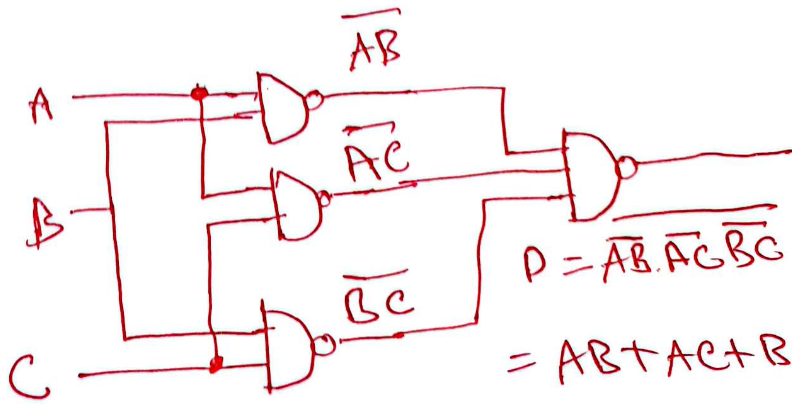
(b)



(c) 14

(d) Yes you can.



$D = \overline{\overline{AB}.\overline{AC}\,\overline{BC}}$

$= AB+AC+BC$

Question 5:[10 Marks]

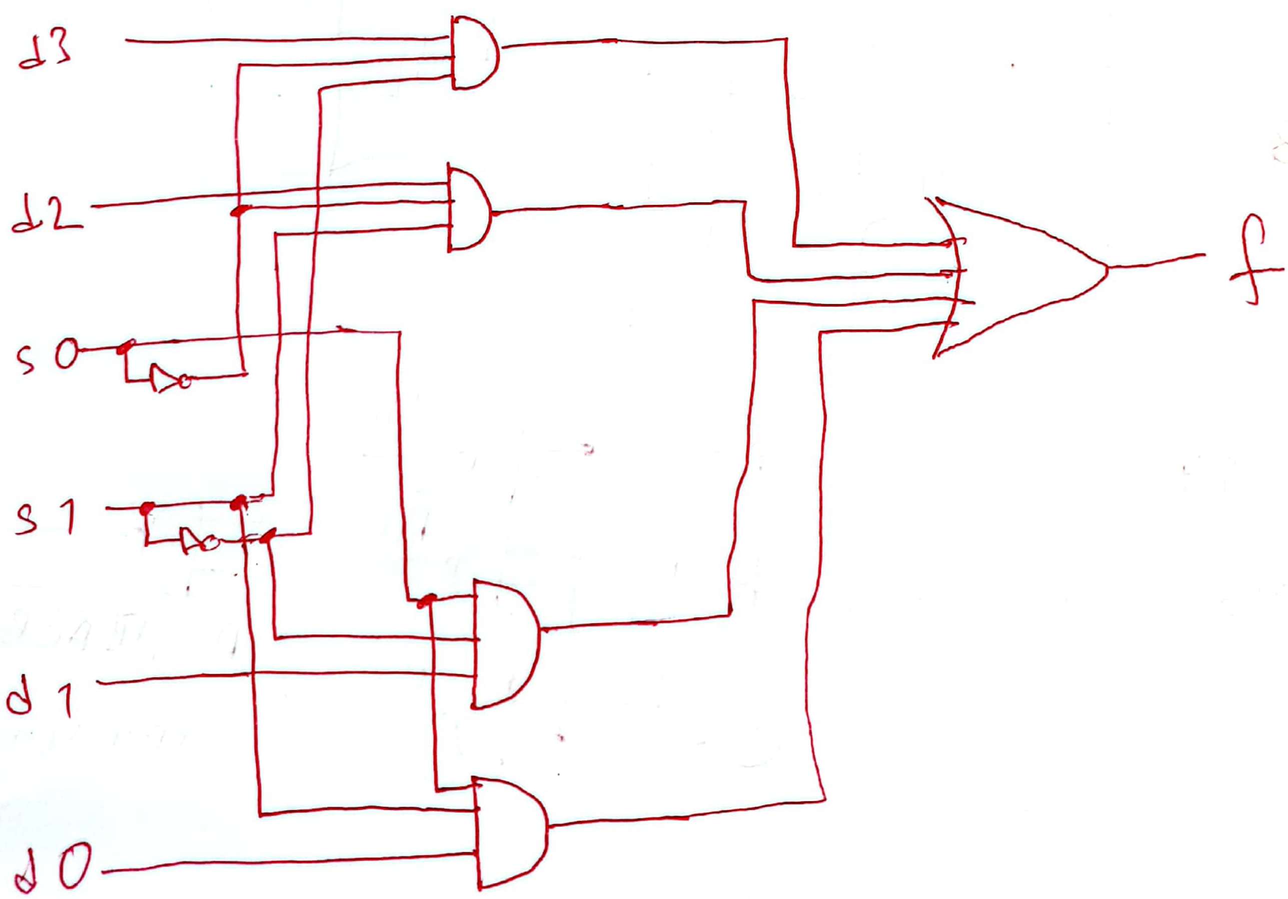
Imagine a logic circuit with 1 output f, and 4 input lines *d3, d2, d1, and d0*.

- Let's define a 2-bit selector input S = *s1 s0*
- The output **f** is determined as follows:

S	f
00	*d3*
01	*d2*
10	*d1*
11	*d0*

(a) Write the Boolean expression for this logic and implement the circuit using basic gates.
(b) Implement this logic using a 2-to-1 multiplexer.

(a) $f = \overline{s0}\,\overline{s1}\,d3 + \overline{s0}\,s1\,d2 + s0\,\overline{s1}\,d1 + s0\,s1\,d0$



Question 5:[10 Marks]

Imagine a logic circuit with 1 output **f**, and 4 input lines ***d3, d2, d1, and d0***.

- Let's define a 2-bit selector input **S** = ***s1 s0***
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S	f
00	*d3*
01	*d2*
10	*d1*
11	*d0*

(a) Write the Boolean expression for this logic and implement the circuit using basic gates.
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(b)