BRAC University
Department of Computer Science and Engineering

Semester: **Summer 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Midterm Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **3rd September, 2023**

Set B

Student ID:	Name:	Section:

[Answer **both questions 1 and 2**. You can answer any **one** question from **questions 3 and 4**.]

[Each question carries equal marks.]

[After the exam, *the question paper should be turned in along with the answer script.*]

1. (CO3)

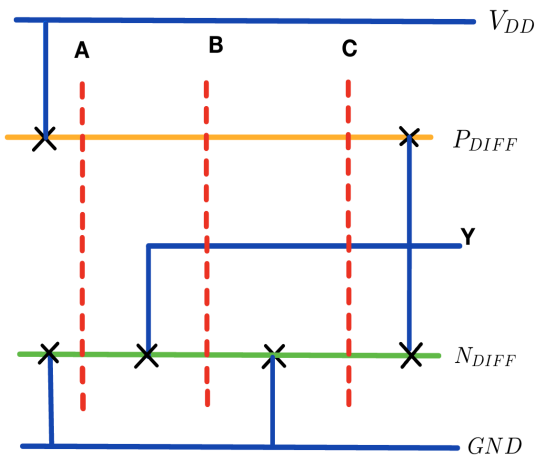
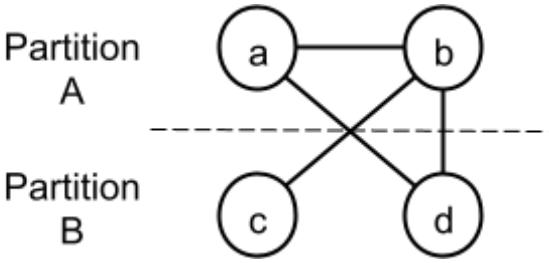
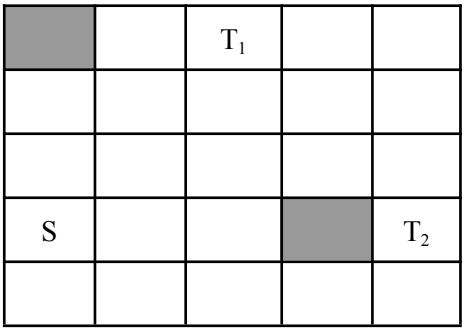


Figure 1: Circuit Diagram for Q.1(a) and (b)

Table-1. Truth table for Q.1(c)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(a)	**Illustrate** the CMOS logic represented by the stick diagram from Figure 1.	**5**
(b)	**Draw** the cross-sectional view of Figure 1 along the P_{DIFF} region.	**3**
(c)	**Draw** the stick diagram for the logic described in the truth table. **Estimate** the area in lambda (λ).	**5+2**

2. (CO4)	(a)	The graph below (nodes a-d) can be optimally partitioned using the Kernighan-Lin algorithm. The dotted line represents the initial partitioning. Assume all the edges have the same weight.  	
		i. **Calculate** the initial cut cost.	**1**
		ii. **Identify** how many iterations are needed in a single pass.	**1**
		iii. **Perform** the first pass of the algorithm and **determine** the new cut cost of the optimum output of the first pass. [Hint: For the "i"th iteration of the first pass, until all the nodes are swapped and fixed, do the following: ● Compute the node costs of all unfixed nodes ● Find the maximum gain of swapping a pair of nodes (Δg_i) ● Swap the pair and draw the updated graph ● Calculate cumulative gain, G_i]	**7**
		iv. Should you perform subsequent passes of the algorithm? Why or why not?	**1**
	(b)	Lee's Maze algorithm can be used to find the shortest path between two nodes avoiding obstacles. Dark regions are obstacles or components.  	
		Find the shortest path from source, S to both the targets, T_1 and T_2. Rule of thumb should be taken into consideration.	**5**

3. (CO1)

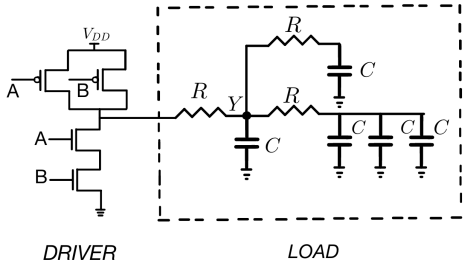


Figure 2: Circuit Diagram for Q.3

(a)	**Find** the individual transistor widths k_{nMOS} and k_{pMOS} for the <u>*Driver*</u> to achieve the worst-case effective rise and fall resistance equal to that of a unit inverter, R.	**2**
(b)	**Draw** the simplified RC circuit for Figure 2.	**6**
(c)	i) **Derive** the expressions for t_{pdr} and t_{pdf} for node **Y**. ii) **Calculate** t_{pdr} and t_{pdf} in s (second) from the simplified RC expression from (i) when R= 2 kΩ and C= 1 pF.	**5+2**

4. (CO1) Consider the circuit diagram in Figure 3, which is being driven by a system frequency of **0.1 GHz** and a supply voltage of **3 V**. The inputs to the circuit are $\mathbf{in_A}$ and $\mathbf{in_B}$, while the output node is **Y**. $\mathbf{n_1}$ and $\mathbf{n_2}$ are two intermediate nodes. The input and output capacitances of the individual circuit blocks are listed in **Table-2**. The timing diagram of input, output and intermediate nodes are provided in Figure 4 for **32 nanoseconds**.

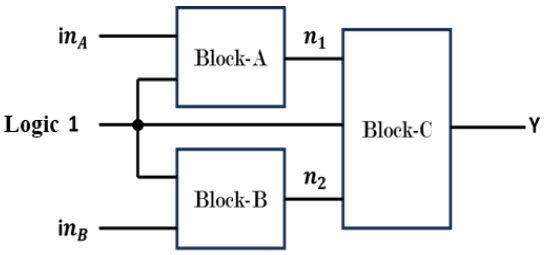


Figure 3: Circuit Diagram for Q.4(b)

Table-2. Capacitance values for Q.4(b)

Block	Input Capacitance	Output Capacitance
Block-A	6 pF	6 pF
Block-B	5 pF	8 pF
Block-C	13 pF	9 pF

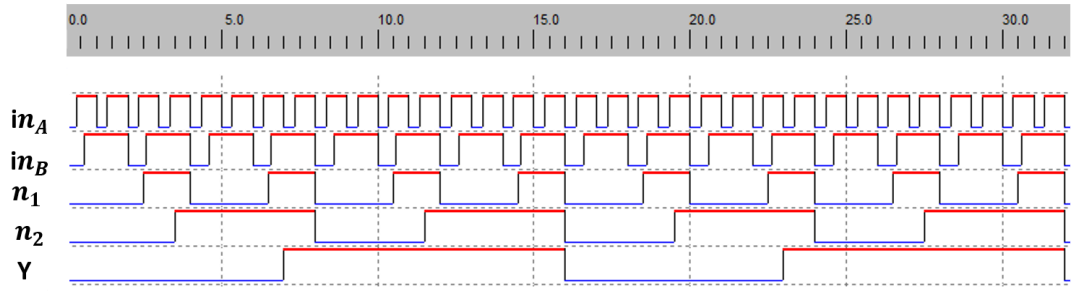


Figure 4: Timing Diagram for Q.4(a) (the timescale is in nanoseconds)

(a)	**Determine** the activity factors at nodes: $\mathbf{in_A}$, $\mathbf{in_B}$, $\mathbf{n_1}$, $\mathbf{n_2}$ and **Y.**	**5**
(b)	**Calculate** the total capacitances at nodes: $\mathbf{in_A}$, $\mathbf{in_B}$, $\mathbf{n_1}$, $\mathbf{n_2}$ and **Y.**	**5**
(c)	**Compute** the total switching power consumption of the circuit assuming no power is being consumed at the **Logic 1** node.	**5**