BRAC University

Semester: Spring 2020
Course No: CSE 460
Course Title: VLSI Design
Sections: 12, 13
Faculty: Tanvir Ahmed (TAA)

Midterm Exam
Full Marks: 60
Time: 1 hour 40 minutes
Date: 5th March, 2020

[Question number 1 is compulsory, answer any 2 from the rest.]

1. You are given the task of designing the control circuitry of a CD/DVD Drive using finite state machines. The drive has one push button w, a high signal which causes the tray to open if it was already closed, or causes the tray close if it was already opened. The task is to generate an output signal z. which determines if the drive should be opened (z = 1) or closed (z = 0) with the following instructions:

- If the tray is closed, pushing the button (setting w = 1) should immediately generate the signal (z = 1) to open the tray
- If the tray has been open for less than 3 clock cycles, pushing the button (setting w = 1) should immediately generate the signal (z = 0) to close the tray
- The tray should automatically close after being open for 3 clock cycles

Answer the following: [3+10+7+10]

(a) What should be the frequency of the clock if the tray cannot stay open for more than 5 seconds?

(b) Draw the state diagram for the machine

(c) Derive a state assigned table from (b)

(d) Implement your FSM using D flip-flops

2. (a) Estimate the area of a standard cell implementing the function $F = \overline{(A + B).(C + D)}$ for a 32nm process.

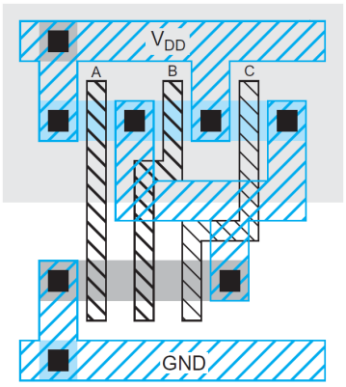
(b) Design a negative edge triggered flip flop using transmission gates.

[10+5]

3. (a) What is body tapping? Why is it necessary?

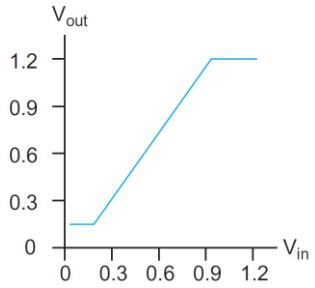
(b) Briefly discuss the following terms: (i) Photo lithography (ii) Ion implantation

(b) For a self-aligned process, draw the set of masks for the following layout:

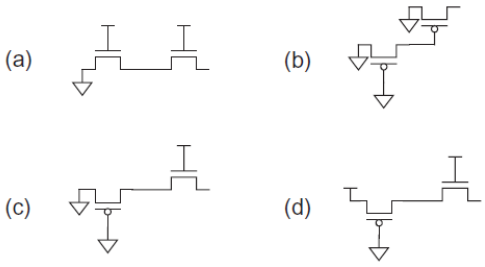


[4+4+7]

4. (a) A buffer circuit has the transfer characteristics shown below. What are the values of V_{IL}, V_{IH}, V_{OL}, and V_{OH} that give best noise margins? What are these high and low noise margins?



(b) Give an expression for the output voltage for the pass transistor networks shown below. Neglect the body effect. The symbols have their usual meanings.



(c) Sketch a 2-input NOR with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R) in the worst case scenario. Also sketch the RC equivalent circuit.

[4+6+5]