CSE460 Midterm Fall 2020

Slot: 1
Full Marks: 40
Time: 1 hour 50 minutes (1 hour 35 mins for exam, 15 mins for pdf preparation & google form submission)
Your Name, ID, Section, Date, Signature should be written at the starting of your script.
Faculty helpline: meet.google.com/hfb-dama-vpg

Answer any 4 questions

1. Design the truth table of an 8 to 3 priority encoder with the following priority: 4>0>1>2>3>7>6>5. Explain the logic behind your answer. **[10]**
2. Design a tristate buffer using CMOS technology with restoring properties. Explain why/why not transmission gates can be used for this particular design. **[10]**
3. Design a CMOS compound gate that implements the following function: Y=A(B+C)D, where A, B, C, D are the inputs and Y is the output. Clearly mark your networks. **[10]**

4.

Present State	Next State		Output
	w = 0	w = 1	
y2 y1	Y2 Y1	Y2 Y1	z
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

5. An FSM is defined by the state table above. **[10]**
   - Prepare a state assigned table using binary encoding
   - Derive the next state and output expressions
   - Derive the final circuit that realizes this FSM using D flip-flops
6. Suppose you are building an electron microscope, for which you need to design the control circuit of the electron gun first. You can activate the electron gun (z=1) by pressing a button (w=1). The electron gun should stay ON (z=1) for exactly 3 cycles, then turn OFF (z=0). Once the gun is activated, pressing the button (w) would not do anything unless the gun has completed its full 3 cycle of staying ON. Opt for moore model for this particular problem. **[10]**
   - Draw the state diagram (Clearly mark transitions and Reset)
   - Derive a state assigned table
   - Derive the next state and output expressions
   - Derive the circuit that realizes this FSM using D flip-flops (Bonus question)

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Slot: 2
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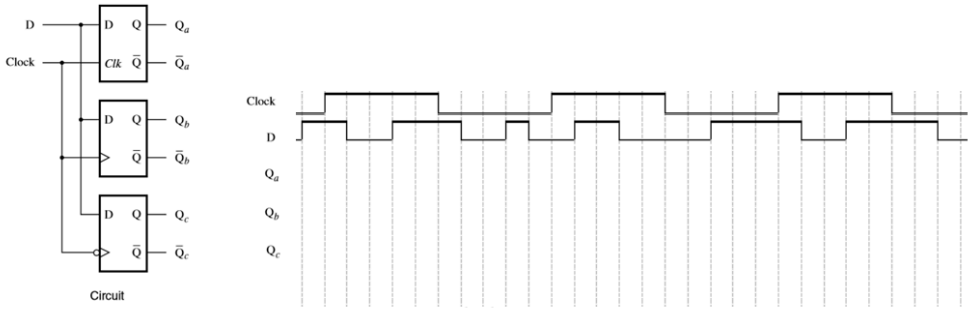
Answer any 4 questions

1. For the following figure, complete the waveforms Qa, Qb and Qc. Explain your reasoning behind your answer. **[10]**



2. Design a 2x1 non-inverting MUX using CMOS technology that has restoring capabilities. Using your previous design, derive a 4x1 MUX. **[10]**
3. Design a CMOS compound gate that implements the following function: Y=AB+CD+EF, where A, B, C, D, E are the inputs and Y is the output. Clearly mark your networks. **[10]**

4.

Present State	Next State		Output
	w = 0	w = 1	
y2 y1	Y2 Y1	Y2 Y1	z
A	C	D	0
B	B	A	0
C	D	A	0
D	C	B	1

5. An FSM is defined by the state table above. **[10]**

a) Prepare a state assigned table using binary encoding

b) Derive the next state and output expressions

c) Derive the final circuit that realizes this FSM using D flip-flops

5. Design a 3-bit FSM binary counter that counts in the following sequence: 7>6>5>7>6>5... **[10]**

- It has so start its count from 7
- It should have a 1-bit input **w**, a clock signal, a reset and a multi-bit output **z**
- The machine should increase its count whenever **w = 1,** and hold its previous count otherwise
- It should output the binary value of its current count, in binary

a) Draw the state diagram (Clearly mark transitions & Reset)

b) Derive a state assigned table

c) Derive the next state and output expressions

d) Realize the FSM using D flip-flops (Bonus question)