*BRAC UNIVERSITY*
*CSE460*
*VLSI DESIGN*
*Quiz - 3*
*Time: 30 minutes*
*Set-A*

---

***Name:*** ***ID:*** ***Section:***

---

## Question 1: [20 Marks]

Suppose you are working with a 180 nm technology with a clock frequency of 1 GHz and a supply of 0.7 V. The chip you are designing has 2 billion transistors, of which 500 million remain active at any given time. The gate and diffusion capacitances are 1.2 fF/μm and 0.5 fF/μm, respectively, for all transistors. The gate width is 2λ. You also obtain the following power consumption data **for a single transistor**:

- Short circuit power = 5 nW
- Gate leakage power = 1 nW
- Junction leakage power = 2 nW
- Subthreshold power = 3 nW

The acceptable total power consumption **for a single transistor** is 45 nW.

(a) Find the activity factor. [2]
(b) Calculate the switching power consumption **of the chip**. [6]
(c) Calculate the dynamic, static, and total power consumption **for a single transistor**. [6]
(d) Is the total power consumption within the acceptable range? If not, find the maximum activity factor to keep the total power within the acceptable range. Assume every other quantity has the same value. [6]