BRAC University	
Semester: Summer 2020 Course No: **CSE 460** Course Title: **VLSI Design** Sections: 11, 12, 13 Faculty: Tanvir Ahmed (TAA)	**Midterm Exam (Slot 1, 2, 3)** Full Marks: 50 Time: **2 hour** Date: 21st Aug, 2020, held on **buX**

[Question number 5 is compulsory, answer any 3 from the rest.]

SLOT 1

1. Explain the conduction complement rule with a suitable example. **[10]**

2. Explain the operation of a CMOS negative-edge-triggered D flip flop using a suitable timing diagram. Show the intermediate variables. **[10]**

3. Design a 4-1 MUX using CMOS transmission gates and sketch the transistor-level diagram of your design. The data inputs are D0, D1, D2, D3 and the selector pins are S0, S1. Assume you have both the complemented (S0', S1') and original (S0, S1) version of the selector pins available. **[10]**

4. Design a CMOS tri-state buffer and draw its transistor level diagram. Does this design follow the conduction complement rule? **[8+2]**

5. (Mandatory) Design an FSM that has an input w and an output z. The machine has to generate z = 1 when the previous three values (including the present value) of w were **101 or 111**; otherwise, z = 0. Overlapping input patterns are allowed. An example of the desired behavior is:
0**101 111**0 0110 0**111 11**00 (w)
000**1** 0**11**0 0000 000**1 11**00 (z)

(the input and output are given in 4 bit blocks for clarity, both the input w and the output z are continuous)

(a) Derive the state diagram **[8]**
(b) Derive a state assigned table **[4]**
(c) Derive a circuit realization of the FSM using D Flip-flops. **[8]**

SLOT 2

1. A 3:2 priority encoder is defined by the following set of equations: Y0 = A0' . (A1 + A2'), Y1 = A0' . A1' where A0, A1, A2 are inputs and Y0, Y1 are outputs. You may assume you have both true and complementary versions (A0', A1', A2') of the inputs available. Sketch the transistor-level CMOS diagram that implements these logic functions. **[10]**

2. Design a D latch using CMOS and explain its behavior using a suitable timing diagram. **[10]**

3. Design a 4-1 MUX using tri-state buffers and sketch the transistor-level CMOS diagram. **[10]**

4. Briefly explain different ways to encode the states in a sequential circuit along with their advantages and disadvantages. **[10]**

5. (Mandatory) Sowmitra Das is a crazy mathematician, who is absolutely obsessed with prime numbers. Everything about him needs to be related to prime numbers. In this problem, you are tasked to design a 3-bit FSM prime number counter for Mr. Das. The counter starts with the initial prime value 010, as it is the first 3-bit prime number and counts through the other 3-bit prime numbers. Other specifications are:

- It should have a 1-bit input **w**, a clock signal, a reset and a multi-bit output **z**
- The machine should increase its count whenever **w = 1,** and hold its previous count otherwise

(Hint: The 3-bit prime numbers are: 2, 3, 5, 7 and your counting sequence should be 2>3>5>7>2>3>5>7>...)

(a) Derive the state diagram for this counter **[7]**
(b) Derive a state assigned table **[5]**
(c) Derive a circuit realization of the FSM using D Flip-flops. **[8]**

SLOT 3

1. Sketch a transistor-level schematic for a compound CMOS logic gate that implements the following function: Y = (A + B + C) . (D + E + F) **[10]**

2. Sketch a gate-level schematic for a 4-1 MUX and determine the total number of transistors being used in that circuit for CMOS technology. The logic expression for a 4-1 MUX is given by: Y = w0'w1'D0 + w0w1'D1 + w0'w1D2 + w0w1D3. The data inputs are D0, D1, D2, D3 and the selector pins are w0, w1. Assume you have both the complemented (w0', w1') and original (w0, w1) version of the selector pins available. **[10]**

3. Explain the operation of pass transistors and transmission gates as switches. **[10]**

4. Write down the differences between edge-triggered and level-triggered elements with suitable examples. **[10]**

5. (Mandatory) Alice and Bob are really great friends. For their next experiment, Alice would like to send a really high energy light signal to Bob, who just lives a few blocks away from Alice. For this purpose, Alice wants you to help her make an automated light controlling machine. The machine has the following specs:

- It should have a input switch w, a clock, a reset and a output z
- Once Alice presses the input switch i.e. w=1, the machine should switch on the light i.e. generate z=1
- Since Bob is really busy with other parts of the project, the light needs to stay turned "on" (z=1) for exactly 3 consecutive clock cycles (irrespective of the input switch w) for Bob to notice
- After 3 consecutive clock cycles, the light should automatically turn off (z=0) because Alice does not want to waste energy
- Since Alice does not care about storage, she wants the states of her machine to be one-hot-encoded.

(a) Derive the state diagram for Alice's machine **[8]**
(b) Derive a state assigned table (states should be one-hot-encoded) **[4]**
(c) Derive a circuit realization of the FSM using D Flip-flops. **[8]**