BRAC University
Department of Computer Science and Engineering

Semester: **Spring 23**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 40 minutes**
Date: **May 02, 2023**

Set A

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO3) A digital system is driven by a clock frequency of **1 MHz** and a supply voltage of **10 V**. A small part of the system can be modeled by a CMOS inverter driving a capacitive load ($\mathbf{C_L}$), the figure of which is given below. When the input node **Vin** is low, the output node **Vout** is high, and to make the output node high *once*, **10 nJ** of energy is supplied by the voltage source, $\mathbf{V_{DD}}$. [A joule (J) is the SI unit of energy. Assume the threshold voltages to be $\mathbf{V_{tn} = |V_{tp}| = 0.1*V_{DD}}$]

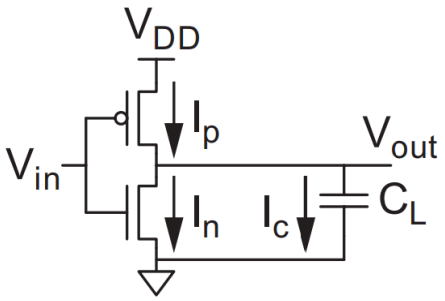
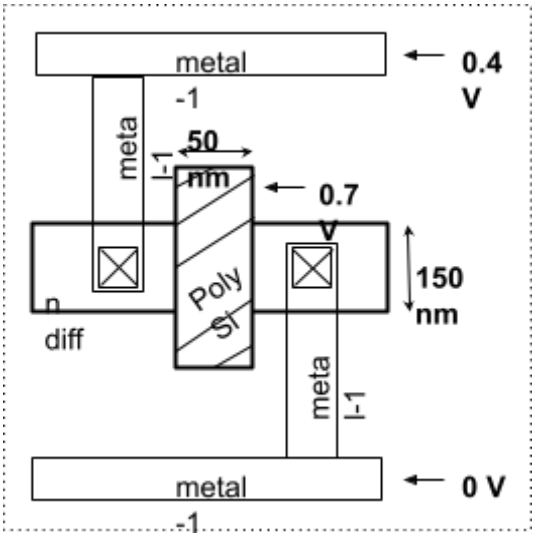
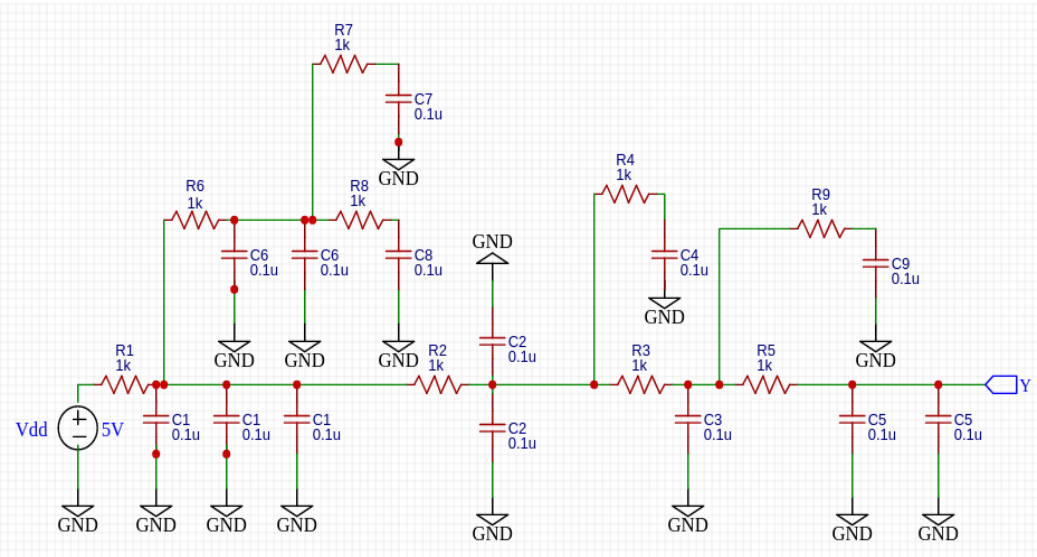
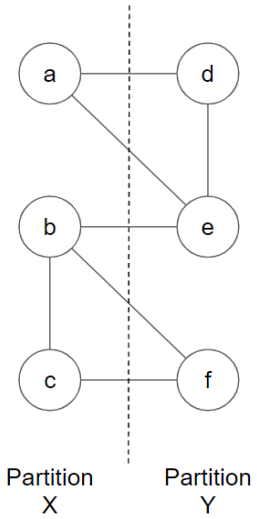


Figure 1: An inverter driving a capacitive load

(a)	Assuming that **Vin** stays low, how much of the energy supplied by the voltage source ($\mathbf{V_{DD}}$) is stored in the load capacitor $\mathbf{C_L}$?	**3**
(b)	What is the capacitance of the load capacitor $\mathbf{C_L}$?	**3**
(c)	If the activity factor of the output node is **0.2**, calculate the average switching power dissipation of the CMOS inverter.	**3**
(d)	If the beta ratio of the CMOS inverter is **5**, *neatly* sketch its DC response and clearly mark $\mathbf{V_{IL}}$, $\mathbf{V_{IH}}$, $\mathbf{V_{OL}}$ & $\mathbf{V_{OH}}$ on the response.	**4**
(e)	For the above CMOS inverter, are the two noise margins equal? If not, comment on which one is bigger.	**2**

2. (CO3)	Consider the layout (top view) of a MOSFET in the following figure. The gate oxide thickness is 100 nm. Estimate the mobility of electrons to be $620\ cm^2/V.s$ and the threshold voltage is 0.35 V. $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}\ F/cm$. 		
	(a)	Evaluate C_{ox} and β.	**4**
	(b)	Find the operating region of the transistor and the current (I_{ds}) through it.	**6**
	(c)	What will be the value of current if drain voltage is doubled keeping the other voltages as they are?	**5**
3. (CO3)	 Figure3: A RC network		
	(a)	Draw the simplified RC network for Figure 3.	**2**
	(b)	i) Determine the expression for the elmore delay, $\mathbf{t_{pd}}$ for node Y. ii) Calculate $\mathbf{t_{pd}}$ in s (second) from the simplified RC expression from (i)	**4+2**
	(c)	Sketch the transistor level diagram of a **CMOS NOR-4** gate and the resulting stick diagram. Estimate the area of the gate in terms of lambda.	**2+3 +2**

4. (CO4, CO5)	The graph below (nodes a-f) can be optimally partitioned using the Kernighan-Lin algorithm. The dotted line represents the initial partitioning. Assume all the edges have the same weight.  		
	(a)	What is the initial cut cost?	**1**
	(b)	Perform the first pass of the algorithm. For the "i"th iteration of the first pass, until all the nodes are swapped and fixed, do the following: i. Compute the node costs of all unfixed nodes ii. Find the maximum gain of swapping a pair of nodes (Δg_i) iii. Swap the pair and draw the updated graph	**9**
	(c)	Finish the first pass by computing the maximum positive gain, G_m. Suggest how many swaps should be actually executed in the first pass.	**4**
	(d)	Should you perform subsequent passes of the algorithm? Why or why not?	**1**