BRAC University

Department of Computer Science and Engineering

Semester: **Spring 2022**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 40 minutes**
Date: **13th May 2022**

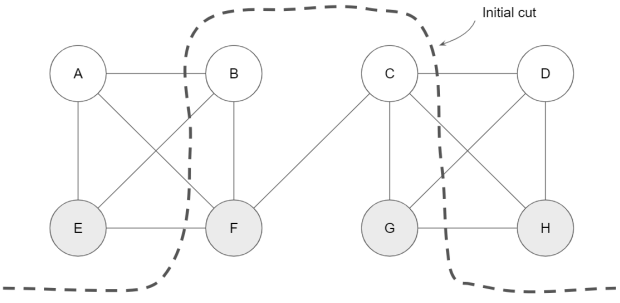
Student ID:	Name:	Section:

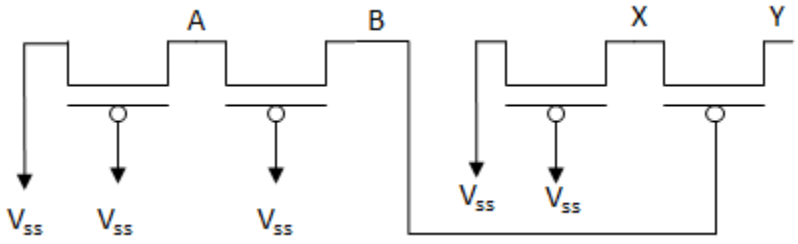
[Answer any **THREE** questions out of **FOUR**.]

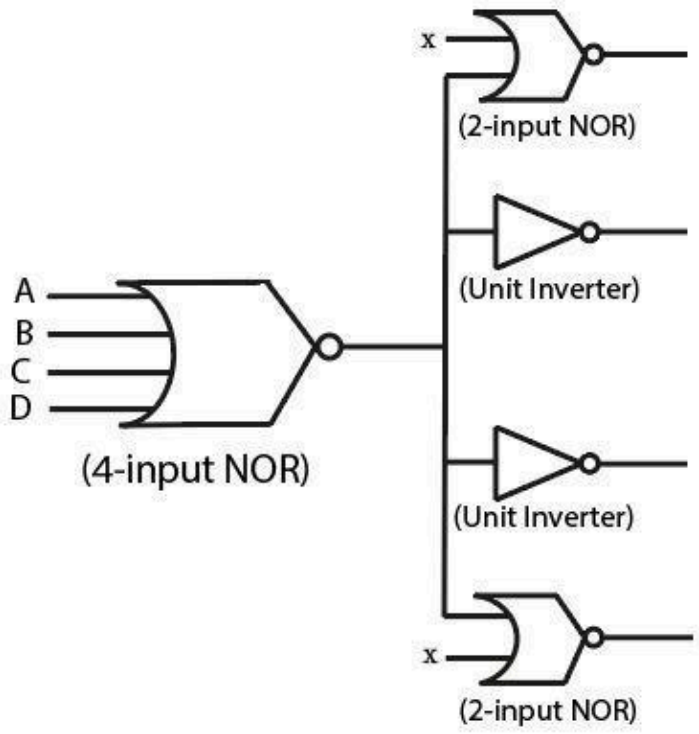
[Numbers on the right margin indicate full marks.]

[After the exam, the question paper should be turned in along with the answer script.]

[Make reasonable assumptions for any missing value.]

1. (CO4, CO5)	For a certain chip planning task, you are given three blocks with the following widths and heights: Block A: $w_A = 1$, $h_A = 4$ or $w_A = 4$, $h_A = 1$ or $w_A = 2$, $h_A = 2$ Block B: $w_B = 1$, $h_B = 2$ or $w_B = 2$, $h_B = 1$ Block C: $w_C = 1$, $h_C = 3$ or $w_C = 3$, $h_C = 1$		
	(a)	**Define** chip planning. **Find** and **draw** a floorplan with the *minimum* total area enclosed by its global bounding box.	6
	An initial cut for a partition of 8 circuit elements (A, B, C, D, E, F, G, and H) is given below: 		
	(b)	**Calculate** the *initial* cut cost, and the cost of moving each node.	6
	(c)	By inspection (without using an algorithm or any calculation), propose a better cut for the circuit.	3

2. (CO3)	**(a)**	From the perspective of the charging and discharging of a capacitor, explain the energy dissipation in the CMOS inverter circuit.	5
	A digital system-on-a-chip in a 1V 65 nm process (with 50 nm drawn channel lengths and λ=25 nm) has 2.1 billion transistors, of which 100 million are used for building logic gates and the rest are used in memory arrays. The average logic transistor width is 14 λ and the average memory transistor width is 6 λ. The memory arrays are divided into banks and only the necessary bank is activated, so the memory activity factor is 0.03. The static CMOS logic gates have an average activity factor of 0.15. Assume each transistor contributes 1.01 fF/μm of gate capacitance and 0.84 fF/ μm of diffusion capacitance. Neglect the wire capacitance.		
	(b)	i) What are the capacitance values of total logic gates and memory arrays?	6
	(b)	ii) What is the switching power when the operating frequency is 1 GHz?	4
3. (CO3)	Consider a CMOS inverter in a 65 nm 2 V process, where the channel lengths of pMOS & nMOS are equal but the pMOS has three times the width than that of the nMOS. Assume the ratio of electron mobility to hole mobility to be 2, and the threshold voltages to be $\|V_{tp}\| = V_{tn} = 0.3$ V.		
	(a)	Evaluate the beta ratio of the inverter.	3
	(b)	Find the inverter threshold voltage.	3
	(c)	Plot I_{ds} vs. V_{ds} for the nMOS if $V_{gs} = 0.5$ V. Evaluate $V_{ds(sat)}$ and show it in the plot.	5
			
	(d)	If Vss = 0.001 V, Find the voltage of X & Y.	4

4. (CO3)	A 4-input NOR gate is driving two 2-input NOR gates and two unit inverters at its output as shown in the circuit diagram below:  		
	(a)	Assuming all diffusion nodes are contacted, draw the CMOS diagram of the circuit along with the corresponding width parameter specifications of the transistors required to achieve equal rise and fall resistances of that of a unit inverter.	4
	(b)	Draw the RC equivalent circuit. (You don't need to draw the full RC circuits of the loads, only show the capacitances offered by the individual loads at the output of the driver)	3
	(c)	Derive the expressions for the worst-case falling propagation delay (t_{pdf}).	4
	(d)	Derive the expressions for the best-case rising contamination delay (t_{cdr}).	4