BRAC University
Department of Computer Science and Engineering

Semester: **Spring 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **8th May 2023**

Set A

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1.CO3

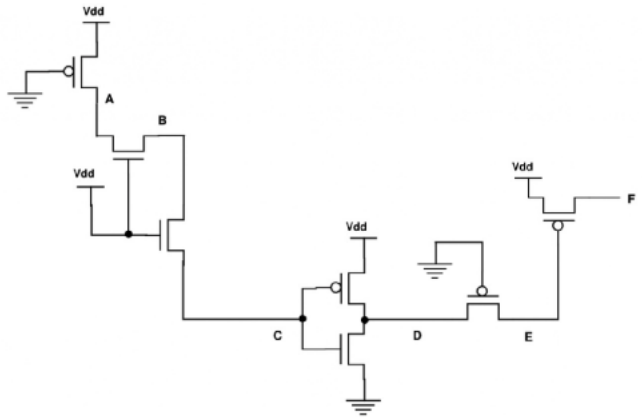


Figure 1

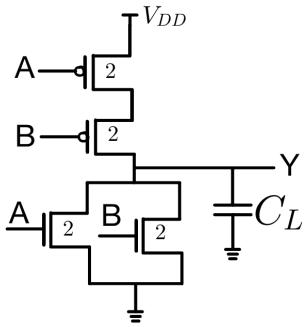


Figure 2

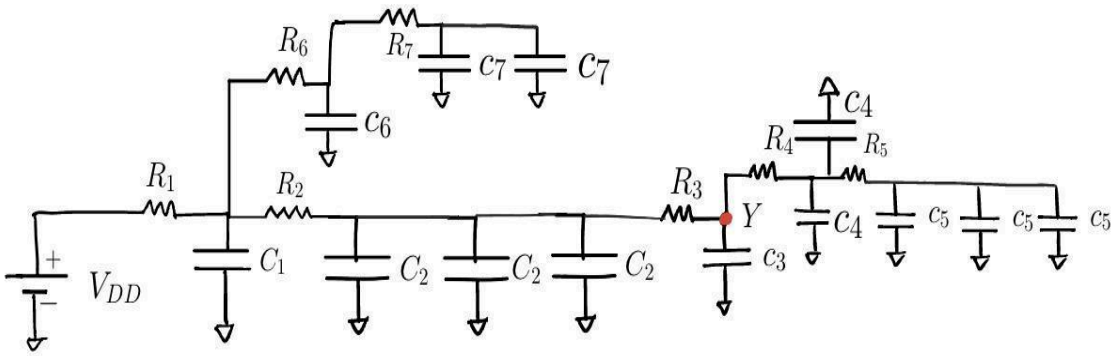
Given, V_{DD} = 5 V, GND= 0 V, V_{tn} = 0.5 V and $|V_{tp}|$= 1.5 V.

(a)	**Calculate** voltages at each of the nodes, A, B, C, D, E, F from figure 1	[6]

A digital system-on-chip has the above gate from **figure 2** implemented on it. Individual transistor widths $k_{nMOS} = 2$ and $k_{pMOS} = 2$ were chosen to achieve the effective rise and fall resistance equal to that of a unit inverter, R for the given gate. The system has $\mathbf{V_{DD}}$**=1V**, activity factor, **α= 0.2**, unit transistor's width, **W = 6 µm**, load capacitor, $\mathbf{C_L}$ **= 2 pF** and parasitic diffusion capacitance for both PMOS and NMOS transistors are **0.5 fF/µm**. Here, 1G = 10^9, 1p = 10^{-12}, 1f = 10^{-15}.

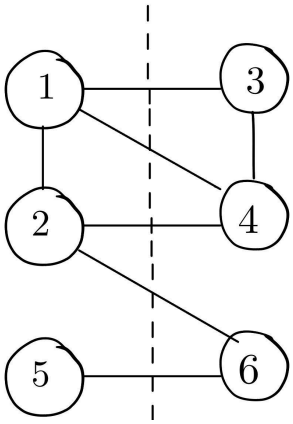
(b)	**(i) Calculate** the total capacitance at node **Y**.	[4]
	(ii) Estimate the Switching power when operating in **1.4 GHz.**	[3]
	(iii) Determine if the system can switch *faster* or *slower*, when $\mathbf{V_{DD}}$ is *halved* while the switching power and the capacitance remain *same* [as (ii)].	[2]

2.CO3



(a)	Draw the simplified RC network for the given figure.	[2]
(b)	i) **Determine** the expression for the Elmore delay, $\mathbf{t_{pd}}$, for node Y. ii) **Calculate** $\mathbf{t_{pd}}$ in s (second) from the simplified RC expression from (i), $R = 1\ k\Omega$ and $C = 1\ fF$. iii) Comment if the delay is propagation rising or falling delay from the circuit.	[4+3 +1]
(c)	Sketch the initial and simplified RC circuit of a CMOS -NAND2 gate, driving h=5 identical CMOS NOR-2 gates(initial: all capacitors should be considered; simplified: only total capacitance at each node should be shown)	[5]

3.CO4 ,CO5 The graph below (nodes 1-6) can be optimally partitioned using the Kernighan-Lin algorithm. The dotted line represents the initial partitioning. Assume all the edges have the same weight.



(a)	**Find** the initial cut cost?	[2]
(b)	Perform the first pass of the algorithm. For the "i"th iteration of the first pass, until all the nodes are swapped and fixed, do the following: i. Compute the node costs of all unfixed nodes ii. Find the maximum gain of swapping a pair of nodes (Δg_i) iii. Swap the pair and draw the updated graph	[3+6 +2]
(c)	Finish the first pass by computing the maximum positive gain, G_m.	[2]

4.CO3	Consider a CMOS inverter in a 45 nm 1 V process, where the pMOS transistor has **3** times the **width** of the nMOS transistor. The ratio of electron mobility to hole mobility is **3:2**, and the threshold voltages are $\mathbf{|V_{tp}| = V_{tn} = 0.2\ V.}$ Assume all other parameters are the same for both of the transistors.		
	(a)	**Calculate** the beta ratio (r) of the inverter.	[3]
	(b)	**Determine** the inverter threshold voltage (V_{inv}).	[3]
	(c)	**Draw** an approximate transfer characteristic curve (V_{out} vs V_{in}) for the inverter.	[3]
	(d)	**Plot** the I_{ds} vs. V_{ds} curve for the nMOS using the following values of V_{ds}. Given, V_{gs} = 0.4 V, and β_n = 120 μA/V^2. **Evaluate** $V_{ds(sat)}$ and show the value of $V_{ds(sat)}$ in the plot.	[6]

V_{ds}	0.10 V	0.15 V	0.20 V	0.25 V