BRAC University
Department of Computer Science and Engineering

Semester: **Summer 2022**
Course Code: **CSE460**
Course Title: **VLSI Design**

Midterm Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **9th September 2022**

Set A

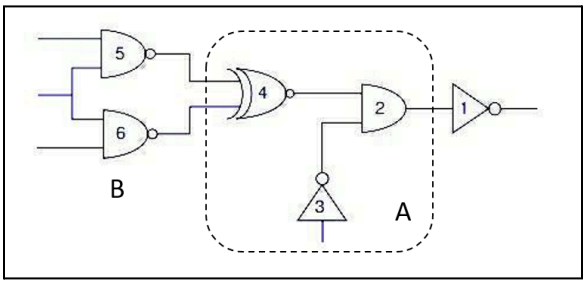
Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO4, CO5)

Mr. Xin Chao is a VLSI engineer in a renowned chip manufacturing company. He sets the physical positions of all the components on a chip to optimize the delay and power consumption. Suppose, Mr. Xin is working on a chip that consists of 6 nodes illustrated in the figure below. Firstly, he partitions the nodes into two equal-sized blocks, and then, using the Kernighan-Lin algorithm, he minimizes the number of connections between the blocks. After floor-planning, placement, and maintaining all other design considerations, Mr. Xin can dispatch the chip to the fabrication unit.



The dotted line in the figure represents the initial partitioning with **A (2,3,4)** & **B (1,5,6)** blocks. For the *first* iteration, answer the following:

(a)	**Draw** the corresponding graph representation of the above circuit.	**2**
(b)	**Find** the initial cut cost.	**2**
(c)	**Calculate** the cost of each node.	**3**
(d)	**Evaluate** necessary gains (Δg) for the first iteration.	**4**
(e)	**Perform** the first swap and **compare** the new cut cost with the initial one.	**4**

2. (CO3) Consider a CMOS inverter in a 45 nm 1 V process, where the pMOS transistor has **3** times the **width** of the nMOS transistor. The ratio of electron mobility to hole mobility is **3:2**, and the threshold voltages are $\mathbf{|V_{tp}| = V_{tn} = 0.2\ V.}$ Assume all other parameters are the same for both of the transistors.

(a)	**Calculate** the beta ratio (r) of the inverter.	**3**
(b)	**Determine** the inverter threshold voltage (V_{inv}).	**3**
(c)	**Draw** an approximate transfer characteristic curve (V_{out} vs V_{in}) for the inverter.	**3**
(d)	**Plot** the I_{ds} vs. V_{ds} curve for the nMOS using the following values of V_{ds}. Given, V_{gs} = 0.4 V, and β_n = 120 μA/V^2. **Evaluate** $V_{ds(sat)}$ and show the value of $V_{ds(sat)}$ in the plot. **[6]**	**6**

V_{ds}	0.10 V	0.15 V	0.20 V	0.25 V

3. (CO3) A CMOS compound gate, **Y=** $\overline{A + B + C}$ is driving h identical CMOS compound gates with same function in a $1\ \mu m$ process

(a)	**Identify** and **design** the CMOS circuit (indicate both nMOS and pMOS networks).	**2**
(b)	**Determine** the individual transistor widths k_{nMOS} and k_{pMOS} to achieve the effective rise and fall resistance equal to that of a unit inverter, R, in the worst case.	**2**
(c)	**Sketch** the simplified RC circuit.	**5**
(d)	**Derive** the expressions for t_{pdf} and t_{cdf}. (Sketch the *corresponding* RC network from part (c) to derive the expressions.)	**6**

4. (CO3, CO4)

(a) Consider the following logic circuit, which is being driven by a system frequency of **1 GHz** and a supply voltage of **3.2 V**. The inputs to the circuit are **A**, **B**, **C**, and **D**, while the output node is **Y**. $\mathbf{N_1}$ and $\mathbf{N_2}$ are two intermediate nodes. The activity factors of nodes $\mathbf{N_1}$, $\mathbf{N_2}$, and **Y** with respect to the system frequency are given in table 1. The input and output capacitances of the individual logic gates are listed in table 2.

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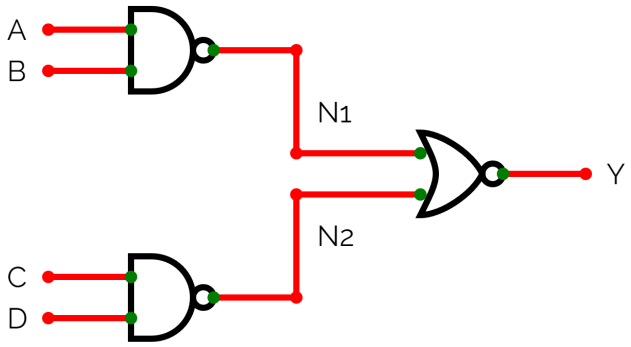

Figure: Logic circuit for problem 4 (a) (i), 4 (a) (ii)

Table 1

Node	Activity factor
N_1	$\frac{3}{4}$
N_2	$\frac{3}{4}$
Y	$\frac{1}{16}$

Table 2

Gate	Input capacitance	Output capacitance
NAND-2	4 pF	6 pF
NOR-2	5 pF	6 pF

- 1 GHz = 10^9 Hz
- 1 pF = 10^{-12} F

(i)	**Find** out the total capacitances at nodes N_1, N_2, and Y.	**3**
(ii)	**Compute** the total switching power of the logic circuit, assuming no power is being consumed at nodes A, B, C, and D.	**8**
(b)	**Prove** that an nMOS transistor cannot properly pass a high voltage signal (corresponding to a logical 1).	**4**