BRAC University
Department of Computer Science and Engineering

Semester: **Fall 2022**
Course Code: **CSE460**
Course Title: **VLSI Design**

Midterm Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **11th November 2022**

Set B

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO2)	**(a)**	**Design** a CMOS compound gate that implements the following function: Y = (A.B + C.D) . E	**6**
	(b)	Imagine a *gate*-level logic circuit with 1 output **f**, and 4 inputs ***x1***, ***x0***, ***y1***, and ***y0***. ● Let X = ***x1 x0*** be a two-digit binary number, where the four possible values of X are 00, 01, 10, and 11, which represent the four decimal numbers 0, 1, 2, and 3 respectively. ● Let Y = ***y1 y0*** be another number with the same four possible values. ● The output **f** should be **1** if the sum of numbers represented by X and Y is ***less*** than decimal **3**. Otherwise, the output **f** should be **0**.	
		i) **Create** a truth table for all 16 combinations of the 4 inputs.	**3**
		ii) **Derive** the boolean expression of the output using k-map.	**4**
		iii) **Implement** the function **f** with logic gates.	**2**

2. (CO2)	**Given** is a pattern for a sequence detector.		

CLK	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	t_{18}
w	**1**	**1**	**1**	0	1	0	**1**	**1**	**0**	**0**	1	0	1	**0**	**0**	**0**	1	0
z	0	**1**	**1**	0	0	0	0	**1**	0	**1**	0	0	0	0	**1**	**1**	0	0

	(a) Identify the sequence and the type of FSM for the above input-output combinations. [Hint: The above table contains two sequences]	**1+ 1**
	(b) Design the state diagram, state table, ***gray encoded*** state assigned table. **[Overlapping allowed].**	**3+ 2+ 2**
	(c) Determine the logic expressions of the next state and output variables using K-map.	**6**
3. (CO2)	**(a) Complete** the truth table shown in Figure 2 for the circuit shown in Figure 1	**5**

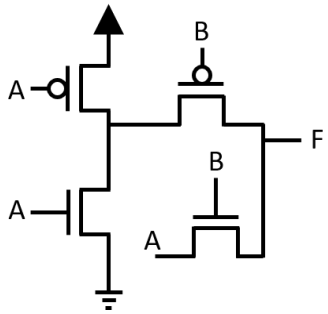

Figure 1: A Logic Circuit

A	B	F
0	0	
0	1	
1	0	
1	1	

Figure 2: Truth Table

(b) A D flip-flop is made by cascading two D latches as shown in Figure 3. Data input (**D**) and clock (**CLK**) for the circuit are shown in Figure 4. **Draw** the waveforms for $\mathbf{Q_M}$ and **Q**. (Use a pencil to draw the signals and draw on the question paper, no need to draw the diagram in your answer script separately.) **9**

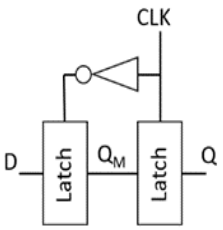

Figure 3

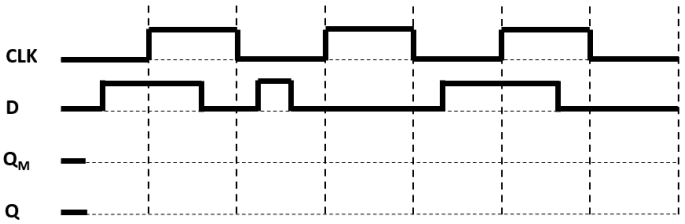

Figure 4

(c) **Identify** the type of the flip-flop shown in Figure 3. **1**

4. (CO1) Observe figure 5 and answer the following questions.

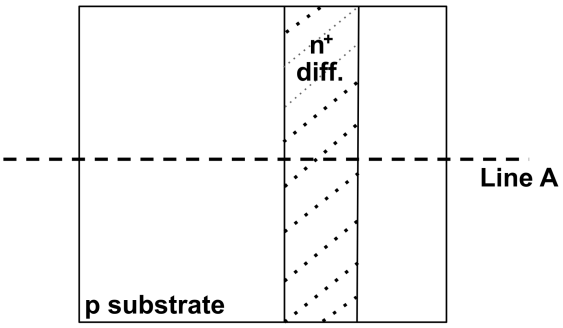

Figure 5: Top view of a wafer after fabricating an n+ diffusion region (dotted region)

(a) **Draw** the cross-sectional view of the above figure along 'Line A' and **label** the different regions. **3**

(b) Briefly **describe** and **illustrate** the necessary steps to fabricate the n+ diffusion region on a blank wafer as shown in the figure. **12**