BRAC University

Department of Computer Science and Engineering

Midterm Exam

Semester: **Spring 2024**
Course Code: **CSE460**
Course Title: **VLSI Design**

Full Marks: **15 x 3 = 45**
Time: **1 hour 15 mins**
Date: **8^{th} Mar 2024**

Set B

Student ID:	Name:	Section:

[**Question 4** is **mandatory.** You may answer any **TWO** questions out of the remaining **THREE** along with **Question 4**. In total, you need to answer **THREE** questions out of **FOUR**.]

1. (CO1)

i. Complete the truth table in **Figure 1b** for the circuit shown in **Figure 1a**

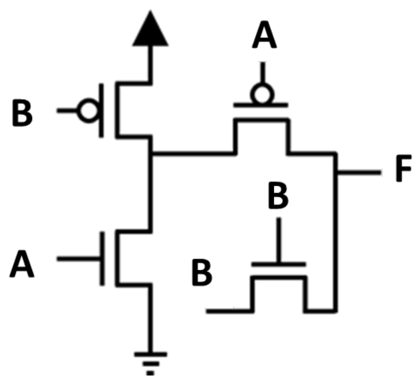


Figure 1a

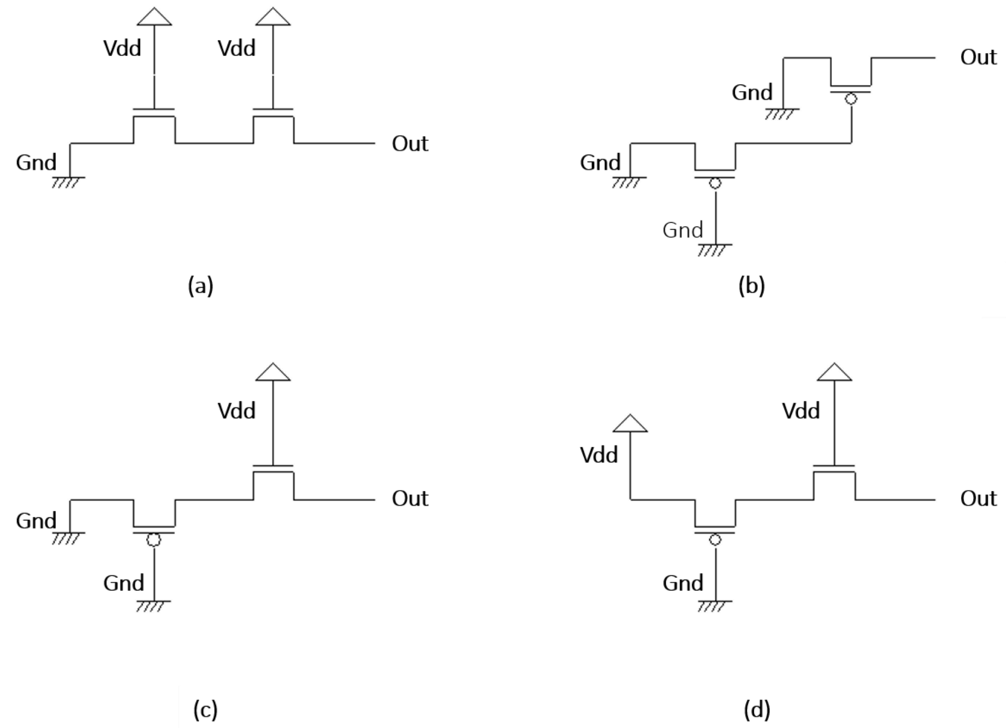
A	B	F
0	0	
0	1	
1	0	
1	1	

Figure 1b

(a)	Complete the truth table in **Figure 1b** for the circuit shown in **Figure 1a**.	4
(b)	**Explain** your reasoning for the output **F** when **A = 1**, **B = 0**.	2

ii. For a **0.8-µm** process technology, **tox = 15 nm, µ = 275 cm^2/V.s, εox = (3.9)(8.85 × 10^{-14}) F/cm and Vt = - 0.7 V.**

(a)	Judging from the value of **Vt** and **µ**, **comment** on whether the MOSFET is NMOS or PMOS.	2
(b)	**Calculate** Cox.	2
(c)	For a MOSFET with aspect ratio **W/L = 20, calculate** the values of **β**, **Vsg** and **Vsd(min)** needed to operate the transistor in the saturation region with a dc current of **Id = 0.1 mA**.	5

2. (CO1)	**(a)**	Design a CMOS compound gate that implements the following function: **$Y = A \cdot ((B \cdot C \cdot D) + E)$**	**7**
	(b)		
		Determine the value of **Out** in all above conditions considering **Vdd = 3V**, **Vtp = -0.4V**, **Vtn = 0.5V** and **Gnd = 0V**	**8**
3. (CO1)	Consider you need to design a temperature control system for your classroom at BRAC University. Your system has 1 Output **D**, 3 inputs **A**, **B** and **C** that come directly from three different sensors installed at the room. When a certain threshold of the temperature is crossed, each sensor gives a logical **LOW** output. Your logic circuit should turn on the AC (**D = 1**) when the **majority** of inputs are **LOW**. **[You can assume that you have the inputs available both in uncomplemented and complemented form]**		
	(a)	**Write** the truth table for the system.	**5**
	(b)	**Determine** the boolean logic function of the system using K-MAP and **design** the circuit. How many MOSFETs do you require to implement your design? Can you **design** the circuit using **NAND** gates only? **Show** how.	**4+2 +2+ 2**

4. (CO2)

Fig 2a shows that three 4-bit registers (**R1**, **R2**, and **R3**) are connected to a data bus. If the 'in' pins are high, the respective registers store the value from the data bus in the corresponding registers. Similarly, if the 'out' pins are high, the registers make the stored value available in the data bus. **R2** has an additional functionality of left shifting. If the **L_shift** pin is **high**, **R2 left** shifts its content by **1 bit**. A control unit (**Fig 2b**) controls the registers and it generates the outputs sequentially as listed in **Table I**. The control unit completes the operation irrespective of the value of **w** once it's triggered by **w = 1** initially.

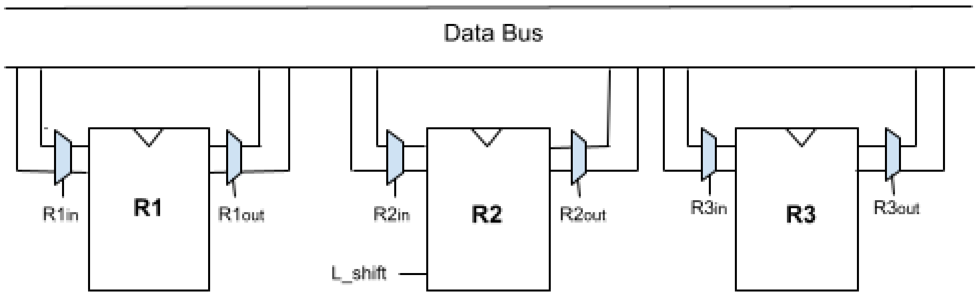


Fig 2a: Register arrangement

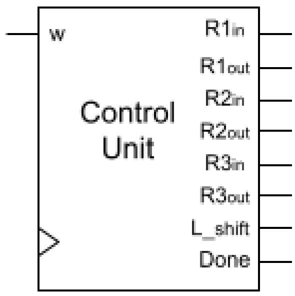


Fig 2b: Control Unit

Clock cycle	R1in	R1out	R2in	R2out	R3in	R3out	L_shift	Done
t1	0	0	1	0	0	1	0	0
t2	0	0	0	0	0	0	1	0
t3	1	0	0	1	0	0	0	1

Table I: Output values

(a) Assume the initial stored values of the registers as follows:
R1 = 0101, **R2 = 0011**, **R3 = 0010**.

What are the stored values of the registers after each clock cycle and briefly describe what's happening? **6**

(b) Design the internal circuit of the 'Control Unit'. You can use any type of state diagram and state assignment scheme to derive the circuit. **9**