BRAC University
Department of Computer Science and Engineering

Semester: **Summer 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Midterm Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **16th July 2023**

Set B

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO1) Observe the I-V characteristics of an nMOS transistor as shown in Figure 1 and answer the following questions:

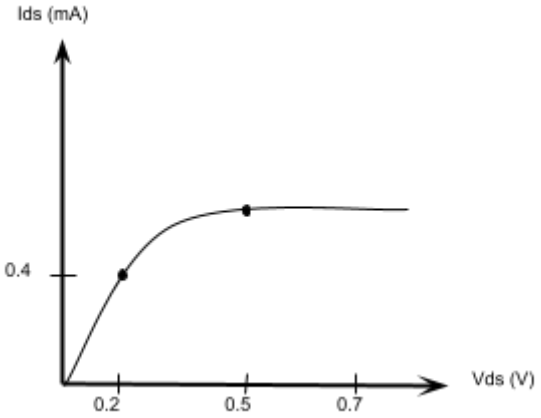


Figure 1: I-V characteristics of an nMOS transistor

Consider threshold voltage, electron mobility, gate oxide thickness and permittivity to be 0.2 V, 450 cm^2/V.s, 1 nm and $3.9 \times 8.85 \times 10^{-14}\ F/cm$ respectively. The drain to source current ***increases*** until V_{ds} = 0.5 V.

(a)	**Evaluate** V_{gs}.	**3**
(b)	**Calculate** the aspect ratio (W/L) of the mosfet.	**7**
(c)	**Find** the current when V_{ds} = 0.7 V. Comment on the current through the device if the drain-source voltage is further increased.	**4+1**

2. (CO1) **(a)** "Y" is a circuit element that produces output **Qy** from input **Dy** with a clock signal, **CLKy**, as shown in Figure 2:

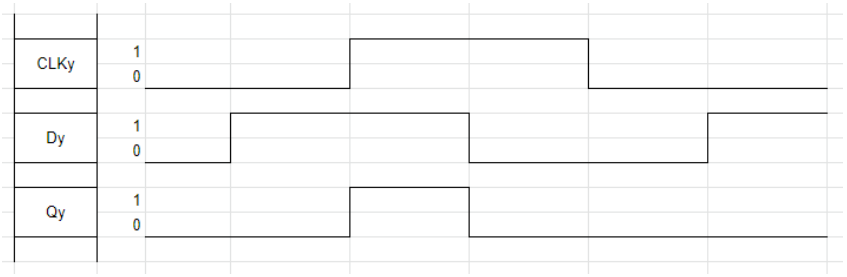


Figure 2: Timing Diagram for circuit element "Y"

Draw the circuit diagram of "Y" using transmission gates.	**4**

(b) Consider the Tri-state circuit shown in Figure with inputs: **A**, **B**, **En** and output: **Out**. The Tri-state circuit further consists of two sub-circuits: Circuit-1 and Circuit-2.

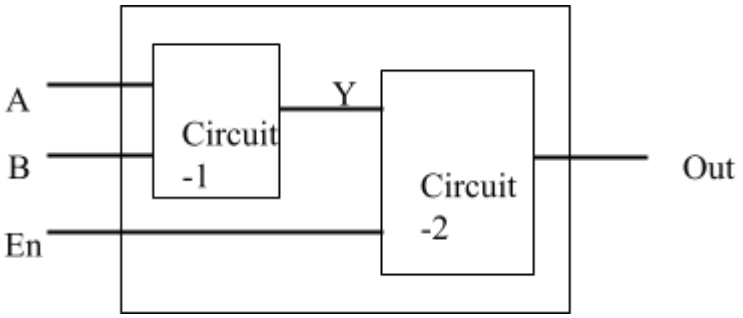


Figure 3: Tri-state circuit

The truth tables for both Circuit-1 and Circuit-2 are given below:

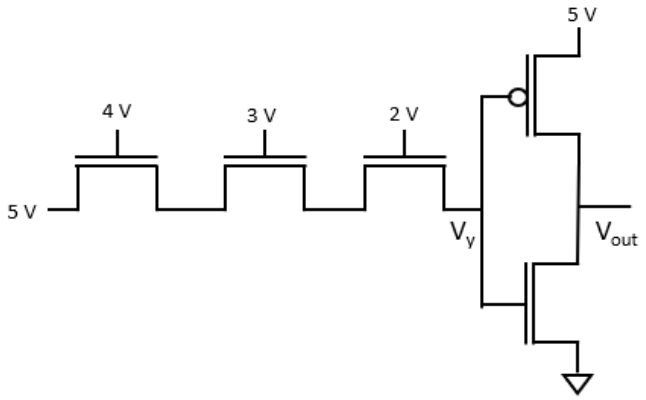
The truth table for Circuit-1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

The truth table for Circuit-2

En	Out
0	z
1	$\overline{Y}$

i. **Determine** the boolean expression of ***Y.***	**2**
ii. **Draw** the CMOS circuit diagram for Circuit-1.	**5**

		iii. **Draw** the circuit diagram for Circuit-2.	**4**
3. (CO1)		 Figure 4: Circuit Diagram for Q.3 For the circuit diagram in Figure 4, the NMOS and PMOS were fabricated in a process where $\mu_n C_{ox}$=120 μA/V^2, $\mu_p C_{ox}$=60μA/V^2, V_{tn}=-V_{tp}=1 V .	
	(a)	**Find** the value of the voltage marked at V_y.	**3**
	(b)	**Determine** V_{inv} for the inverter if the NMOS and PMOS have the same *width to length ratio*.	**5**
	(c)	Given, V_{OL} = 0.6 V and V_{OH} = 4.3 V for the inverter shown in the circuit. **Identify** the High and Low Noise Margins *for an inverter added after* V_{out} which has $V_{IH} = 1/8\ (5V_{DD} - 2\lvert V_{tp}\rvert)$ and $V_{IL} = 1/8\ (3V_{DD} + 2\lvert V_{tp}\rvert)$.	**7**
4. (CO2)		A car was in a stand still condition. To *start* the car, a start/stop button, ***w*** should be pressed. An output, ***z*** *=1* confirms that the car is *moving (accelerating) or running (optimum constant speed)*. ● If ***w*** =0, the car should remain *still* initially. For, ***w***=1, the car should start *moving* (if it was *still*) or stop (if it has just started *moving*, but not *running* yet). ● Once moving, the car should reach the optimal speed within two consecutive clock cycles without pressing the start/stop button, ***w.*** ● After two cycles, it will automatically gain the optimal speed to keep *running.* The car should maintain its speed independent of the value of ***w*** while *running.* ● The break, ***b*** can only be pressed for an emergency stop while *running*. If the car is *still* or *moving*, break, ***b*** *can be ignored.* [Hint: The system has two inputs: ***w, b*** and one output: ***z***]	
	(a)	**Design** the state diagram for the given FSM. [The FSM should be Moore type.]	**5**
	(b)	**Derive** a state table and the state-assigned table from **(a)** using the *gray*-encoding technique.	**4**
	(c)	**Determine** the logic expressions of the next state and output variables using k-maps.	**6**