BRAC UNIVERSITY
CSE460
VLSI DESIGN
Quiz - 4
Time: 30 minutes
Set-A

Name: ***ID:*** ***Section:***

Question 1: [20 Marks]

Suppose you have a NAND-2 driving h number of inverters.

(a) Find kn and kp for both gates if you want equal rise and fall times. [2]
(b) Draw the RC equivalent circuit for the NAND gate with the inverter load in its output node. [6]
(c) Find the expressions of t_{pdr}, t_{cdr}, t_{pdf}, and t_{cdf}. [8]
(d) If R = 5 kΩ.μm and C = 20 fF/μm in a 20 nm technology, find the values of the four delays whose expressions you found in (c). Suppose you have 100 inverters as load. [4]