BRAC University
Department of Computer Science and Engineering

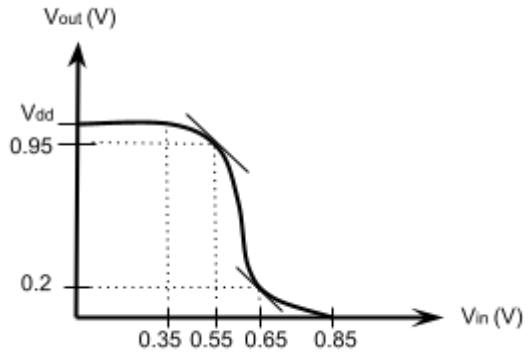
Semester: **Fall 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Midterm Exam
Full Marks: **10 x 3 = 30**
Time: **1 hour**
Date: **4th Nov 2023**

Set B

Student ID:	Name:	Section:

[**Question 3** is **mandatory.** You may answer any **TWO** questions out of the remaining **THREE** along with **Question 3**. In total, you need to answer **THREE** questions out of **FOUR**.]

1. (CO1)	Observe the dc response of an inverter and answer the following questions:  Figure 1: DC response curve of a CMOS inverter V_{dd} = **1V** and beta ratio, **r = 1**.		
	(a)	**Calculate V_{tn}, V_{tp}, V_{inv}.**	**5**
	(b)	**Evaluate** high and low noise margins and comment on its skewness.	**3**
	(c)	Why are there one nMOS and one pMOS parallelly connected in a transmission gate?	**2**
2. (CO1)	**(a)**	Design a CMOS compound gate that implements the following function: **Y = (A + B). (C + (D . E))**	**4**

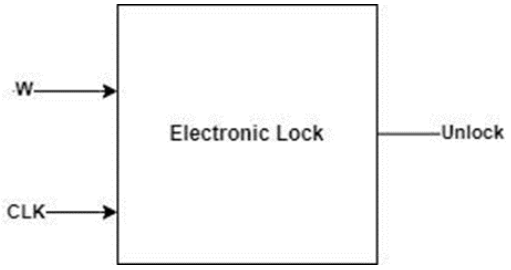
(b) Imagine a *gate*-level logic circuit with 1 output **f**, and 4 input lines ***d3, d2, d1 and d0***.

- Let's define a 2-bit selector input **S = *s1 s0***
- The output **f** is determined as follows:

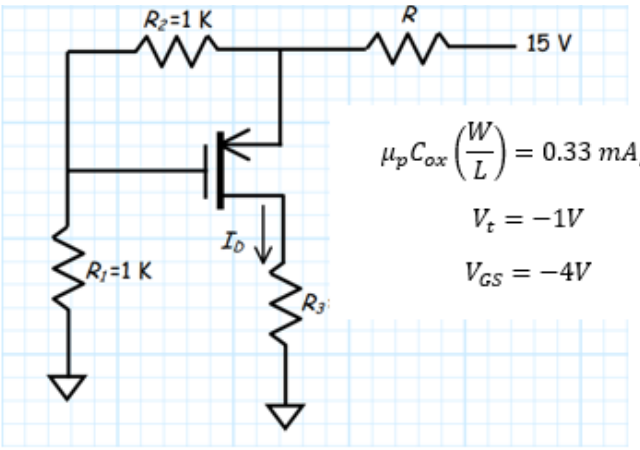
S	f
00	*d2*
01	*d3*
10	*d0*
11	*d1*

i.	**Find** the boolean expression of **f**.	**2**
ii.	**Implement** the circuit using transmission gates.	**4**

3. (CO2) Suppose you are designing an Electronic Lock system for a briefcase. The system has one input ***w*** and an output signal ***unlock*.** When the input pattern **101** is detected in three consecutive clock cycles, the output ***unlock*** attains the value of **1** thus unlocking the briefcase. Otherwise, the value of ***unlock*** remains at **0.**



(a)	**Draw** the state diagram for the corresponding FSM, considering it as a *Moore* type FSM.	**4**
(b)	**Draw** the state table and state assigned table from your state diagram in **(a).**	**4**
(c)	**Evaluate** the boolean expression of the output signal (***unlock***) using K-Map	**2**

4. (CO1)	Consider the following circuit diagram:  Figure 2: Circuit Diagram for Question 4.		
	(a)	Assuming the PMOS in saturation, **calculate** the gate, source and drain voltages.	**6**
	(b)	**Determine** the value of the resistance R. Justify the assumption of the PMOS being in saturation.	**4**