BRAC University
Department of Computer Science and Engineering

Semester: **Spring 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 40 minutes**
Date: **2nd May 2023**

Set A

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO3)

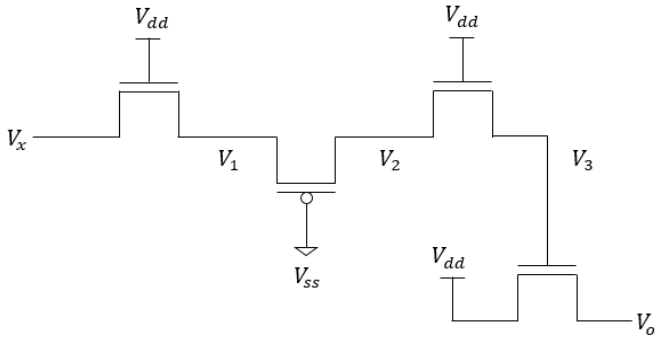


Figure 1

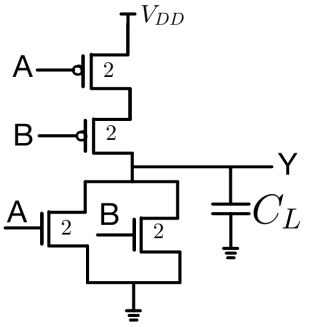


Figure 2

(a) The pass transistor circuit in **figure 1** has the following specifications:
$V_{DD} = 5V, V_{ss} = 0V, V_{tp} = -0.5V, V_{tn} = 0.5V, V_o = 2.5V$ and $0.5V < V_x < 4.5V$

(i) **Calculate** the unknown voltage values: V_x, V_1, V_2, V_3 **[5]**

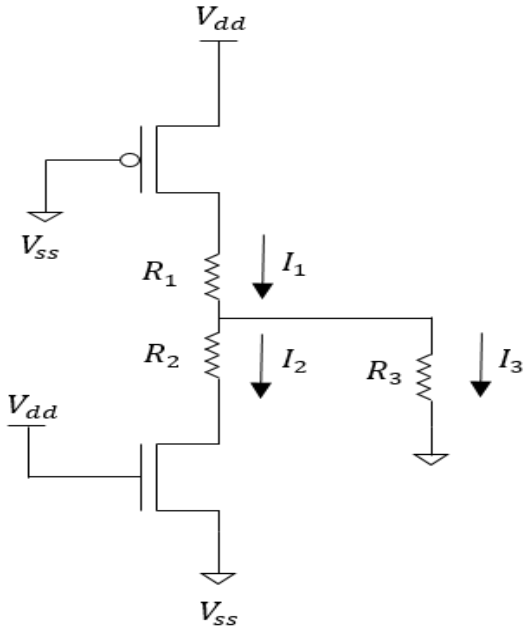
(b) A digital system-on-chip has the above gate from **figure 2** implemented on it. Individual transistor widths $k_{nMOS} = 2$ and $k_{pMOS} = 2$ were chosen to achieve the effective rise and fall resistance equal to that of a unit inverter, *R* for the given gate. The system has $\mathbf{V_{DD}}$**=1V**, activity factor, **α= 0.2**, unit transistor's width, **W = 6 µm**, load capacitor, $\mathbf{C_L}$ **= 2 pF** and parasitic diffusion capacitance for both PMOS and NMOS transistors are **0.5 fF/µm**. Here, 1G = 10^9, 1p = 10^{-12}, 1f = 10^{-15}.

(i) **Calculate** the total capacitance at node **Y**. **[4]**

(ii) **Estimate** the Switching power when operating in **1.4 GHz.** **[3]**

(iii) **Determine** if the system can switch *faster* or *slower*, when $\mathbf{V_{DD}}$ is *halved* while the switching power and the capacitance remain *same* [as (ii)]. **[3]**

2. (CO3) Consider the following circuit:



The circuit has the following specifications:

- **nMOS specifications**: $W_n = 1\ \mu m$, $L_n = 0.18\ \mu m$, $\mu_n C_{ox} = 50 \mu A/V^2$, $V_{tn} = 0.4V$
- **pMOS specifications**: $W_p = 2\ \mu m$, $L_p = 0.18\ \mu m$, $\mu_p C_{ox} = 100 \mu A/V^2$, $V_{tp} = -0.4V$
- **Other specifications**: $I_2 = 1mA$, $I_3 = 0.5mA$, $R_2 = 0.5k\Omega$, $R_3 = 2.5k\Omega$, $V_{dd} = 3V$, $V_{ss} = 0V$

(a)	**Calculate** the current constants (β_p, β_n) for both of the transistors.	**[3]**
(b)	**Find** the voltage across the R_3 resistance.	**[3]**
(c)	**Determine** the operating mode of the nMOS transistor.	**[5]**
(d)	**Identify** the value of R_1 in order to keep the pMOS transistor in the "linear" operating mode.	**[4]**

3. CO3) Observe the figure and the truth table and answer the following questions. Assume the effective rise and fall resistances of all the components are equal to that of a unit inverter (**R**) in the worst case.

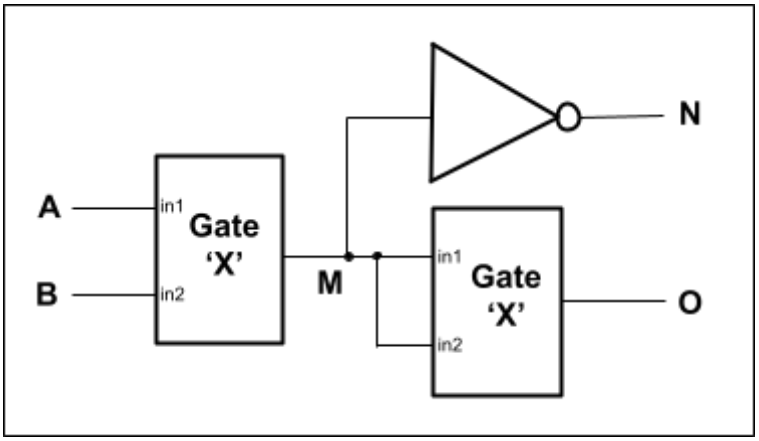
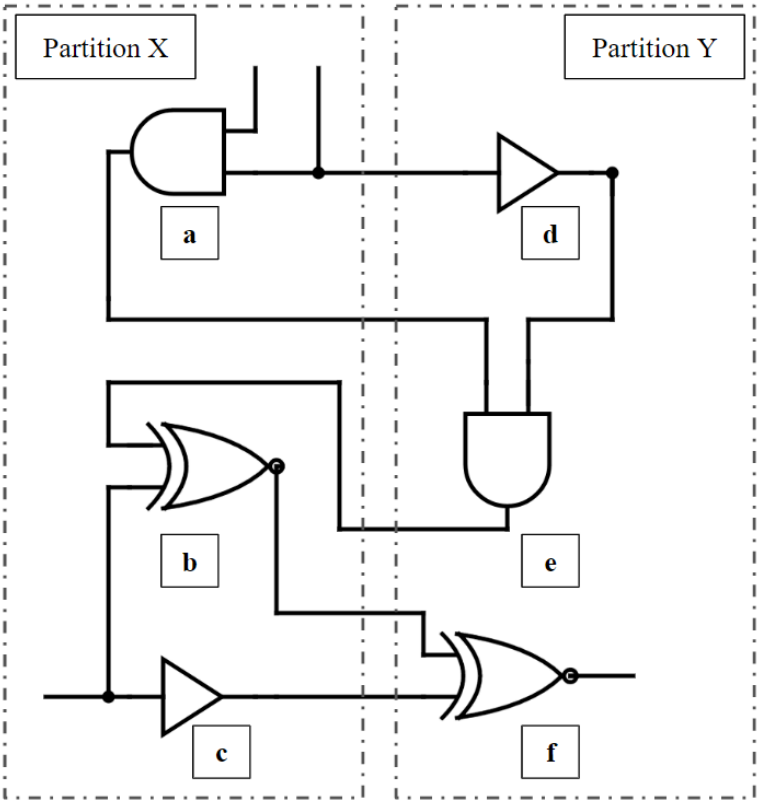


Figure: Two-input CMOS gate 'X' is driving another 'X' gate and an inverter.

Truth Table for node N

A	B	N
0	0	0
0	1	0
1	0	0
1	1	1

(a)	**Identify** gate 'X'.	**[2]**
(b)	**Calculate** the capacitances of nodes A, B, and M with the necessary figures.	**[6]**
(c)	**Calculate** 'propagation delay rise (t_{pdr})' at node M.	**[4]**
(d)	'N and O nodes have identical outputs but the N node is faster' - do you agree with the statement? **Explain** qualitatively.	**[3]**

4. (CO4, CO5)	Consider the following circuit with 6 logic gates (a-f) and the initial partitioning marked by the dotted lines.  		
	(a)	**Represent** the given circuit and the initial partitioning using a graph.	**[3]**
	(b)	**Compute** the initial cut cost.	**[1]**
	(c)	**Perform** the first pass of the algorithm. For every "i"th iteration inside the first pass, until all the nodes are swapped and fixed, do the following: i. Compute the node costs of all unfixed nodes ii. Find the maximum gain of swapping a pair of nodes (Δg_i) iii. Swap the pair and draw the updated graph	**[6]**
	(d)	Finish the first pass by computing the maximum positive gain, G_m. **Suggest** how many swaps should be actually executed in the first pass.	**[4]**
	(e)	Should you perform subsequent passes of the algorithm? Why or why not?	**[1]**