

# MOSFET

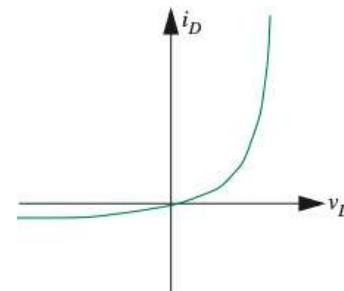
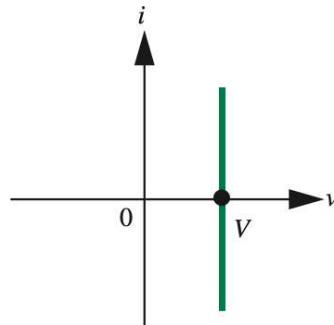
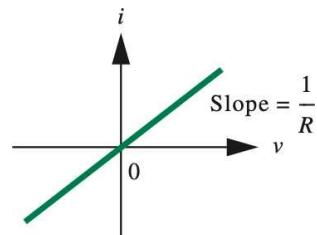
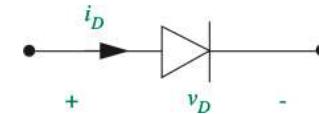
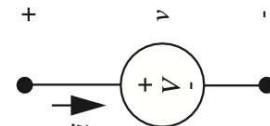
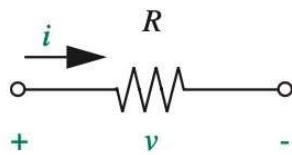
**Lecture 11, 12 & 13**

Course No: CSE 251

Course Title: Electronic Devices and Circuits

# Three terminal devices

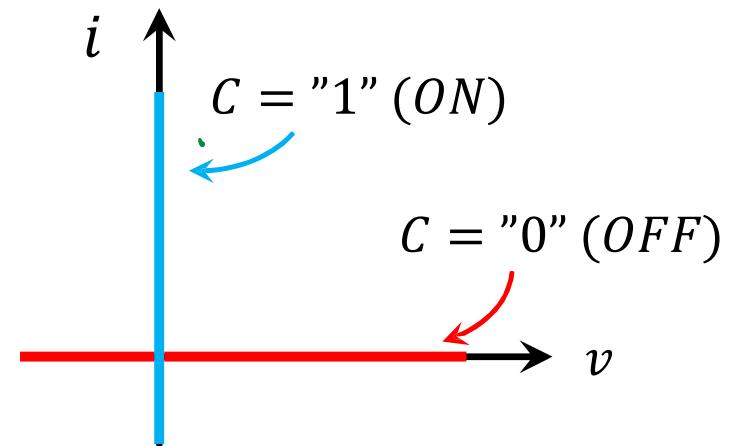
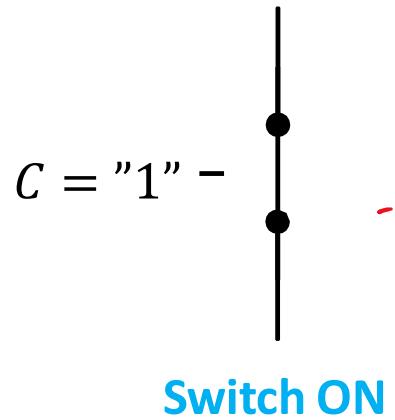
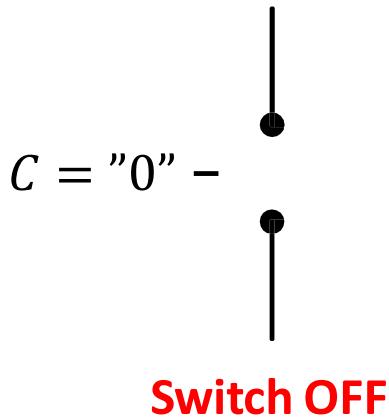
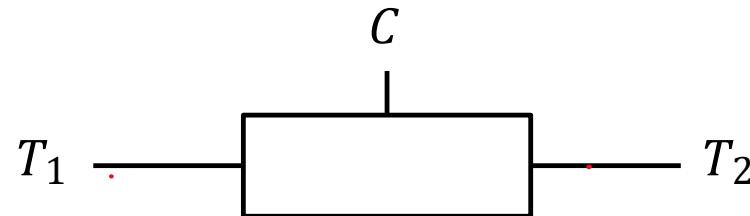
- Two terminal devices have fixed IV characteristics



- Three terminal devices – IV of two terminal can be controlled using the third terminal.
- Examples – Switch (linear), Transistors (non-linear)

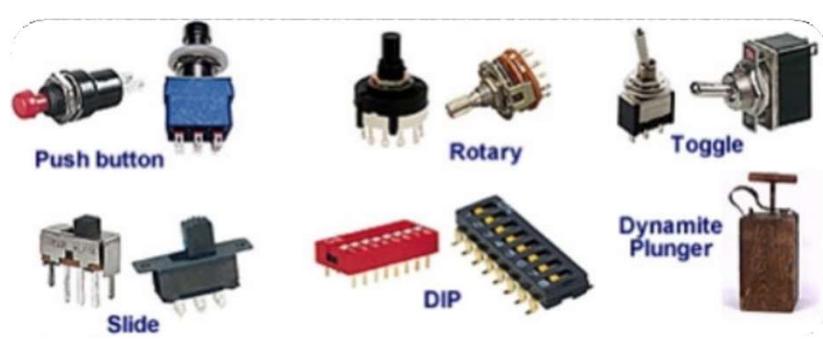
# Switch – IV Characteristics

- IV characteristics between terminal  $T_1$  and  $T_2$  is controlled by  $C$

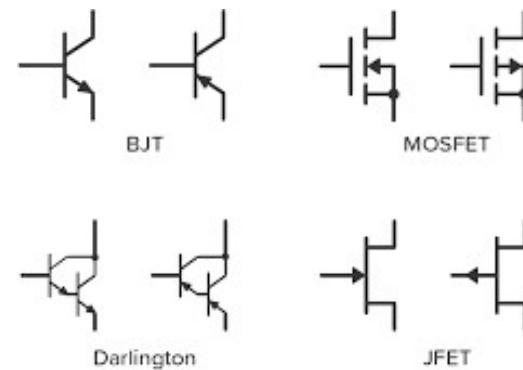


# Switch – Types

- Depending on the control, the switch can be
  - **Analog:** Controlled using physical toggle/button
  - **Digital:** Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



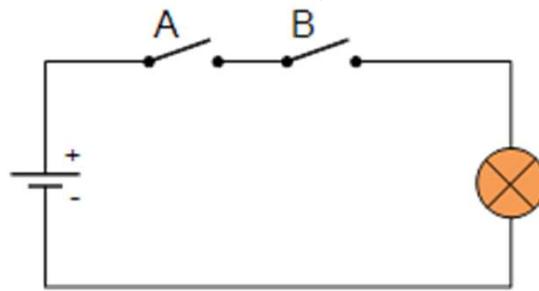
Analog switches



Digital switches (Transistors)

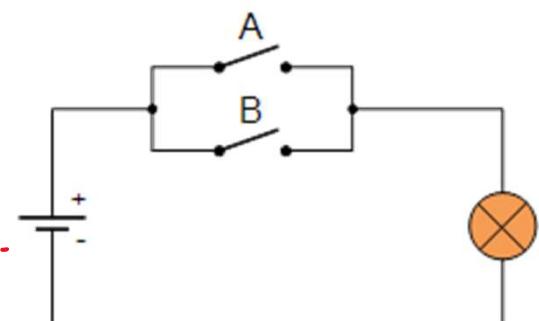
# Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

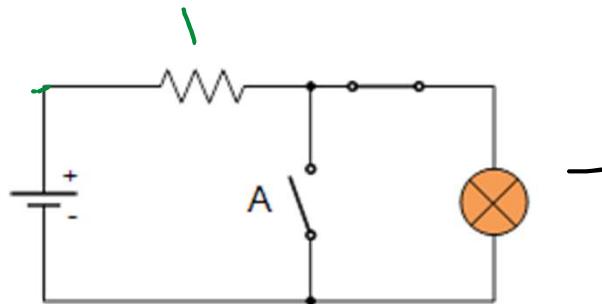
**AND operation**



A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

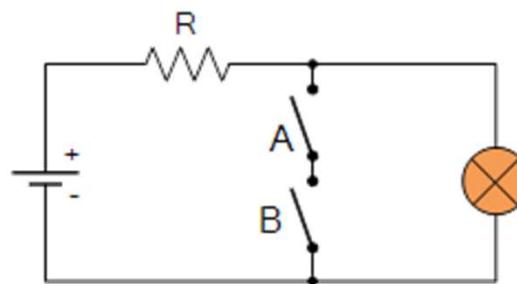
**OR operation**

# Switch Application – Logic Gates



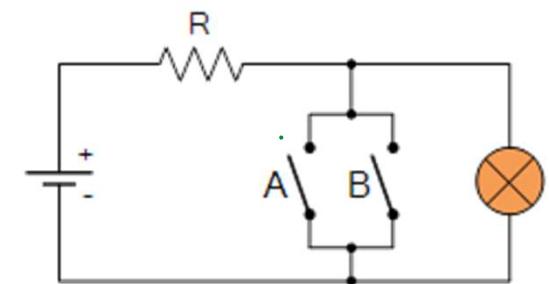
A	Bulb
0	ON
1	OFF

**NOT operation**



A	B	Bulb
0	0	ON
0	1	ON
1	0	ON
1	1	OFF

**NAND operation**



A	B	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

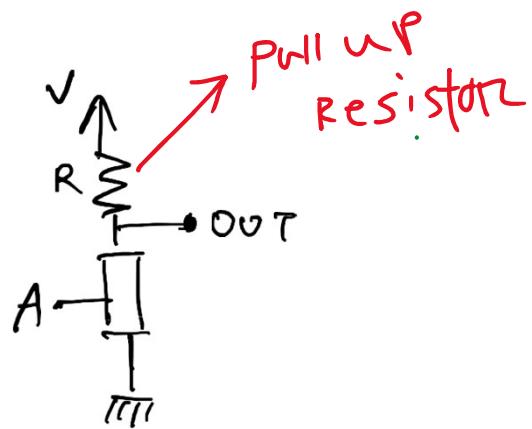
**NOR operation**

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits

-> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

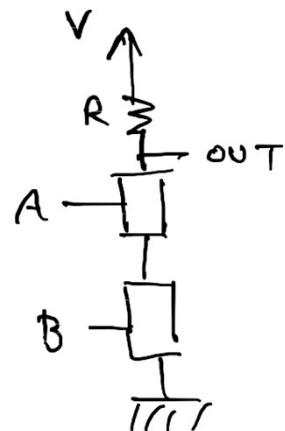
# Switch Application – Logic Gates

Alternative representations:



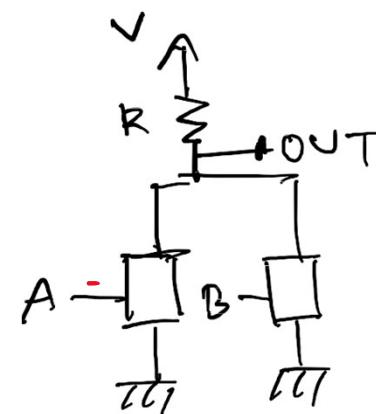
$$OUT = \overline{A}$$

(NOT)



$$OUT = \overline{AB}$$

(NAND)

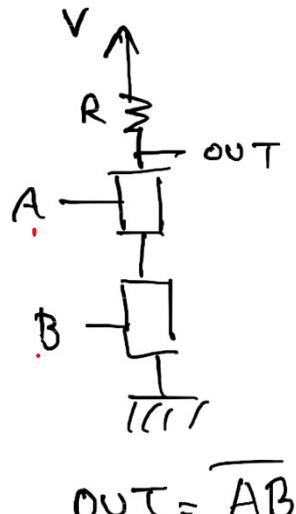


$$OUT = \overline{A+B}$$

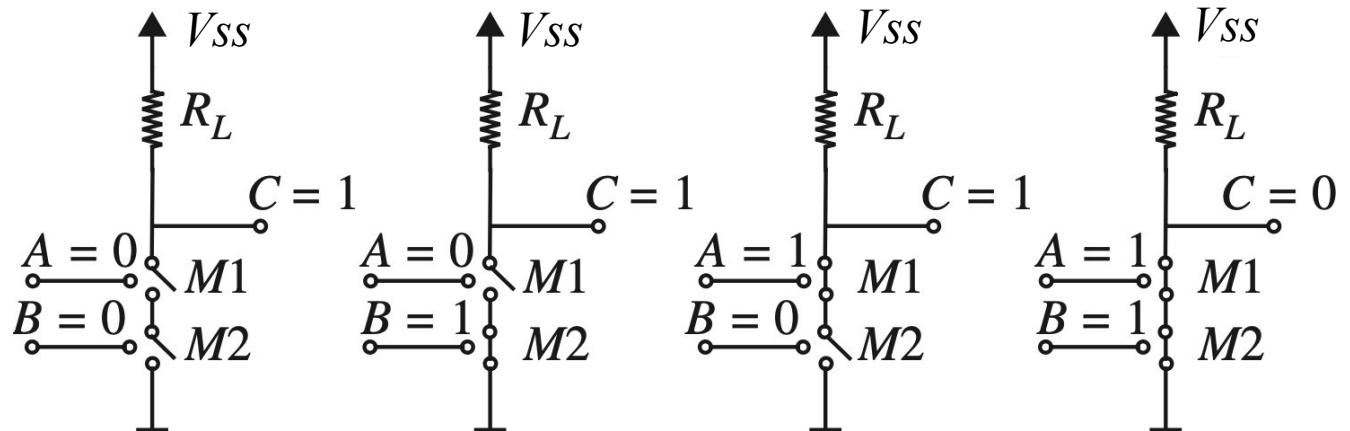
(NOR)

# Switch Application – Logic Gates

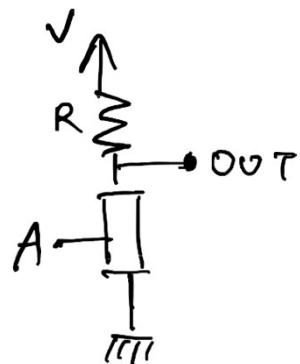
Alternative representations:



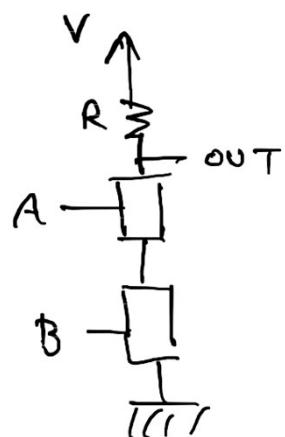
(NAND)



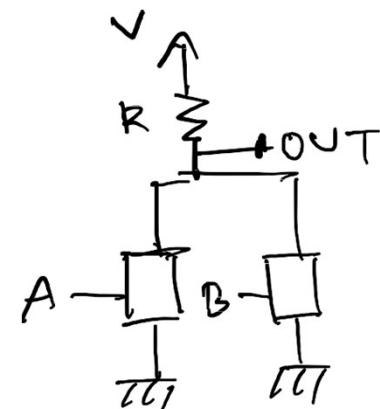
# Switch Application – Logic Gates



$$OUT = \overline{A}$$



$$OUT = \overline{AB}$$



$$OUT = \overline{A+B}$$

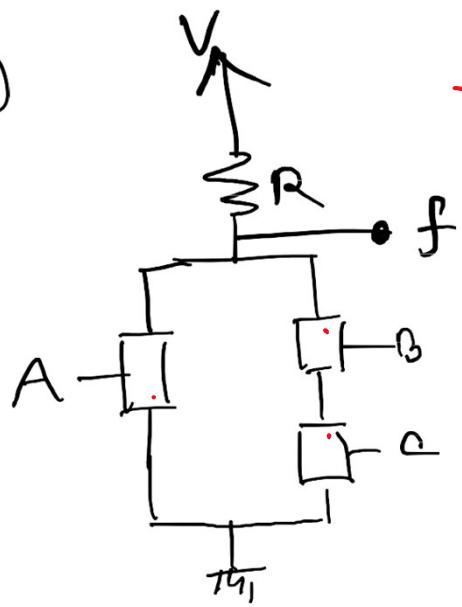
<i>A</i>	<i>V<sub>OUT</sub></i>
0	5V
1	0V

<i>A</i>	<i>B</i>	<i>V<sub>OUT</sub></i>
0	0	5V
0	1	5V
1	0	5V
1	1	0V

<i>A</i>	<i>B</i>	<i>V<sub>OUT</sub></i>
0	0	5V
0	1	0V
1	0	0V
1	1	0V

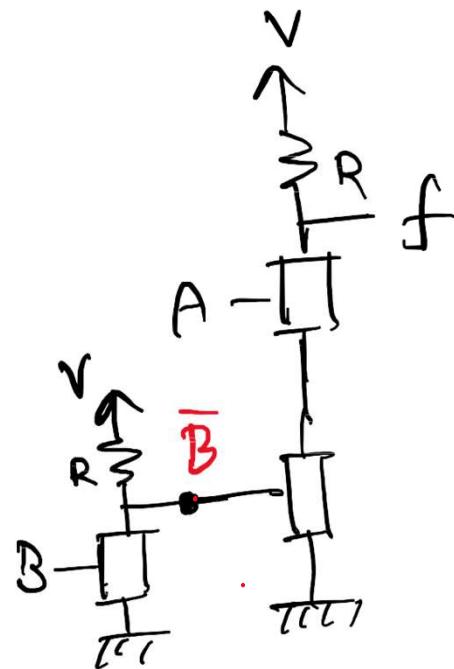
# Examples

①



$$f = \overline{A + B \cdot C}$$

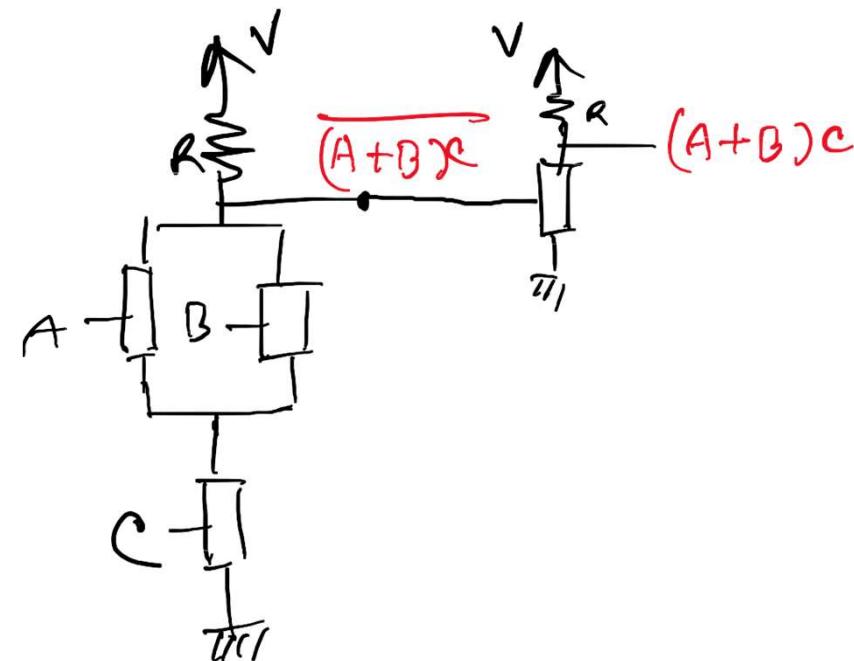
②



$$f = \overline{A \bar{B}}$$

# Example

Implement using switches:  $f = (A + B)C$



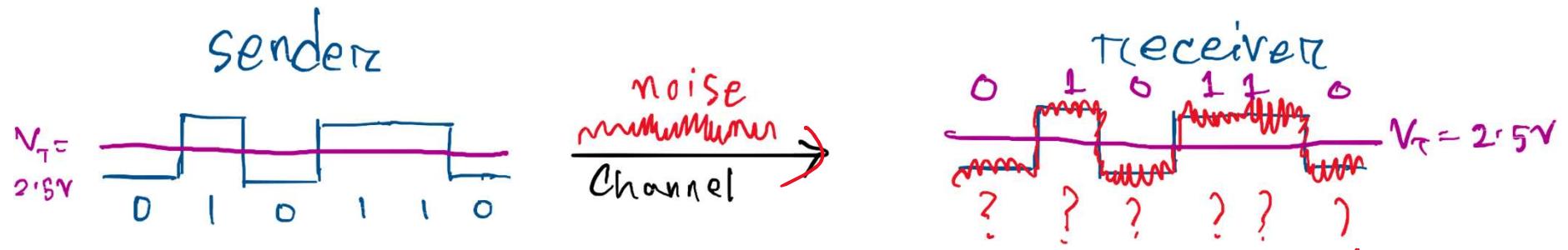
# Digital Representation

- Binary → Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

Voltage	Current	State
5V → 1	2mA → 1	ON → 1
0V → 0	3mA → 0	OFF → 0
0V → 1		Low resistance → 1
3.3V → 0		High resistance → 0

# Digital Representation

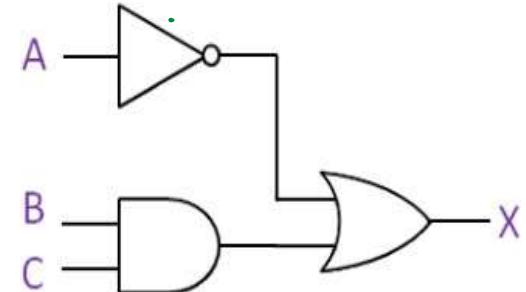
Suppose you want to send 010110



- Single value based representation fails in the presence of noise
- Better approach – threshold-based system
- Simplest:  $\text{Logical } 0 = V < V_T$        $\text{Logical } 1 = V > V_T$

# Static Discipline

**Single specification for all devices in a system**



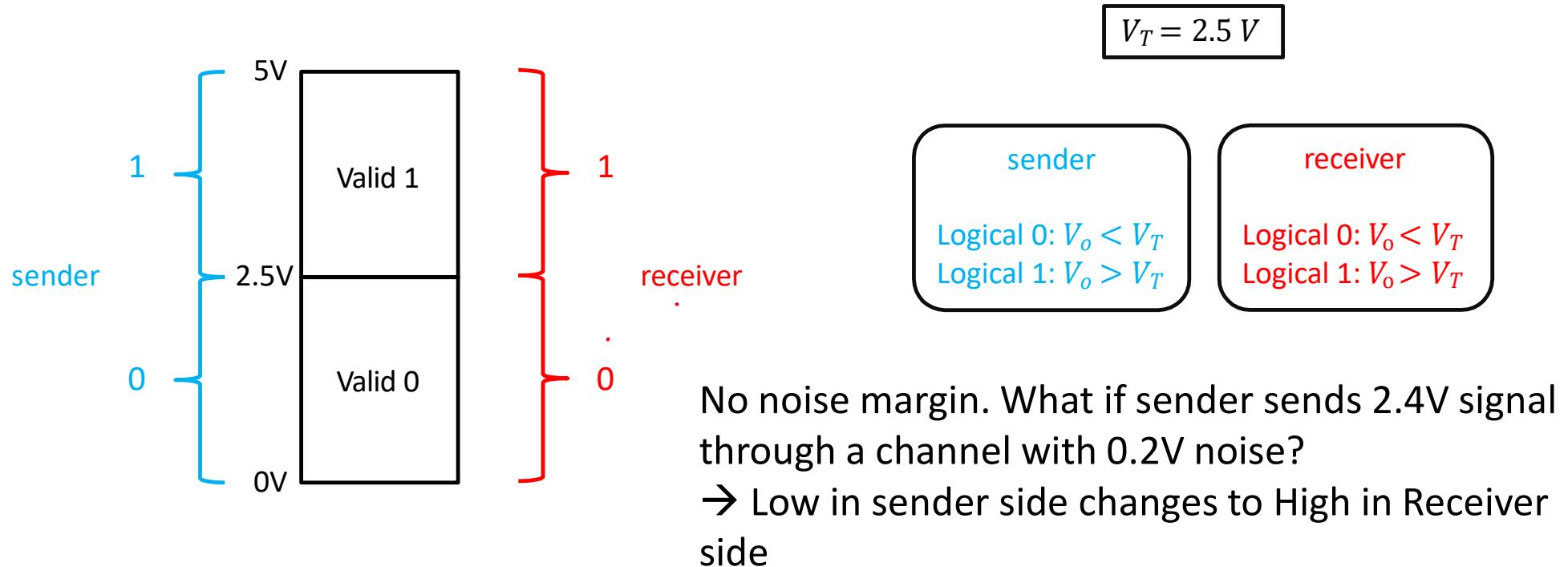
- Specification for digital devices
- Requires devices to adhere to common representation to ensure that **valid input produces valid output**
- This means, if

• Sender sends "0"  $\xrightarrow[\text{Channel}]{\text{noise}} \text{Receiver interprets as "0"}$

• Sender sends "1"  $\xrightarrow[\text{Channel}]{\text{noise}} \text{Receiver interprets as "1"}$

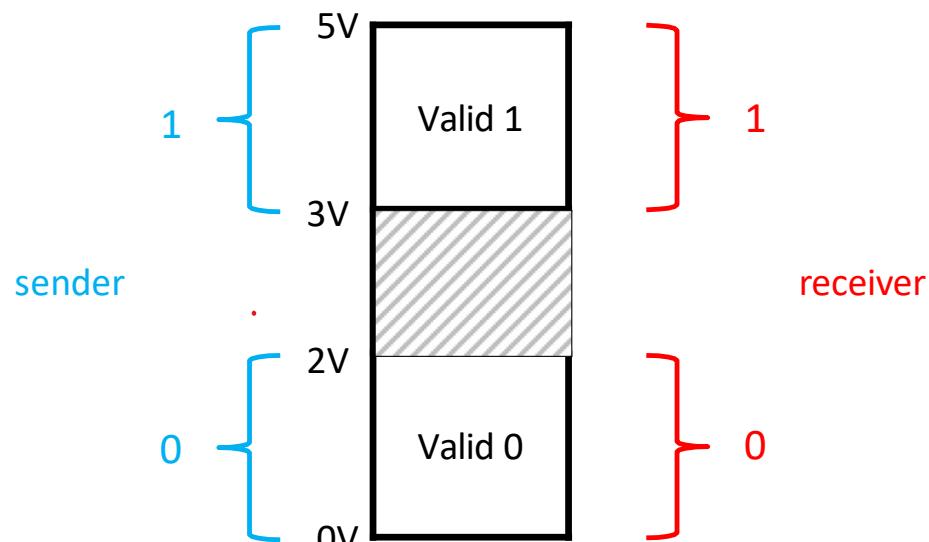
# Static Discipline

Naïve approach: **Single threshold** based system



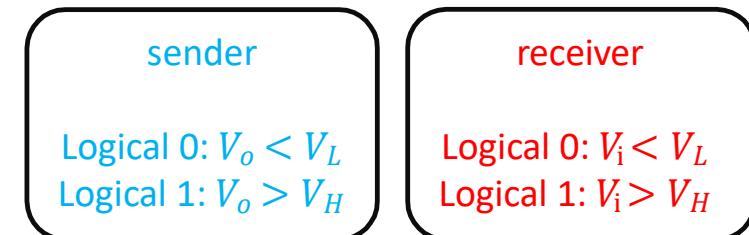
# Static Discipline

## Double threshold based system



$V_H$  = High voltage threshold = 3V

$V_L$  = Low voltage threshold = 2V



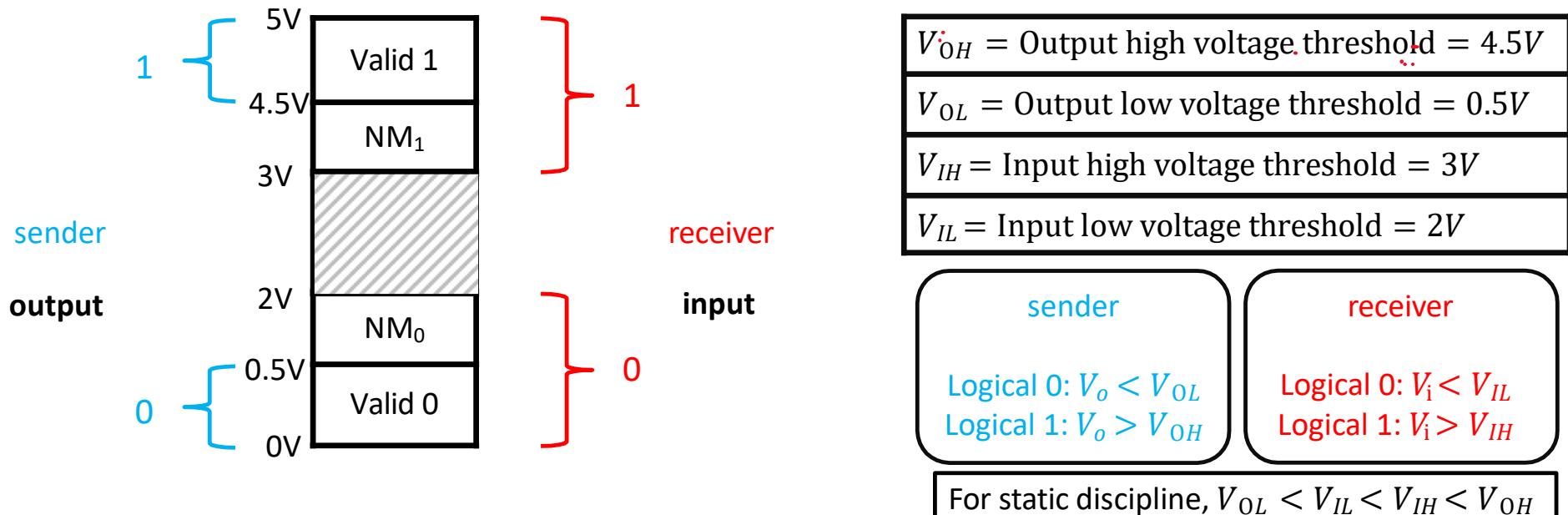
What if  $V_o = 1.9V$  and channel noise is  $0.5V$ ?

$$V_i = 1.9V + 0.5V = 2.4V = \text{invalid}$$

→ valid output producing invalid input,  
i.e., no margin for noise

# Static Discipline

Four threshold based system → Tighter restriction on sender (**output**)



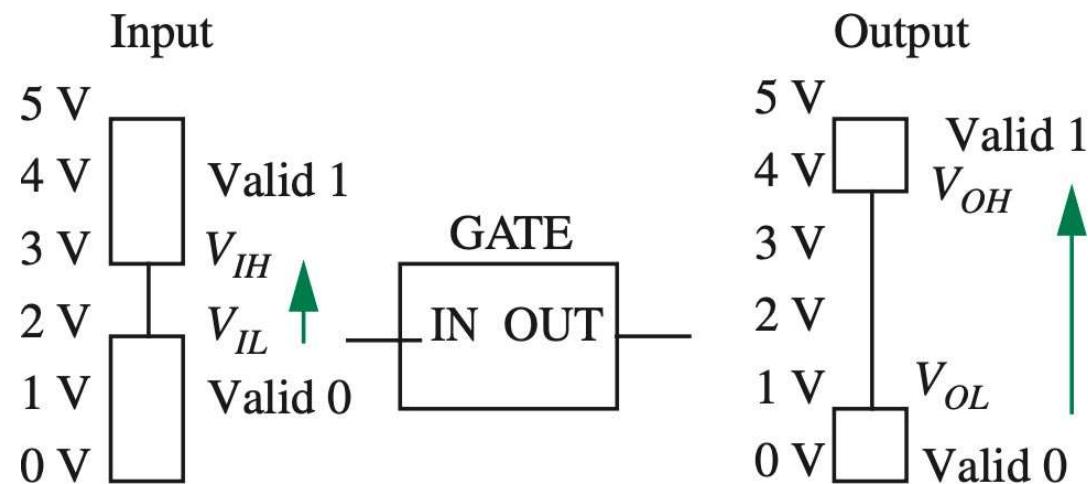
Noise margins (NM):

- $NM_1 = V_{OH} - V_{IH} = 4.5 - 3 = 1.5V$  (significance?)
- $NM_0 = V_{IL} - V_{OL} = 2 - 0.5 = 1.5V$  (significance?)

If sender wants to send 1 or 0, even a channel with 1.5V noise wouldn't cause error.

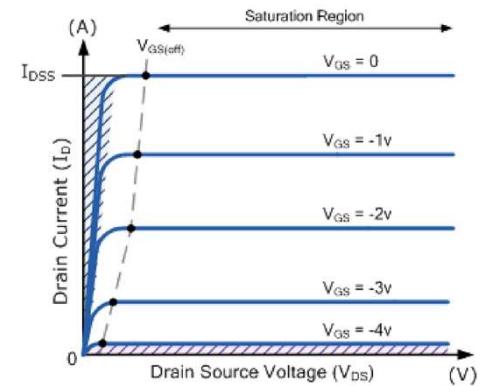
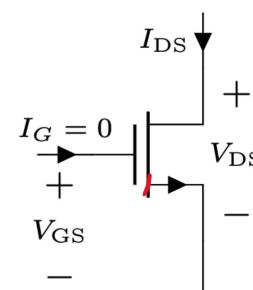
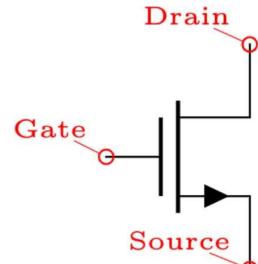
# Static Discipline

Four threshold based system → Tighter restriction on sender (**output**)



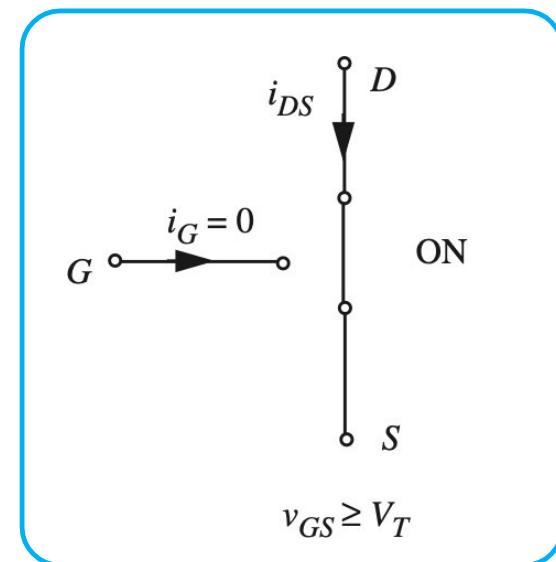
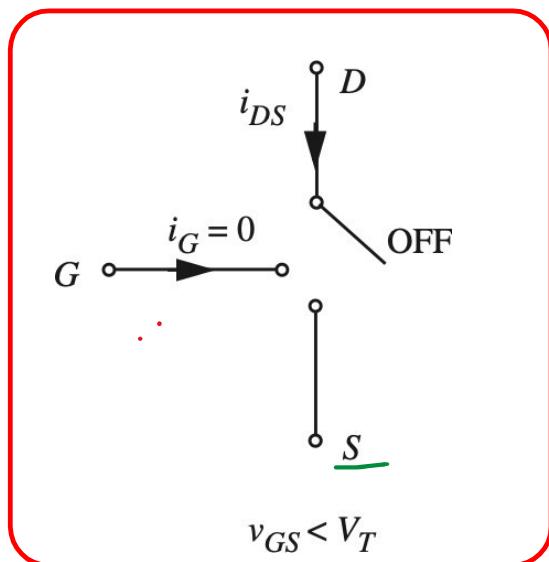
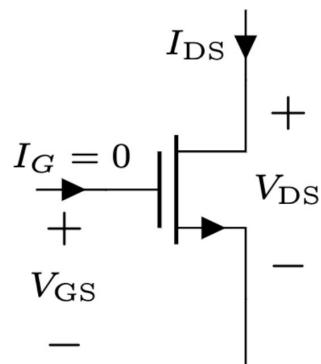
# Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – Voltage Controlled, Current Controlled
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are voltage controlled
- Control,  $C = V_{GS}$ . The IV characteristics ( $I_{DS}$  vs  $V_{DS}$ ) depends on  $V_{GS}$
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)

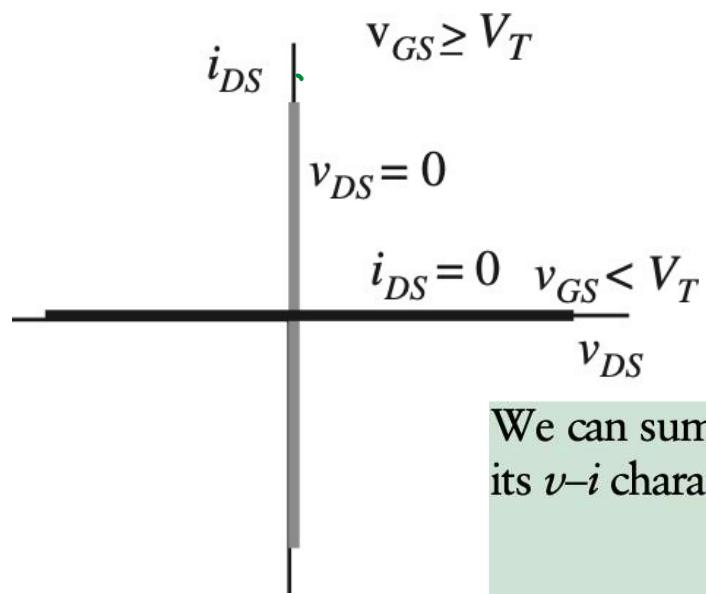


# MOSFET S-Model

- The MOSFET (approximately) behaves like a switch
- $C = V_{GS}$ . Here,  $C = "0"$   $\Rightarrow V_{GS} < V_T$ , and  $C = "1"$   $\Rightarrow V_{GS} \geq V_T$



# MOSFET S-Model



We can summarize the S model for the MOSFET in algebraic form by stating its  $v-i$  characteristics as follows:

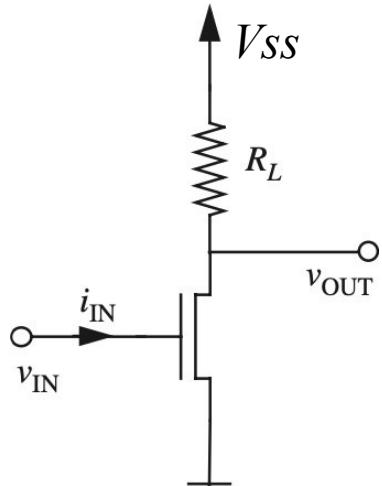
$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

and

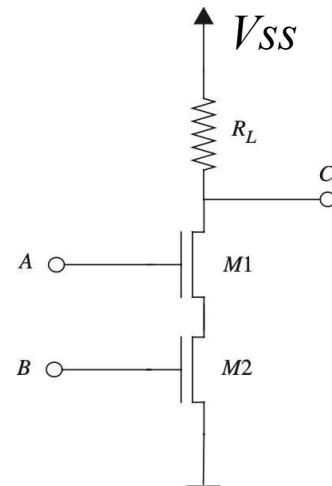
$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \quad (6.2)$$

# Logic Gates using MOSFET

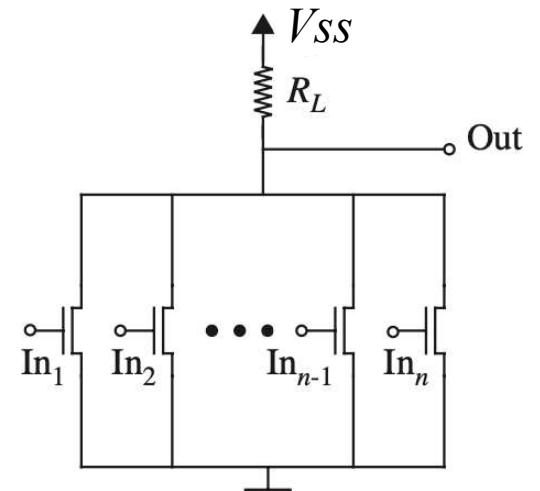
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

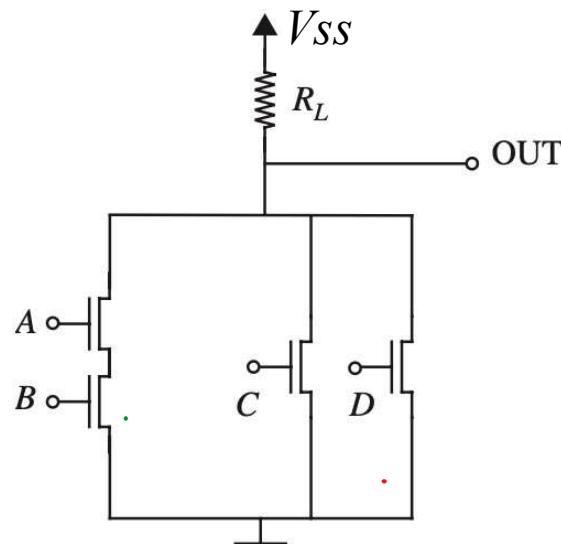


NAND Gate (Inverter)

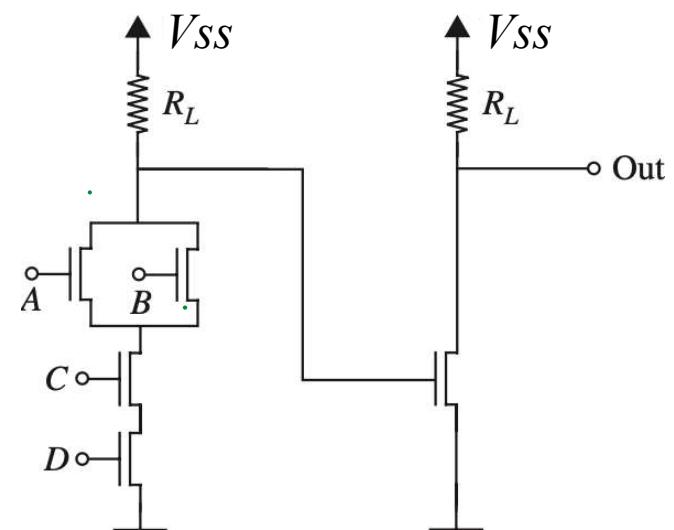


NOR Gate (Inverter)

# MOSFET Logic Gates – More Examples

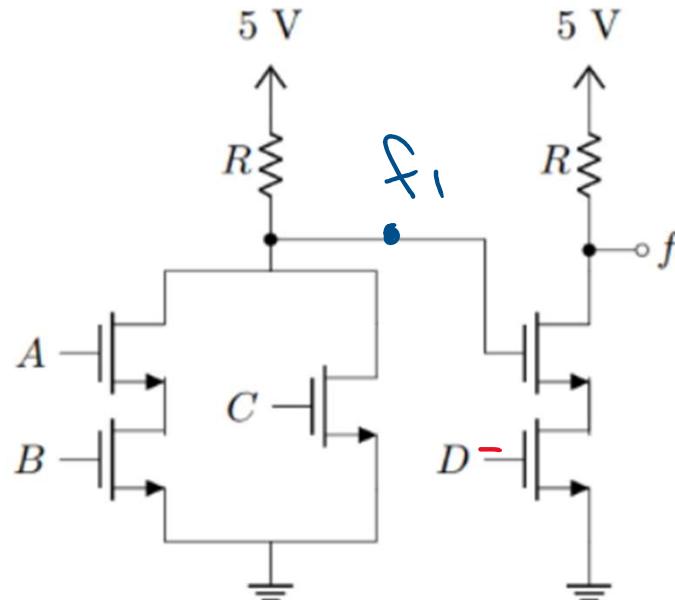


$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

# MOSFET Logic Gates – More Examples



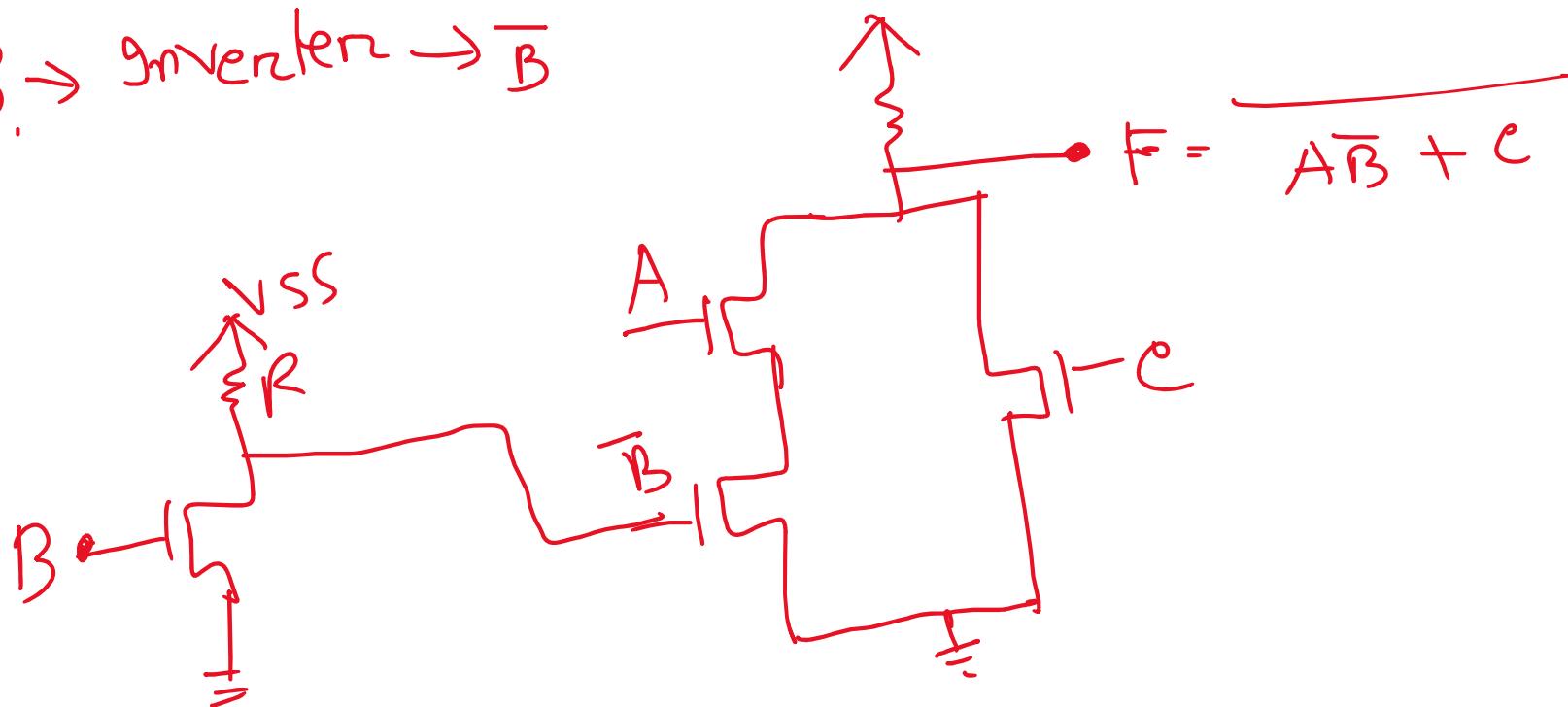
Circuit 2

$$\begin{aligned}f_1 &= \overline{AB+e} \\f &= \overline{f_1.D} \\&= \overline{(AB+e) \cdot D}\end{aligned}$$

# MOSFET Logic Gates – More Examples

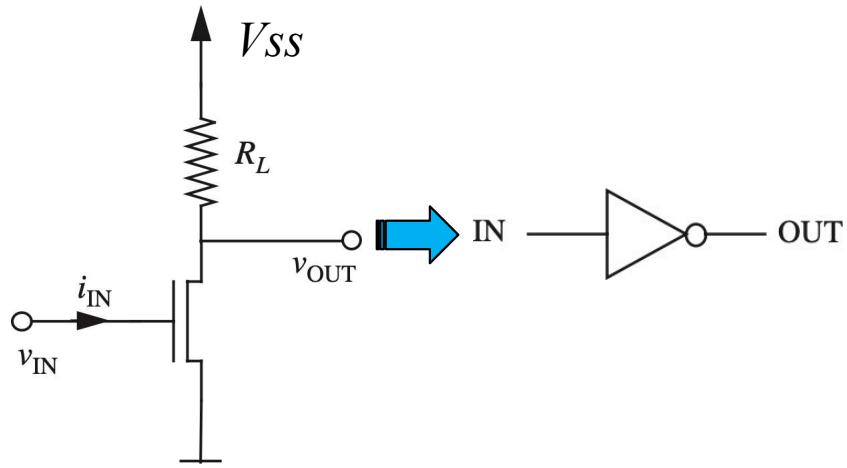
Use MOSFET to implement the Boolean Logic function,  $F = \overline{A\overline{B}} + C$

$B \rightarrow \text{Inverter} \rightarrow \overline{B}$



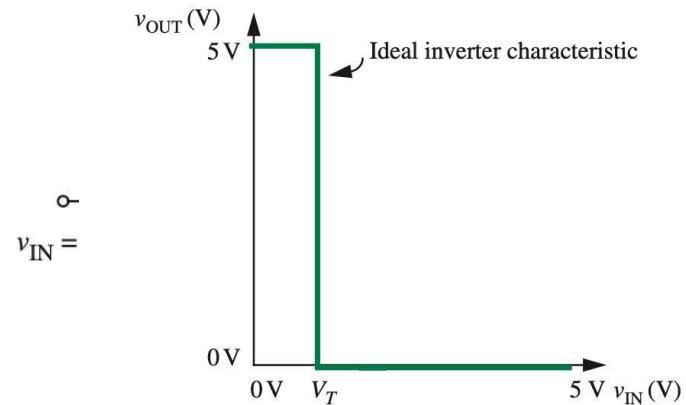
# Voltage Transfer Characteristics (VTC)

- Reminder: VTC is a graph where x axis = input voltage, y axis = output voltage
- Why? Design logic gates to follow a given static discipline

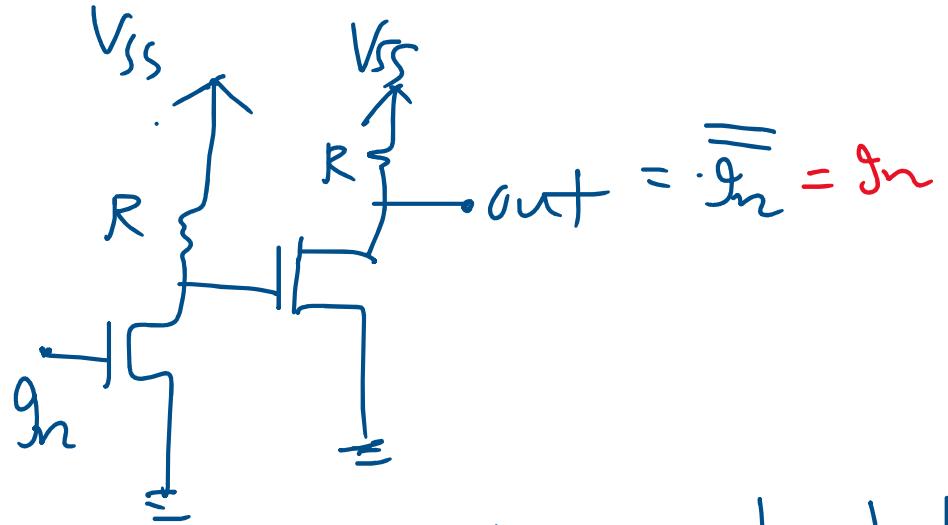


When  $v_{IN} < V_T$  (Logical 0)  $v_{OUT} = V_s = 5V$  (Logical 1)

When  $v_{IN} \geq V_T$  (Logical 1),  $v_{OUT} = 0$  (Logical 0)

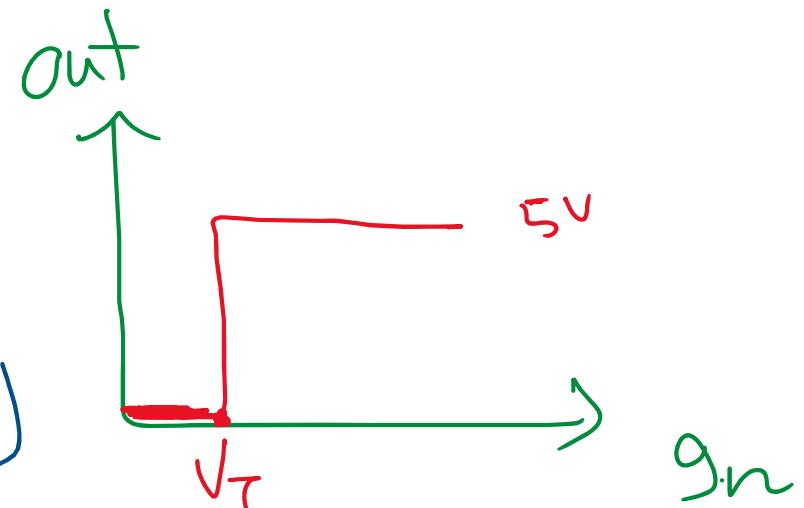


## VTC of double inverters



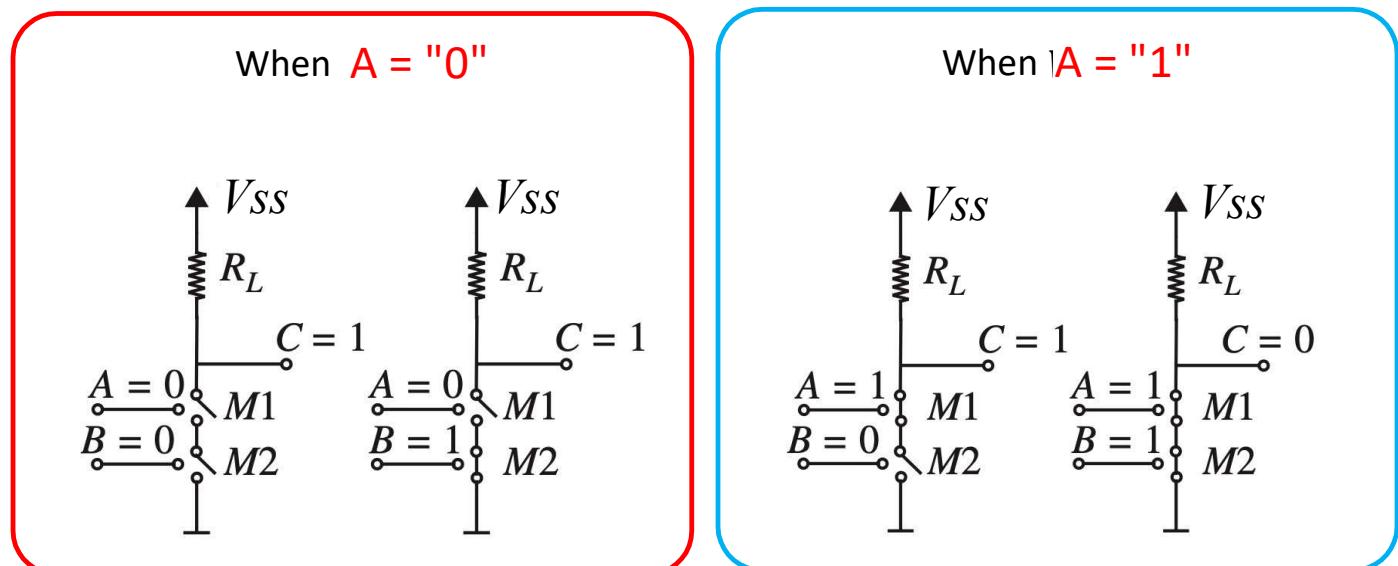
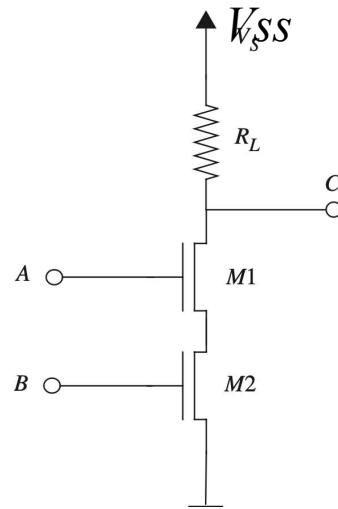
$g_m < V_T$  (low)  $\rightarrow$  output low (0V)

$g_m > V_T$  (high)  $\rightarrow$  output high (5V)



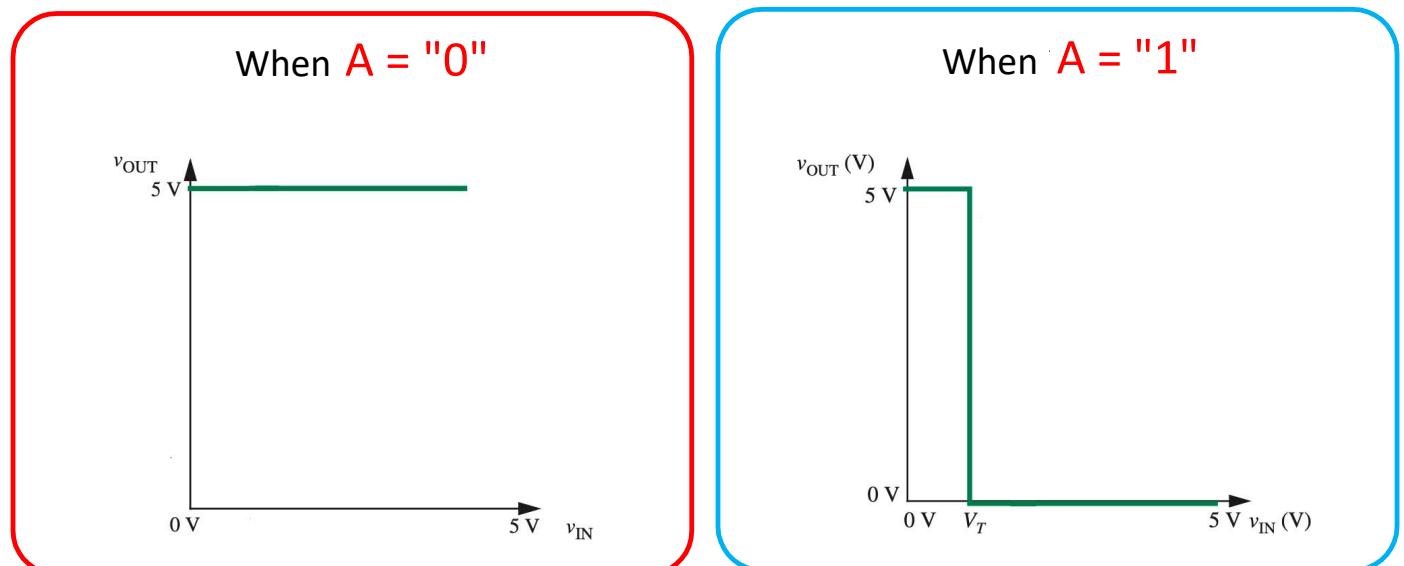
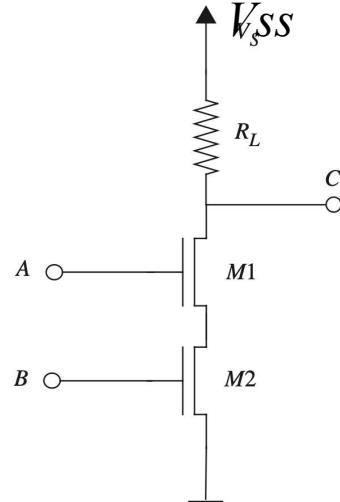
# VTC of NAND gate

- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering  $\bar{A} = "0"$ , one considering  $A = "1"$



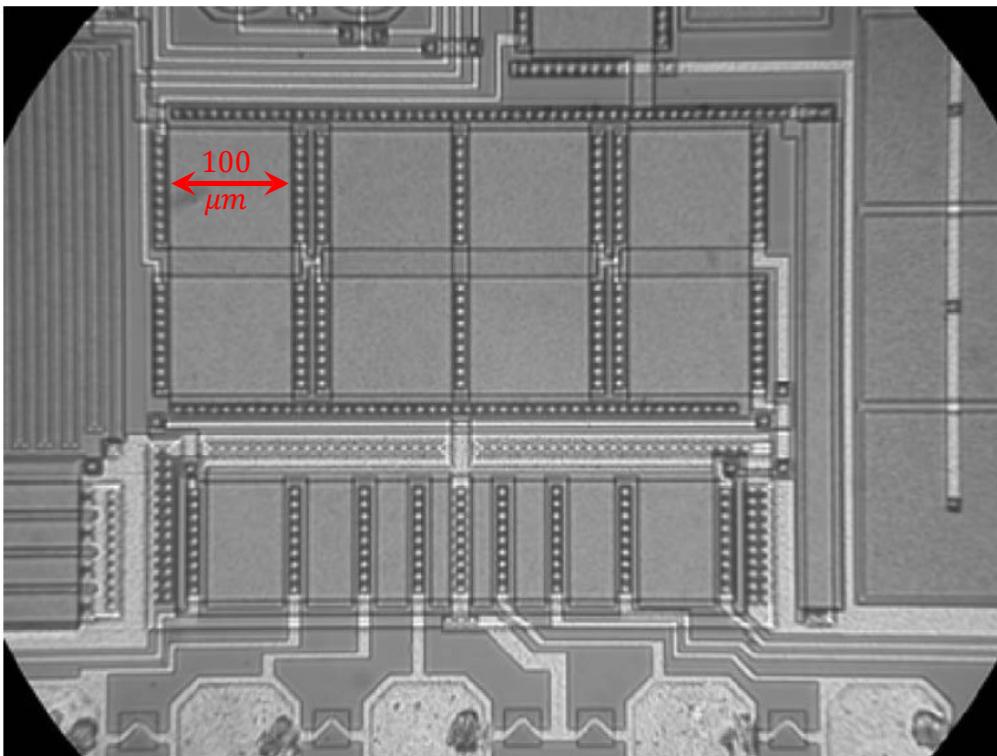
# VTC of NAND gate

- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering  $A = "0"$ , one considering  $A = "1"$



Homework: Find VTC for NOR gate

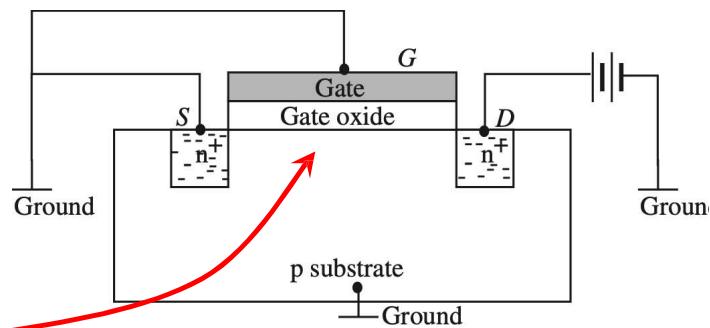
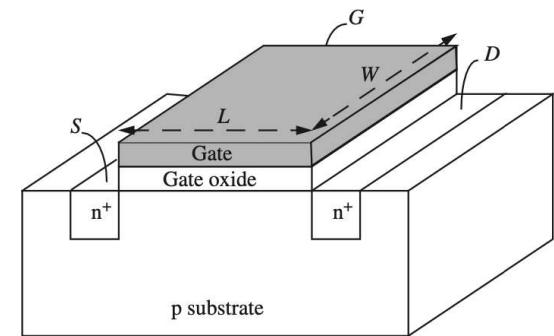
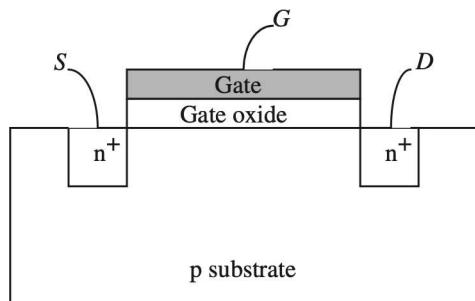
# Construction of Real MOSFET



Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of  $100 \mu\text{m}$ . (Photograph Courtesy of Maxim Integrated Products.)

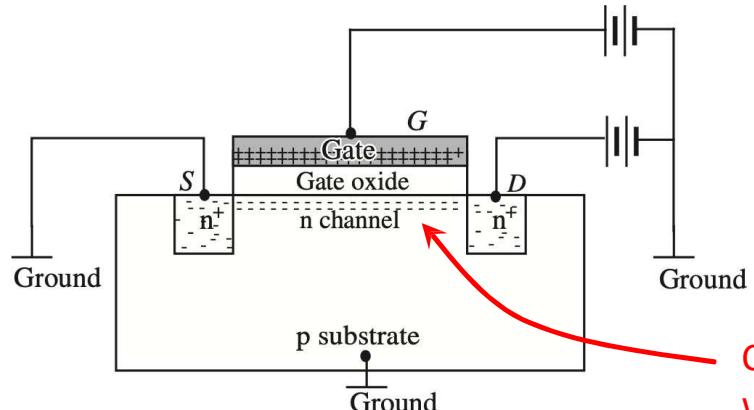
# Construction of Real MOSFET

Simplified cross section  
and 3D view



No channel, open ckt

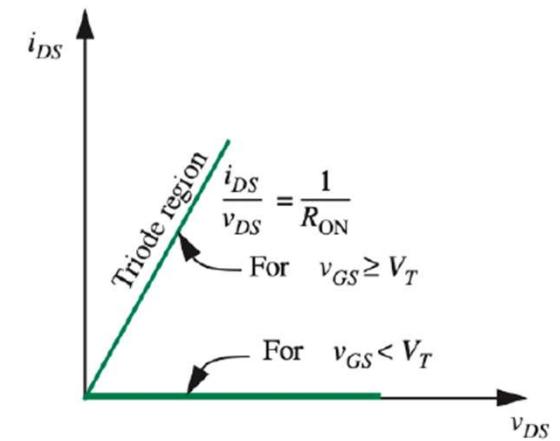
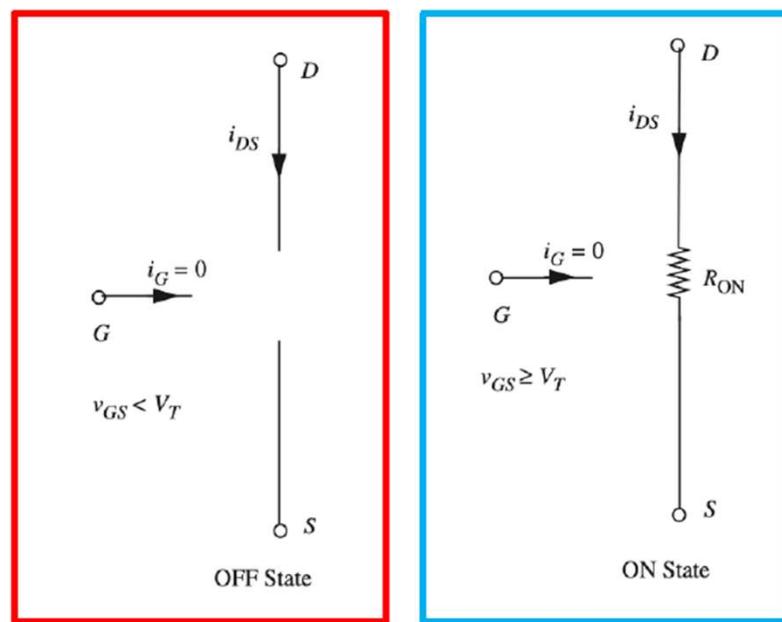
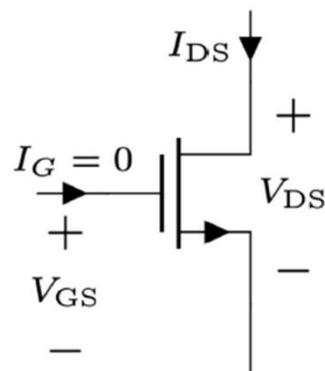
$$V_{GS} = 0V$$



$$V_{GS} > V_T$$

Channel created  
Will have some R  
-> SR model

# SR Model

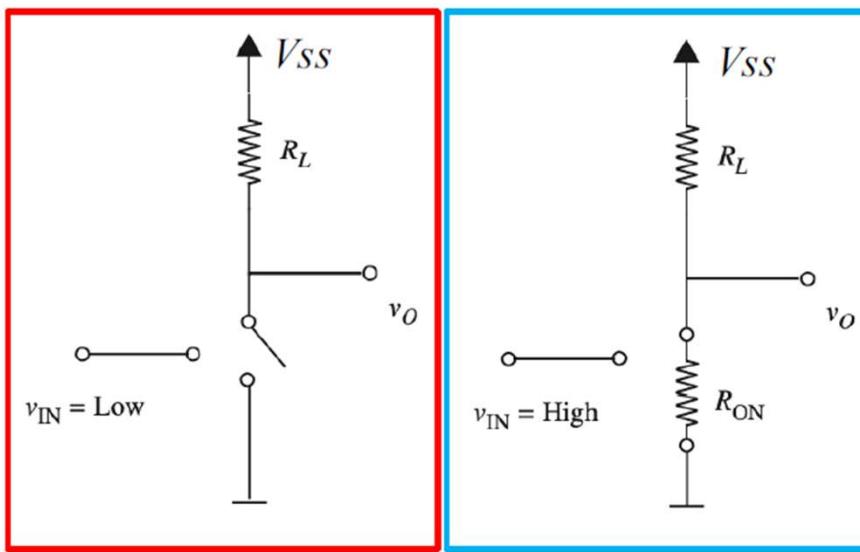
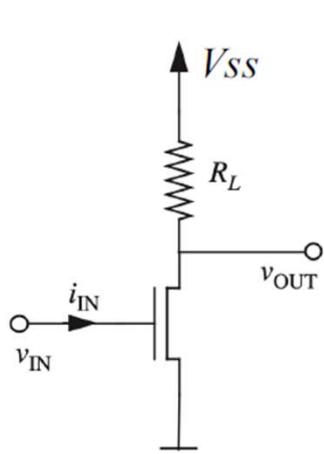


$$R_{ON} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{k V_{OV}}$$

Unit of  $k = mA/V^2$

- SR model is a better approximation than S model
- However, still an approximation. This model fails when  $V_{DS}$  increases to around  $V_{GS} - V_T$

# SR Model - Inverter

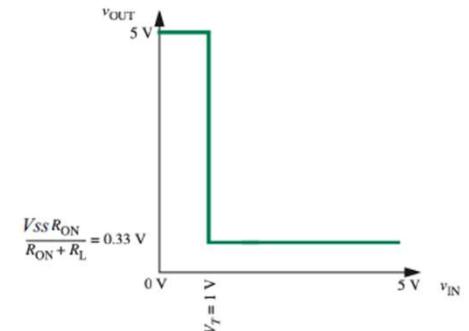


$$v_{OUT,High} = V_{SS}$$

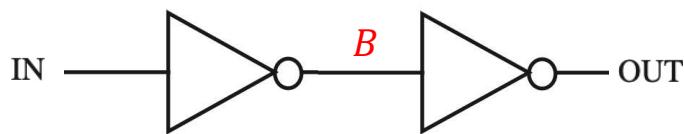
$$v_{OUT,Low} = V_{SS} \frac{R_{ON}}{R_{ON} + R_L} \neq 0$$

For example, if  $V_{SS} = 5V$ ,  
 $R_{ON} = 1 k\Omega$ ,  $R_L = 14 k\Omega$

$$V_{SS} \frac{R_{ON}}{R_{ON} + R_L} = 0.33 \text{ V.}$$

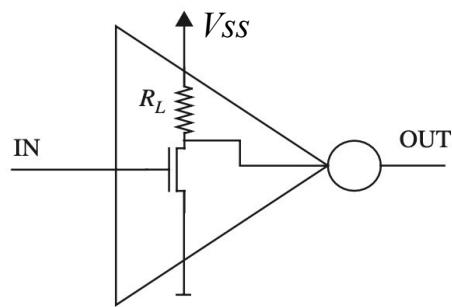


# Design of logic gates



Expected

<i>IN</i>	<i>B</i>	<i>OUT</i>
Low ( $V_{IN} < V_T$ )	High (5V)	Low ( $V_{OUT} = V_{OUT,Low}$ )
High ( $V_{IN} > V_T$ )	Low ( $V_{OUT,Low}$ )	High (5V)



Actual

<i>IN</i>	<i>B</i>	<i>OUT</i>
Low ( $V_{IN} < V_T$ )	High (5V)	Low ( $V_{OUT} = V_{OUT,Low}$ )
High ( $V_{IN} > V_T$ )	Low ( $V_{OUT,Low} = 0.5 V$ )	Low ( $V_{OUT} = V_{OUT,Low}$ )

$$V_T = 0.4 V, V_{SS} = 5V, R_{ON} = 1 k\Omega, R_L = 9 k\Omega$$

$$V_{OUT, High} = V_{SS} = 5V$$

$$V_{OUT, Low} = V_{SS} \frac{R_{ON}}{R_{ON} + R_L} = 5 \frac{1}{1+9} = 0.5 V$$

Therefore, need to design logic gates properly such that

$$V_{SS} \frac{R_{ON}}{R_{ON} + R_L} < V_T.$$

# Design of logic gates - Example

Assume the following values for the inverter circuit parameters:  $V_S = 5 V$ ,  $V_T = 1 V$ , and  $R_L = 10 k\Omega$ . Assume, further, that  $\frac{1}{k'_n V_{OV}} = 5$  for the MOSFET. Determine a  $\frac{W}{L}$  sizing for the MOSFET so that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter.

**Solution:**

$$\begin{aligned}V_S \frac{R_{ON}}{R_{ON} + R_L} &< V_T \\ \Rightarrow 5 \frac{R_{ON}}{R_{ON} + 10} &< 1 \\ \Rightarrow 5R_{ON} &< R_{ON} + 10 \\ \Rightarrow R_{ON} &< \frac{10}{4} = 2.5\end{aligned}$$

Now,

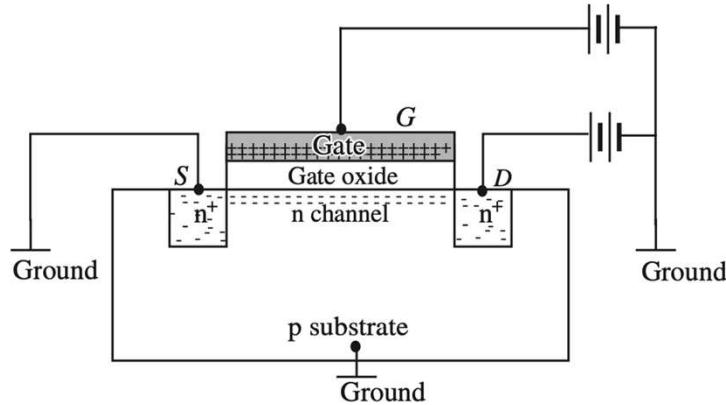
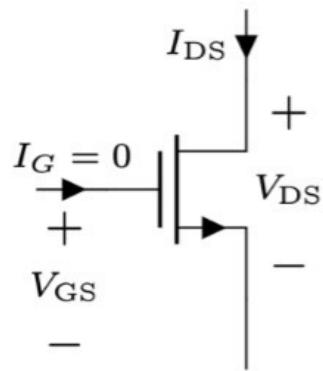
$$R_{ON} = \frac{1}{k'_n \frac{W}{L} V_{OV}} = 5 \times \frac{1}{W/L}$$

Hence

$$\frac{5}{W/L} < 2.5 \Rightarrow \frac{W}{L} > \frac{5}{2.5}$$

$$\Rightarrow \frac{W}{L} > 2$$

# Review – MOSFET



Control =  $V_{GS} = V_G - V_S$ , controls the IV between drain-source ( $I_{DS}$  vs  $V_{DS}$ )

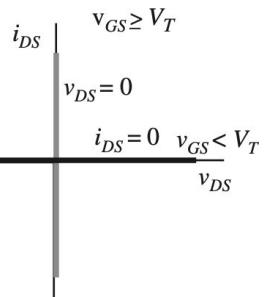
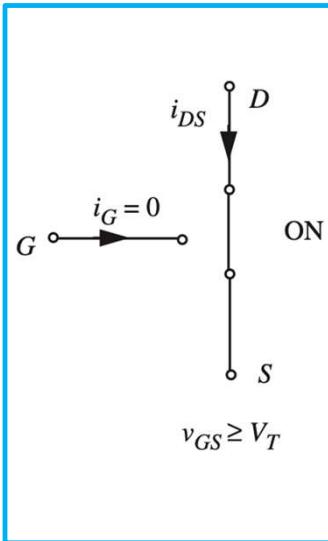
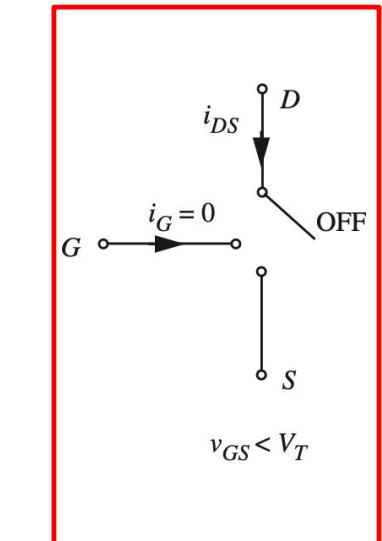
Threshold voltage =  $V_T$ , minimum voltage required to create the channel

## Models

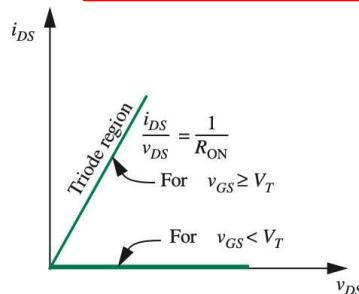
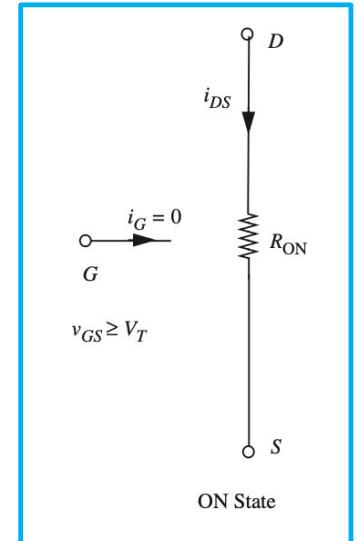
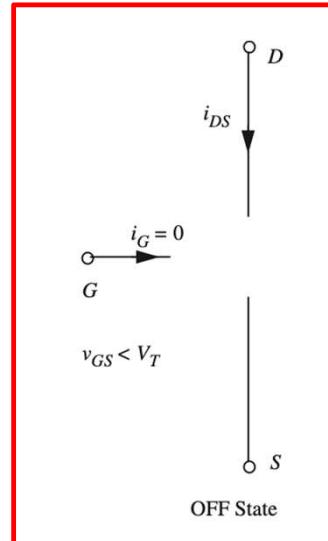
1. **S Mode:** Assumes an ideal channel with zero resistance
2. **SR Model:** Assumes finite channel resistance,  $R_{ON}$ , depends on  $V_{GS} - V_T = V_{OV}$

# MOSFET Linear Models

S Model



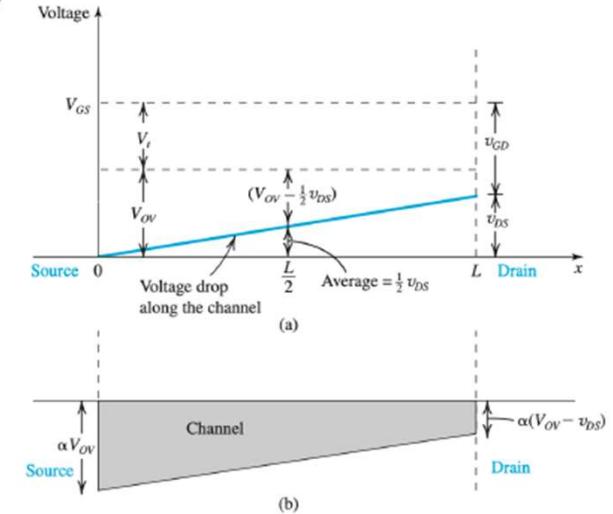
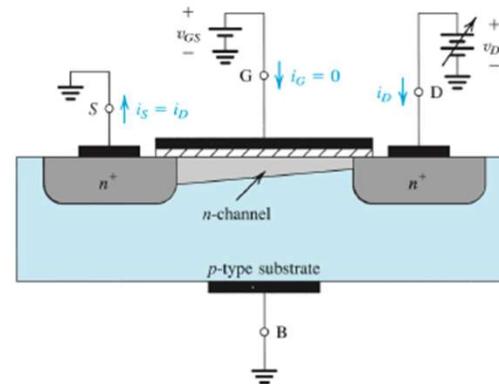
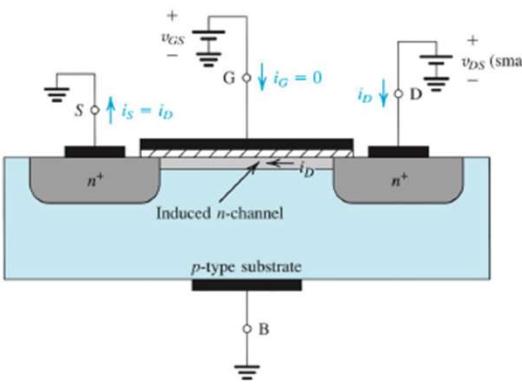
SR Model



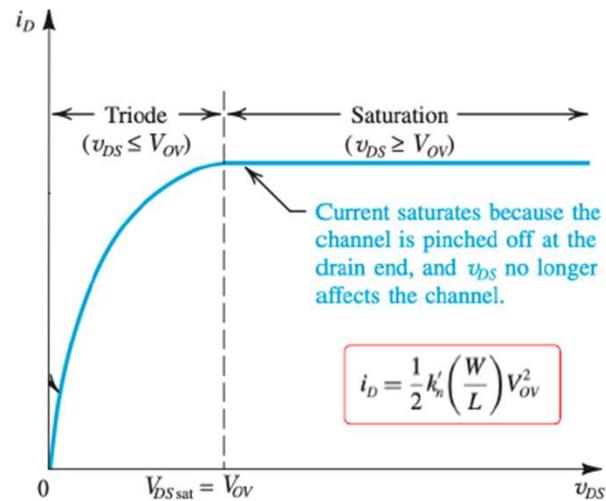
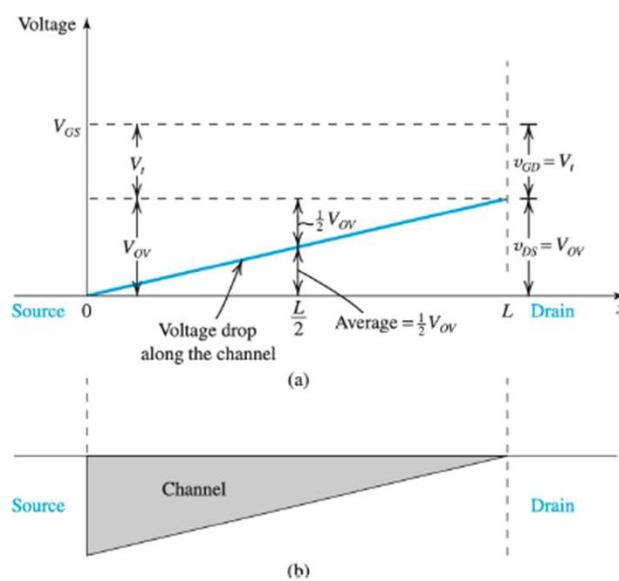
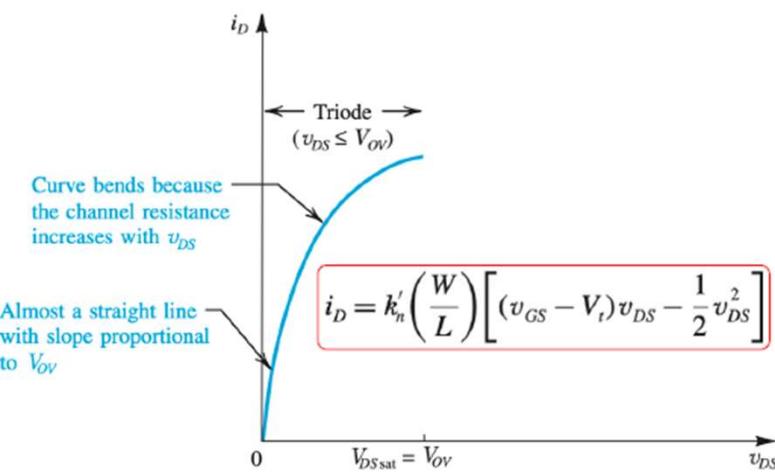
$$R_{ON} = \frac{1}{k_n^* \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{kV_{0V}}$$

# Real MOSFET

- Why  $R_{ON} = \frac{1}{k' \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{kV_{OV}}$ ? Because channel width  $\propto V_{OV}$ , and  $R \propto \frac{1}{\text{width}}$
- For small  $V_{DS}$ , uniform channel, hence fixed  $R_{ON}$ , therefore SR model valid.
- As  $V_{DS}$  is increased, channel becomes tapered cause  $V_{GD} \downarrow$ . Resistance  $\uparrow$ , slope  $\downarrow$ .
- This mode is called the **triode mode**. Condition:  $V_{DS} < V_{OV}$

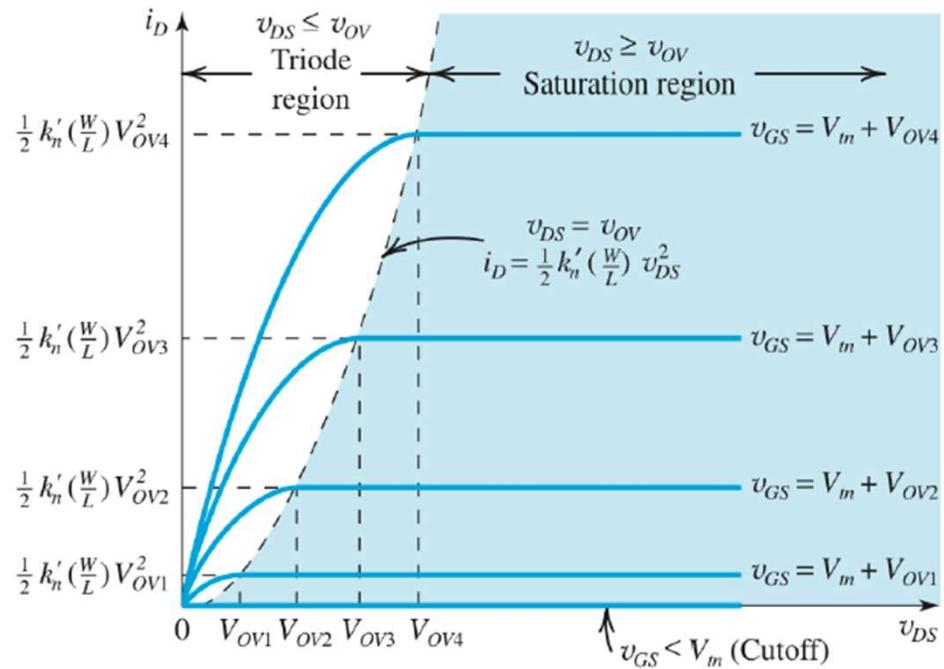


# Real MOSFET



- When  $V_{DS} = V_{OV}$ , channel pinches off.
- Increasing  $V_{DS}$  further have no effect on channel shape. Hence, current saturates
- This mode is called the **saturation mode**. Condition:  $V_{DS} \geq V_{OV}$
- Behaves like a current source (constant current) that depends on  $V_{OV}$

# IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \geq V_T$ $V_{DS} < V_{OV}$	$I_D = k [V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2]$
Saturation	$V_{GS} \geq V_T$ $V_{DS} \geq V_{OV}$	$I_D = \frac{k}{2} V_{OV}^2$

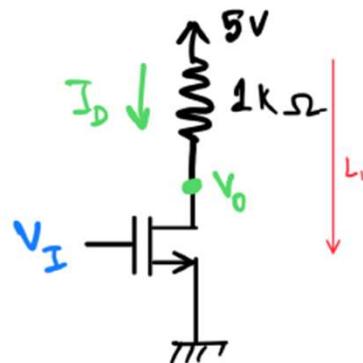
$$V_{OV} = V_{GS} - V_T$$

$$k = k'_n \left(\frac{W}{L}\right)$$

# Solving Circuits with MOSFET

- Use **Method of Assumed State!**
- Three steps:
  - **Assume:** One of the modes (Cutoff, Triode, Saturation)
  - **Solve:** Use corresponding equation and KCL+KVL
  - **Verify:** Check if the conditions of  $V_{GS}$  and  $V_{DS}$  are satisfied. If not, repeat.
- Might need to solve quadratic equation ( $ax^2 + bx + c = 0$ ).
- If we get two roots, choose the one that's *favorable* to your assumption

# Example 1



The MOSFET is specified as  $V_T = 1V$  and  $k = 0.5 \text{ mA/V}^2$ . Find  $I_D$  and  $V_O$  for  $V_I = 2V$ .

## Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2:  $I_D = \frac{k}{2} V_{OV}^2$  Here,  $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 2V$   
Therefore,  $V_{OV} = V_{GS} - V_T = 2 - 1 = 1V$

$$\therefore I_D = \frac{0.5}{2} (1)^2 = 0.25 \text{ mA}$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_O$$

$$\text{KVL along } L_1: I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega$$

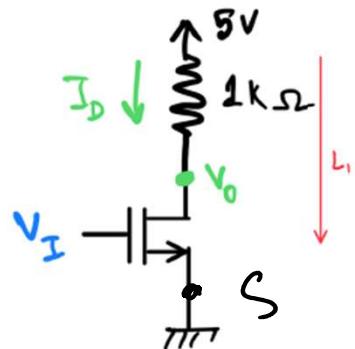
$$\Rightarrow V_o = 5 - 0.25 \times 1 = 4.75 \text{ V} = V_{DS}$$

Step 3:  $V_{GS} = 2V > V_T \checkmark$  Therefore, **assumption correct!**

$$V_{DS} = 1V > V_{OV} \checkmark$$

Correct ans:  $I_D = 0.25 \text{ mA}, V_o = 4.75 \text{ V}$

## Example 2



The MOSFET is specified as  $V_T = 1V$  and  $k = 0.5 \text{ mA/V}^2$ . Find  $I_D$  and  $V_o$  for  $V_I = 5V$ .

### Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2:  $I_D = \frac{k}{2} V_{OV}^2$  Here,  $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$   
Therefore,  $V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$

$$\therefore I_D = \frac{0.5}{2} (4)^2 = 4 \text{ mA}$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$$

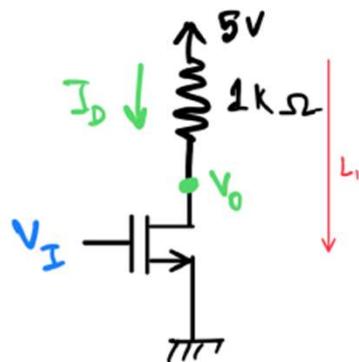
$$\text{KVL along } L_1: I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega$$

$$\Rightarrow V_o = 5 - 4 \times 1 = 1 \text{ V} = V_{DS}$$

Step 3:  $V_{GS} = 5V > V_T \checkmark$  Therefore, **assumption wrong!**

$$V_{DS} = 1V \not> V_{OV} \times$$

## Example 2



The MOSFET is specified as  $V_T = 1V$  and  $k = 0.5 \text{ mA/V}^2$ . Find  $I_D$  and  $V_o$  for  $V_I = 5V$ .

### Repeat:

Step 1: Assume the MOSFET in **triode**

$$\text{Step 2: } I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$$

$$\text{Therefore, } V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o. \text{ Assuming } V_{DS} = x$$

$$\text{KVL along } L_1: I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow I_D = \frac{5-V_{DS}}{1} = 5 - x$$

$$\therefore I_D = 0.5 \left[ 4 \times V_{DS} - \frac{1}{2}V_{DS}^2 \right] \Rightarrow (5 - x) = 0.5 \left[ 4x - \frac{1}{2}x^2 \right]$$

$$\Rightarrow 5 - x = 2x - 0.25x^2 \Rightarrow 0.25x^2 - 3x + 5 = 0$$

$$\text{Solving, } x = 2V, x = 10V$$

Since  $V_{DS} = x$  is small in triode, smaller value of  $x$  is favorable

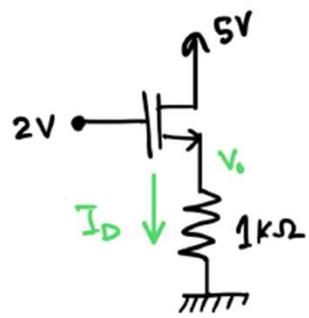
$$\text{Therefore, } V_o = V_{DS} = x = 2V, \text{ and } I_D = 5 - x = 3 \text{ mA}$$

Step 3:  $V_{GS} = 5V > V_T$  ✓ Therefore, **assumption correct!**

$$V_{DS} = 2V < V_{OV}$$

Correct ans:  $I_D = 3 \text{ mA}, V_o = 2V$

# Example 3



The MOSFET is specified as  $V_T = 1V$  and  $k = 4 \text{ mA/V}^2$ .

Find  $I_D$  and  $V_o$

**Solution:**

Step 1: Assume the MOSFET in **saturation**

$$\text{Step 2: } I_D = \frac{k}{2} V_{ov}^2$$

Let's assume  $V_0 = V_S = x$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - V_0 = 2 - x$$

$$\text{Therefore, } V_{ov} = V_{GS} - V_T = (2 - x) - 1 = 1 - x$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - V_0 = 5 - x$$

$$\text{Ohm's law for the resistor: } I_D = \frac{V_0 - 0}{1k\Omega} = x$$

$$\therefore x = \frac{4}{2}(1 - x)^2 \Rightarrow x = 2(1 - 2x + x^2) \Rightarrow x = 2 - 4x + 2x^2 \\ \Rightarrow 2x^2 - 5x + 2 = 0$$

$$\text{Solving, } x = 0.5, x = 2$$

Since  $V_{DS} = 5 - x$  is large in saturation  
smaller value of  $x$  is favorable

$$\therefore V_o = V_S = x = 0.5V, I_D = x = 0.5 \text{ mA}, \\ V_{DS} = 5 - x = 4.5V, V_{GS} = 2 - x = 1.5V, \text{ and } V_{ov} = 1 - x = 0.5V$$

Step 3:  $V_{GS} = 1.5V > V_T \checkmark$  Therefore, **assumption correct!**

$V_{DS} = 4.5V > V_{ov} \checkmark$  Correct ans:  $I_D = 0.5 \text{ mA}$ ,  $V_o = 0.5 V$

# Practice

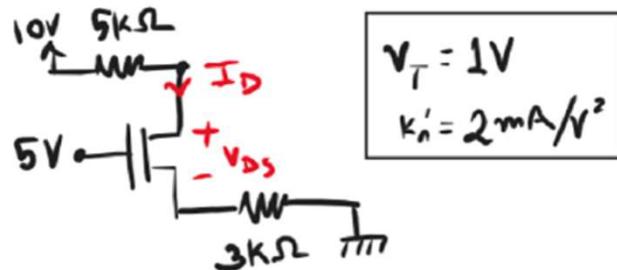
## Question 4 [CO1, CO4]

10

Analyze the following circuit to find the values of  $I_D$  and  $V_{DS}$  using the Method of Assumed State. You must validate your assumptions.

[7 + 3]

Hint: Use  $I_D$  as unknown  $x$ . Use Ohm's law to represent  $V_D$  and  $V_S$  in terms of  $x$ .



### Hint Explanation

Assume  $I_D = x$ . For  $5k\Omega$ :  $I_D = \frac{10 - V_D}{5} \Rightarrow V_D = 10 - 5x$ .

For  $3k\Omega$ :  $I_D = \frac{V_S - 0}{3} \Rightarrow V_S = 3x$ .

Therefore,  $V_{GS} = V_G - V_S = 5 - 3x$ , and  $V_{OV} = V_{GS} - V_T = (5 - 3x) - 1$

Also,  $V_{DS} = V_D - V_S = (10 - 5x) - 3x = 10 - 8x$

Now if you assume saturation:

$$I_D = \frac{k}{2} V_{OV}^2 \Rightarrow x = \frac{2}{2} (4 - 3x)^2$$

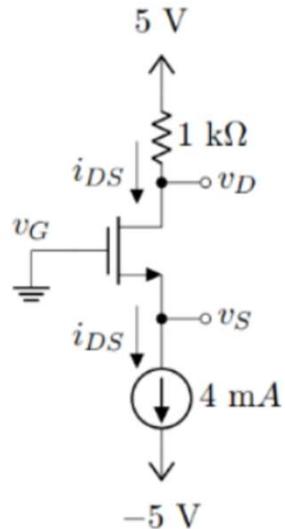
And if you assume triode:

$$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\Rightarrow x = 2[(4 - 3x)(10 - 8x) - 0.5 \times (10 - 8x)^2]$$

Solve for  $x$ , take the \_\_\_\_\_ root

## Question 5



Circuit 1

Refer to the **Circuit** above. For the MOSFET,  $V_T = 1$  V and  $k = k'_n \frac{W}{L} = 4$  mA/V<sup>2</sup>.

- Identify** the value of the gate voltage  $v_G$  and the drain-source current  $i_{DS}$ .
- Calculate** the value of the drain voltage  $v_D$  using the 1 kΩ resistor.
- Analyze** the circuit to find  $v_S$ . Here, **use** the Method of Assumed State. You must **validate** your assumptions. [Hint: assume  $v_S = x$ ]

a)  $V_G = 0$ ,  $I_{DS} = 4mA$

b)  $I_{DS} = \frac{5 - V_D}{1k\Omega}$   
 $\Rightarrow 5 - V_D = 4mA \times 1k\Omega = 4V$

$$\therefore V_D = 5 - 4 = 1V$$

c) assuming saturation mode,

$$V_S = x, V_{SS} = V_G - V_S = 0 - x = -x$$

$$V_{PS} = V_D - V_S = 1 - x$$

$$V_{OV} = V_{GS} - V_t = -x - 1$$

$$\therefore I_{DS} = \frac{\kappa}{2} V_{OV}^2$$

$$\Rightarrow 4 = \frac{\kappa}{2} (-x - 1)^2$$

$$\Rightarrow 2 = (\kappa + 1)^2 \Rightarrow \kappa^2 + 2\kappa - 1 = 0$$

$$\therefore \kappa = 0.414, -2.414$$

If  $\kappa = 0.414 \rightarrow V_{DS} = 1 - \kappa = 0.586$

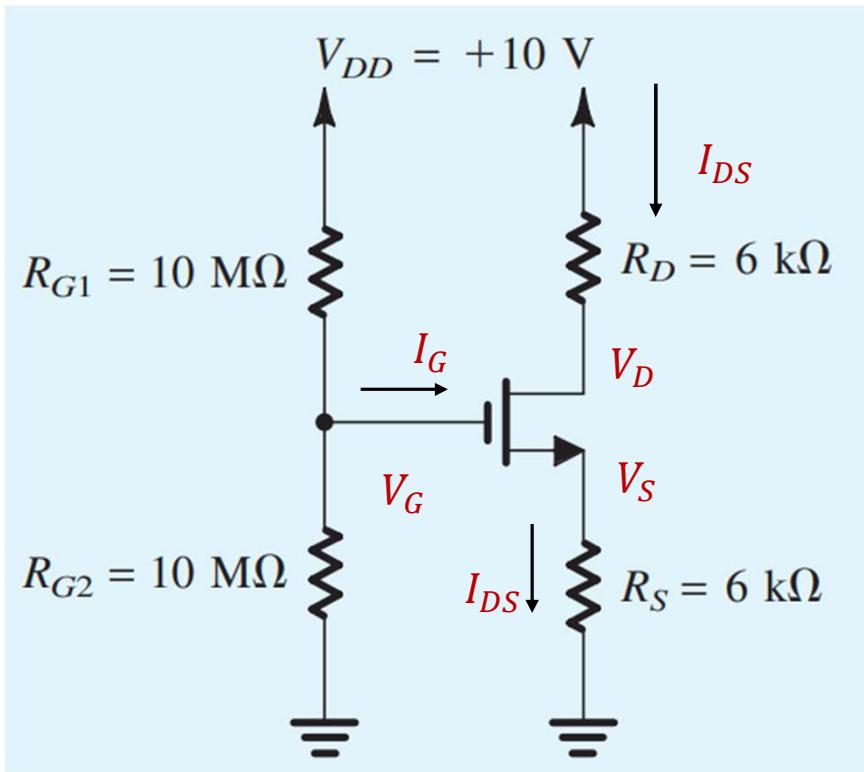
$$V_{OV} = -x - 1 = -1.414V$$

but if  $V_{OV} < 0$  MOSFET should be in cutoff mode

$\therefore \kappa \neq 0.414$ , when  $\kappa = -2.414, V_{DS} = 3.414V$

$$\therefore V_{DS} > V_{OV} \therefore \text{correct assumption } E: V_S = x = -2.414V$$

## Question 6



$$\boxed{\begin{aligned}V_T &= 1\text{V} \\k &= kn' \frac{W}{L} = 2 \text{ mA/V}^2\end{aligned}}$$

Analyze the circuit to find  $I_{DS}$  and  $V_D$  using Method of Assumed State. You must validate your assumptions.

## Solution Q6

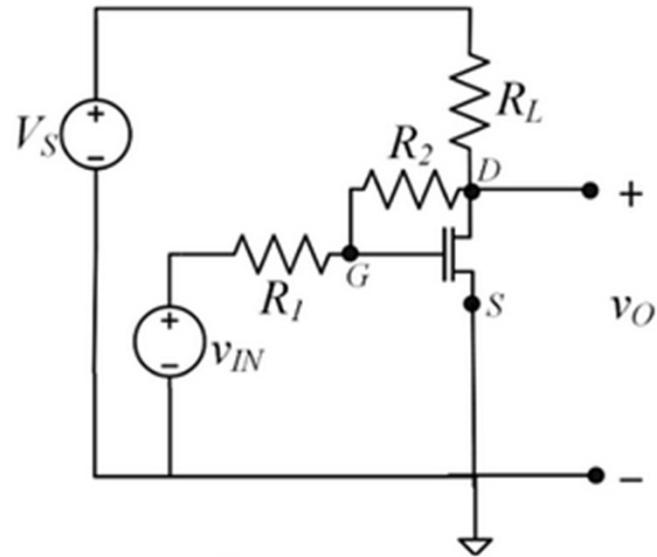
As gate current  $I_G = 0 \text{ mA}$ , gate voltage can be found by voltage divider rule,

$$V_G = \frac{R_{G2}}{R_{G2} + R_{G1}} \times V_{DD} = \frac{10 \text{ M}\Omega}{10\text{M}\Omega + 10\text{M}\Omega} \times 10 \text{ V} = 5\text{V}$$

Assume  $I_D = x$  and find  $V_D$ ,  $V_S$  in terms of  $x$  with Ohm's law.

Follow **question 4** for the remaining solution.

## Question 7



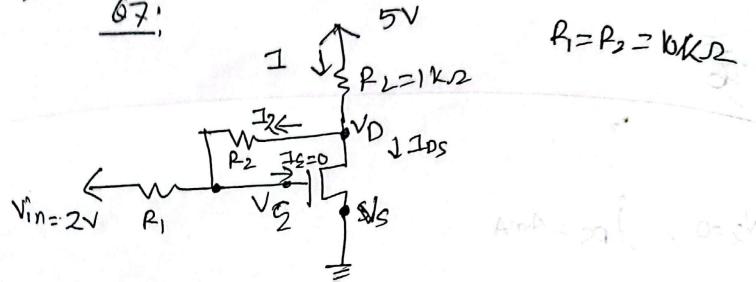
$$V_T = 1V$$

$$k = kn' \frac{W}{L} = 1 \text{ mA/V}^2$$

Analyze the circuit to find  $i_D$  and  $v_0$  using Method of Assumed States. You must validate your assumptions.

Assume,  $V_S = 5V$ ,  $V_{IN} = 2V$ ,  $R_1 = R_2 = 10 \text{ k}\Omega$  and  $R_L = 1 \text{ k}\Omega$

Q7:



$$R_1 = R_2 = 1 \text{ k}\Omega$$

gate current,  $I_G = 0$

so, nodal analysis at gate terminal,

$$\frac{V_G - 2}{R_1} + \frac{V_G - V_D}{R_2} = 0$$

$$\Rightarrow \frac{V_G - 2}{10} + \frac{V_G - V_D}{10} = 0$$

$$\therefore V_G = 1 + \frac{V_D}{2}$$

$$V_S = 0V$$

$$\therefore V_{ov} = V_{GS} - V_T = 1 + \frac{V_D}{2} - 1 = \frac{V_D}{2}$$

now, applying KCL at Drain (D) terminal,

$$I = I_2 + I_{DS}$$

$$\Rightarrow \frac{5 - V_D}{1 \text{ k}\Omega} = \frac{V_D - V_G}{R_2} + I_{DS}$$

$$\Rightarrow 5 - V_D = \frac{V_D}{10} - \frac{1}{10} \left( 1 + \frac{V_D}{2} \right) + I_{DS}$$

$$\therefore I_{DS} = 5.1 - 1.05 V_D$$

now, assuming saturation mode

$$I_{DS} = \frac{k}{2} V_{ov}^2$$

$$\Rightarrow 5.1 - 1.05 V_D = \frac{1}{2} \left( \frac{V_D}{2} \right)^2$$

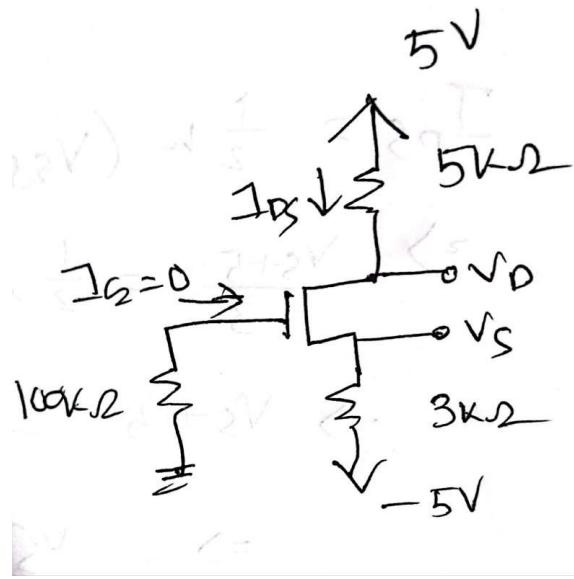
$$\therefore V_D = 3.44V, -11.84V$$

$$\text{if } V_D = 3.44V, \quad V_{ov} = \frac{V_D}{2} = 1.72V$$

$$\& V_{DS} = 3.44V$$

$\therefore V_{DS} > V_{ov}$   $\therefore$  assumption correct

## Question 8



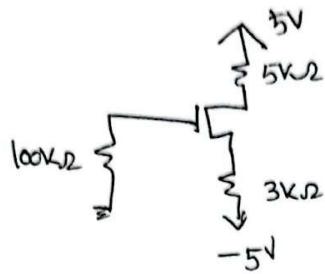
$$V_T = 1V$$

$$k = kn' \frac{W}{L} = 2 \text{ mA/V}^2$$

Analyze the following circuit to find the values of  $I_{DS}$  and  $V_{DS}$  ( $= V_D - V_S$ ) using the method of assumed states. You must validate your assumptions.

[Hint: Use  $I_{DS}$  as unknown  $x$ . Use Ohm's law to represent  $V_D$  and  $V_S$  in terms of  $x$ .]

## Solution Q8



$$V_G = 0V, V_T = 1V$$

$$I_{DS} = x$$

$$x = \frac{5 - V_D}{5}$$

$$\therefore V_D = 5 - 5x \quad \text{--- (1)}$$

$$x = \frac{V_S + 5}{3}$$

$$\therefore V_S = 3x - 5 \quad \text{--- (2)}$$

assume, saturation

$$I_{DS} = \frac{1}{2} \times x \times V_{DS}^2$$

$$\Rightarrow x = \frac{1}{2} \times 2 \times (-3x + 4)^2$$

$$\Rightarrow 9x^2 - 25x + 16 = 0$$

$$\therefore x = 1.778, 1V$$

If  $x = 1V$ ,  $\boxed{V_{DS} = 10 - 8 = 2V}$   
 $V_{DS} = -3.1 + 4 = 1V$

$$\therefore V_{DS} > V_{DS}$$

$\therefore$  correct assumption

$$\boxed{I_{DS} = \frac{1}{2} \times 2 \times 1^2 = 1mA}$$

## Question 9

In the circuit shown in the figure below, the transistor is characterized by  $V_T = 1 \text{ V}$ ,  $k = 1 \text{ mA/V}^2$ . (Hint: Identify the modes of the two MOSFET, and equate the two currents.)

- (a) [3 marks] Find the value of  $V_O$  indicated in the figure.
- (b) [3 marks] Find the values of  $I_{DS}$ ,  $I_{G1}$  and  $I_{G2}$ .

## Solution Q9

$$a) V_{G1} = V_{D1} = 3V$$

$$V_{S1} = V_{D2} = V_{G2} = V_0, V_{S2} = 0V$$

$$\text{Here, } I_{DS1} = I_{DS2}$$

$$\Rightarrow (V_{GS1} - VT)^2 = (V_{GS2} - VT)^2$$

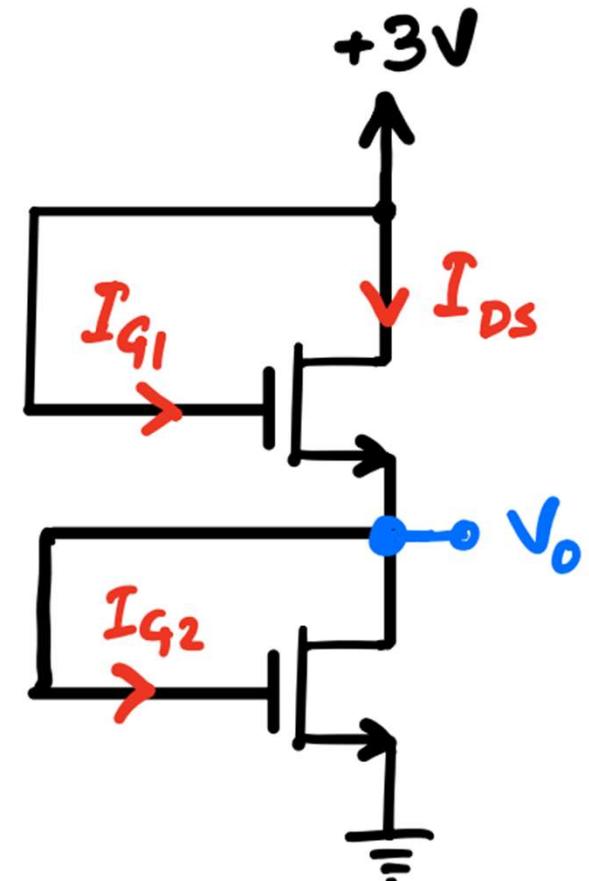
$$\Rightarrow (V_{G1} - V_{S1} - VT)^2 = (V_{G2} - V_{S2} - VT)^2$$

$$\Rightarrow (3 - V_0 - 1)^2 = (V_0 - 0 - 1)^2$$

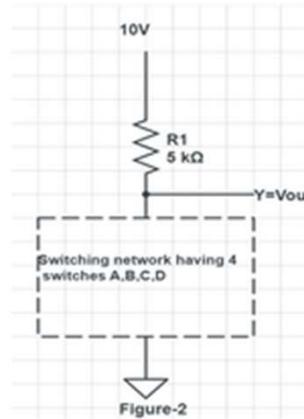
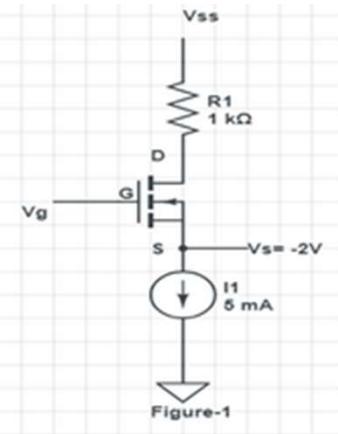
$$\Rightarrow 4 - 4V_0 = -2V_0 + 1$$

$$\Rightarrow V_0 = 3/2 = 1.5 \text{ V}$$

$$I_{DS} = I_{DS2} = k/2 * (V_{GS2} - VT)^2 = 1/2 * (1.5 - 1)^2 = 0.125 \text{ mA}$$



## Question 10



- a) For the MOSFET in Figure-1,  $V_T = 1\text{ V}$  and  $k_n' = 2\text{ mA/V}^2$ . Assume that the MOSFET is in Saturation mode. Determine the gate voltage,  $V_g$  and the minimum supply voltage,  $V_{ss}$  to operate the device in this condition. [Hint:  $V_{OV} = V_{DS}$ ] [3+2]

- b) In Figure-2, the MOSFET switching network turns ON the following conditions MUST be fulfilled -
- 'A' MUST be ON
  - 'B' and 'C' MUST be ON or 'D' MUST be ON

Deduce the logic function, F, using Boolean variables A, B, C, and D to implement these conditions. [2]

- c) Assume, only A and D switches are ON in the switching network of Figure-2. Find out the output voltage,  $V_{out}$ . Let,  $R_{ON} = 0.1\text{ k}\Omega$  and use the SR model. [3]

- d) [BONUS] In Figure-2, assume the input on a NOT gate is connected to  $V_{out}$ . Explain mathematically whether it will be possible to turn OFF the NOT gate when  $V_{out}$  is LOW. Assume,  $V_T = 0.5\text{ V}$ ,  $V_{out} = V_{out(LOW)}$  of 'part-b'. [2]

## Solution Q10

a) see part

$$I_{DS} = \frac{1}{2} k V_{DS}^2$$

$$\Rightarrow 5 = \frac{1}{2} \times 2 \times V_{DS}^2$$

$$\Rightarrow V_{DS} = \sqrt{5}$$

$$\therefore V_{GS} - V_T = \sqrt{5}$$

$$\Rightarrow V_{GS} = \sqrt{5} + V_T = \sqrt{5} + 1 = 3.29$$

$$\therefore V_g - V_s = 3.29$$

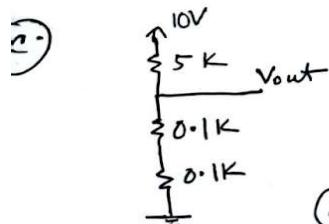
$$\Rightarrow V_g = 3.29 + V_s = 3.29 - 2$$

$$= 1.29 V$$

2nd part minimum  $V_{GS}$

$$\begin{aligned} \text{Given } V_{SS} &= 5 \times 1 + V_{DS} + V_s \\ &= 5 + \sqrt{5} - 2 \\ &\approx 5.29 V \end{aligned} \quad \left| \begin{array}{l} V_{DS} = V_{DS} = \sqrt{5} \\ V_s = V_{DS} = \sqrt{5} \end{array} \right.$$

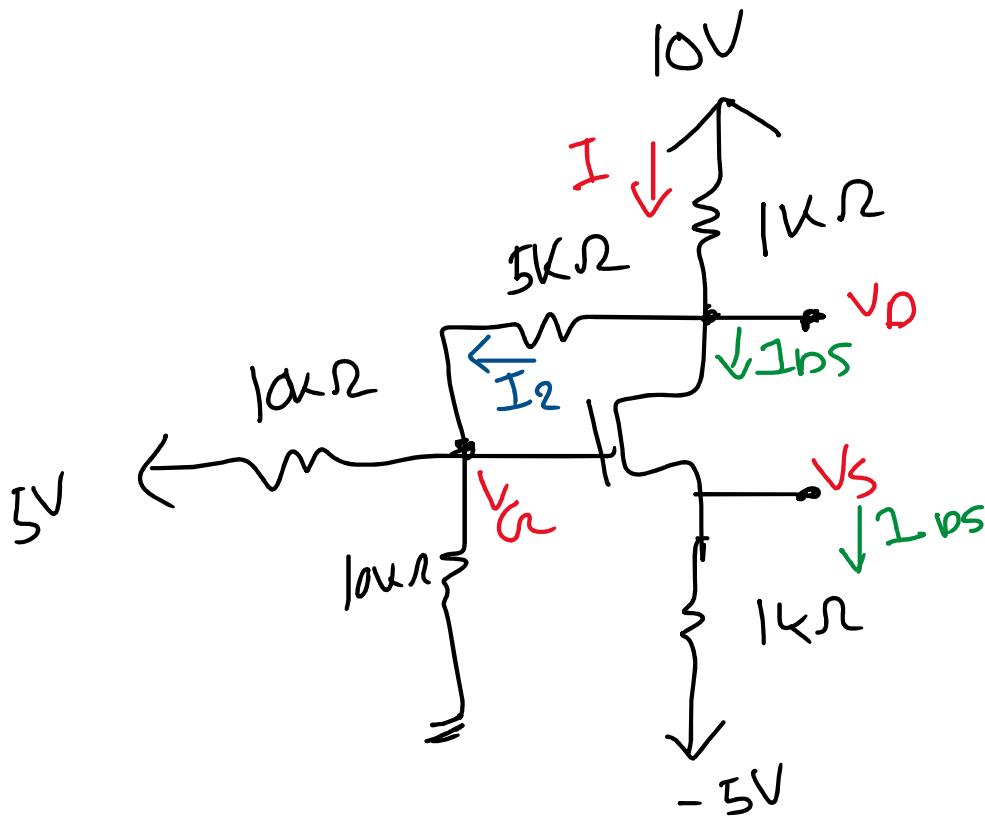
b)  $Y = \overline{A(Bc+D)}$



$$\begin{aligned} V_{out} &= 10 \times \frac{0.2}{5+0.2} \\ &= 0.385 V \end{aligned}$$

c)  $V_{out} < V_T$ , so possible to turn off

## Practice Yourself



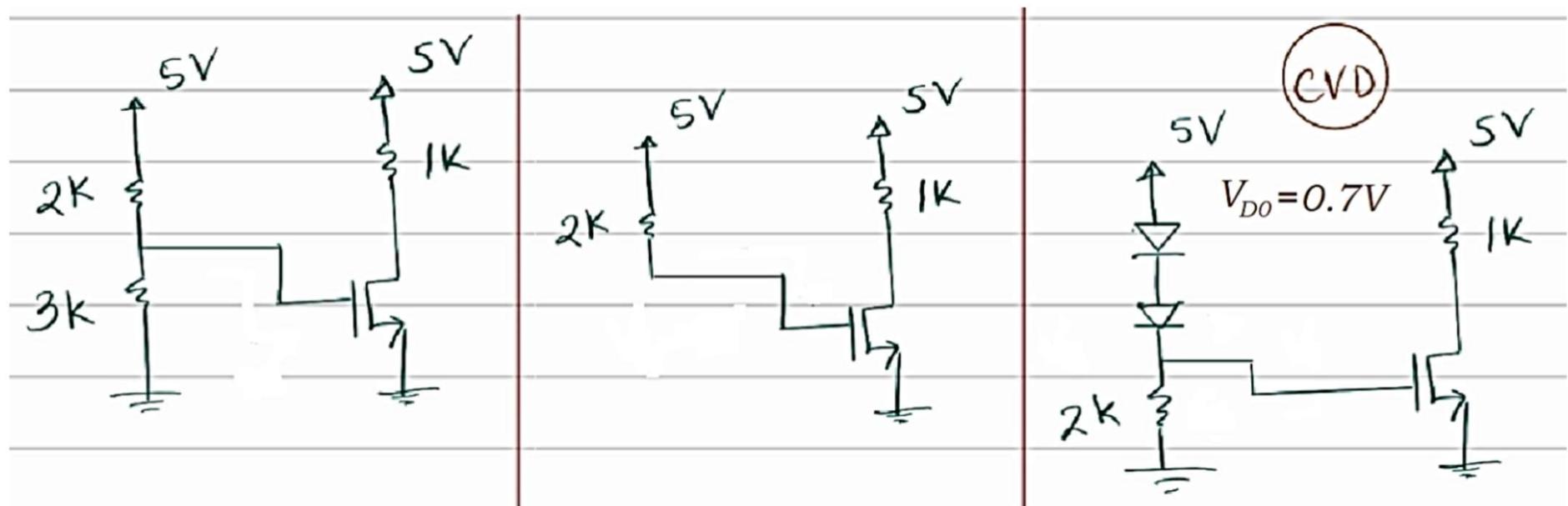
$$V_T = 1V$$

$$k = kn' \frac{W}{L} = 2 \text{ mA/V}^2$$

Analyze the following circuit to find the values of  $I_{DS}$  and  $V_D$  using the method of assumed states. You must validate your assumptions.

[Hint: Use  $I$  as unknown  $x$ . Use Ohm's law to represent  $V_D$  and  $V_S$  in terms of  $x$ . Using nodal analysis find relation between  $V_G$  and  $V_D$ , then represent also  $V_G$  in terms of  $x$ . Using KCL at drain terminal, represent  $I_{DS}$  in terms of  $x$ .]

Q3. For all three circuits below, you are given  $V_T = 1V$ ,  $K_n = 1 \text{ mA/V}^2$ . Determine which one of the three  $1k\Omega$  dissipates the most power? [20+15+30=65]



Thank You