BRAC University
Department of Computer Science and Engineering
Semester: **Summer 2024**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 40 minutes**
Date: **28th September 2024**

Set A

Student ID:	**Name:**	**Section:**

[Answer any **THREE** questions out of **FOUR**. Each question carries **15 marks**. Return the question paper with the answer script.]

1. (CO4) An initial cut for a partition of 8 circuit elements (**a, b, c, d, e, f, g**, and **h**) is given in **Figure 1**.

The cut line divides the circuit elements into two partitions named **A** and **B**.

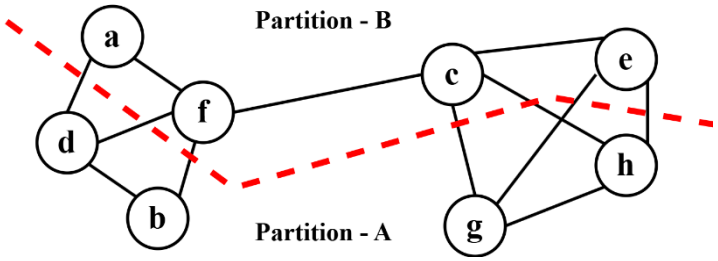


Figure 1

(a) **Calculate** the initial cut cost, and the cost of moving each node. **[1]**

(b) **Perform** the first pass of the algorithm. For every "**i**"th iteration inside the first pass, until all the nodes are swapped and fixed, do the following: **[9]**

i. Compute the node costs of all unfixed nodes
ii. Find the maximum gain of swapping a pair of nodes (Δg_i)
iii. Swap the pair and draw the updated graph

(c) **Compute** G_i of each iteration and find the maximum $G_i = G_m$. **Suggest** how many swaps should be actually executed in the first pass. Redraw the optimized graph. **[4]**

(d) Should you perform subsequent passes of the algorithm? Why or why not? **[1]**

2. (CO1) Brook is a chip designer who works specifically on the $\lambda = 1.5$ µm process. However, he has messed up the layout design of a **3-input NOR gate** (Figure 2(a)) because of which, the NOR gate has **an equivalent rise resistance that is four times its equivalent fall resistance.** Also, the NOR gate's **equivalent rise resistance is twice the rise resistance of a unit inverter** for that design process. But at least he made sure to keep the source-drain terminals shared where possible to reduce capacitance. The gate capacitance and parasitic (diffusion) capacitance of are **0.5 fF/µm.**

This **NOR gate** is loaded with a **Unit inverter** and the output node **Y** has a voltage waveform as shown in Fig. 2(c).

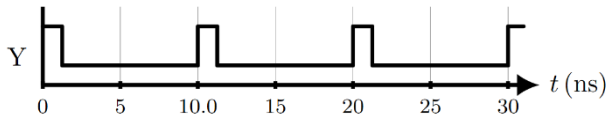


Figure 2(c): Voltage waveform at node **Y**

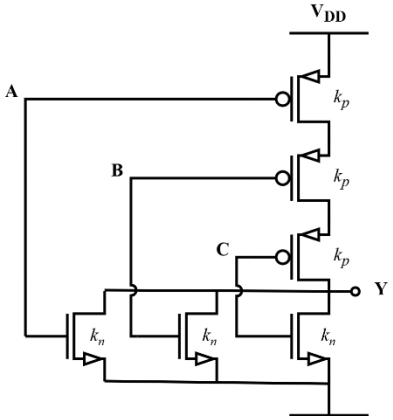


Figure 2(a): CMOS implementation of a 3 - input NOR gate

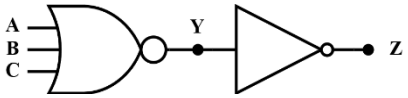


Figure 2(b): A 3-input NOR gate loaded with a **Unit Inverter**

(a) **Find** the value of width scaling factors - k_p and k_n of the NOR gate designed by Brook. Thereafter, calculate the actual width of the **pMOS** and **nMOS**. **[2]**

(b) **Draw** the RC equivalent model of the above 3-input NOR gate. Lump the capacitances together where possible. **[5]**

(c) **Find** the capacitance of the **Y** node (in **fF** units), when it is loaded with a unit inverter, as shown in Fig. 2(b). **[2]**

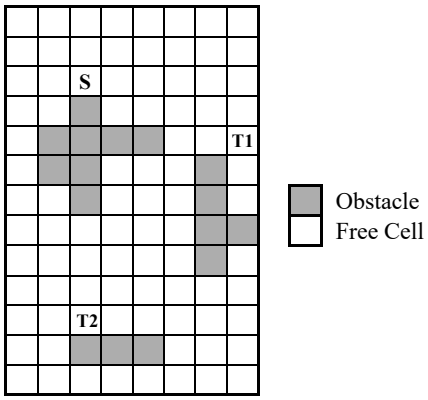
(d) Find the worst-case falling edge **propagation delay** (t_{pdf}) of **Y**-node in terms of **R** and **C** - the equivalent resistance and capacitance of a unit sized MOS. [**Hint:** You do not need Elmore modelling.] **[2]**

(e) **Find** the switching power of the **Y**-node, if the system has a supply voltage of **5 V**. **[3]**

3. (CO4) For question (a) you are given a certain **chip planning task.** You have three blocks with the following widths and heights:

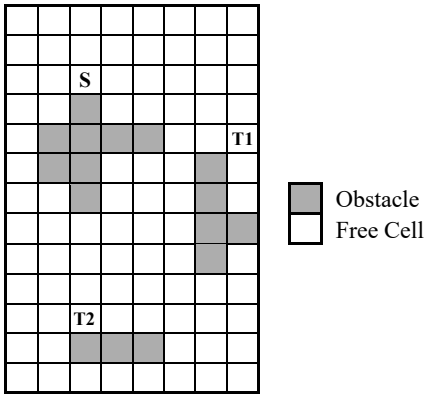
Block A: $w = 2, h = 3$ or $w = 3, h = 2$
Block B: $w = 1, h = 2$ or $w = 2, h = 1$
Block C: $w = 1, h = 4$ or $w = 4, h = 1$

For questions (b-e) refer to the adjacent figures on the right of the paper, you can see the grid layout of a system with a source (**S**) and two targets – **T1** and **T2.** The obstacles and free cells are shown.



(a) **Define** chip planning. **Find** and draw a floorplan with the minimum total area enclosed by its global bounding box. **[3]**

(b) Using the Lee's Maze Algorithm, **find** the shortest path from **S** to **T1** and **T2** *allowing minimum bends*. **[4]**
Answer this question on the grids on the question paper.

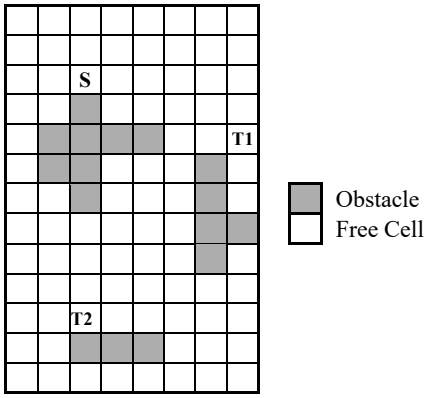


(c) **Find** the total memory usage of the given grid if the sequence is a series of natural numbers. **[3]**

(d) If the maximum memory requirement of the provided grid is **36 bytes**, **calculate** the maximum number of bits that each cell can hold. **[3]**

(e) **Find** the number of consecutive and unique numbers (starting from 1) that can be used for wave propagation in the Lee's Maze algorithm, for the given memory constraint. **[2]**

What should be a full sequence for wave propagation?



4. (CO1) Suppose the technology you are using to design a VLSI system has $\boldsymbol{\lambda} = 80$ nm, a clock frequency of **5 MHz**, and a supply is **5 V**. The chip you are designing has **5 million transistors**, of which 1 million remain **active** at any given time. The activity factor is defined by the fraction of total components which remain active. The gate and diffusion capacitances are 12 fF/μm and 5 fF/μm, respectively for all the 5 million transistors. The gate width is **20λ**. You also obtain the following power consumption data:

- Short circuit power = 0.5 W
- Leakage power = 0.01 W
- Subthreshold power = 0.02 W

The **acceptable TOTAL power consumption** of a chip is **3 W.**

(a) **Find** the activity factor and load capacitance of the system described above. **[2]**

(b) **Calculate** the switching power consumption of the chip. **[3]**

(c) **Calculate** the dynamic and static power of the chip. Thereafter calculate the **TOTAL** power consumption. **[3]**

(d) Is the **TOTAL** power consumption within the acceptable range? If not, **find** the maximum clock frequency to keep the **TOTAL** power within the acceptable range? **[4]**

(e) For a **10-input NAND gate**, what should be the ratio of width scaling factors – $\boldsymbol{k_p/k_n}$ - for the NMOS and PMOS to keep the rise and fall resistances equal? **[3]**

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[Answer any **THREE** questions out of **FOUR**. Each question carries **15 marks**. Return the question paper with the answer script.]

1. (CO4) An initial cut for a partition of 8 circuit elements (**a, b, c, d, e, f, g**, and **h**) is given in **Figure 1**.

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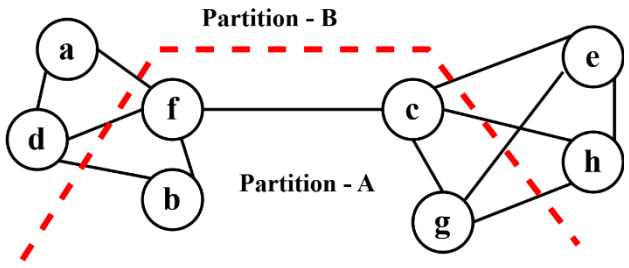

Figure 1

(a) **Calculate** the initial cut cost, and the cost of moving each node. **[1]**

(b) **Perform** the first pass of the algorithm. For every "**i**"th iteration inside the first pass, until all the nodes are swapped and fixed, do the following: **[9]**

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(c) **Compute** G_i of each iteration and find the maximum $G_i = G_m$. **Suggest** how many swaps should be actually executed in the first pass. Redraw the optimized graph. **[4]**

(d) Should you perform subsequent passes of the algorithm? Why or why not? **[1]**

2. (CO1) Bob is a chip designer who works specifically on the $\lambda = 0.25$ µm process. However, he has messed up the layout design of a **3-input NAND gate** (Figure 2(a)) because of which, the NAND gate has **an equivalent rise resistance that is four times its equivalent fall resistance.** Also, the NAND gate's **equivalent rise resistance is 1.5 the rise resistance of a unit inverter** for that design process. But at least he made sure to keep the source-drain terminals shared where possible to reduce capacitance. The gate capacitance and parasitic (diffusion) capacitance of are **2.42 fF/µm.**

This **NOR gate** is loaded with a **Unit inverter** and the output node **Y** has a voltage waveform as shown in Fig. 2(c).

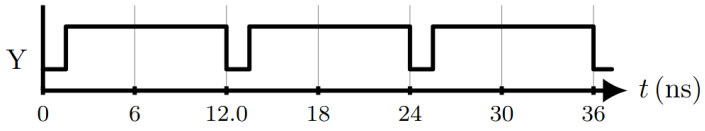
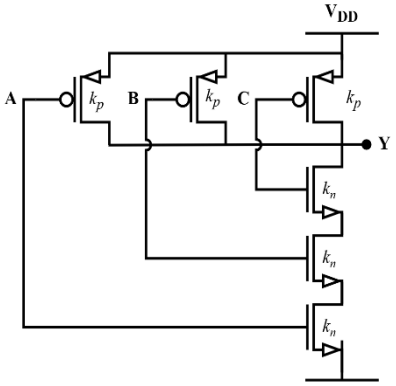


Figure 2(c): Voltage waveform at node **Y**



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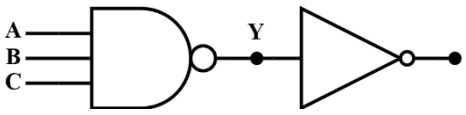

Figure 2(b): A 3-input NAND gate loaded with a **Unit Inverter**

(a) **Find** the value of width scaling factors - k_p and k_n of the NOR gate designed by Bob. Thereafter, calculate the actual width of the **pMOS** and **nMOS**. **[2]**

(b) **Draw** the RC equivalent model of the above 3-input NAND gate. Lump the capacitances together where possible. **[5]**

(c) **Find** the capacitance of the **Y** node (in **fF** units), when it is loaded with a unit inverter, as shown in Fig. 2(b). **[2]**

(d) Find the worst-case rising edge **propagation delay (t_{pdr})** of **Y**-node in terms of **R** and **C** - the equivalent resistance and capacitance of a unit sized MOS. [**Hint:** You do not need Elmore modelling.] **[2]**

(e) **Find** the switching power of the **Y**-node, if the system has a supply voltage of **3.3 V**. **[3]**

3. (CO4) For question (a) you are given a certain **chip planning task.** You have three blocks with the following widths and heights:

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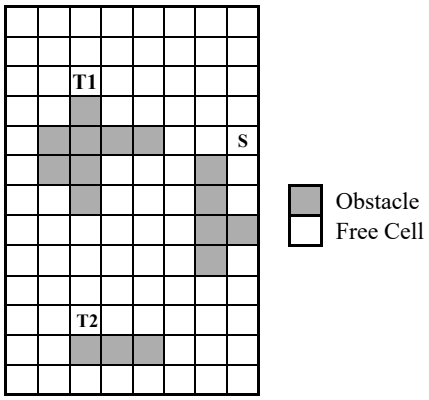

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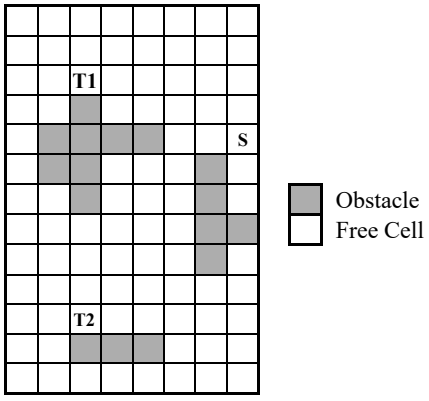

(c) **Find** the total memory usage of the given grid if the sequence is a series of natural numbers. **[3]**

(d) If the maximum memory requirement of the provided grid is **24 bytes**, **calculate** the maximum number of bits that each cell can hold. **[3]**

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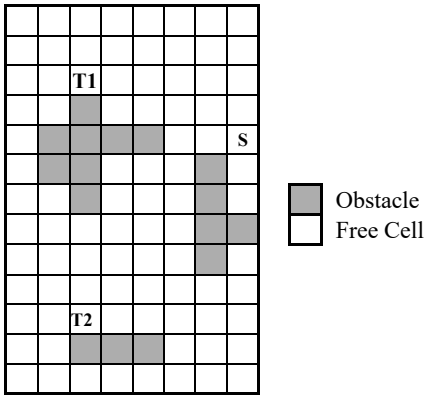
What should be a full sequence for wave propagation?



4. (CO1) Suppose the technology you are using to design a VLSI system has $\boldsymbol{\lambda} = 40$ nm, a clock frequency of **2.5 MHz**, and a supply is **5 V**. The chip you are designing has **10 million transistors**, of which 4 million remain **active** at any given time. The activity factor is defined by the fraction of total components which remain active. The gate and diffusion capacitances are 12 fF/μm and 5 fF/μm, respectively for all the 10 million transistors. The gate width is **20λ**. You also obtain the following power consumption data:

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