BRAC University
Department of Computer Science and Engineering

Semester: **Fall 2023**
Course Code: **CSE460**
Course Title: **VLSI Design**

Final Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **15th Dec 2023**

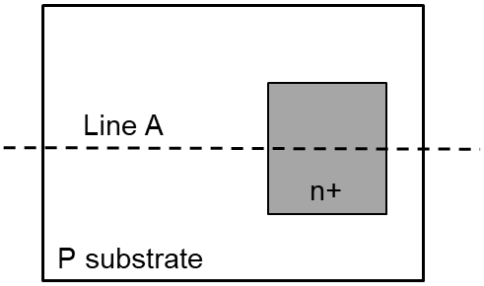
Set B

Student ID:	Name:	Section:

[Answer **both questions 1 and 2**. You can answer any **one** question from **questions 3 and 4**. In total, you need to answer **three** questions out of **four**.]

[Each question carries equal marks.]

[After the exam, *the question paper should be turned in along with the answer script.*]

1. (CO3)	**(a)**	Consider a CMOS compound gate that implements the following function: $Y = \overline{AB + C + D}$		
		(i)	**Draw** the stick diagram of the given CMOS gate.	**7**
		(ii)	**Find** the total area of the stick diagram in **(i)** in terms of Lambda (λ).	**3**
	(b)	Observe **Figure 1** and answer the following questions.  **Figure 1:** Top view of a wafer after fabricating an n+ diffusion region (dark region)		
		(i)	Briefly **explain** why n-well is required in CMOS fabrication.	**3**
		(ii)	**Draw** the cross-sectional view of **Figure 1** along 'Line A' and **label** the different regions.	**2**

2. (CO1) Consider the following truth tables for two logic gates

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

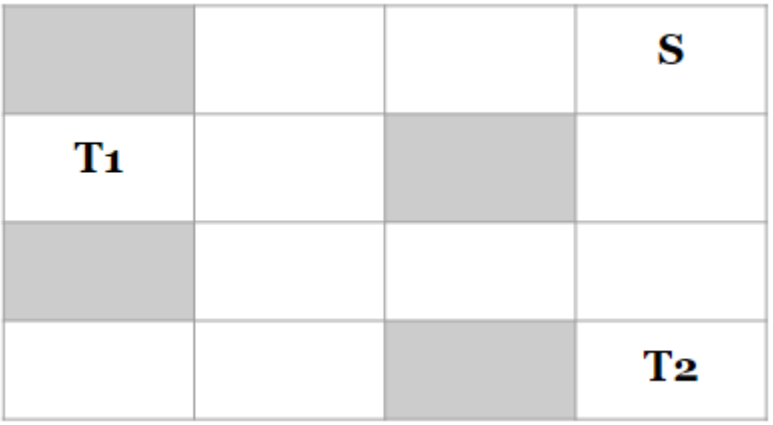
Gate 1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Gate 2

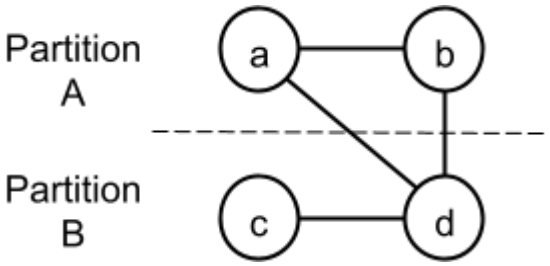
(a)	**Identify** the logic gates and draw their CMOS circuit representation.	**2**
(b)	**Determine** the individual transistor widths k_{nMOS} and k_{pMOS} for both of the gates to achieve the effective rise and fall resistances equal to that of a unit inverter, **R**, in the worst case.	**2**
(c)	**Draw** the simplified RC circuit only for **Gate 1** and **determine** the input capacitance of **Gate 2** in terms of **C**	**4+1**
(d)	Consider **Gate 1** is driving **12** identical **Gate 2** circuits (only one of the inputs of each). Now **derive** the expressions for t_{pdr} and t_{cdr} by **sketching** the corresponding RC networks from **(c)**.	**6**

3. (CO4) For the 4 × 4 maze below, the dark regions are obstacles or components.



The total memory requirements for the maze is **4 bytes**.

(a)	**Calculate** the number of bits per cell (n) and the maximum value that a cell can store (L) as per the memory requirements	**2+1**

	(b)	**State** the sequence for wave propagation as per the memory requirements. Perform wave propagation to find the shortest path from source, **S** to both of the targets, $\mathbf{T_1}$ and $\mathbf{T_2}$	**2+6**
	(c)	**Show** the shortest path for each of the targets.	**4**
4. (CO4)	The graph below (nodes a-d) can be optimally partitioned using the **Kernighan-L**in algorithm. The dotted line represents the initial partitioning. Assume all the edges have the same weight.  		
	(a)	**Calculate** the initial cut cost.	**2**
	(b)	**Identify** how many iterations are needed in a single pass?	**2**
	(c)	**Perform** the first pass of the algorithm and **determine** the new cut cost of the optimum output of the first pass. [Hint: For the "i"th iteration of the first pass, until all the nodes are swapped and fixed, do the following: ● Compute the node costs of all unfixed nodes ● Find the maximum gain of swapping a pair of nodes (Δg_i) ● Swap the pair and draw the updated graph ● Calculate cumulative gain, G_i]	**9**
	(d)	Should you perform subsequent passes of the algorithm? Why or why not?	**2**