BRAC University

Department of Computer Science and Engineering

Semester: **Summer 2022**
Course Code: **CSE460**
Course Title: **VLSI Design**

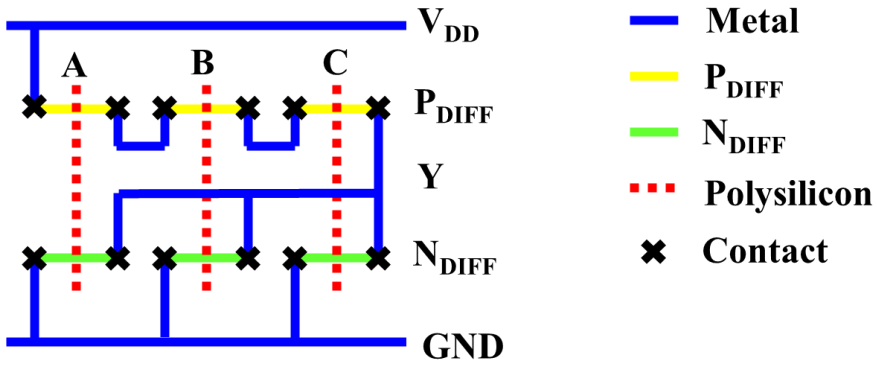
Midterm Exam
Full Marks: **15 x 3 = 45**
Time: **1 hour 30 minutes**
Date: **27th July 2022**

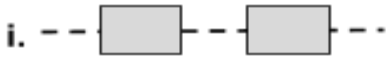
Set B

Student ID:	Name:	Section:

[Answer any **THREE** questions out of **FOUR**. Each question carries equal marks.]

[After the exam, the question paper should be turned in along with the answer script.]

1. (CO2)	**(a)**	**Sketch** the transistor level schematic of the boolean logic function $F = \overline{A \cdot B + C}$	**3**
	(b)	From the schematic in part-a, **design** a stick diagram for the given logic function.	**7**
	(c)	A designer has created the stick diagram for a 3-input NOR gate. After a close inspection you see that the design is *not* area efficient and can be *further optimized*:  **Draw** the *optimized* stick diagram for this circuit.	**5**
2. (CO1)	In a CMOS fabrication process, two <u>p-diffusion</u> regions are required on the wafer. A VLSI engineer has designed a mask arrangement [figure 1(i)] to fabricate the desired pattern on a blank wafer [figure 1(ii)]. After the successful completion of photolithography and doping procedures, the desired structure was fabricated.		



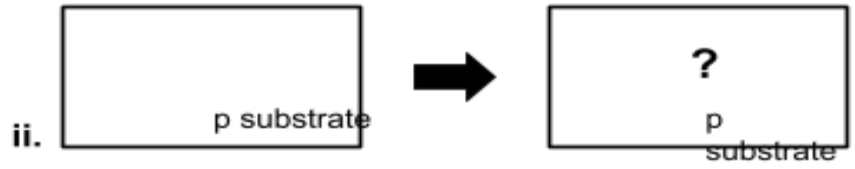
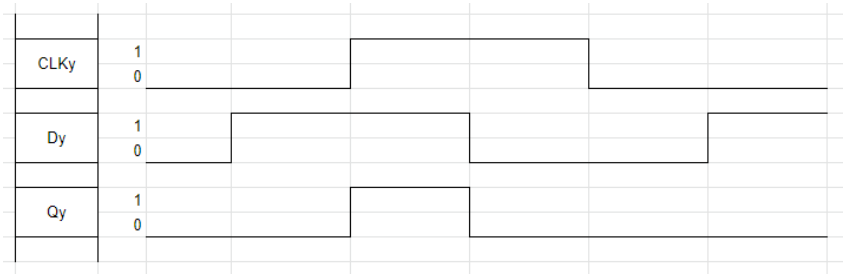
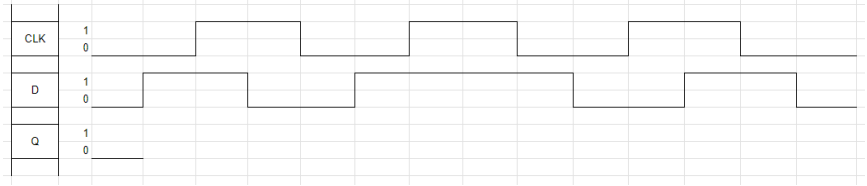


Figure 1: **(i)** p+ diffusion mask (**top** view)
(ii) Blank wafer (**Cross-section** view).

Figure 2: **Cross-section** view of the wafer after forming p+ diffusion regions.

	(a)	**Draw** and complete figure 2. Properly **label** the different regions in the figure.	**6**
	(b)	Briefly **explain** the following terms for the CMOS photolithography process: (i) Polysilicon (ii) p-type and n-type dopants	**6**
	(c)	What are well and substrate taps?	**3**
3. (CO2)	**(a)**	"Y" is a circuit element that produces output **Qy** from input **Dy** with a clock signal, **CLKy**, as shown in <u>figure 1</u>:  Figure 1: Timing Diagram for circuit element "Y" **Design** a negative-edge triggered D-flip flop using circuit element "Y".	**7**
	(b)	**Complete** the timing diagram in <u>figure 2</u> for the designed negative-edge triggered D-flip flop where **D** is the input, **CLK** is the clock signal and **Q** is the output to be drawn. (Use a pencil to draw the signal and draw on the Question Paper itself, no need to draw the diagram in your answer script separately)  Figure 2: Timing Diagram of Negative-edge triggered D flip-flop to be completed	**8**

4. (CO2)

Consider a sequential circuit with two inputs (***p1*** & ***p2***) and a single output, ***z***. TENCON is a prestigious conference where researchers from all over the world submit their research articles. These articles are handled by two reviewers, Reviewer A & Reviewer B. They review each article independently & either approve a submitted article (denoted by 1) or reject it (denoted by 0). The decisions of Reviewer A are given by a bit stream, ***p1***, whereas the decisions of reviewer B are given by ***p2***. **<u>If for three consecutive articles, both of their decisions are the same (i.e. *p1* = *p2* for three consecutive clock cycles), then they receive a consistency reward (*z* = 1) from the conference committee *after* a period.</u>**

Here, the decisions of reviewer A & reviewer B for a number of submitted articles & their corresponding reward instances are given below.

p1	0	1	1	0	1	1	1	0	0	0	1
p2	1	1	1	0	0	0	1	0	0	1	1
z	0	0	0	0	1	0	0	0	0	1	0

Note:

- You **must** use Gray encoding to assign states.
- The overlapping of the input bits (***p1*** & ***p2***) is *not* allowed.

(a)	What type of FSM would you need for the given problem?	**1**
(b)	**Design** the state diagram for the corresponding FSM.	**4**
(c)	**Derive** the state-assigned table from your state diagram in (a).	**4**
(d)	**Evaluate** the <u>next state</u> & <u>output</u> logic expressions to implement the FSM & **calculate** the number of flip-flops required for the circuit implementation. (You don't need to draw the circuit implementation.)	**5 + 1**