Transimpedance Amplifiers for Extremely High Sensitivity Impedance Measurements on Nanodevices

Giorgio Ferrari, Fabio Gozzini and Marco Sampietro

Abstract The paper highlights the critical aspects in the design of high performance transimpedance amplifiers to be used for the electrical characterisation of nano-biodevices. Current sensitivity, bandwidth, dynamic range and leakage current discharge are discussed to cope the tight needs in impedance spectroscopy measurements at the nanoscale. An implementation in a standard 0.35 μm CMOS technology using dual power supply of ±1.5 V is described in detail: thanks to an active resistor of equivalent value up to 300 GΩ and minimum noise, a transimpedance amplifier operating from few Hz is obtained, featuring an operative dynamic range for ac current signals independent of the amount of the leakage current and allowing an unlimited measuring time, ideal for attoFarad capacitance measurements of biological samples in their physiological medium.

1 Introduction

The electrical characterization of single molecules and nanometer-scaled devices (referred as Device Under Test – DUT) requires the capability of detecting extremely low signals as a consequence of their very small dimension and of their very poor conductance. In most cases, and irrespectively of the specific measurement to be performed (quasi static current-voltage curves, impedance spectroscopy, noise analysis), the electrical quantity to be sensed is a current, whose value may be well below the pA in nowadays nano-bio research [1–4].

Transimpedance amplifiers, in which the signal current made available by the DUT is converted into a voltage with maximum signal-to-noise ratio ready for further processing, are perfectly suited to this task: thanks to the input virtual ground made available by the feedback architecture (see Fig. 1) the current flowing in the DUT can be measured with high accuracy irrespective of the overwhelming stray capacitances introduced by the connections. By applying a sinusoidal input

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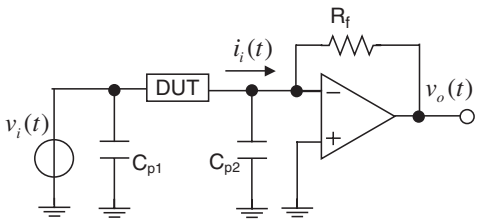

Fig. 1 Measurement setup for the electrical characterization of a device (DUT) exploiting the peculiarities of transimpedance amplifiers. C_{p1} and C_{p2} are the stray capacitances given by the connections not influencing the accuracy of the measurement

voltage and by sensing the in-phase and in-quadrature current components, the device impedance upon the frequency can be extracted. Indeed, impedance spectroscopy is an essential tool to study the frequency response of a variety of systems and to obtain characteristic parameters of devices such as dielectric constant, charge carrier density, junction capacitance, electron mobility [5–8], as well as in electrochemistry [9, 10] to study interface adsorption and charge transfer reaction.

In the scheme of Fig. 1 the impedance resolution (maximum detectable ac resistance and minimum detectable capacitance) and the frequency range of the measurement are essentially determined by the transimpedance amplifier. Once fixed the noise floor given by the current-to voltage amplifier, higher resolution can only be achieved by continuously acquire the signal to filter out the noise fluctuations, thus paying the penalty of slowing down the measurement system. Therefore efforts must be put in the design of very low noise and adequate bandwidth transimpedance amplifiers to cope with the request of very high sensitivity.

Bandwidth is required not only to extend the frequency range of impedance measurements and to increase sensitivity. Fast circuits are also desired to track the time evolution of the nanoscopic system, for example in discriminating ionic current variations in detecting the chemical identity of single molecules passing through a ion channel [11, 12] or in conjunction with scanning probe microscopes (SPM), to operate in fast scanning mode so to investigate dynamical processes and to reduce the effects of the mechanical drift and of environmental noise [13]. In addition, the ability to discharge steady currents of non-negligible values is also an important feature. This is the case when measuring for example the capacitance of a living biomolecule with a precision better then the attofarad, having the molecule in its physiological medium, and consequently with large steady leakage currents [14, 15].

2 Transimpedance Amplifier Architectures

The classic configuration of a transimpedance amplifier (see Fig. 2a) having a simple resistor in the feedback path of an Operational Amplifier (OpAmp) cannot be adopted in single-chip realisations because of the difficulty to integrate a stable linear resistor of sufficiently high value (GΩ values are currently used in discrete

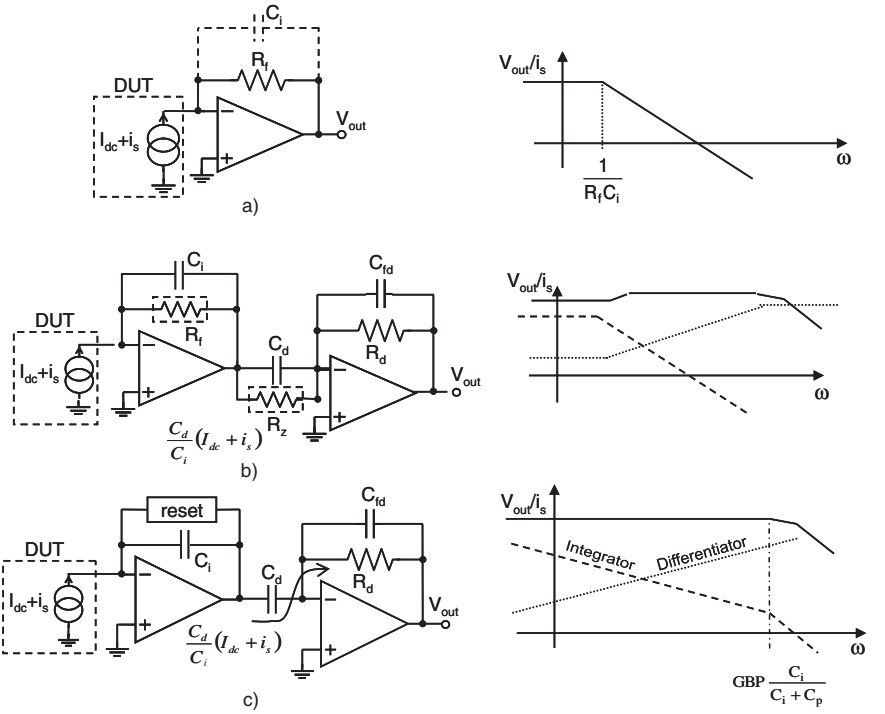

Fig. 2 Transimpedance amplifier configurations: (**a**) classical, (**b**) pole-zero compensated and (**c**) integrator-differentiator

realisations) and of the corresponding limited bandwidth due to the unavoidable stray capacitances in parallel to the resistor itself. Note that the feedback resistor would define the sensitivity of the transimpedance amplifier, as it sets the current noise at the input node ($4kT/R_f$) and the precision of the instrument as it sets the current-to-voltage conversion factor; therefore, to improve the current resolution, the feedback resistor must be chosen as large as possible.

The lack of high-value, stable and linear resistor-like structures in most of the available integrated technologies has solicited the design of alternative topologies of transimpedance amplifier. At first, to extend its bandwidth the circuit of Fig. 2a can be followed by an amplifier with a gain that increases at frequencies greater than $1/(2\pi\, R_f\, C_i)$, as in the example of Fig. 2b, obtaining a flat overall frequency response [16, 17].

In the scheme of Fig. 2b a precise zero-pole compensation is obtained in the case of $R_f\, C_i = R_z\, C_d$. The disadvantage of this solution is the accurate calibration of the pole-zero compensation necessary to have a perfectly flat frequency response over the desired bandwidth. Usually in a totally integrated solution the two resistors are substituted by a matched pair of non-linear devices, typically transistors, conveniently operated (ohmic, saturation or subthreshold region) to obtain the desired conductance value [17, 18]. In this case the input offset of the amplifiers unbalances

the voltage across transistors and sets their transconductances to different values. This gives an unavoidable mismatch between resistances and capacitances that may prevent a flat response: at low frequencies the response is given by the ratio of the channel resistances and at high frequencies the response is given by the ratio of the capacitances. Furthermore the frequency of this gain discontinuity changes as the dc current from DUT changes because the channel resistances change their absolute values. These effects become important when the current is reduced, typically below the pA, irrespective of transistor operation, that is when the transistor voltages become comparable to the offset of the amplifiers. As a last disadvantage of this configuration, the leakage from the DUT changes the output voltage of the OpAmp and reduces the dynamic range of the circuit for the signal.

The substitution of the feedback resistor R_f with a switched-capacitor resistor cannot be used in our context of high-sensitivity wide bandwidth applications. Since a clock frequency greater than the signal bandwidth is required to avoid aliasing effects, the charge injection during the switching becomes a critical parameter. For example, a clock frequency of 10 MHz and a charge injection as low as 1fC give a spurious current of 10 nA! The successful application of switched capacitor concept is limited to the measurement of small capacitance variations of purely capacitive DUT [19, 20].

3 Integrator-Differentiator Scheme

The ideal architecture would be the integrator-differentiator scheme of Fig. 2c where the feedback resistor of the OpAmp is substituted by a well stable in value capacitor, thus obtaining a large bandwidth integrating stage and where a differentiating amplifier has been added to recover the desired linear relationship between input current and output voltage. Obviously a reset element must be added in parallel to the capacitance in order to prevent saturation of the integrator stage by the leakage currents to the input node from the DUT or from the OpAmp. This architecture offers the best trade-off in term of minimum noise (besides the OpAmp noise, along the signal path only the resistor R_d affects the input noise but reduced by the square of the amplifying factor C_d/C_i), of accuracy of the current-to-voltage conversion factor (the gain being given by the ratio of two capacitances) and of large bandwidth practically approaching the gain bandwidth product (GBP) of the OpAmp.

Note that technology aspects play an important role in defining the amplifier characteristics. Taken a maximum practical value of R_d in the range of 100 kΩ and a maximum practical value of C_d of 20 pF, to produce a noise of R_d at the input equivalent to a 4 GΩ resistor (therefore negligible with respect to the white noise of any practical reset network), a ratio $C_d/C_i > 200$ is required, thus setting C_i in the 100 fF range. Given a DUT+strays capacitance of 1 pF and a GBP of the OpAmp of 100 MHz (see Par.7 for details), the overall operating frequency limit of the transconductance amplifier is around 10 MHz, well above the classical scheme of Fig. 2a and adequate for a large set of applications.

The low frequency limit of operation of the transimpedance amplifier in the integrator-differentiator configuration instead depends on the details of the reset system of the integrator. A simple switch in parallel to C_i operated when the integrator output voltage reaches a defined threshold, would ensure a good extension in the low frequency region but would set a limit to the time interval available to measure the DUT current. This time depends both on the DUT leakage current and on C_i: if $C_i = 100\,\text{fF}$ and $I_{leak} = 10\,\text{nA}$, a discharge period of only few tens of μs would result, largely inferior to the time required to measure accurately the impedance in many applications.

To obtain an unlimited measuring time, the switch should be replaced by a continuously-active system that resets the DC but leaves untouched the signal over a large bandwidth. In other words, the integrator stage should behave like a pure integrator starting from very low frequencies and consequently the singularities in the reset system should be placed at even lower frequencies, namely in the tens of Hz range. Because of this requirement, the successful solutions available in the literature to reset the feedback capacitance of charge preamplifiers [21–23] cannot be directly transferred to transimpedance amplifiers. Those architectures are not conceived to have poles at such low frequency and do not give the possibility to insert an equal number of low frequency zeros to provide the necessary feedback stability. In addition, charge preamplifiers used as transimpedance amplifiers have a mean value of the integrator output voltage defined by the dc leakage current, thus loosing the feature of having rail-to-rail dynamic range for ac current signals independent of the amount of the dc current.

In the following, we analyze a fully integrated solution to these problems consisting of a stable active reset network having poles and zeroes in the Hz range, providing a DC path to ground for the DUT leakage current, rail-to-rail dynamic for the signal and a signal extended bandwidth up to few MHz.

4 Active Discharge System

The conceptual scheme of the proposed active reset circuit, made of an amplifier H(s) in series to a resistive element R_{dc} , is shown in Fig. 3. The amplifier H(s) has a gain from node A to node B greater than 1 for the dc component and a strong attenuation in the signal bandwidth, as sketched in the figure.

The loop gain of the new feedback loop can be written (see details in [24]) as

$$G_{loop} = H(s)\frac{A}{1 + s(1 + A)C_i R_{dc}} \tag{1}$$

where A is the gain of the integrator OpAmp. At low frequencies the loop gain is strong enough to control the voltage across R_{dc} and to collect the leakage current, I_{dc}, in the resistor. At higher frequencies the feedback is not active and consequently not affecting the input signal, i_s, that is integrated in the capacitance C_i. Therefore

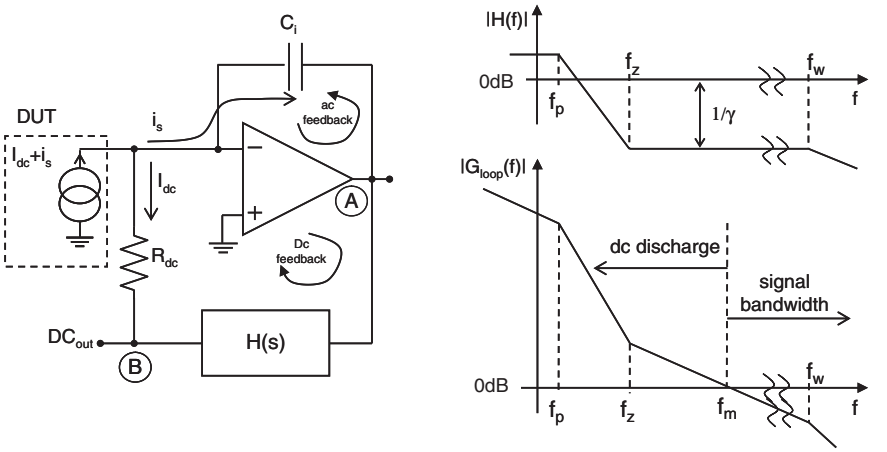

Fig. 3 Concept of the feedback network to discharge the standing current from the DUT in the integrator stage (*left*), corresponding transfer function of the H(s) block (*upper right*) and overall loop gain to ensure stability (*lower right*)

the frequency f_m at which $|G_{loop}(f_m)| = 1$ defines the lower limit for the signal bandwidth.

To ensure stability to the feedback network, since the integrator introduces a pole at very low frequency, the phase margin is fixed only by the amplifier H(s) and is given by $\phi_m = 90^\circ - \angle H(f_m)$. By using an amplifier H(s) with one pole at a frequency f_p and one zero at a frequency $f_z > f_p$, as sketched in Fig. 3, a phase margin greater than 45° is ensured providing that $f_z < f_m$. In this condition the minimum frequency amplified by the circuit is given by the following expression:

$$f_m = \frac{1}{2\pi \cdot R_{dc} C_i \cdot \gamma} \tag{2}$$

where γ is the attenuation of H(s) for frequencies greater than f_z and is a free parameter that can be tuned to obtain the desired value of the minimum frequency of signal, f_m, amplified by the transimpedance amplifier.

The challenges of implementing an integrated solution using a low-noise "resistance R_{dc}" and an amplifier H(s) with pole and zero frequencies well below 100 Hz are discussed in the following sections.

5 Realisation of Very Large-Value Resistors

As the current noise of the resistance $R_{dc}(4\,kT/R_{dc})$ would be injected directly into the input node, to sense femtoAmpere currents it is essential to use an equivalent resistor in the GΩ range. Since technological limits prevent the integration of a physical resistor of such high value, an active very low-noise circuit should be

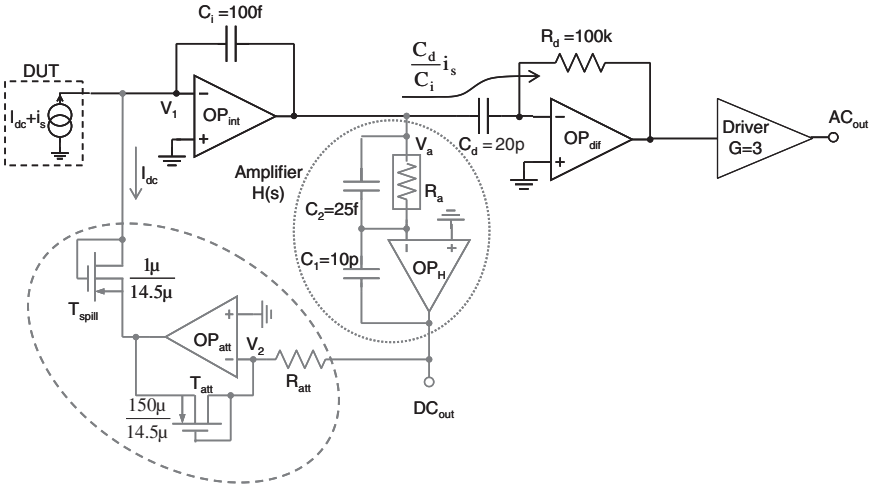

Fig. 4 Schematics of the transimpedance circuit with the active network to draw the DUT steady current (*dashed ellipse on the left*) and with the amplifier H(s) (*dotted ellipse on the right*). The large value "resistor" R_a is, in turn, implemented by cascading 4 current reducer systems (see Fig. 5)

chosen. Note that although the linearity of element R_{dc} positively does not affect directly the signal path, a non-linear element such as a simple transistor would give a frequency f_m (and consequently a loop stability) dependent on the input dc current. Our solution uses a linear transconductor as shown in the dashed ellipse on the left in Fig. 4.

The core of this system are the matched MOSFET T_{att} and T_{spill} connected with source-well short circuited: with negative V_{GS}, the device operates as a pMos-diode; with positive V_{GS}, the parasitic drain-well (p-n) junction is forward biased, and the transistor acts as a diode [25]. The matched MOSFET's have the same channel length and are biased with the same voltage, thus their current density is the same irrespective to the sign of the current I_{dc} flowing in T_{spill}. By designing T_{att} M-times larger than T_{spill}, the overall system acts as a linear and accurate current reducer by factor M. Figure 5 (left) shows the measured I-V characteristic certifying an equivalent resistance of more than 45 MΩ with very good linearity over the full voltage swing of ±1.5 V and occupying a very small area.

The implemented scheme is very beneficial from the sensitivity point of view: the current noise of the physical resistor R_{att} is in fact injected into the input of the circuit reduced by the factor M^2. In this way, chosing a reducing factor of 150 and a resistor R_{att} of 300 kΩ, the noise injected in the input is equivalent to a very large resistance of about 6.5 GΩ, although the I/V characteristic shows a resistance of "only" 45 MΩ. This low noise condition is preserved for currents less than the pA. For greater I_{dc} currents the shot noise ($2qI_{dc}$) of the T_{spill} transistor operating in sub-threshold regime or as p-n diode becomes dominant. The flicker noise of T_{spill} has been made negligible in the signal band by using a non-minimal area MOSFET.

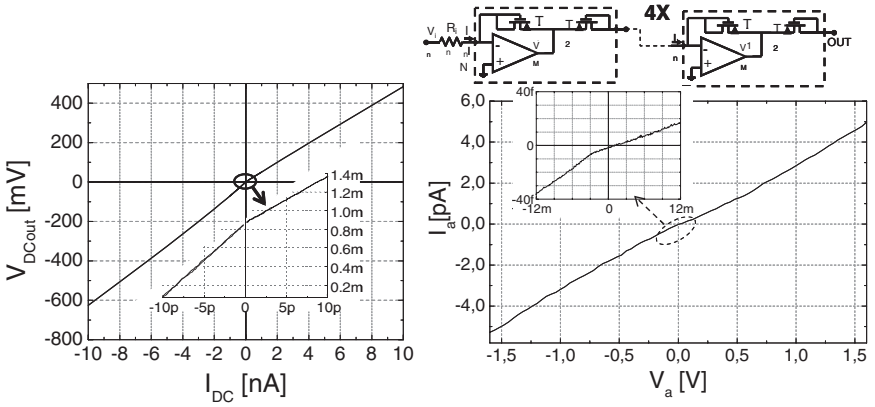

Fig. 5 Measured I-V characteristics of the current reducers realized with the matched MOSFET scheme certifying an equivalent resistance of more than 45 MΩ used as reset element for the standing DUT current (*left*) and of 300 GΩ used to set the very low frequency pole in the H(s) network (*right*). In the insets the magnification around zero showing the capability of this system to drive very low current in the fA range

6 Feedback Network Design

Another critical aspect of the project is the realisation of the feedback network H(s) which should have (i) zeros and poles at frequencies well below 100 Hz given by the low limit of the signal bandwidth and (ii) a high DC gain, H(0), to keep the output of the integrator close to zero irrespective of the dc input current, ensuring the maximum input range for the signal and a high linearity of the integrator in any bias condition. We adopted a first order filter (see Fig. 4) characterized, up to the GBP frequency of the amplifier OP_H, by the transfer function:

$$H(s) = \frac{A_0(1 + sC_2R_a)}{1 + sR_a\,[C_2 + C_1(1 + A_0)]} \tag{3}$$

where A_0 is the DC gain of OP_H.

With this solution the crucial point is the design of the "resistor" R_a. Given a technical limit for C_1 of 10 pF, a value f_m of about 100 Hz can be obtained with a γ factor (see Fig. 3) equal to 400 and $C_2 = 25$ fF. To set the zero at least 1 decade before f_m the "resistor" R_a must be in the order of hundreds GΩ. To accomplish this, a cascade of 4 current reducers similar to that discussed in the previous section has been implemented. Figure 5 (right) reports the measured I-V characteristic and shows that with this technique it is possible to make transconductors as low as 1/300 GΩ together with a good linearity. Note that the circuit can properly work at current levels as low as fA, with parasitic currents playing no role because all MOSFET terminals are actively controlled by the operational amplifier and the leakage current of Nwell-substrate is driven directly by the amplifier output. These properties are strictly necessary in this application in order to keep stable the loop in every bias conditions.

7 Forward Amplifier Design

The forward amplifier of the integrator stage plays a major role in the sensitivity of the instrument, as it sets the noise of the system, and in its operating capabilities, as it sets the high frequency bandwidth of the full transimpedance and the DC voltage of the input node. This latter point has solicited the use of a differential input configuration, powered at ±1.5 V, to control the potential of the virtual ground of the integrator and to apply very small and accurate DC signal across the DUT without an additional voltage source. For this reason, a simple common source configuration, typical in many low noise applications, has not been used.

In order to achieve the desired very high sensitivity, the differential input stage uses a pair of p-MOS transistors (to minimize the flicker noise contribution in the signal bandwidth, despite a slightly higher white noise than in n-MOS) and is purely resistively loaded (an active load with a current mirror would have fully added its noise, whose white component would be higher than the one of a simple resistor and whose 1/f component would be very high considering that nMOSFET should be used). Parallel (current) noise of the input pair can of course be neglected. The voltage noise, instead, plays a role as it is amplified through the total input capacitance seen from the inverting OpAmp's input (sum of C_i, the feedback capacitance, of C_{DUT}, the equivalent capacitance of the DUT and of the relative interconnections, and of C_{gate} of the MOSFET) giving an equivalent input current noise of:

$$\overline{i_{eq}^2} = (2\pi f)^2 (C_i + C_{DUT} + C_{gate})^2 \cdot \overline{v_n^2} \tag{4}$$

Because of the frequency dependence, this noise becomes dominant at the high frequency of the signal bandwidth and must be minimized. Special care should consequently be drawn in the design of the differential input transistors that set both C_{gate} and $\overline{v_n^2}$, whose expressions are:

$$\overline{v_n^2} = 2 \cdot \left[\frac{2}{3} \frac{4kT}{g_m} \right] = 2 \cdot \left[\frac{2}{3} \frac{4kT}{\mu_p} \frac{L^2}{C_{gate}(V_G - V_T)} \right] \tag{5}$$

$$C_{gate} = C'_{ox} W L \tag{6}$$

where the constant 2 reflects the presence of the two MOSFETs of the differential pair, k is the Boltzman constant, μ_p is the hole carrier mobility in the channel and C_{ox}, W, L are respectively the gate capacitance per unit area, the channel width and length of the transistors. The suggestion of minimizing C_{gate} given by Eq. 4 is counter balanced by the suggestion of maximizing it in Eq. (5); optimum is obtained by differentiating Eq. (4) giving the following condition for the gate capacitance [26, 27]:

$$C_{gate} = C_i + C_{DUT}$$

In our case, with C_i already set at 100 fF and C_{DUT} estimated in the range of 0.5 pF (basically due to the on chip interconnection and to the bonding pad), we

obtained $C_{gate} = 600\,\text{fF}$ leading to $L = 0.6\,\mu\text{m}$, the minimum value that guarantee a good matching of the differential pair and a good drain resistance and W=220 μm. Note that the additional capacitance of the real DUT which will be connected to the bonding pad (molecules or nanometer-scale devices) do not alter this choice. In this framework, the amplifier can be used in many different applications without a need of a re-design.

The chosen configuration of differential input stage with simple resistive loads ensures also that the noise produced by the stage is not boosted higher by the fact that the two inputs of the differential pair are connected to significantly different impedances. This effect usually is present in commercial OpAmp made with complex input differential stage which is sensitive, from a noise point of view, to the difference on the input impedance [28].

The second stage of our OpAmp (see Fig. 6) is again a differential pair with active load that injects its current in a multipath nested Miller compensation stage [29, 30] to obtain the highest possible gain with strong loop stability. The overall Gain-Bandwidth product of the OpAmp ended to be of 100 MHz, thus providing about 10 MHz bandwidth to the transimpedance amplifier.

The output stage is not made with a common "push pull" topology because even if it has a good driving capability, the source output limits the dynamic range: the

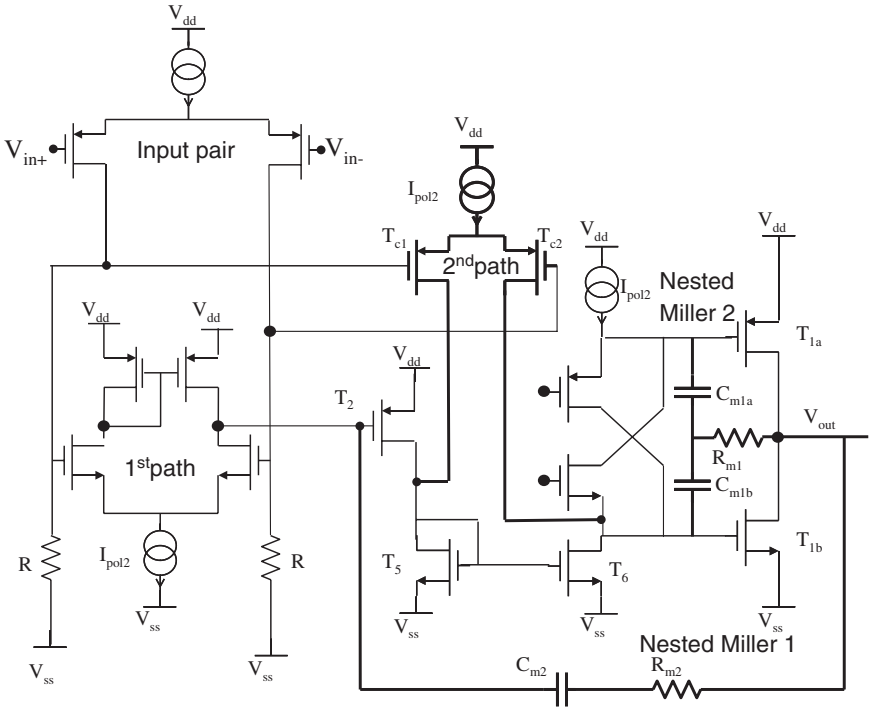

Fig. 6 Schematic of the OpAmp used in the integrator stage. Note the resistive load of the input stage to obtain minimum input noise

gate source potential in fact cannot drop below the threshold voltage so even if the gates of the output MOSFETs are actively driven rail-to-rail, the output voltage swing would be $V_{supply} - V_{thP} - V_{thN} \simeq 1.5$, too small for our purpose. The necessary capability to drive rail-to-rail the integrator output voltage is fully accomplish by a simple CMOS inverter [31].

Concerning the differentiator stage, its forward amplifier has an input stage similar to the one just described. A different compensation technique has been used because of the absence of the feedback capacitance now substituted by the resistance R_d that introduces a pole in the loop gain at the frequency $1/2\pi R_d C_d = 80\,\text{kHz}$. A standard compensation, achieved by adding a feedback capacitance C_{fd} in parallel to the resistance R_d, is not straightforward because the singularity $1/2\pi R_d C_{fd}$ should be at frequency greater than 10 MHz not to limit the differentiator bandwidth. This imposes a gain-bandwidth product of the operational amplifier greater than $10\,\text{MHz} \cdot C_d/C_{fd} = 1.25\,\text{GHz}$. Instead, without affecting the closed-loop transfer function we introduced a zero directly in the forward path in the Miller compensation network, as well known from the literature [32–34].

8 Dynamic Range Considerations

The maximum amplitude of the current signal that the circuit can process depends on the frequency and is limited by the saturation to the supply voltage of three different nodes (see Fig. 4): the DCout, the integrator output and the AC_{out}. At very low frequencies (DC range), where the amplifier H(s) has a high gain, both the integrator's output and the AC_{out} are not moved by the input signal; therefore, as reported in Fig. 7, the input current is limited by the saturation of the DC_{out} and given by $1.5\,V/R_{DC}$, that is about 25 nA for both negative or positive DUT currents. This condition holds as long as the gain of the amplifier H(s) is larger than 1. Over this limit (few tens of mHz) the integrator output node becomes the limiting node

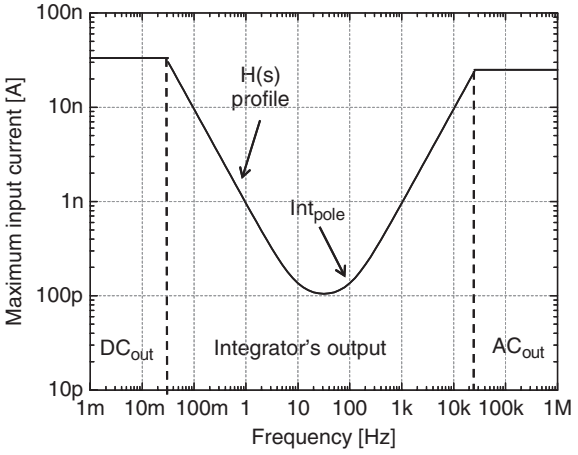

Fig. 7 Maximum input current that can be accepted by the transimpedance input node as a function of the frequency of the input signal

and the maximum input current decreases with frequency until the minimum value of $1.5\,\mathrm{V}/(\gamma R_{DC}) \cong 50\,\mathrm{pA}$ after the zero of the amplifier H(s) (10 Hz) when the attenuation γ is maximum. This low value is kept until the feedback network is deactivated (100 Hz) and then increases with the frequency since the module of the integrator transfer function decreases. In this raising region the maximum input current is given by $|I_{max}| = 1.5\,\mathrm{V} \cdot (2\pi f C_i)$. Finally, when the differentiator gain become larger than 1, the saturation of the transimpedance output voltage (AC_{out}) becomes dominant and the maximum input current is given by $1.5/60\,\mathrm{M\Omega} = 25\,\mathrm{nA}$.

9 Experimental Performance of the Circuit

The overall frequency response of the circuit, implemented on standard 0.35 μm CMOS technology [35], measured in the frequency range 10 Hz–10 MHz is reported in Fig. 8. The full bandwidth of the integrator expected by the theoretical analysis is fully confirmed by the experimental value: the minimum frequency is set by eq. 3 and the maximum frequency is limited only by integrator loop in agreement with its GBP of about 100 MHz and taking a C_{stray} of about 800 fF of the input device (giving a $C_i + C_{stray} = 1\,\mathrm{pF}$).

Note in Fig. 4 that the amplifier has actually two outputs: the signal output AC_{out} with bandwidth 100 Hz–5 MHz and a dc output DC_{out} that senses the voltage across R_{att} containing the frequency components lower than 100 Hz. Even if the feedback network is made by non-linear elements, the I/V characteristic of the DC_{out}, reported in Fig. 5 (left), shows a good linearity on a wide current range from 1 pA to 10 nA with only a slight asymmetry between positive and negative currents. This is due to the offset between the virtual grounds V_1 and V_2 and to the mismatch between the MOSFETs $T_{spill} - T_{att}$ working as MOS-diode when the current is negative or as drain-Nwell diode when the current is positive. Despite this small asymmetry, the DC_{out} is well suited to monitor the bias condition of the DUT during the measurement and to track continuously the low frequency variation of the DUT if needed.

Figure 9a shows the equivalent input noise measured on the integrator-differentiator prototype, operating with the lowest bias current. The experimental result is in agreement with the theoretical prediction given by

$$\overline{i_n^2} \approx \frac{4kT}{R_{att}M^2} + \overline{i_{Tspil}^2} + \frac{4kT}{R_D\,(C_d/C_i)^2} + \overline{e_{\mathrm{int}}^2} \cdot \omega^2 \cdot \left(C_i + C_{input}\right)^2 \qquad (7)$$

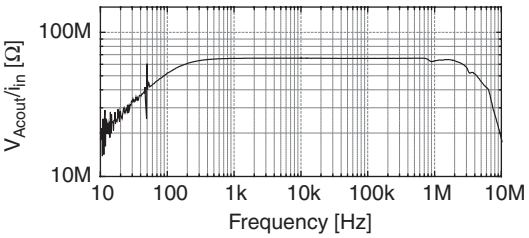

Fig. 8 Experimental frequency response of the transimpedance amplifier

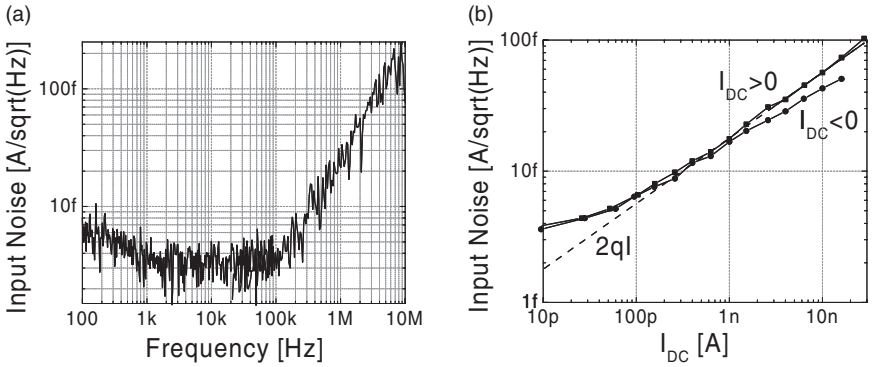

Fig. 9 (**a**) Experimental equivalent input current noise when operating the amplifier with low bias current. The raise in the spectrum at higher frequencies is due to the total input capacitances. (**b**) Experimental white noise as a function of the input dc current

where $\overline{i^2_{Tspil}}$ is the current noise of T_{spil}, $\overline{e^2_{int}} \cong (4nV)^2/Hz$ is the noise voltage source of the integrator OpAmp; $C_{input} \cong 700\,fF$ is the total capacitance at the input node of the integrator stage due to the operational amplifier, the DUT and the input stray capacitance. The thermal noise of the physical resistors R_{att} and R_d gives a contribution as low as $3\,fA/\sqrt{Hz}$ equivalent to the thermal noise of a $2\,G\Omega$ resistor. The current noise of MOSFET T_{spil} depends on the input dc current, it is negligible for currents smaller than 30 pA and then increases by increasing the input bias current as shown in Fig. 9b. The increase follows a theoretical shot noise as expected for a transistor operating in sub-threshold regime or as a p-n diode. For large negative current the transistor T_{spil} operates in inversion regime and the noise is correspondingly less than the shot noise. The 1/f noise a frequencies lower than 1 kHz is added by the differentiator stage and therefore is independent from the input bias.

10 Conclusions

A transimpedance amplifier to be coupled to sub-pF capacitance DUTs has been designed and tested. The high sensitivity and the wide bandwidth achieved make it suitable for sensing very low and fast signals (pA on 100 kHz) or very small capacitances down to the attoFarad even when the biological sample under test can support a voltage signal of only few milliVolt.

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