

Vivado Installation Guide

AIX 2024



Xilinx Vivado Design Suite

- Vivado is a tool we can use for **writing, simulating and implementing Verilog HDL projects.**
- This guide will explain how to install vivado, create a simple project and simulate it(windows)

<Download Vivado>

- Visit Xilinx website to download vivado
 - <https://www.xilinx.com/support/download.html>
- Here, select a version and download
- This tutorial will explain using 2021.1 version
- You have to create a Xilinx account to install Vivado

 Xilinx Unified Installer 2021.1: Windows Self Extracting Web Installer

(EXE - 226.04 MB)

MD5 SUM Value : 6bc01c7518717bea1c4aefcfc90d6f1b

Download Verification 

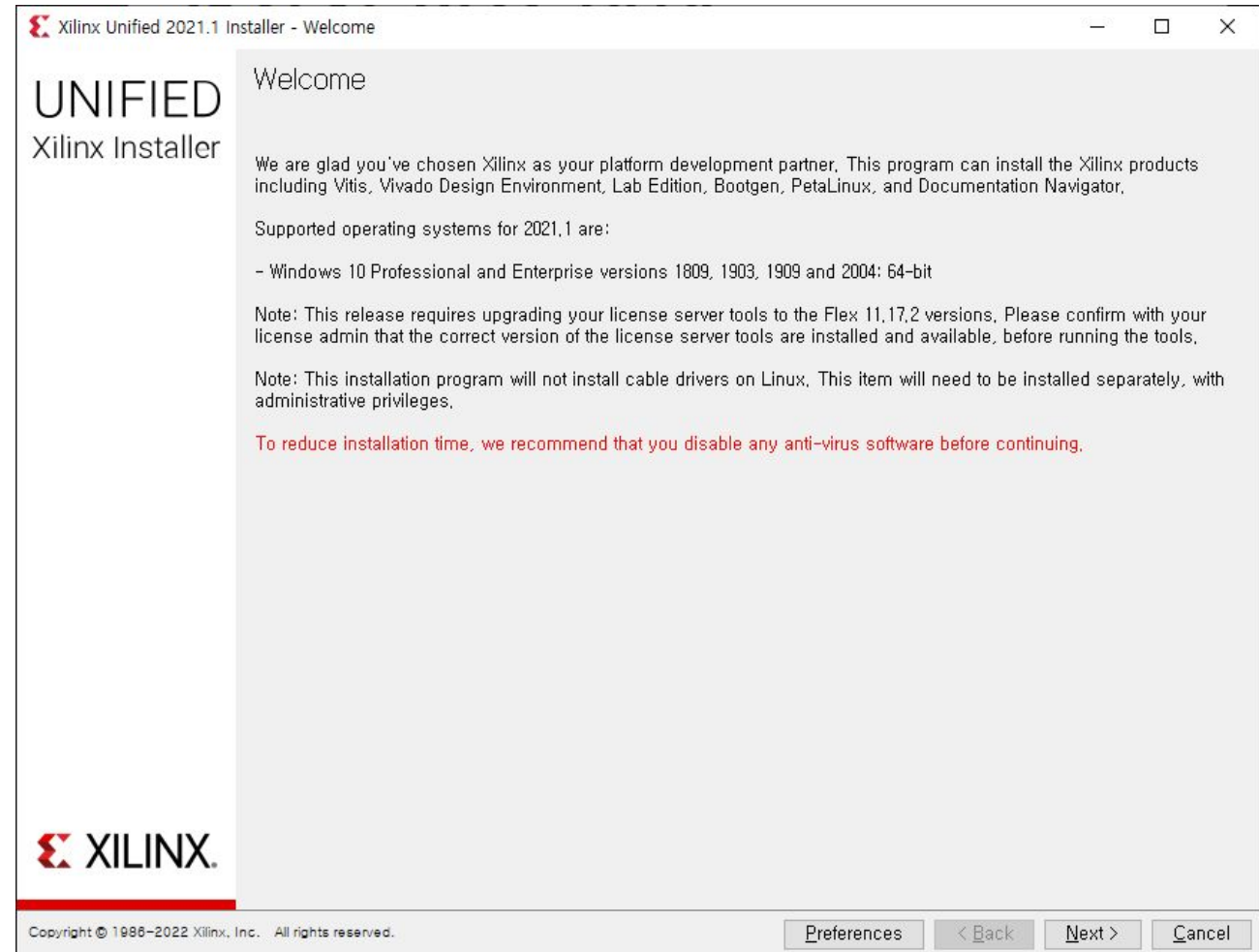
Digests

Signature

Public Key

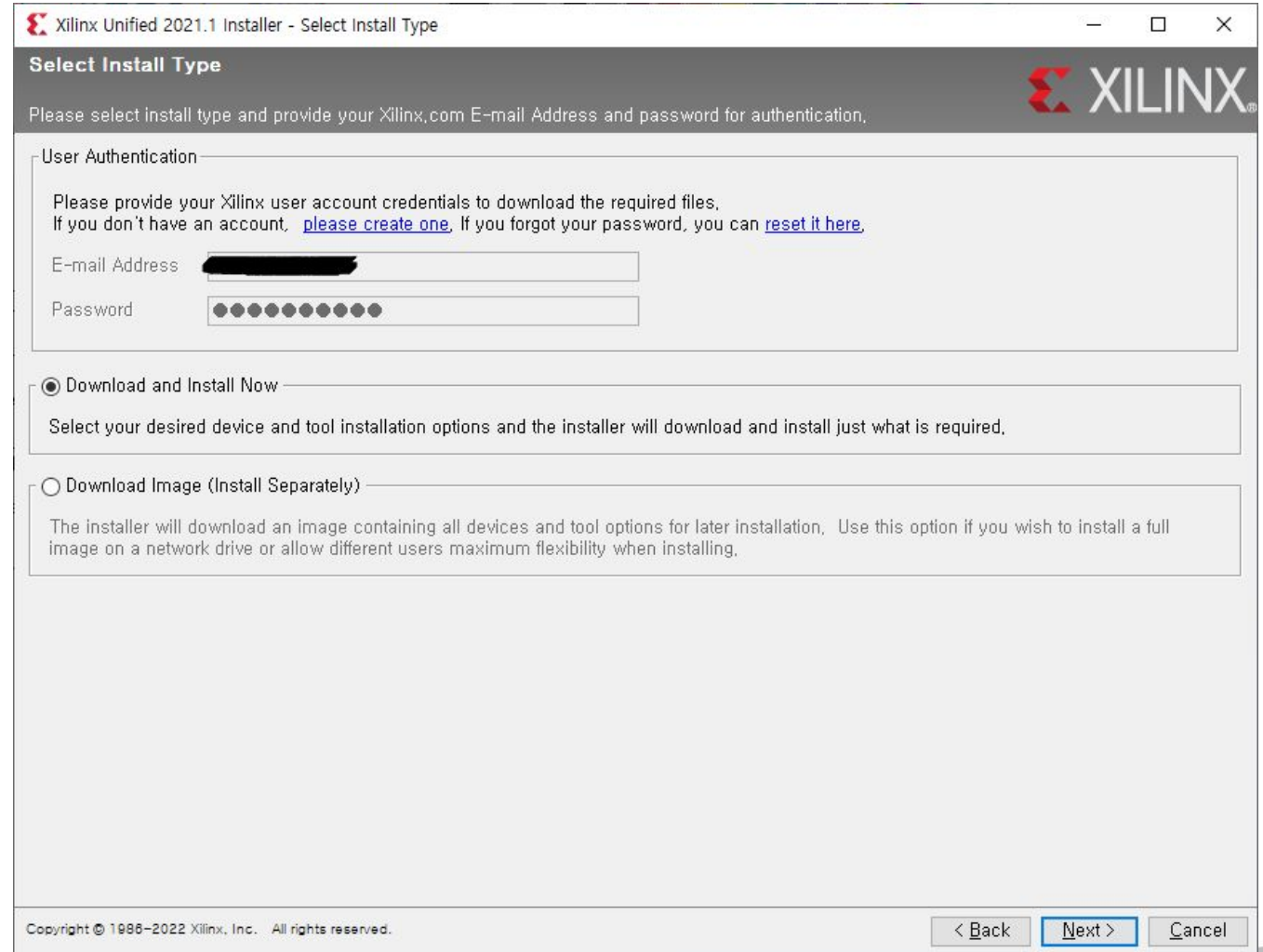
1. Installation

- After downloading, run the downloaded file



1. Installation

- Enter your Xilinx account
- Select download and install now
- Click next



The screenshot shows the 'Xilinx Unified 2021.1 Installer - Select Install Type' window. The title bar includes the Xilinx logo and the text 'Xilinx Unified 2021.1 Installer - Select Install Type'. The window has a dark header bar with the Xilinx logo and the text 'XILINX'. Below the header, the text 'Select Install Type' is displayed. A subtitle reads: 'Please select install type and provide your Xilinx.com E-mail Address and password for authentication.' The main content area is divided into three sections. The first section, 'User Authentication', contains the text: 'Please provide your Xilinx user account credentials to download the required files. If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).' Below this text are two input fields: 'E-mail Address' and 'Password'. The second section, 'Download and Install Now', is selected with a radio button. It contains the text: 'Select your desired device and tool installation options and the installer will download and install just what is required.' The third section, 'Download Image (Install Separately)', is unselected with a radio button. It contains the text: 'The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.' At the bottom of the window, there is a footer with the text 'Copyright © 1986-2022 Xilinx, Inc. All rights reserved.' and three buttons: '< Back', 'Next >', and 'Cancel'.

Xilinx Unified 2021.1 Installer - Select Install Type

Select Install Type

Please select install type and provide your Xilinx.com E-mail Address and password for authentication.

User Authentication

Please provide your Xilinx user account credentials to download the required files.
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

E-mail Address

Password

☒ Download and Install Now

Select your desired device and tool installation options and the installer will download and install just what is required.

☐ Download Image (Install Separately)

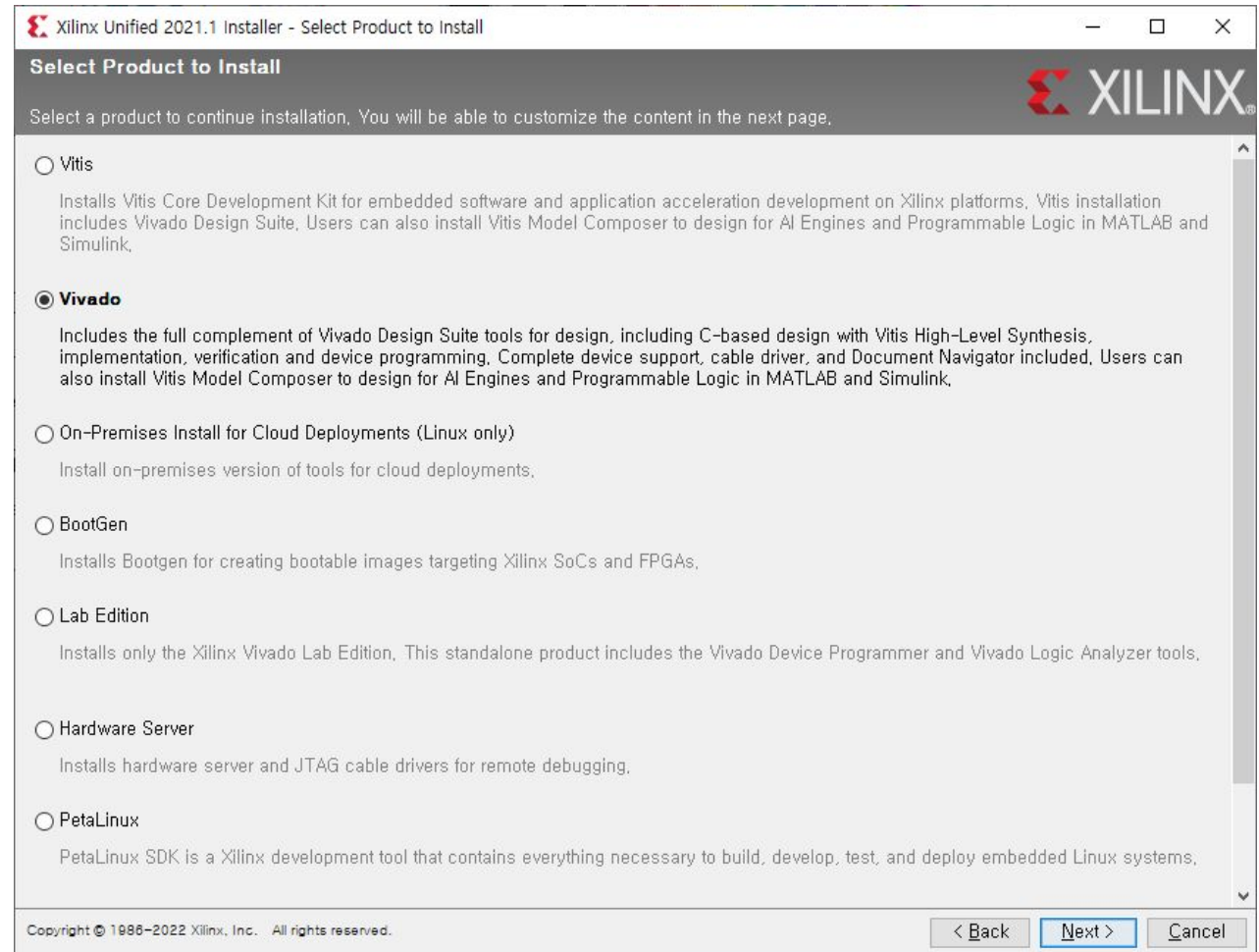
The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

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< Back Next > Cancel

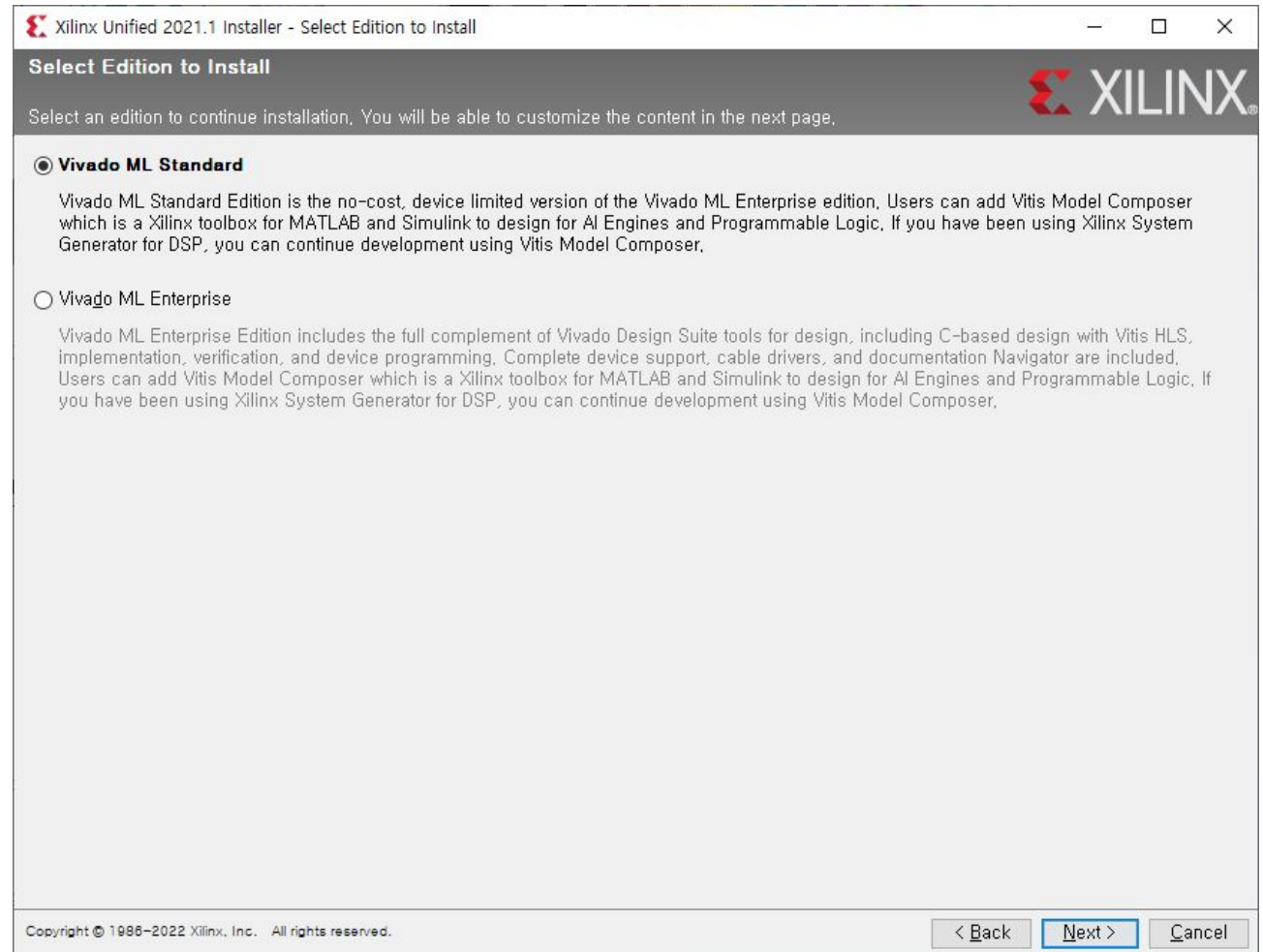
1. Installation

- Select Vivado, click next



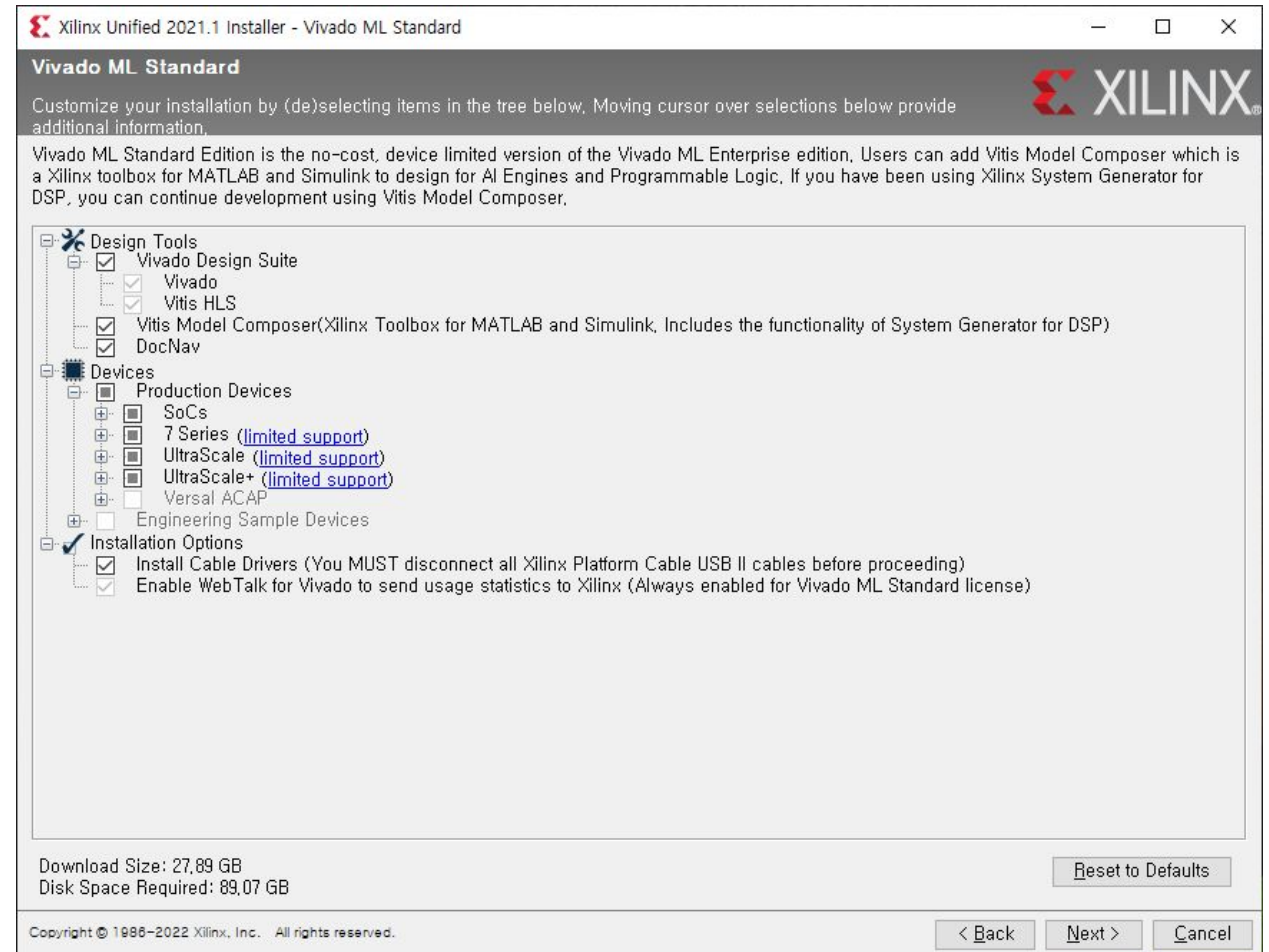
1. Installation

- Select Vivado ML Standard, click next



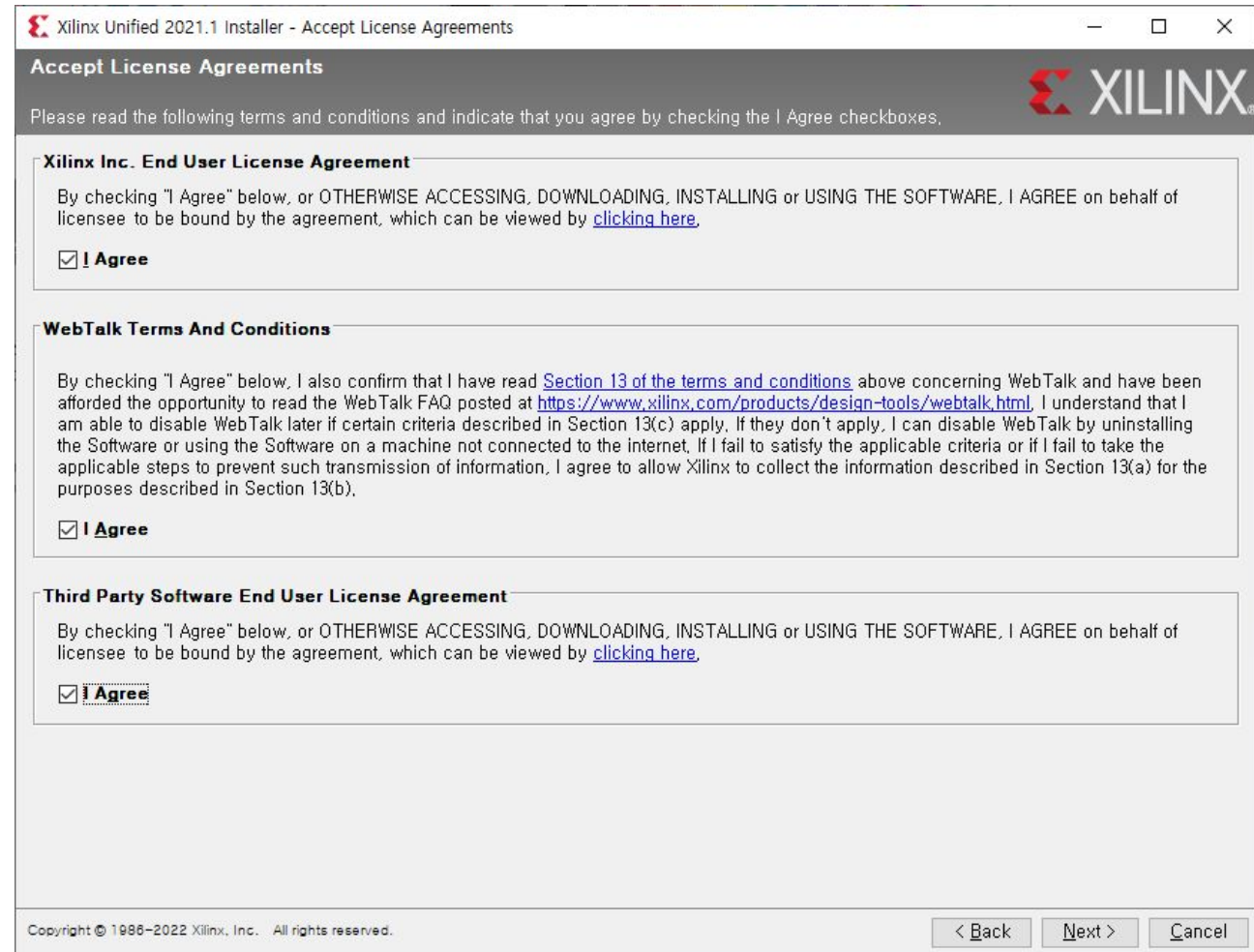
1. Installation

- Click next



1. Installation

- Select I agree, and click next



Xilinx Unified 2021.1 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

WebTalk Terms And Conditions

By checking "I Agree" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ I Agree

Third Party Software End User License Agreement

By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

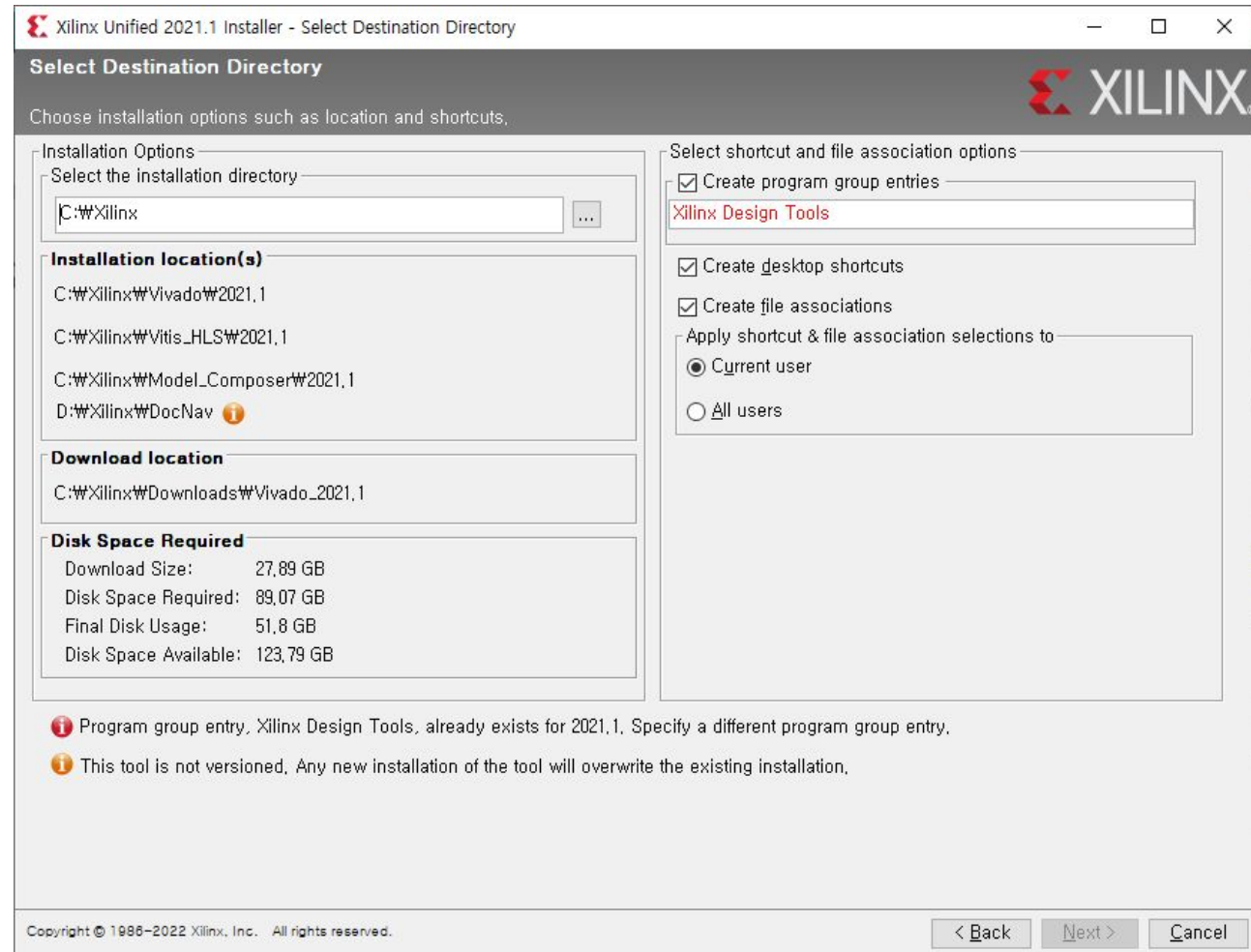
☒ I Agree

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< Back Next > Cancel

1. Installation

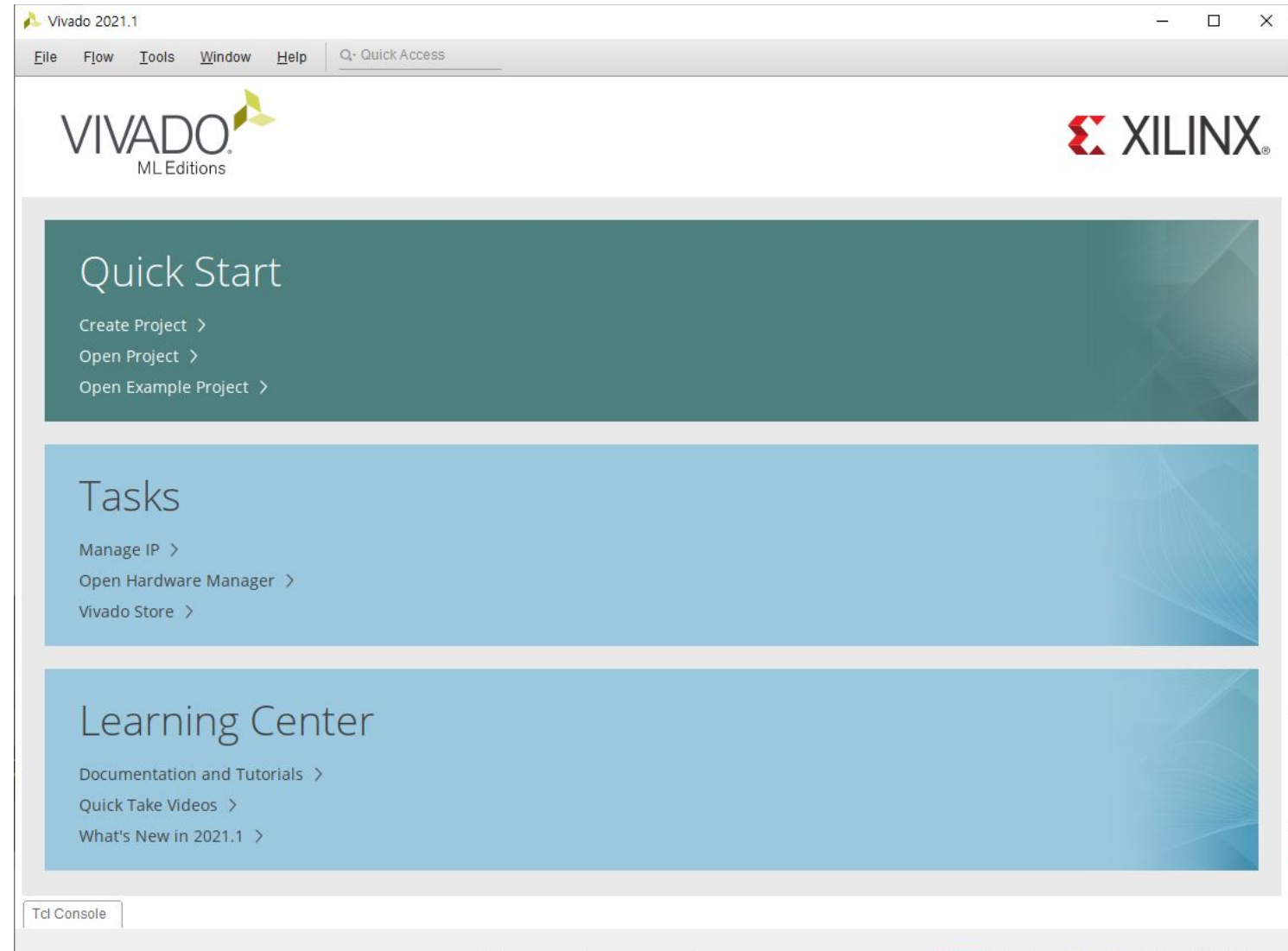
- Select installation directory, and click next
- After this, it will take quite long to finish installing



2. Create a new project

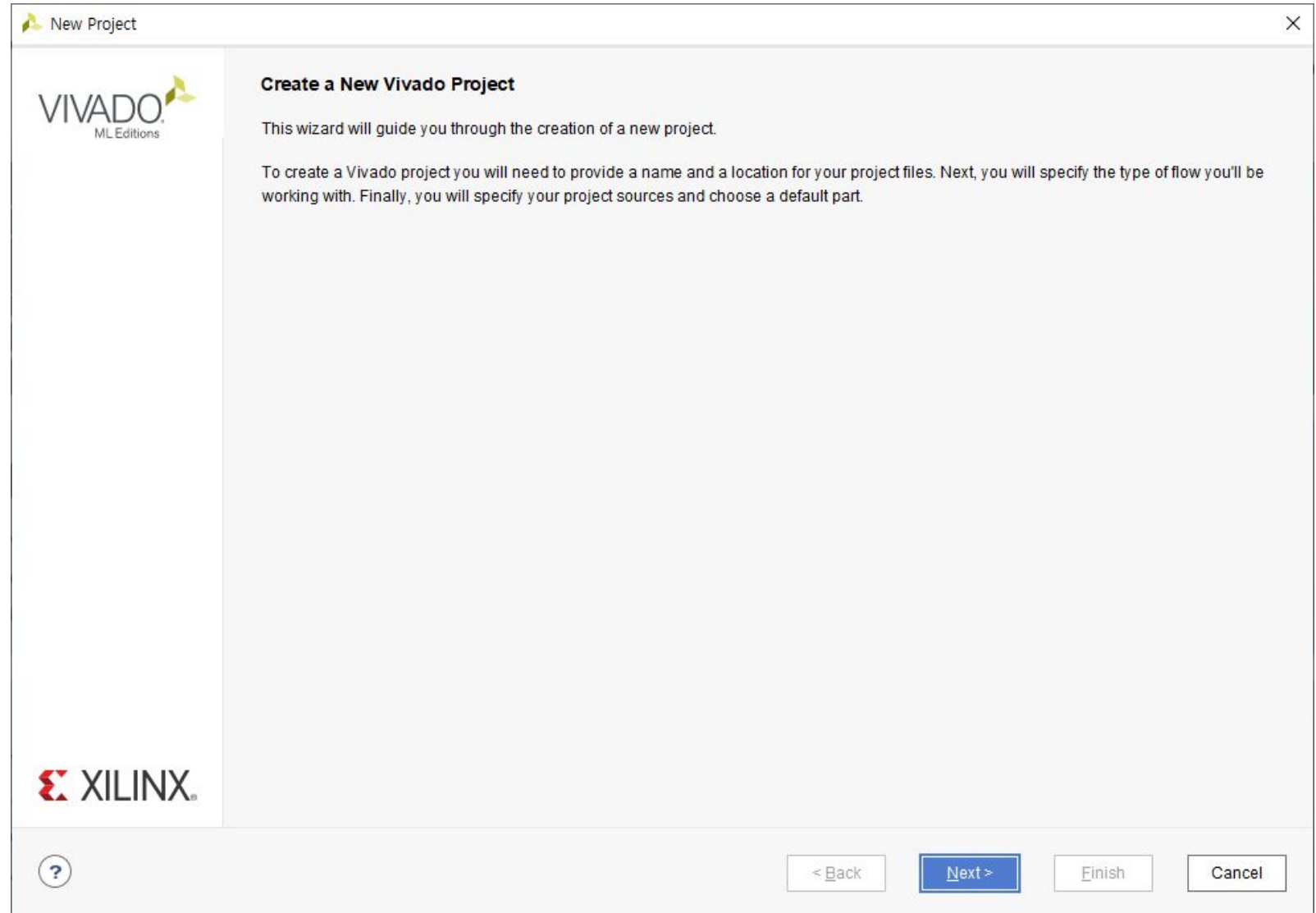
2. Creating an example project

- Run Vivado
- Click Create Project



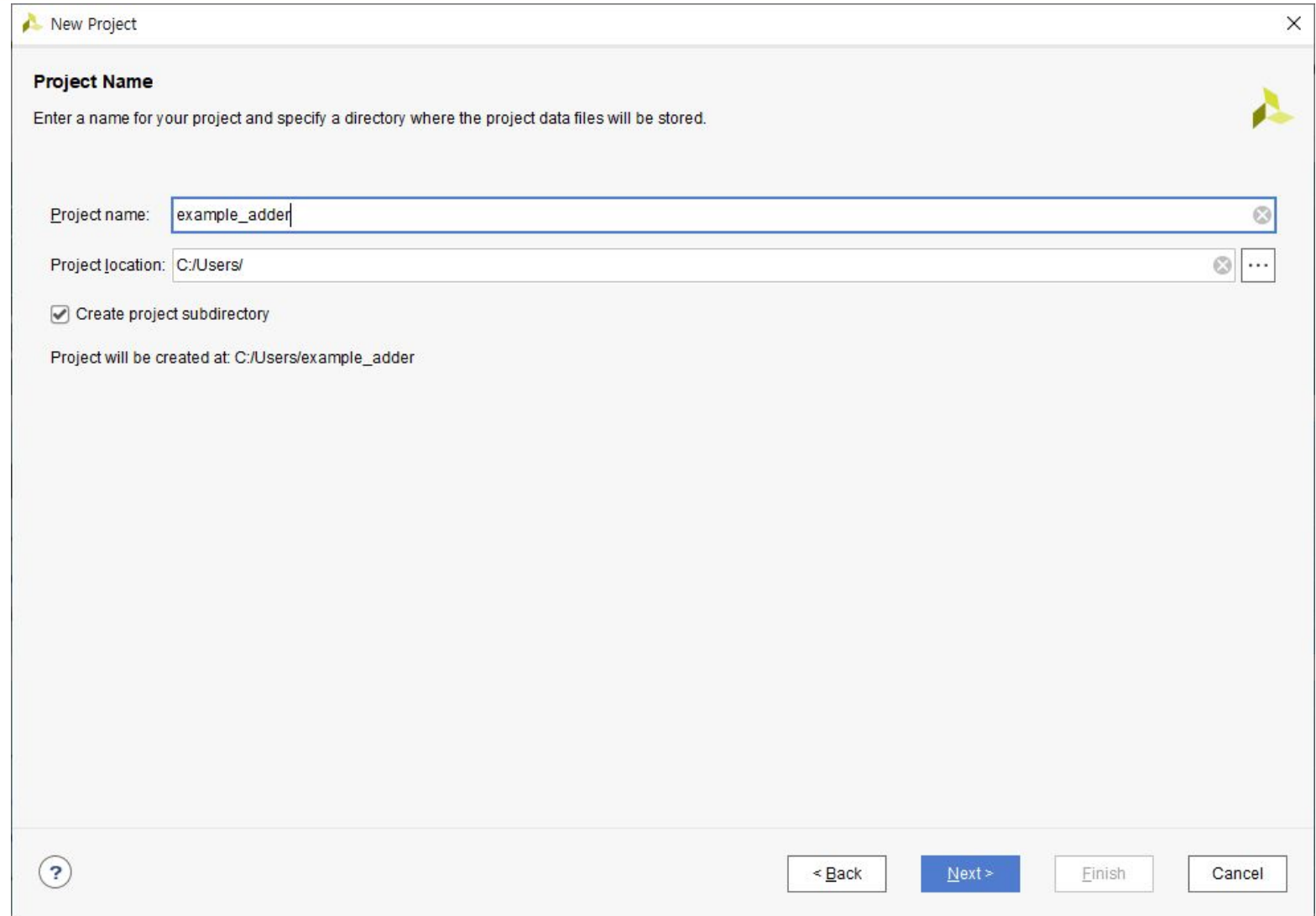
2. Creating an example project

- Click next



2. Creating an example project

- Select project name and location
- Click next



The screenshot shows a 'New Project' dialog box with a title bar containing a green logo and a close button. The main area is titled 'Project Name' and contains the instruction: 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are two input fields: 'Project name:' with the text 'example_adder' and 'Project location:' with the text 'C:/Users/'. To the right of the location field is a button with a green logo and a close button. Below the input fields, there is a checkbox labeled 'Create project subdirectory' which is checked. At the bottom of the main area, it says 'Project will be created at: C:/Users/example_adder'. The bottom of the dialog box has a footer with a help icon (a circle with a question mark) on the left and four buttons on the right: '< Back', 'Next >' (highlighted in blue), 'Finish', and 'Cancel'.

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: example_adder

Project location: C:/Users/

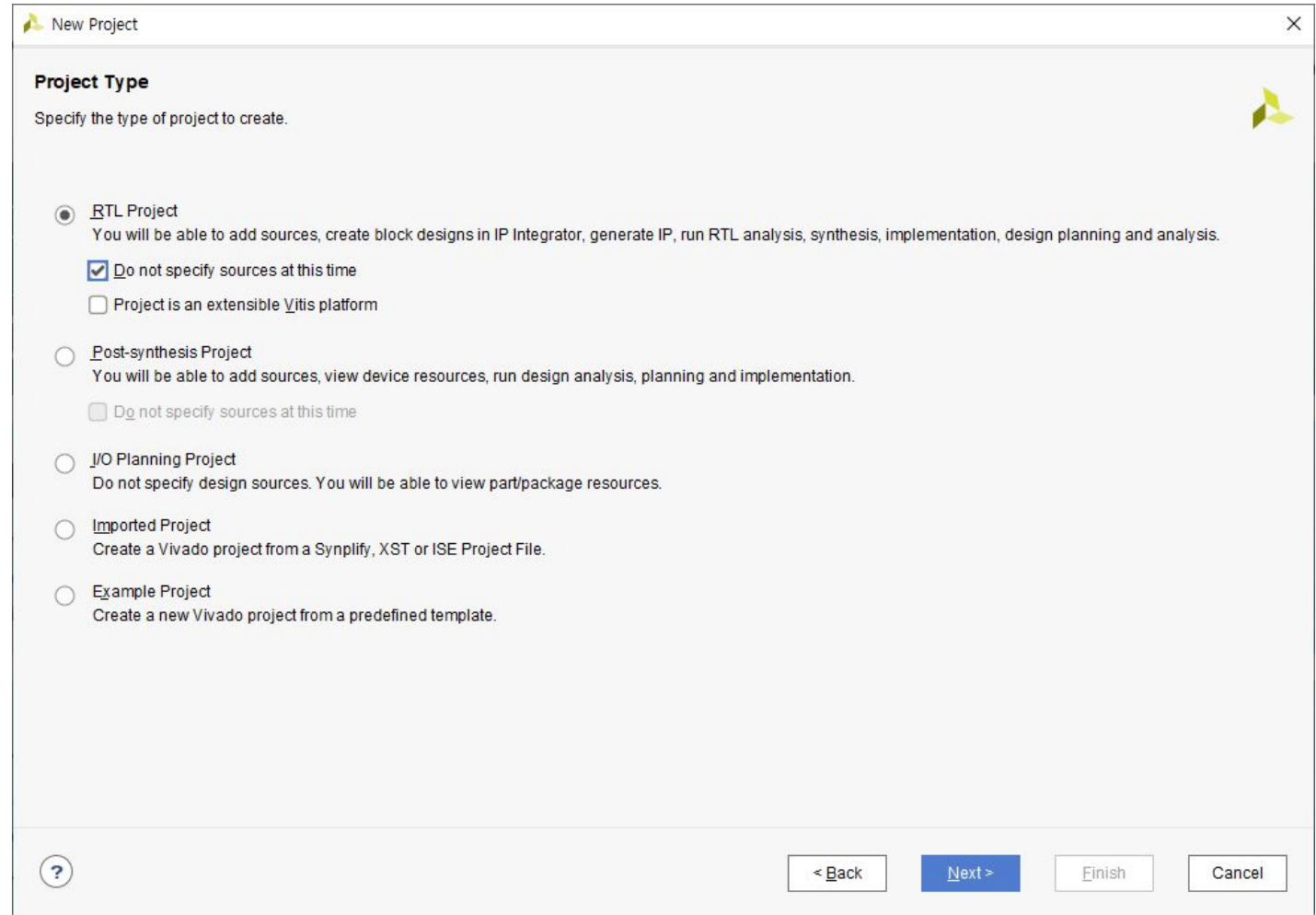
☒ Create project subdirectory

Project will be created at: C:/Users/example_adder

? < Back Next > Finish Cancel

2. Creating an example project

- Click next



The screenshot shows the 'New Project' dialog box in Vivado. The title bar says 'New Project' with a close button. The main area is titled 'Project Type' and contains the instruction 'Specify the type of project to create.' There are five radio button options: 'RTL Project' (selected), 'Post-synthesis Project', 'I/O Planning Project', 'Imported Project', and 'Example Project'. Each option has a description. Under 'RTL Project', there are two checkboxes: 'Do not specify sources at this time' (checked) and 'Project is an extensible Vitis platform' (unchecked). At the bottom, there is a help icon (question mark in a circle) and four buttons: '< Back', 'Next >' (highlighted in blue), 'Finish', and 'Cancel'.

New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time
☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

2. Creating an example project

- This is **board selection**
- For now, we will only simulate the design.
- Click next

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

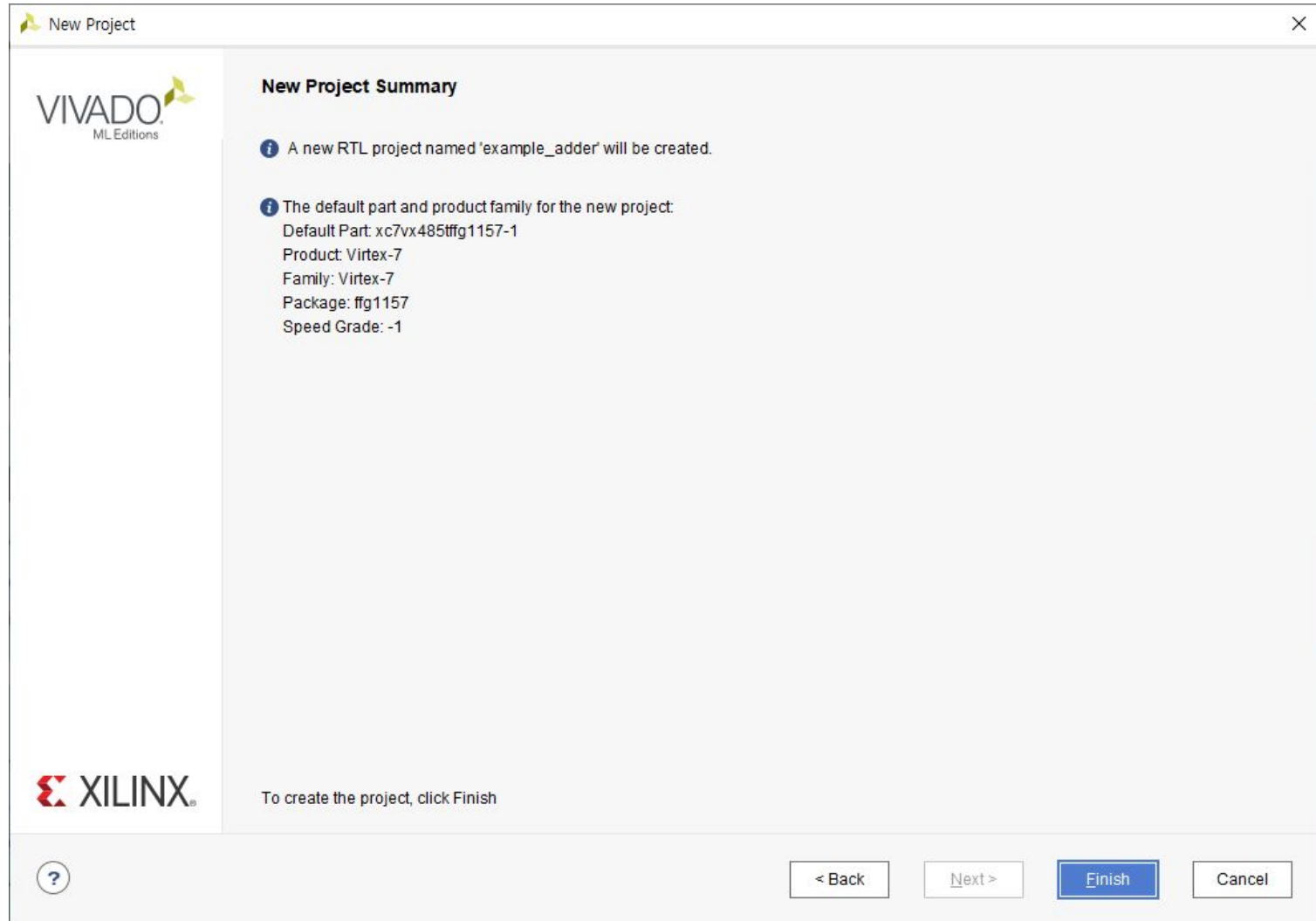
Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160	48	0
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800	48	0

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

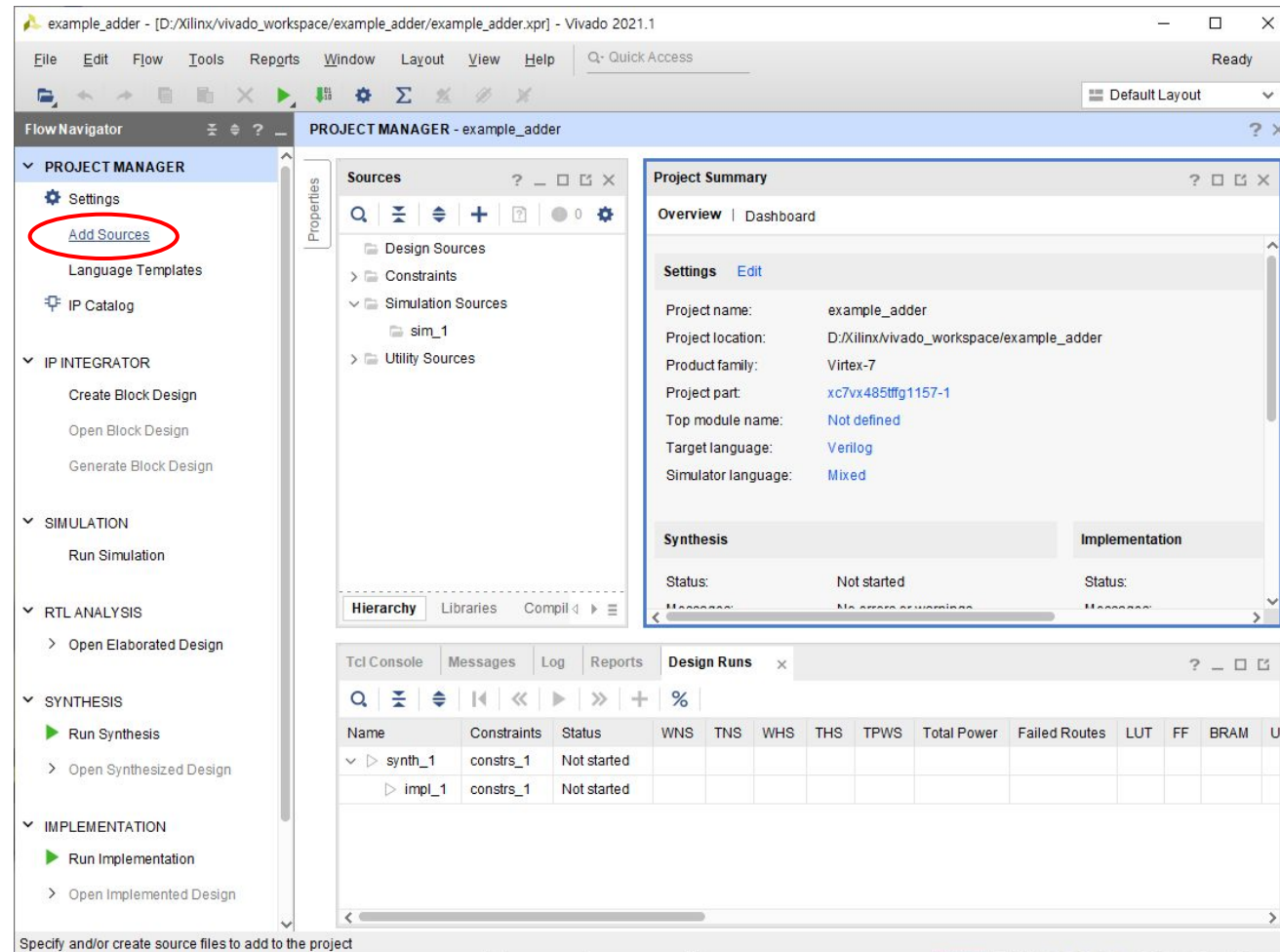
2. Creating an example project

- Click finish



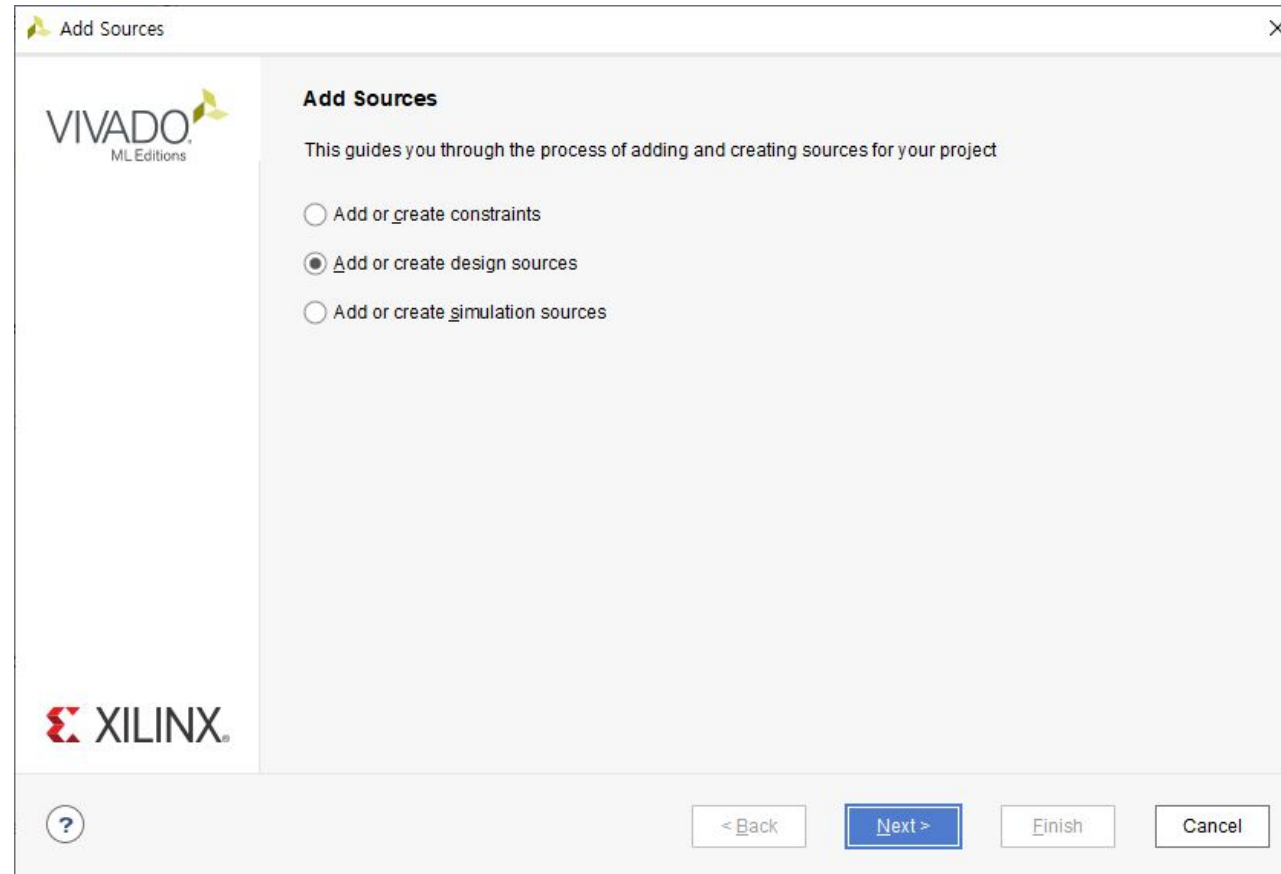
2. Creating an example project

- Click add sources



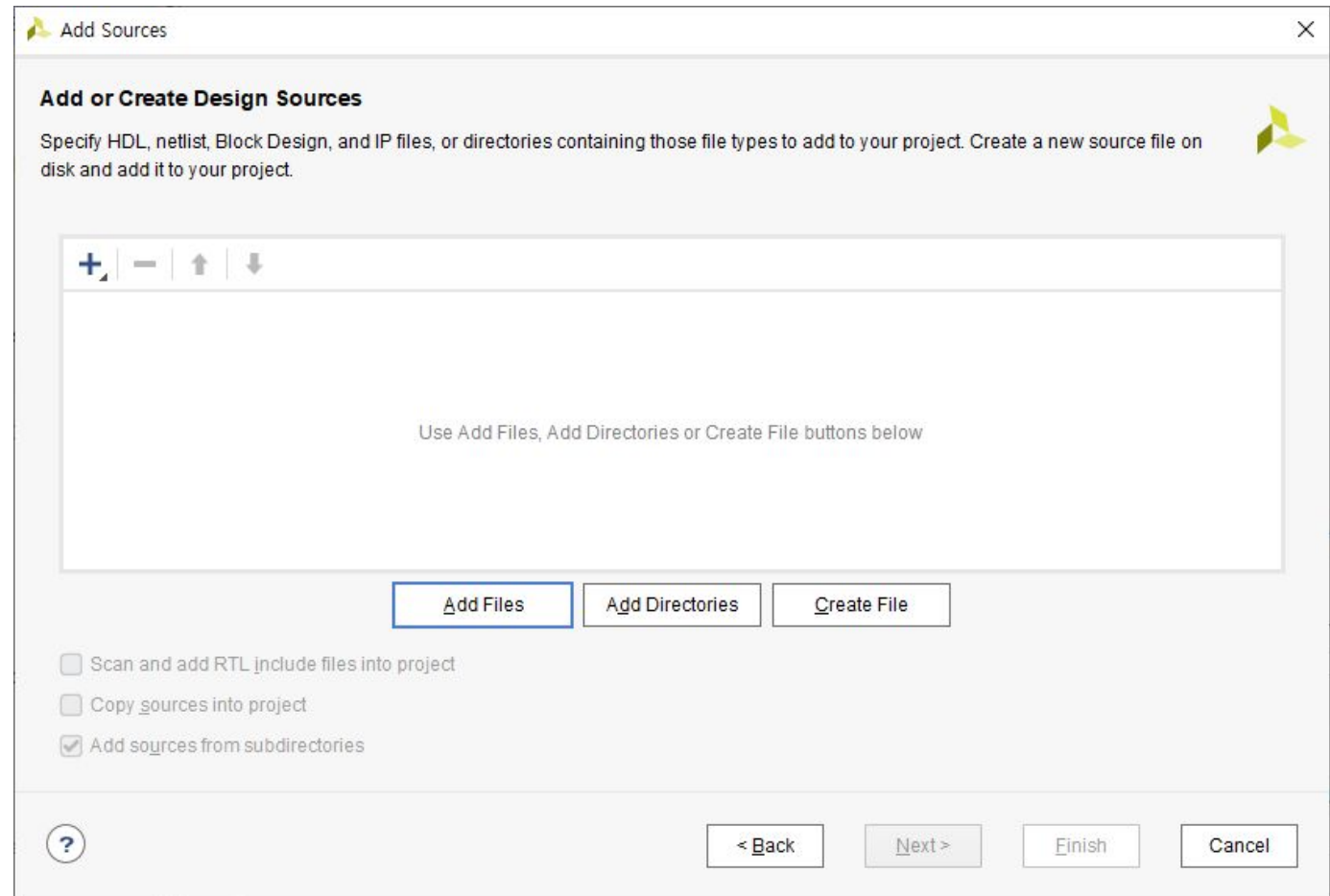
2. Creating an example project

- Select Add or create design sources



2. Creating an example project

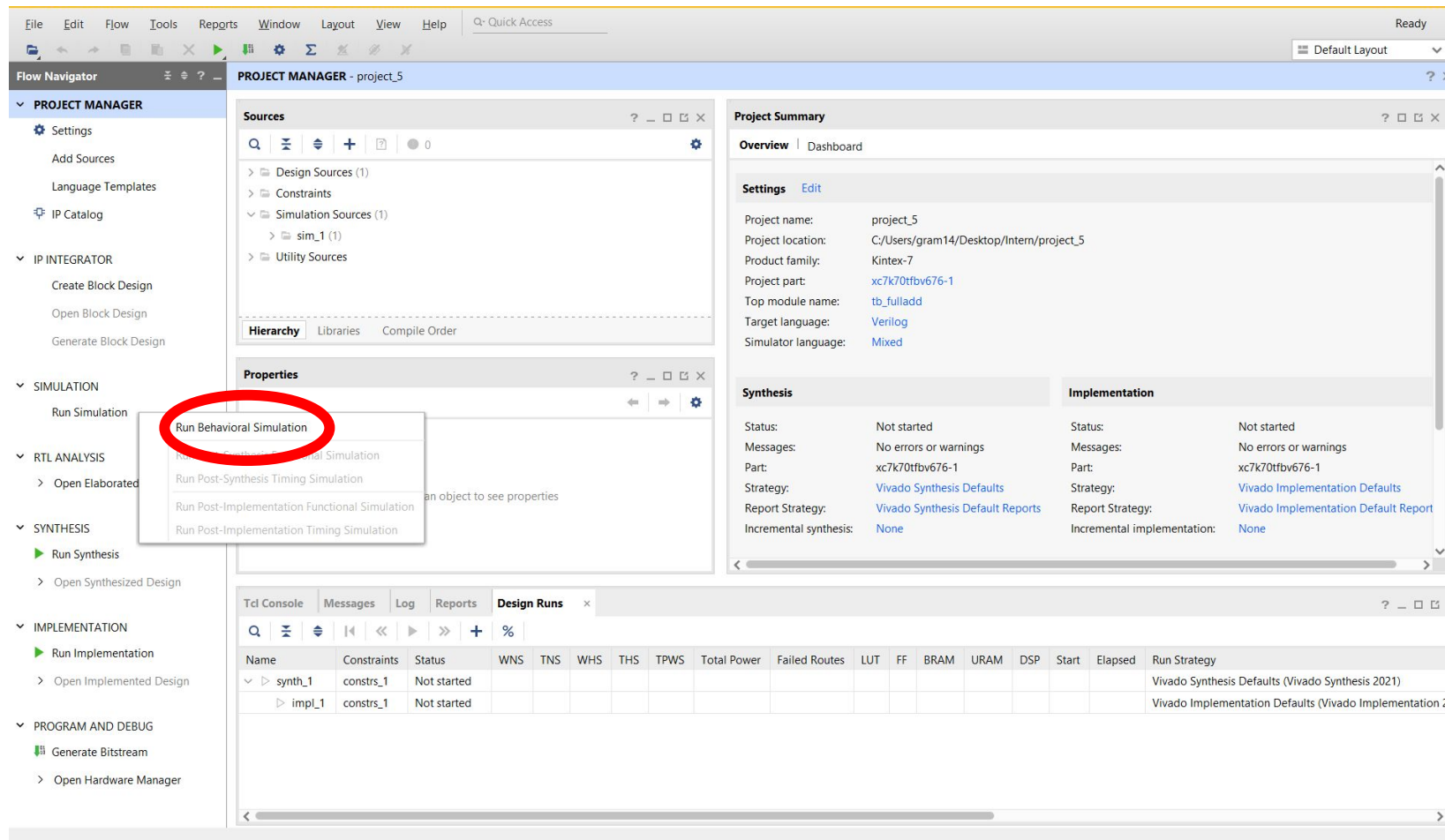
- Select Add Files
- Add the files(source code)
 - Ex)adder.v
 - Ex)adder_tb.v
- The example code is a simple 4-bit adder



3. Simulate the project

3. Simulation

- After adding the source files
- Click run simulation → run behavioral simulation



3. Simulation

- Check the simulation result

The screenshot displays the Xilinx Vivado IDE during a behavioral simulation. The main window is titled "SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_fulladd".

Project Manager: Shows the project structure with "tb_1" (Verilog M), "fulladd" (Verilog M), and "glbl" (Verilog M) under the "SIMULATION" tab.

Scope: Lists the signals being monitored: "a[3:0]", "b[3:0]", "c_in", "sum[3:0]", and "i[31:0]".

Tcl Console: Shows the simulation commands and results. The commands include "run 1000ns" and "a=0000, b=0000, c_in=0, sum=0000". The results show the values of the signals at each time step.

Waveform: Displays a timing diagram for the signals. The signals are "a[3:0]", "b[3:0]", "c_in", "sum[3:0]", and "i[31:0]". The time scale is 1000ns. The waveform shows the signals changing over time, with a vertical yellow line indicating the current time.

Messages: Shows the simulation logs and warnings. The messages include:

- [USF-XSim-8] Loading simulator feature
- [USF-XSim-96] XSim completed. Design snapshot 'tb_fulladd_behav' loaded.
- [USF-XSim-97] XSim simulation ran for 1000ns
- Simulation (2 warnings)
- sim_1 (2 warnings)
- [XSIM 43-4100] "C:/Users/gram14/Desktop/Intern/project_5/project_5.sim/sim_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design doesn't have timescale. (1 more like this)

Sim Time: 1 us