FMC LCD-Camera Module
User Manual
(FSKIII Only)

Libertron Co., Ltd

◆ Contents

✓ Revision History

Ver	Date	Revision
1.1	2020-08-14	1st Initial Version.

1. FMC LCD-Camera Module 개요 및 특징

1.1. 개요

최근 인공지능 산업의 시장확대에 따라 FPGA를 이용한 실시간 AI 영상처리에 대한 개발 및 교육 필요성이 증가되고 있습니다.
이에 물체의 인식 및 분류 등의 Edge AI 영상처리 어플리케이션 실습이 가능하도록 Camera와 LCD가 적용된 옵션보드를 개발하였습니다. FMC LCD-Camera Module의 입출력 인터페이스를 FMC 표준 커넥터로 설계하였고 이에 따라 자사 및 타사의 Evaluation Board 연결하여 사용할 때 구현하고자 하는 기능에만 집중할 수 있도록 구성하였습니다.

1.2. 제품 특징

- FMC (FPGA Mezzanine Card) LPC 적용
- 7인치 TFT-LCD (800x480 Pixel) 적용
- 7인치 Touch-Panel (5-Point) 적용
- Full HD Camera (1080P/30FPS) 적용
- PMOD 커넥터 2EA 적용

2. 제품 구성

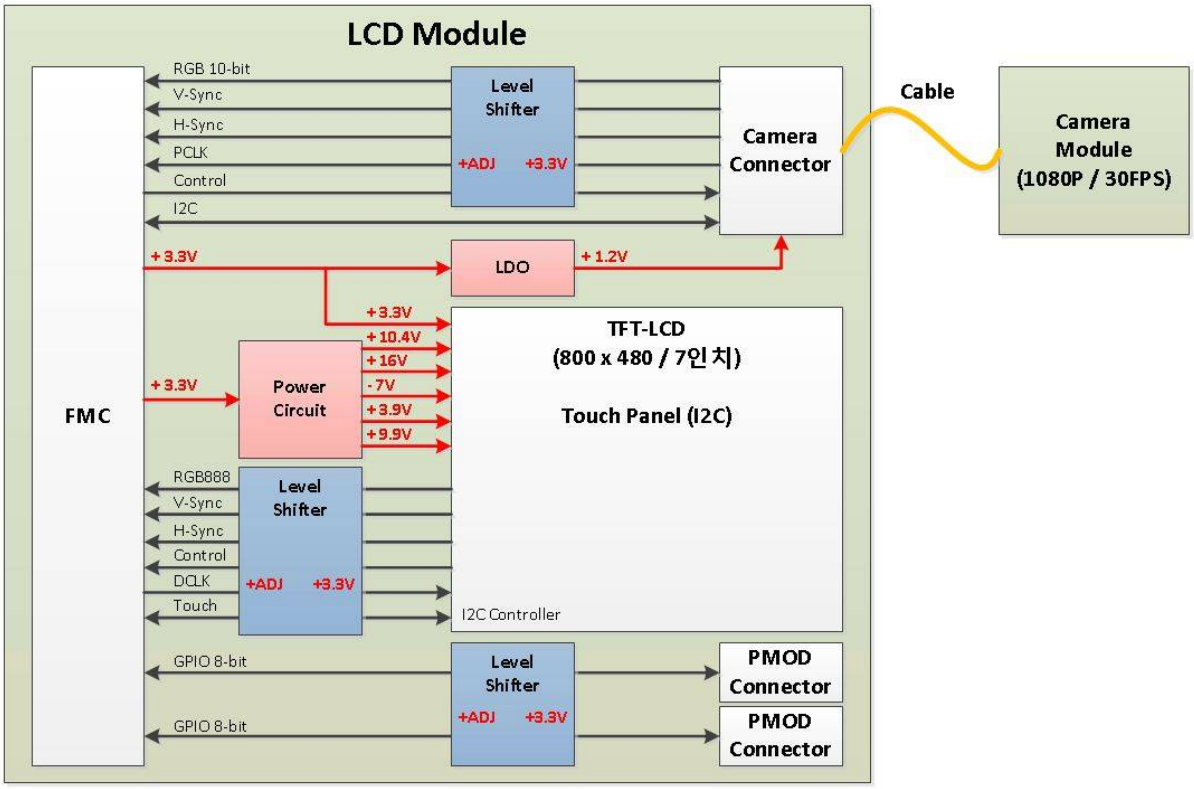
구성	수량	제품사진
LCD Module	**1**	
Camera Module	**1**	
Camera Cable	**1**	

3. Specification

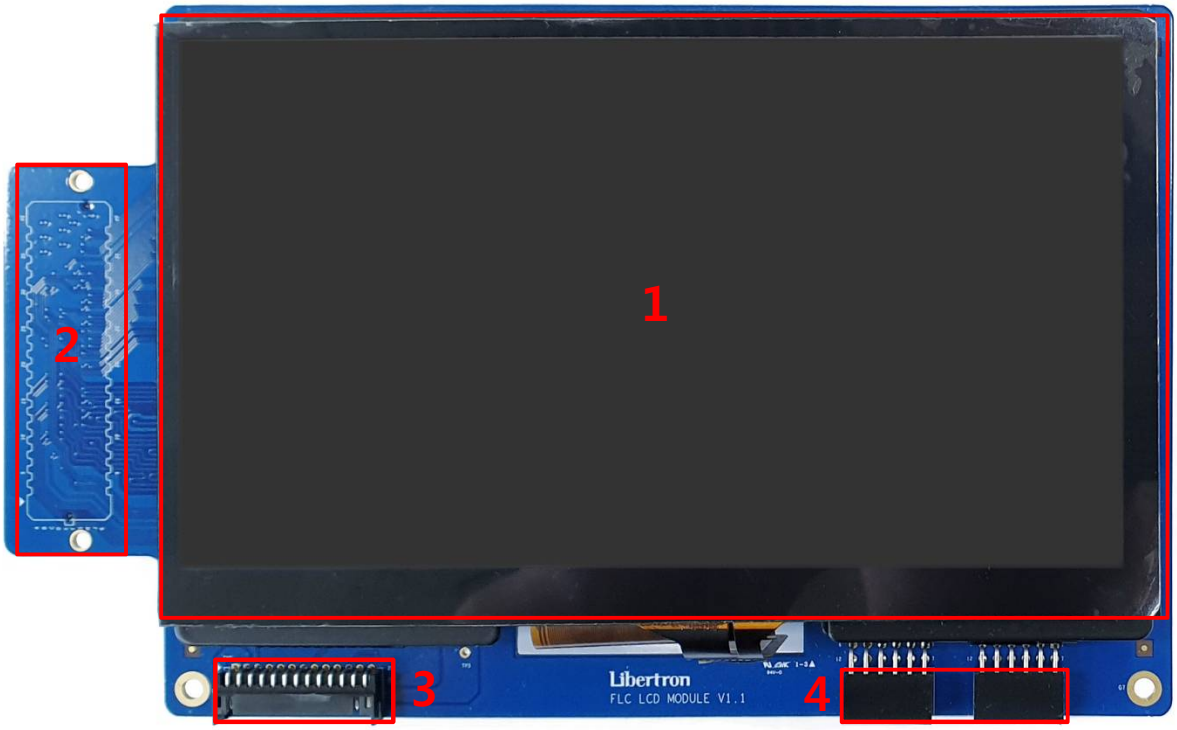
Item	Part	Spec	Note
Display	TFT-LCD	- 800 x 480 Pixel (7인치) - RGB Parallel Interface	
	Touch-Panel	- 7인치 CAP Touch (5-Point) - Controller IC 내장 (I2C)	
Camera	CMOS Image Sensor	- 1080P / 30FPS - Parallel Interface	
Connector	FMC	- Support VITA 57.1 (LPC x 1EA)	
	PMOD	- PMOD Connector x 2EA	
Power	Power Input	- FMC Power Input (+12V, +3.3V, ADJ)	
제품 size	LCD Module	- 205mm x 125mm (W x D) - Height : 40mm ~ 130mm (Adjustable)	
	Camera Module	- 60 x 60 x 17 (W x D x H)	

4. FMC LCD-Camera Module Description

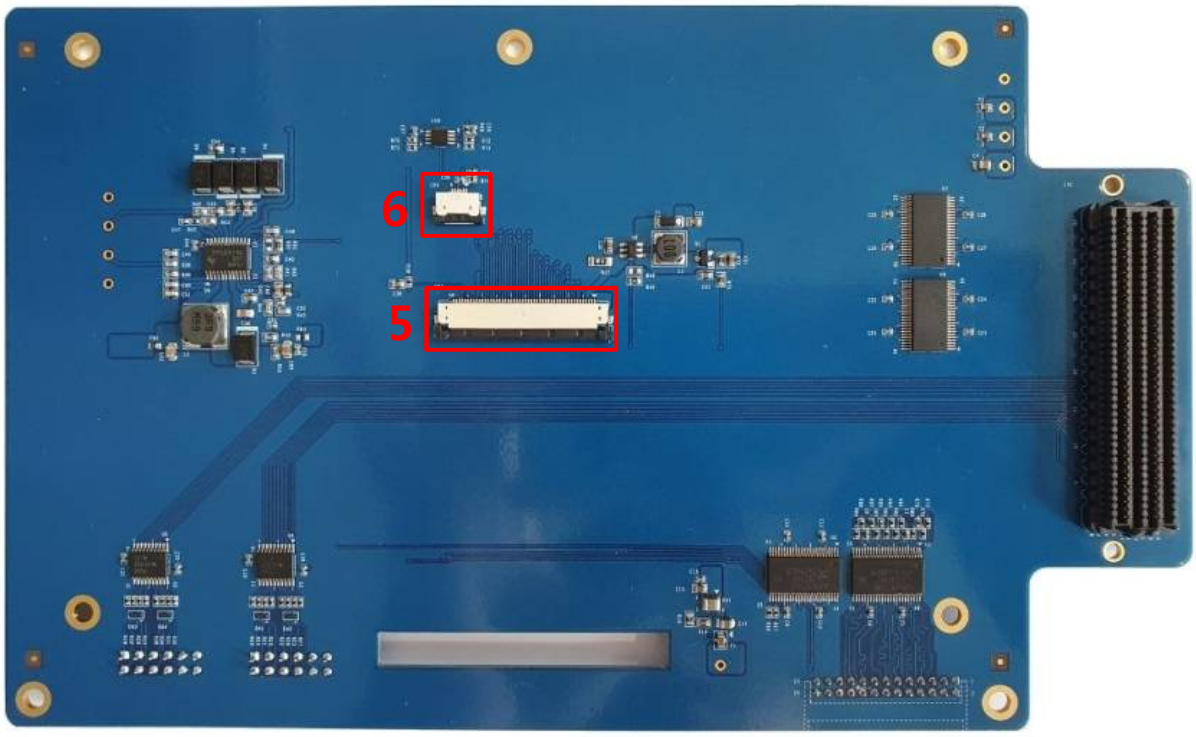
4.1. Block-Diagram



4.2. FMC LCD-Camera Module Location



<Top View>



<Bottom View>

- **FMC LCD-Camera Module Features**

Number	Feature	Schematic Page
1	TFT-LCD / Touch Panel	8 ~ 9 Page
2	Camera Connector	4 Page
3	PMOD Connector 2EA	5 Page
4	FMC (FPGA Mezzanine Card) LPC Connector	2 Page
5	LCD Connector	8 Page
6	Touch Connector	9 Page

4.2.1. TFT-LCD & Touch Panel

- TFT-LCD의 Resolution은 800 x 480 Pixel이며, Frame Rate는 60FPS까지 지원 합니다.
  Parallel 24bit (RGB888) 인터페이스를 사용합니다.
  사용자 편의성을 고려하여 30°~70°까지 기울기 조정이 가능 합니다.
- Touch Panel은 멀티 터치를 지원하며, 최대 5-Point까지 인식이 가능 합니다.
  Touch Controller가 포함 되어 있으며, FPGA와의 인터페이스는 I2C를 사용합니다.

4.2.2. FMC (FPGA Mezzanine Card) Connector

- 자사 제품 및 다른 Board와의 체결을 위하여 Samtec社의 FMC LPC "ASP-134604-01"을 적용하였으며, Description은 아래와 같습니다.

<FMC LPC Description>

FMC Pin Num	FMC Pin Name	Schematic Net Name	FSKIII FPGA Pin	Signal to Part
C2	DP0_C2M_P	No Connect	-	Not Used
C3	DP0_C2M_N			
C6	DP0_M2C_P			
C7	DP0_M2C_N			
C10	LA06_P	FMC_CAM_STDBY	W15	CN2, Camera Connector
C11	LA06_N	FMC_CAM_RST	W16	
C14	LA10_P	FMC_TOUCH_RST	T16	CN6, Touch Connector
C15	LA10_N	FMC_TOUCH_INT	U16	
C18	LA14_P	FMC_W_LED_CTRL	G21	U8, LCD Power Circuit
C19	LA14_N	FMC_LCD_DRV_CTRL	G22	U9, LCD Power Circuit
C22	LA18_P_CC	FMC_LCD_R7	E19	CN7, LCD Connector
C23	LA18_N_CC	FMC_LCD_R3	D19	
C26	LA27_P	FMC_LCD_B7	F19	
C27	LA27_N	FMC_LCD_B3	F20	
C30	SCL	CAM_SCL	T15	CN2, Camera Connector
C31	SDA	CAM_SDA	T14	
C34	GA0	No Connect	-	Not Used
C35	12P0V	VCC_12P0V	-	Power
C37	12P0V			
C39	3P3V	VCC_3P3V	-	

FMC Pin Num	FMC Pin Name	Schematic Net Name	FSKIII FPGA Pin	Signal to Part
D1	PG_C2M	No Connect	-	Not Used
D4	GBTCLK0_M2C_P			
D5	GBTCLK0_M2C_N			
D8	LA01_P_CC	FMC_CAM_MCLK	U15	CN2, Camera Connector
D9	LA01_N_CC	FMC_W_LED_EN	V15	U8, LCD Power Circuit
D11	LA05_P	FMC_CAM_D8	AA15	CN2, Camera Connector
D12	LA05_N	FMC_CAM_D9	AB15	
D14	LA09_P	FMC_CAM_D6	AB16	
D15	LA09_N	FMC_CAM_D7	AB17	
D17	LA13_P	FMC_CAM_D2	Y16	
D18	LA13_N	FMC_CAM_D5	AA16	
D20	LA17_P_CC	FMC_CAM_HS	B17	
D21	LA17_N_CC	FMC_CAM_VS	B18	
D23	LA23_P	FMC_LCD_MODE	E21	CN7, LCD Connector
D24	LA23_N	FMC_LCD_DE	D21	
D26	LA26_P	FMC_LCD_B0	E22	
D27	LA26_N	FMC_LCD_G4	D22	
D29	TCK	No Connect	-	Not Used
D30	TDI			
D31	TDO			
D32	3P3VAUX	VCC_3P3V	-	Power
D33	TMS	No Connect	-	Not Used
D34	TRST_L			
D35	GA1			
D36	3P3V	VCC_3P3V	-	Power
D38	3P3V			
D40	3P3V			

FMC Pin Num	FMC Pin Name	Schematic Net Name	FSKIII FPGA Pin	Signal to Part
G2	CLK1_M2C_P	FMC_CAM_PCLK	V13	CN2, Camera Connector
G3	CLK1_M2C_N	FMC_LCD_RSTB	V14	CN7, LCD Connector
G6	LA00_P_CC	FMC_PMOD_A4	Y11	CN3, PMOD Connector
G7	LA00_N_CC	FMC_PMOD_A3	Y12	
G9	LA03_P	FMC_PMOD_A2	AA13	
G10	LA03_N	FMC_PMOD_A5	AB13	
G12	LA08_P	FMC_CAM_D4	Y13	CN2, Camera Connector
G13	LA08_N	FMC_CAM_D3	AA14	
G15	LA12_P	FMC_CAM_D1	W14	
G16	LA12_N	FMC_CAM_D0	Y14	
G18	LA16_P	FMC_PMOD_B2	F18	CN4, PMOD Connector
G19	LA16_N	FMC_PMOD_B5	E18	
G21	LA20_P	FMC_LCD_B6	D20	CN7, LCD Connector
G22	LA20_N	FMC_LCD_B5	C20	
G24	LA22_P	FMC_LCD_B1	C18	
G25	LA22_N	FMC_LCD_G6	C19	
G27	LA25_P	FMC_LCD_G3	C22	
G28	LA25_N	FMC_LCD_G1	B22	
G30	LA29_P	FMC_LCD_R6	B21	
G31	LA29_N	FMC_LCD_R5	A21	
G33	LA31_P	FMC_LCD_R1	B20	
G34	LA31_N	FMC_LCD_R0	A20	
G36	LA33_P	FMC_LCD_UPDN	A18	
G37	LA33_N	FMC_TOUCH_SDA	A19	CN6, Touch Connector
G39	VADJ	VADJ_FMC	-	Power

FMC Pin Num	FMC Pin Name	Schematic Net Name	FSKIII FPGA Pin	Signal to Part
H4	CLK0_M2C_P	FMC_LCD_DCLK	W11	CN7, LCD Connector
H5	CLK0_M2C_N	FMC_PMOD_A8	W12	CN3, PMOD Connector
H7	LA02_P	FMC_PMOD_A7	AB11	
H8	LA02_N	FMC_PMOD_A6	AB12	
H10	LA04_P	FMC_PMOD_A1	AA9	
H11	LA04_N	FMC_PMOD_B8	AB10	CN4, PMOD Connector
H13	LA07_P	FMC_PMOD_B4	AA10	
H14	LA07_N	FMC_PMOD_B7	AA11	
H16	LA11_P	FMC_PMOD_B3	V10	
H17	LA11_N	FMC_PMOD_B6	W10	
H19	LA15_P	FMC_LCD_HSD	C14	CN7, LCD Connector
H20	LA15_N	FMC_LCD_VSD	C15	
H22	LA19_P	FMC_LCD_B4	D17	
H23	LA19_N	FMC_LCD_B2	C17	
H25	LA21_P	FMC_LCD_G7	B15	
H26	LA21_N	FMC_LCD_G5	B16	
H28	LA24_P	FMC_LCD_G2	D14	
H29	LA24_N	FMC_LCD_G0	D15	
H31	LA28_P	FMC_LCD_R4	C13	
H32	LA28_N	FMC_LCD_R2	B13	
H34	LA30_P	FMC_PMOD_B1	A15	CN4, PMOD Connector
H35	LA30_N	FMC_LCD_SHLR	A16	CN7, LCD Connector
H37	LA32_P	FMC_LCD_DITH	A13	
H38	LA32_N	FMC_TOUCH_SCL	A14	CN6, Touch Connector
H40	VADJ	VADJ_FMC	-	Power

4.2.3. Camera Connector

- Camera Module을 연결하는 Connector로 연호전자 社의 "YDAW200-26"를 적용하였으며, Description은 아래와 같습니다.

<Camera Connector Description>

CN2 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
1	GND	Digital Ground	-	-
2	GND	Digital Ground	-	-
3	VCC_1P2V	Digital Power 1.2V	-	-
4	VCC_3P3V	Digital Power 3.3V	-	-
5	CAM_MCLK	Camera Master Clock "27MHz"	U15	Output
6	CAM_D9	Parallel Pixel Data	AB15	Input
7	CAM_D8	Parallel Pixel Data	AA15	Input
8	CAM_D7	Parallel Pixel Data	AB17	Input
9	CAM_D6	Parallel Pixel Data	AB16	Input
10	CAM_D5	Parallel Pixel Data	AA16	Input
11	CAM_D4	Parallel Pixel Data	Y13	Input
12	CAM_D3	Parallel Pixel Data	AA14	Input
13	CAM_D2	Parallel Pixel Data	Y16	Input
14	CAM_PCLK	Pixel Clock	V13	Input
15	CAM_SCL	Serial Interface Clock	T15	Output
16	CAM_SDA	Serial Interface Data	T14	In/Out
17	CAM_D1	Parallel Pixel Data	W14	Input
18	CAM_D0	Parallel Pixel Data	Y14	Input
19	CAM_VS	Vertical Sync	B18	Input
20	CAM_STDBY	Power Down Operation "Active High"	W15	Output
21	CAM_RST	Camera System Reset "Active Low"	W16	Output
22	CAM_HS	Horizontal Sync	B17	Input
23	VCC_3P3V	Digital Power 3.3V	-	-
24	VCC_1P2V	Digital Power 1.2V	-	-
25	GND	Digital Ground	-	-
26	GND	Digital Ground	-	-

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

4.2.4. PMOD Connector

- PMOD Connector 2-Port를 제공하며 SULLINS 社의 "PPTC062LJBN-RC" 를 적용하였으며, PMOD Interface를 위한 Description은 아래와 같다.

<PMOD Connector Pin Description>

CN3 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
1	PMOD_A1	PMOD Signal	AA9	In/Out
2	PMOD_A2	PMOD Signal	AA13	In/Out
3	PMOD_A3	PMOD Signal	Y12	In/Out
4	PMOD_A4	PMOD Signal	Y11	In/Out
5	GND	Digital Ground	-	-
6	VCC_3P3V	Digital Power 3.3V	-	-
7	PMOD_A5	PMOD Signal	AB13	In/Out
8	PMOD_A6	PMOD Signal	AB12	In/Out
9	PMOD_A7	PMOD Signal	AB11	In/Out
10	PMOD_A8	PMOD Signal	W12	In/Out
11	GND	Digital Ground	-	-
12	VCC_3P3V	Digital Power 3.3V	-	-

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

CN4 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
1	PMOD_B1	PMOD Signal	A15	In/Out
2	PMOD_B2	PMOD Signal	F18	In/Out
3	PMOD_B3	PMOD Signal	V10	In/Out
4	PMOD_B4	PMOD Signal	AA10	In/Out
5	GND	Digital Ground	-	-
6	VCC_3P3V	Digital Power 3.3V	-	-
7	PMOD_B5	PMOD Signal	E18	In/Out
8	PMOD_B6	PMOD Signal	W10	In/Out
9	PMOD_B7	PMOD Signal	AA11	In/Out
10	PMOD_B8	PMOD Signal	AB10	In/Out
11	GND	Digital Ground	-	-
12	VCC_3P3V	Digital Power 3.3V	-	-

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

4.2.5. LCD Connector

- TFT-LCD를 연결하는 Connector로 연호전자 社의 "05004HR-H50ED"를 적용하였으며, Description은 아래와 같다.

<LCD Connector Description>

CN7 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
1	LCD_VLED+	LED Backlight (Anode)	-	-
2	LCD_VLED+	LED Backlight (Anode)	-	-
3	LCD_VLED-	LED Backlight (Cathode)	-	-
4	LCD_VLED-	LED Backlight (Cathode)	-	-
5	GND	Digital Ground	-	-
6	LCD_VCOM	Common Voltage	-	-
7	LCD_3P3V	Digital Power 3.3V	-	-
8	LCD_MODE	DE/SYNC Mode Select - H : DE Mode - L : HSD/VSD Mode	E21	Output
9	LCD_DE	Data Enable	D21	Output
10	LCD_VSD	Vertical Sync	C15	Output
11	LCD_HSD	Horizontal Sync	C14	Output
12	LCD_B7	Blue Data (MSB)	F19	Output
13	LCD_B6	Blue Data	D20	Output
14	LCD_B5	Blue Data	C20	Output
15	LCD_B4	Blue Data	D17	Output
16	LCD_B3	Blue Data	F20	Output
17	LCD_B2	Blue Data	C17	Output
18	LCD_B1	Blue Data	C18	Output
19	LCD_B0	Blue Data (LSB)	E22	Output
20	LCD_G7	Green Data (MSB)	B15	Output
21	LCD_G6	Green Data	C19	Output
22	LCD_G5	Green Data	B16	Output
23	LCD_G4	Green Data	D22	Output
24	LCD_G3	Green Data	C22	Output
25	LCD_G2	Green Data	D14	Output
26	LCD_G1	Green Data	B22	Output
27	LCD_G0	Green Data (LSB)	D15	Output
28	LCD_R7	Red Data (MSB)	E19	Output
29	LCD_R6	Red Data	B21	Output
30	LCD_R5	Red Data	A21	Output

CN7 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
31	LCD_R4	Red Data	C13	Output
32	LCD_R3	Red Data	D19	Output
33	LCD_R2	Red Data	B13	Output
34	LCD_R1	Red Data	B20	Output
35	LCD_R0	Red Data (LSB)	A20	Output
36	GND	Digital Ground	-	-
37	LCD_DCLK	LCD Pixel Clock "33.3MHz"	W11	Output
38	GND	Digital Ground	-	-
39	LCD_SHLR	Left / Right Display Control	A16	Output
40	LCD_UPDN	Up / Down Display Control	A18	Output
41	LCD_VGH	Positive Power for TFT	-	-
42	LCD_VGL	Negative Power for TFT	-	-
43	LCD_AVDD	Analog Power	-	-
44	LCD_RSTB	LCD Reset "Active Low"	V14	Output
45	No Connect	-	-	-
46	LCD_VCOM	Common Voltage	-	-
47	LCD_DITH	Dithering Setting - H : 6-bit Resolution - L : 8-bit Resolution	A13	Output
48	GND	Digital Ground	-	-
49	No Connect	-	-	-
50	No Connect	-	-	-

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

4.2.6. LCD Power Enable

<LCD Power Enable Description>

FMC Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
C19	LCD_DRV_CTRL	LCD Power Drive (Default High)	G22	Output
D9	W_LED_EN	Backlight Power Enable - H : Power Off (Default) - L : Power On	V15	Output
C18	W_LED_CTRL	Backlight Bright Control - PWM 제어 (Default Low)	G21	Output

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

4.2.7. Touch Connector

- Touch-Panel을 연결하는 Connector로 연호전자 社의 "05003HR-H06ED"를 적용하였으며, Description은 아래와 같다.

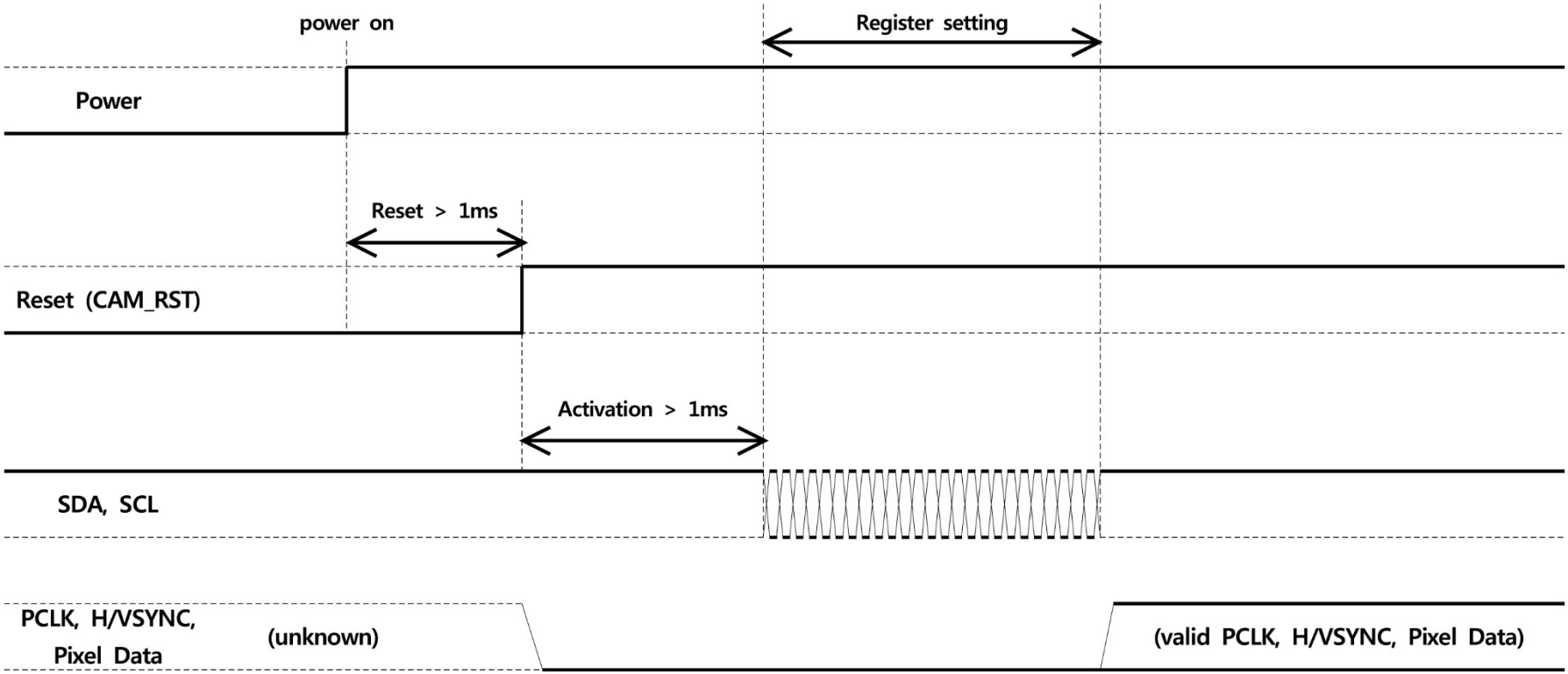
<Touch Connector Description>

CN2 Pin Num	Schematic Net Name	Description	FSKIII FPGA Pin	Pin Type
1	TOUCH_RST	Touch-Panel Reset "Active Low"	T16	Output
2	LCD_3P3V	Digital Power 3.3V	-	-
3	GND	Digital Ground	-	-
4	TOUCH_INT	Interrupt	U16	In/Out
5	TOUCH_SDA	Serial Interface Data	A19	In/Out
6	TOUCH_SCL	Serial Interface Clock	A14	Output

※ Pin Type Input / Output 기준은 FPGA를 기준으로 합니다.

5. Camera Module Interface

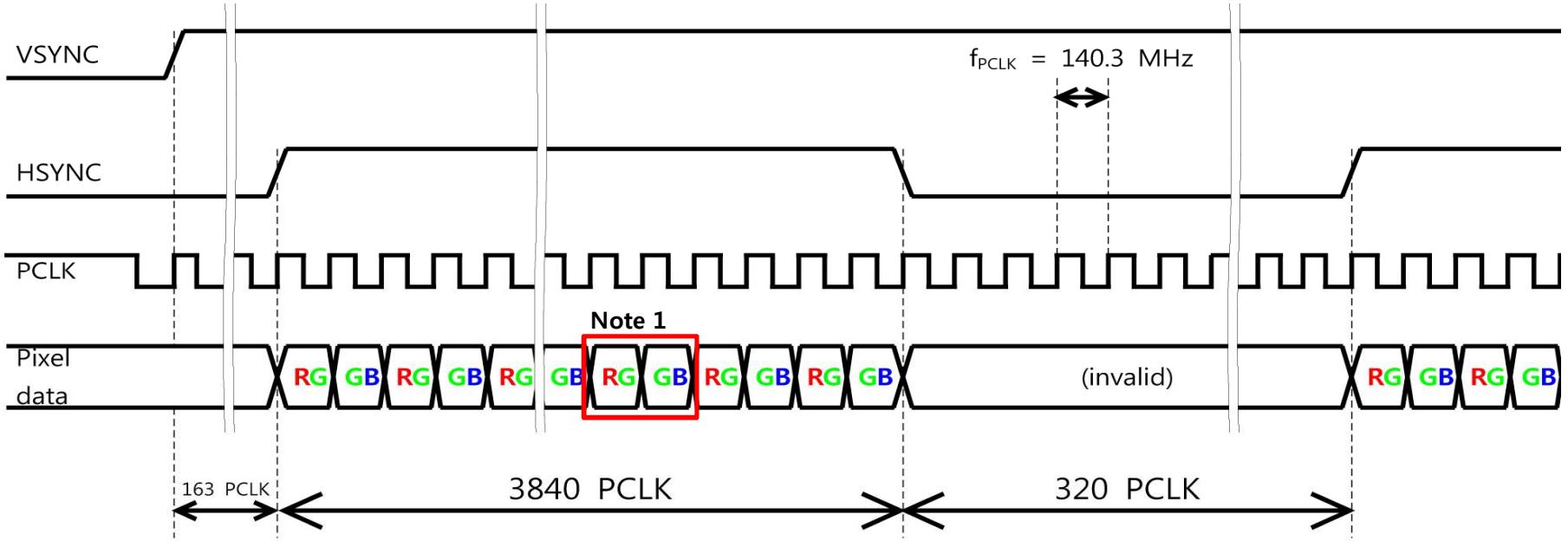
5.1. Initialize



1. Camera Register Setting은 I2C 인터페이스를 사용하며, 리버트론에서 제공하는 Setting Table을 참고하시기 바랍니다.
2. Power Off 하지 않고 Camera Register Setting을 변경할 경우에는, Reset Active Sequence부터 진행합니다.

5.2. Data Format

5.2.1. RGB565 Format



※ Note 1 : RGB 565 pixel data format bit mapping

	MSB									LSB	MSB									LSB
	RG (10 Bit)										GB (10 Bit)									
Bitmap (20 bit)	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	Not Use	Not Use	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	Not Use	Not Use
RGB565 (16 Bit)	R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] B[4] B[3] B[2] B[1] B[0]																			

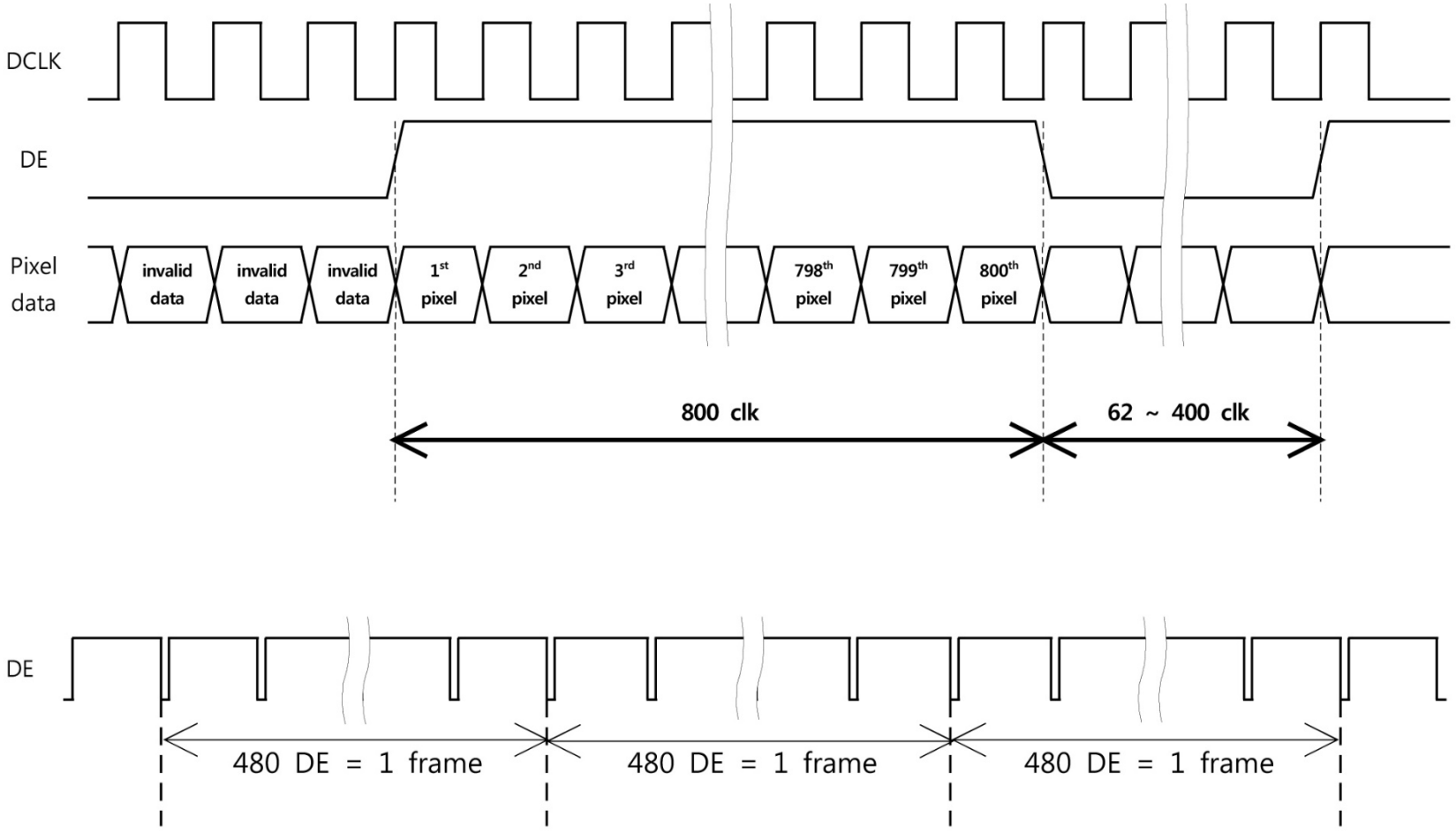
6. LCD Interface

6.1. Timing Parameter

Parameter Name	Symbol	Value			Unit	Remark
		Min	Typical	Max		
DCLK Frequency	fclk	26.4	33.3	46.8	MHz	
Horizontal Display Area	thd	800	800	800	DCLK	
HSYNC Pulse Width	thpw	1	-	40	DCLK	
HSYNC Blanking	thb	46	46	46	DCLK	
HSYNC Front Porch	thfp	16	210	354	DCLK	
One Horizontal Line	th	862	th = thd + thb + thfp	1200	DCLK	
Vertical Display Area	tvd	480	480	480	th	
VSYNC Pulse Width	tvpw	1	-	20	th	
VSYNC Blanking	tvb	23	23	23	th	
VSYNC Front Porch	tvfp	7	22	147	th	
VSYNC Period Time	tv	510	tv = tvd + tvb + tvfp	650	th	

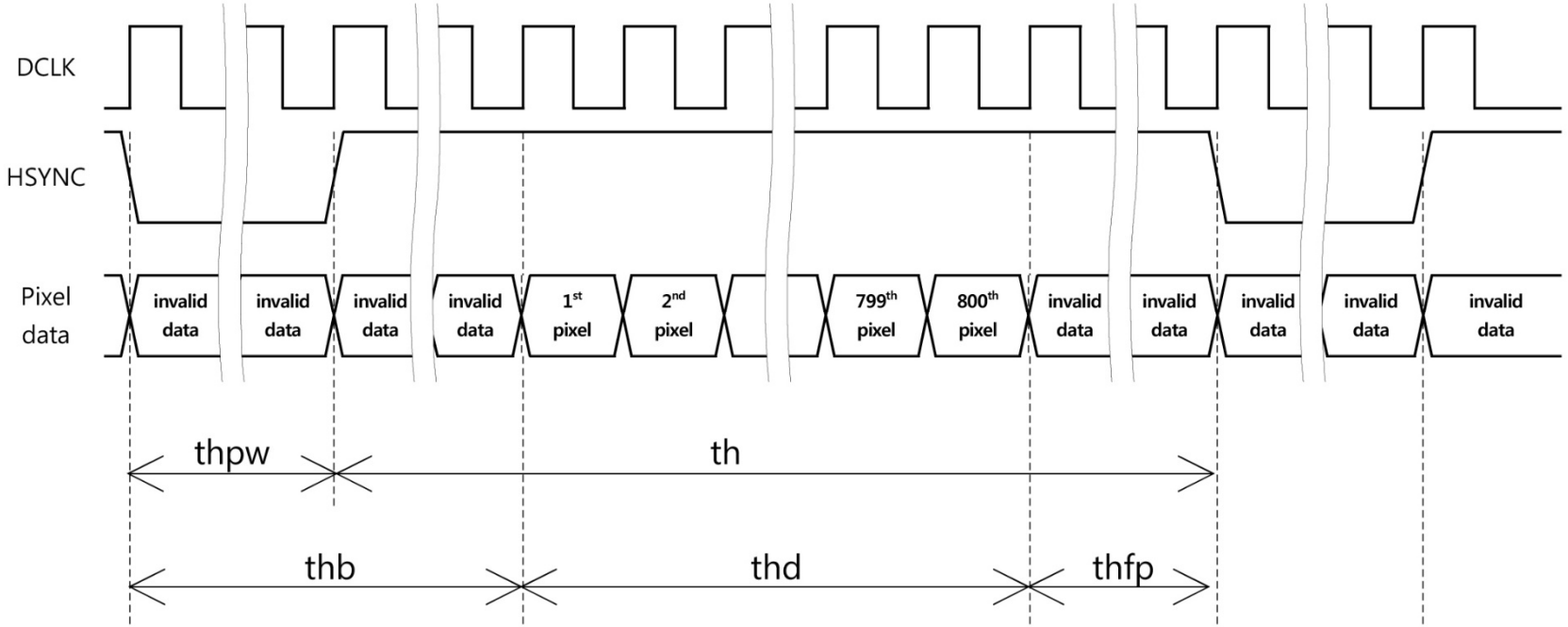
6.2. Timing Diagram

6.2.1. DE Mode (MODE Pin: High)

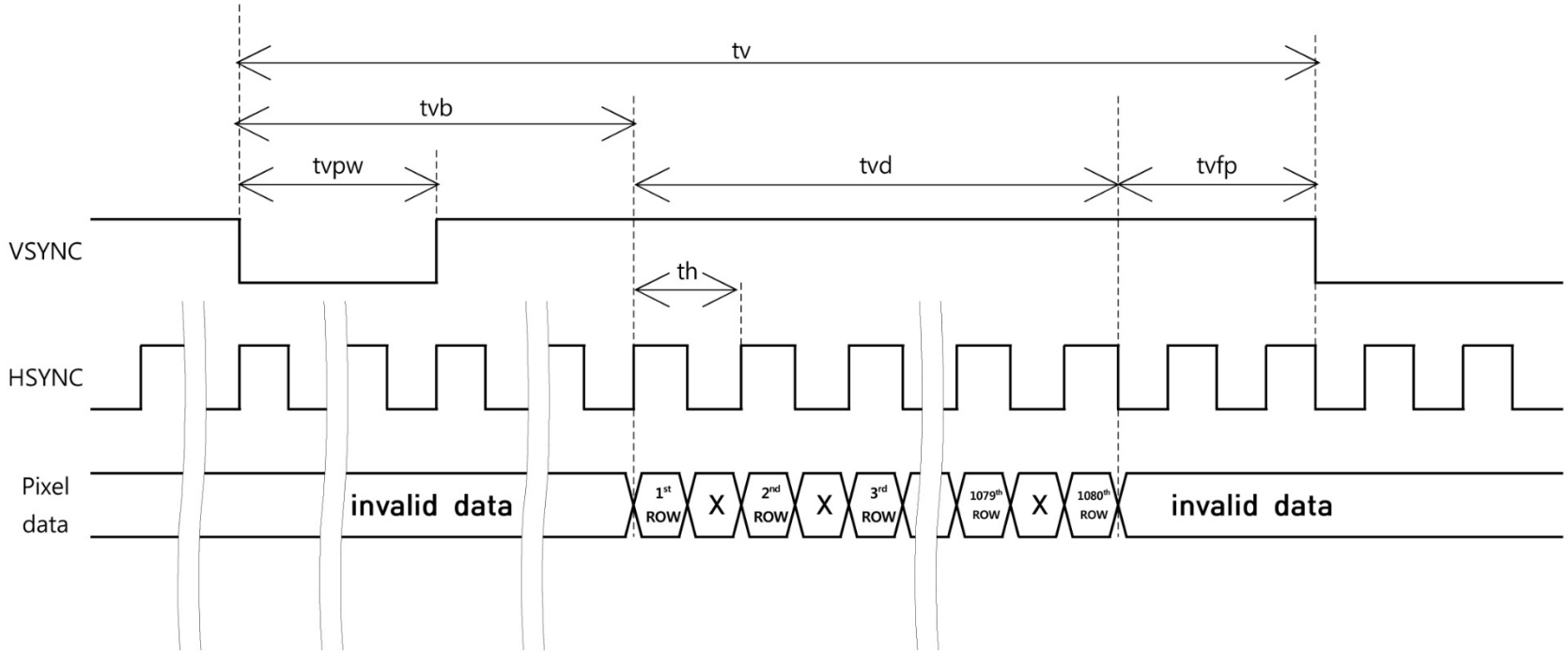


6.2.2. HSD/VSD Mode (MODE Pin: Low)

- HSYNC Timing

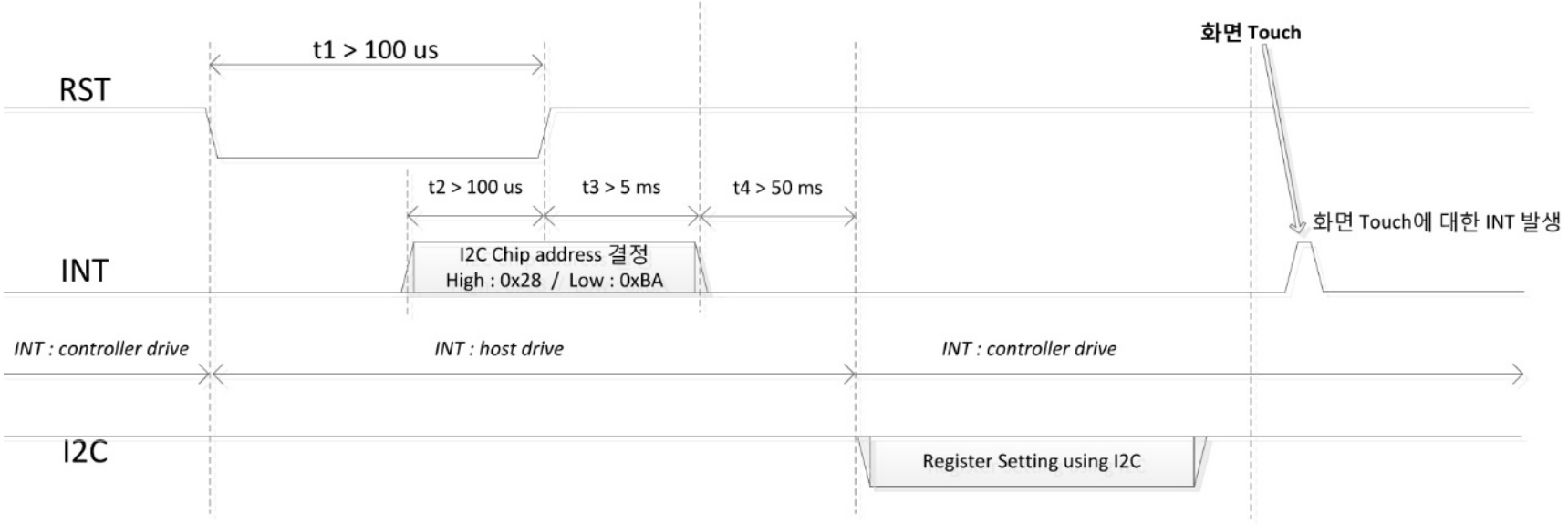


- VSYNC Timing



7. Touch Panel Interface

7.1. Initialize



1. 센서를 초기화 하기 위해 RST 신호는 100μs 이상 Low로 유지한다.
   - RST 신호가 Low 일 때, Host (FPGA)가 INT를 제어 해야 한다.
2. Host (FPGA)는 RST의 Rising Edge부터 적어도 100μs 이전에 INT를 High 혹은 Low로 제어하여 I2C Chip Address를 설정 한다.
   - High: I2C Chip Address 0x28으로 설정
   - Low: I2C Chip Address 0xBA으로 설정
3. Host (FPGA)는 RST의 Rising Edge 이후에도 5ms 이상 INT의 상태를 유지해야 한다.
4. Controller (GT911)는 INT의 Falling Edge 부터 50ms 이후부터 INT Signal을 통해 Interrupt를 발생 시킨다.