EITF35 Template

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By

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(Template by Liang Liu, updated 2017-08-15)

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2017

Abstract

Here are my most important results described, including 1) what has been implemented, 2) which algorithms have been used, 3) which architecture has been used, 3) what is the implementation result. The abstract is usually without abbreviations and references.

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Design specifications

This session briefly describes the design specifications, including functionality and performance requirement.

FSM and FSMD

This session describes the finite state machine (with data path) of the assignment. ASMD (Algorithmic state machine with data-path) of the entire system (or the main part of the system) should be presented and explained.

Figures

Fig 1.wmf

1. Three objects before the Eclipse.

The figure captions, in IEEE style, are written as “Fig. 1.” A figure is often referred in the text as “Fig. 1”, i.e. not as “Figure 1”. Whatever you choose, be consequent!

Equations

All equations should be referred in the text, usually on the IEEE form: “The function is shown in (1)”, not as “The function is shown in equation (1)”, or “The function is shown in equ. (1)”. The only exception is when the sentence starts with a reference, i.e. “Equation (1), shows the function” is correct but not “(1), shows the function” in the beginning of a sentence.

|  |  |
| --- | --- |
|  | (1) |

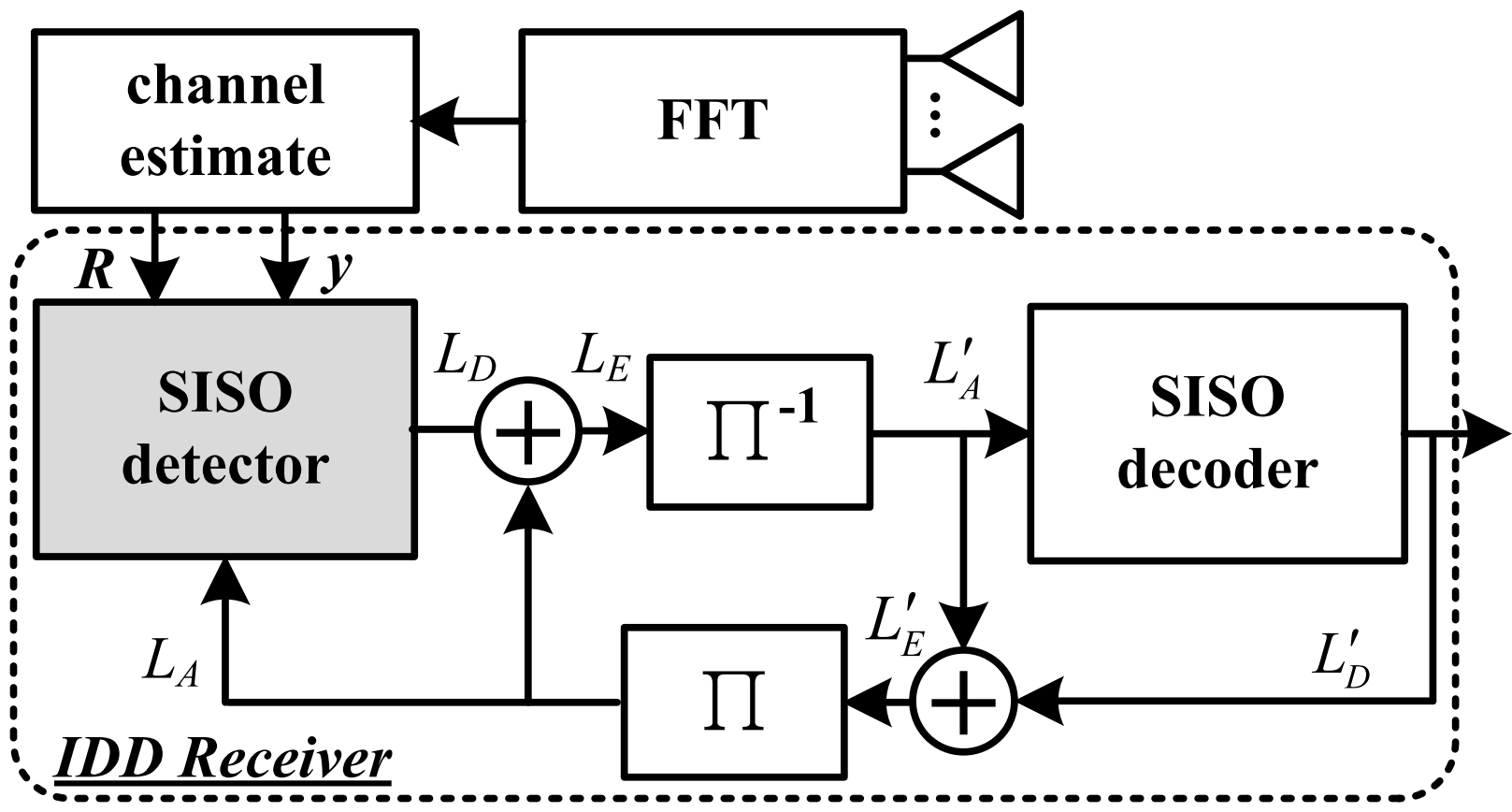
Update Field

When changes are done in captions and cross references, the numbering might need an update. That can be done by right clicking in the text of the caption or cross reference. F9 updates the field as well and CTRL+a followed by F9 update all fields in the document.

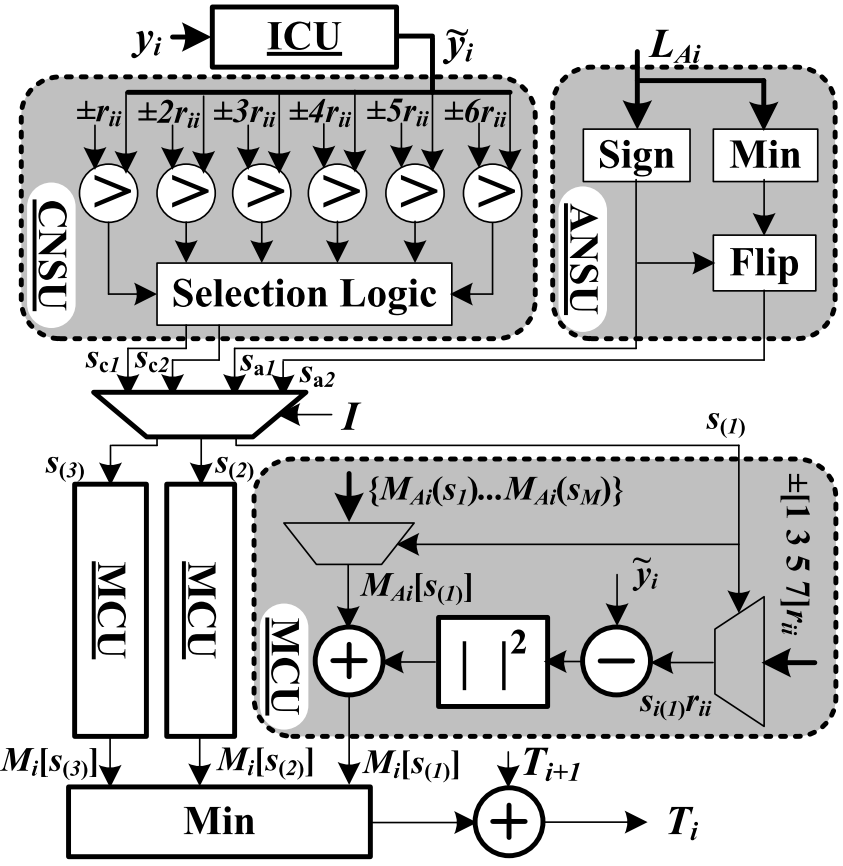
Hardware architecture

This session describes the hardware architecture of the implementation. System level block diagram should be included. The (lower level) diagrams of the key function blocks should also be included.

Examples of the system level and lower level block diagrams



1. System-level block diagram.



1. System-level block diagram.

Implementation results and analysis

FPGA implementation

This session presents the FPGA implementation results, including the resource utilization and timing performance. Generally, tables are used to report implementation results. Here is an example of a table.

1. Example of rounding percentages

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Value | Rounded | Add ε = 0.01 | Rounded |
| A | 40.43 | 40 | 40.44 | 40 |
| B | 32.47 | 32 | 32.48 | 32 |
| C | 16.99 | 17 | 17.00 | 17 |
| D | 9.49 | 9 | 9.50 | 10 |
| E | 0.62 | 1 | 0.63 | 1 |
| Total (%) | 100 | 99 | 100.05 | 100 |

Result analysis

It is important to analyze the implementation results. This can include what can be done if need to improve your implementation in terms of area and/or speed.