Total No. of Questions: 25

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Roll No. _____

3EU3023

B.Tech. III-Sem. (Main/Back) Exam Jan. 2019
Computer Science Engineering
3CSU03 Digital Electronics
3EU3023
(Common to CS/IT)

Time: 03 Hours

Maximum Marks: 100

Min.Passing marks: 33

Instructions to candidates: -

PART A : Short answer questions (up to 25 words) 10 x 2 marks = 20 marks. All ten questions are compulsory.

PART B : Analytical/Problem Solving questions (up to 100 words) 6 x 5 marks = 30 marks. Candidates have to answer six questions out of eight.

PART C : Descriptive/Analytical/Problem solving questions 5 x 10 marks = 50 marks. Candidates have to answer five questions out of seven

PART A

1. What are universal gates? Why are they called so?
2. Represent decimal number (127) in Excess-3, BCD and Gray code
3. Simplify: F= (AB'+A'B)' (A+B).
4. How many 2:1 Multiplexer will be required to realize 128:1 Multiplexer? What is the use of select line in MUX?
5. What is Race around condition?
6. Explain Half Adder circuit. Also give its circuit realization.
7. Differentiate between synchronous and asynchronous counters.
8. Explain in short Universal shift register
9. What do you mean by prime implicants and essential prime implicants?

10. Differentiate between combinational circuits and sequential circuits.

PART B

1. Explain Master slave JK flip-flop in details.
2. Design a 3-bit synchronous Up/Down counters.
3. Implement a Full Subtracter using a 3 to 8 Decoder.
4. Realize the following Boolean function using 4:1 Multiplexer

$$F(A,B,C,D) = \Sigma m(0, 1, 2, 4, 6, 9, 12, 14)$$

5. Perform BCD Addition if A=0111, B=1000 Also, draw the circuit diagram for one digit BCD adder.
6. Draw the logic diagram of a 2-line to 4-line decoder/demultiplexer using two input NOR gate only.
7. Perform using 2's complement arithmetic: (a) 47-21 (b) 23-43 (c) 48-(-23)
8. Using K Map simplify the product-of-sum form the function given by

$F(A,B,C,D) = \Pi M(0, 6, 10, 12) + d(2,4,8,9,14,15)$ Realize it using logic gates.

PART C

1. Explain the process of flip-flop interconversion. Convert T-FF into JK flip-flop.
2. Simplify the logic function using Quine MacClusky minimization technique.

$F(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15) + d(2,13)$

3. Construct a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use the conventional sequential circuit design procedure using JK FF.
4. Convert the following numbers as required in each case.

(a) $(123.45)_{10} = (?)_2$ (b) $(25.625)_{10} = (?)_{16}$ (c) $(603.23)_8 = (?)_2$

(d) $(ABCD)_{16} = (?)_2$ (e) $(15C.38)_{16} = (?)_8$

5. Explain BCD to 7-segment decoder.
6. Make a K-map for the function: $F=AB+AC'+C+AD+AB'C+ABC$., Express F in Canonical SOP form. Realize the minimized expression using NAND gate only.
7. Design: (a) BCD to excess-3 encoder (b) Binary to Gray decoder