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DETAILED LECTURE NOTES

Logic families

Unit 3

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Logic gate and memory devices are fabricated as Integrated circuit, because it uses component as resistor, diodes and bipolar junction transistor.

Characteristics of logical IC

The working of logical family checked by the following Parameter.

1. Speed of operation It is expressed in terms of propagation delay. It is defined as the time taken for the output of a gate to change occurs in the input.

2. Power dissipation It is a measure of the power consumed by the logic gate when fully driven by its input.

3. Fan In It is the gate of input connected without any degradation in the input level

4. Fan out It is the maximum number of similar logic gates that a gate can drive without any degradation in voltage level.

~~voltage~~ immunity The noise denote an unwanted signal like transient, glitches and hum.

6. Operating Temperature They are sensitive by nature.

The operating temperature range for an IC from 0°C to 70°C for the consumer.

7. Power Supply Operating Temperature All IC gate one semiconductor derive that one temperature sensitive by nature. It is the main parameter to be taken into consideration.

8. Current and Voltage Parameters It is very important in designing the digital system and relays.

TRANSISTOR TRANSISTOR logic (TTL)

The most dominating logic family called the (TTL). It has five major division

- Standard
- High Speed
- Low Power
- Schottky Diode
- Low power schottky.

TTL NAND Gate

The basic circuit for the TTL logic family is the NAND gate. The TTL circuit uses a special single multi emitter transistor that is fabricated with several emitters at its input.

The number of emitters depend on the desired fan-in of the circuit. A multi emitter transistor is smaller in area than the diode it replaces.



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2. Standardized Loading: It can source or sink current for providing the output. The negative sign indicates that the conventional current is out of the device; it can connect to TTL emitter to any TTL output.

3. Fan Out: The maximum number of TTL load that can be driven by the TTL drivers is called fan out. The standard fanout for standard TTL is 10. Using the standard unit as ref one load current of 1.6mA into a low output.

4. Noise Immunity: It is unwanted signal voltage

glitches, transients response. Noise can sometime cause the input voltage of a logic gate to drop below $V_{IL}(\text{min})$ or rise above $V_{IH}(\text{max})$ it provides unreliable operation.

Noise immunity is the maximum noise voltage that may appear at the input of the logic gate.

The manufacturer define the noise margin which provide the amplitude of the noise voltage.

5. Operating Temperature

All IC gates are semiconductor device that one temperature sensitive by nature. The operating temp. will vary from 0°C to 70°C for consumer and industrial application.

6. Power Supply Requirement

The amount of power and supply voltage required by an IC, it is the main parameter to be taken into the consideration.

7. Current and Voltage Requirement:

High level input voltage (V_{IH})

Low level input voltage (V_{IL})

High level output voltage (V_{OH})

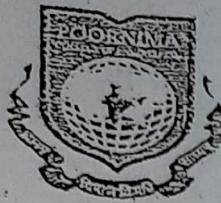
Low level output voltage (V_{OL})

High level input current (I_{IH})

Low level input current (I_{IL})

High level output current (I_{OH})

Low level output current (I_{OL})



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Digital Integrated Circuit

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The IC designed in the form of dual in package technology

SSI (small scale integration) → 10 gate on one chip

MSI (medium Scale integration) → 12 to 100 gate on one chip

LSI (large Scale integration) → 100 to 5000 gate per chip

VLSI → (very large Scale integration) → thousand gate per chip

The logic families classified mainly with two fabrication process

(i) Bipolar

(ii) metal Oxide Semiconductor

IC comes under

following type of package

(i) Dual in line Package (DIP)

(ii) Dual in chip carrier (LCC)

(iii) Plastic leaded chip carrier (PLCC)

(iv) Plastic Quad Flat pack (PQFP)

(v) Pin Grid Array (PGA)

Bipolar logic families

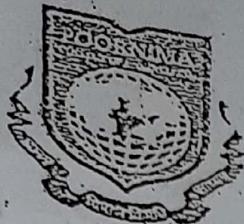
The important content of the families is transistor, Register Diode. Based on two main operation of bipolar IC, there are saturated or non-saturated.

The following are the saturated logic

1. Register Transistor logic (RTL)
2. Direct Coupled Transistor logic (DCTL)
3. Diode Transistor logic (DTL)
4. High Threshold logic (HTL)
5. Transistor Transistor logic (TTL)
6. Integrated injection logic (I^2L)

The following are the non-saturated logic

1. Schottky TTL
2. Emitter Coupled logic (ECL)

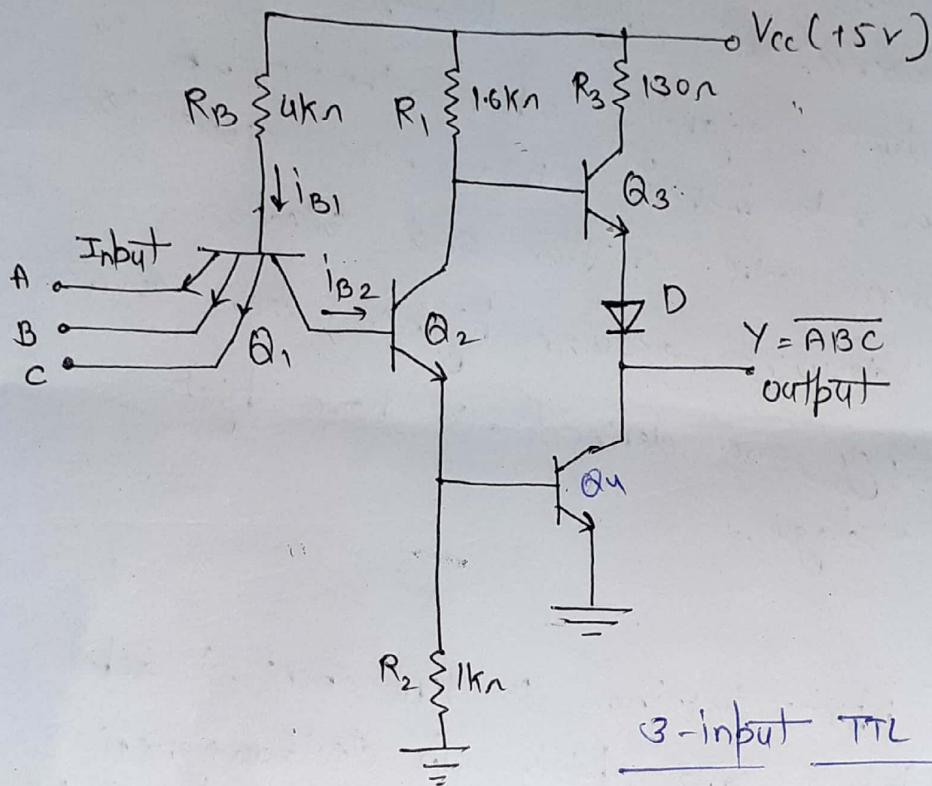


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Smaller area result in the substrate noise and full time. provide lower capacitance nearby the circuit for reducing PAGE NO.



3-input TTL NAND Gate

Circuit Operation: The output is taken from the collector of transistor Q4. Each emitter of Q1 acts like a diode. Therefore, transistor Q1 and the 4kΩ resistor act like a 3 input AND gate and rest of the resistor inverts the signal.

When either or all input (A, B and C) at 0v. The corresponding emitter base junction of Q1 become forward biased. The value of RB is selected to ensure that Q1 is turned ON.

The value of current i_{B2} flowing through the base of Q_2 reduces the potential at the base of Q_2 , and hence transistor Q_2 and Q_3 are cut off so that the output voltage is at V_{cc} .

If all the input one high the emitter base junction of Q_1 is reverse biased so that it has no base current. Hence Q_1 is off. So the collector base junction is forward bias and supplying base current i_{B2} to Q_2 .

In the absence of diode D the transistor Q_3 will conduct slightly when the output is low. In order to prevent this the diode is connected between the emitter and collector.

TTL input circuits require higher drive current than DTL, they are defined to have high power output stage.

TTL Parameters

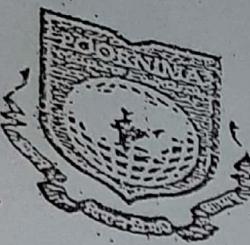
When an input terminal is left open, it acts like small antenna and pick up electromagnetic noise for malfunctioning and erroneous the output.

Current Sourcing and current sinking: When the output of the gate is high it provides current to the input of the gate being driven, the output is said to act as a current source.

The op of a TTL gate goes low, it must be capable for sinking current drawn from gate input

$$I_{IL(\max)} = -1.6 \text{ mA}$$

$$I_{IH} = +40 \text{ mA}$$



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Other TTL Series

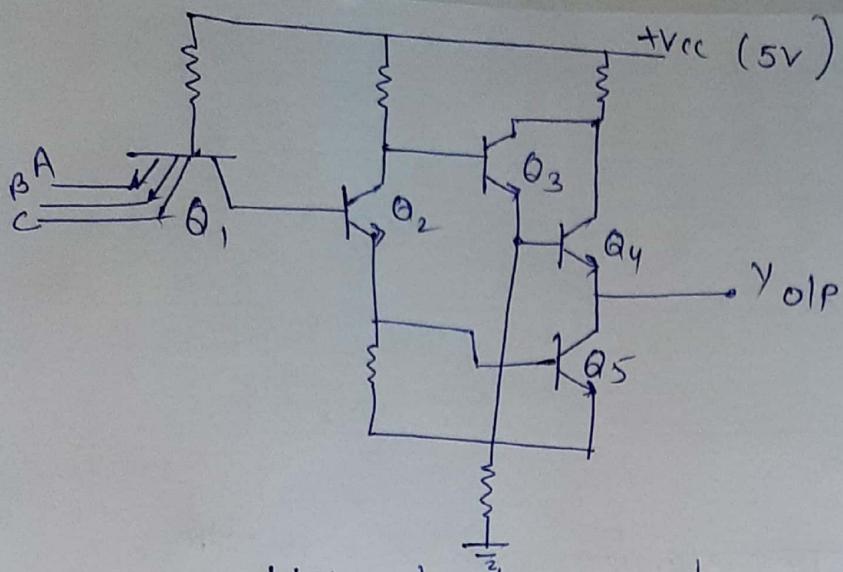
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Standard Series: The standard series was the first version of the TTL family. The use of multiple emitter input and entire pull up op configuration provide the higher variation. It include shift Register, counter, decoder, memories, data selector and arithmetic element to ssi device.

Low power TTL Have same basic circuit the no of Register increased.

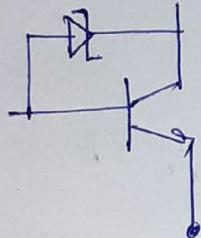
Increase in Register result in the reduction of power dissipation, the requirement of low power gate is less than $\frac{1}{10}$ th of the circuit.

High Speed TTL In this the smaller register values are used and the emitter follower section is replaced by the darlington Transistor Q_3 consist of the Darlington pair. The op section consist of the Transistor pair Q_3 and Q_4 .



High speed TTL gates

Schottky TTL It has the highest speed, it is achieved by Schottky barrier diode clamp. The characteristics of SBD is useful in the low voltage drop and provide fast switching speed.



Transistor and Schottky barrier diode clamp

Low Power Schottky TTL By increasing internal

resistance, manufacturer provides the compromise between low power and high power schottky TTL. It requires considerable less power.



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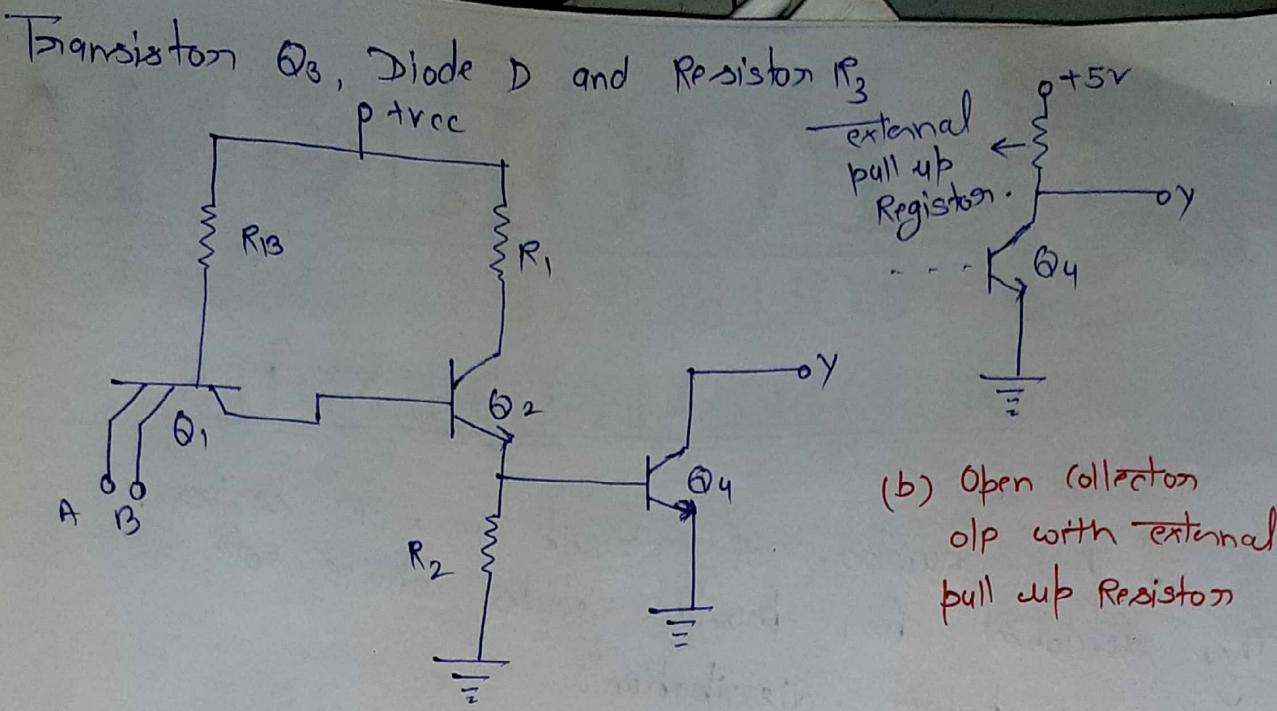
TTL Series

It has number of circuit in the series.
They developed for boride codes choice of
speed and power dissipation.

Version	Abbreviation	Propagation Delay	Power Dissipation	max clock rate	fan out
Standard	TTL	10	10	35	10
Low power	L TTL	33	1	3	10
High Speed	HTTL	6	22	50	10
Schottky	STTL	3	19	125	10
Low power Schottky	L STTL	9.5	2	45	10

Open Collector Output (TTL)

The open collector TTL gate need an external resistor that must be connected between the collector of a pull down transistor and the supply voltage for proper operation. The TTL NAND gate with open collector output is obtained by removing the following component: Transistor Q₃, Diode D and Resistor R₃.



(b) Open collector o/p with external pull up Resistor

(a) Open Collector TTL NAND Gate

As the collector of Q_4 is open, the open collector gate will not work properly unless an external pull up resistor is connected in the fig (b). The o/p is taken at the collector of the transistor Q_4 .

The open collector provide the circuit that can be used by many devices and they are connected with the wired logic. In some system, the same device connected with the wired logic structure.

The main disadvantage of open collector gate is that switching time delay is increased because the pull up resistor is few k Ω . The slow switching speed of open collector TTL device become worse when the o/p goes from low to high.



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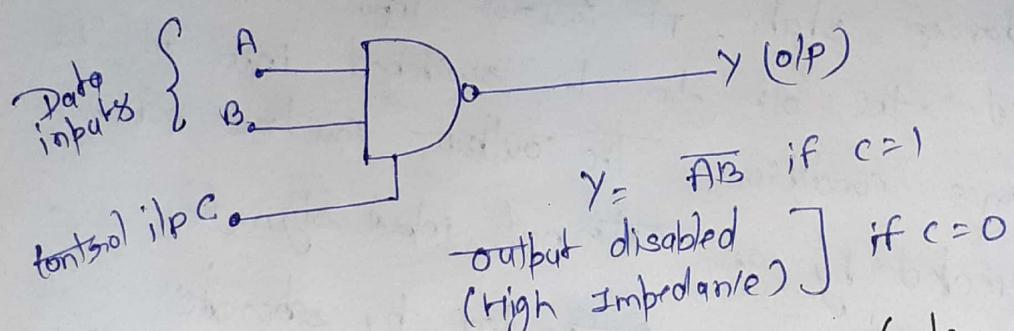
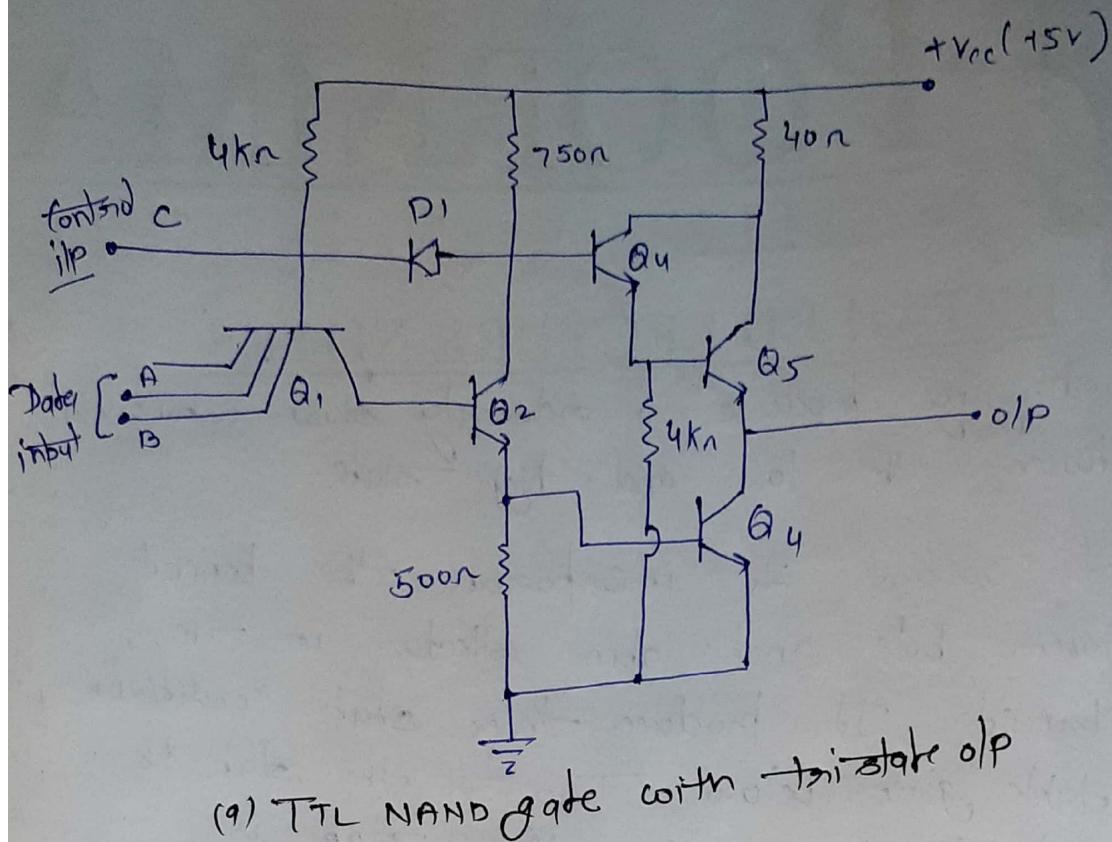
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This changing produce a relatively slow exponential rise between the low and high state.

Tri-state output: It incorporate the benefit of totem pole and open collector in the single circuit. It produce three state conditions in the table given below. Two of the state is logic 0 and logic 1 and the third state is high impedance state. A control input terminal is provided to be switched into to its high impedance condition. The output could not affect by an external input signal.

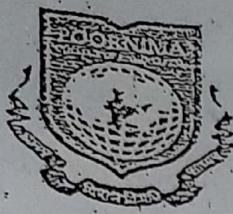
The Third state is controlled by separate control input. A control input terminal is provided to allowed to switched into (on or off). When the control input c is 1, the gate behave like normal NAND gate and provide state of 0 and 1. When the control input c is 0, the output is disable irrespective to the value of the normal input.



(b) Symbol for Tri-state NAND Gate.

Table Truth Table for TTL NAND Gate.

A	B	C	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Y
0	0	1	ON	OFF	OFF	ON	ON	1
0	1	1	ON	OFF	OFF	ON	ON	1
1	0	1	ON	OFF	OFF	ON	ON	0
1	1	1	OFF	ON	ON	OFF	OFF	Open circuit
X	X	0	ON	OFF	OFF	OFF	OFF	



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Operation of Tri State TTL NAND Gate

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When the control input is high and any input A or B is low, Q_1 is ON and both Q_2 and Q_3 are off. Hence Q_4 and Q_5 will be turned ON and output will be at the high level. When the control input C is high and both input A and B are high, transistors Q_1 become off, and thereby drive both the transistors Q_2 and Q_3 , ON. Hence Q_4 and Q_5 are off and the output is low (0). Thus, when the control input C is high the circuit operate like a totem pole output circuit. When the control input is in low state, then diode D_1 conduct and therefore the voltage at the base of transistor Q_4 is 0.7V, which is not enough to make transistor ON.

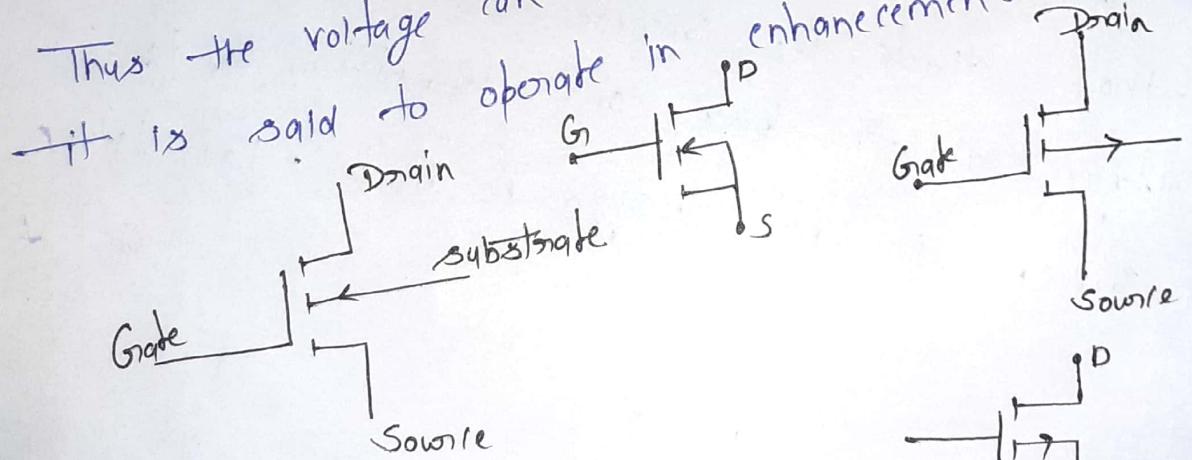
Mos logic families

Metal Oxide Semiconductor derives its name from the basic mos structure of a metal electrode. Mos IC can used large no of circuit element on a single chip than bipolar IC. The disadvantage of mos IC is its low operating speed.

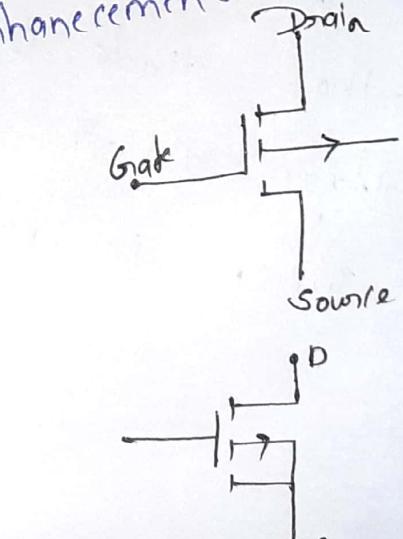
Mosfet metal oxide semiconductor field effect Transistor

In mosfet The channel can be n-type or p-type, depending on the majority carrier. The mode of operation can be enhancement or depletion. If the channel is initially doped lightly with p-type impurity, a conducting channel exists at zero gate voltage and device to be said in depletion mode. If the region beneath the gate is left initially unchanged, a channel must be induced by the gate field before current can flow.

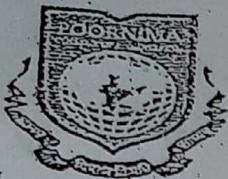
Thus the voltage can be enhanced by such voltage. It is said to operate in enhancement mode.



(a) n-channel



(b) p-channel



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Pmos is use only for p-channel enhancement.

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Mosfet. A Resistor at the o/p of a pmos circuit could be used to drop the high level voltage to one suitable for nmos circuit. Holes are the current carriers for pmos.

Nmos is only n-channel enhancement mosfet.

Nmos has a greater packing density than pmos.

Free electrons are the current carriers in nmos.

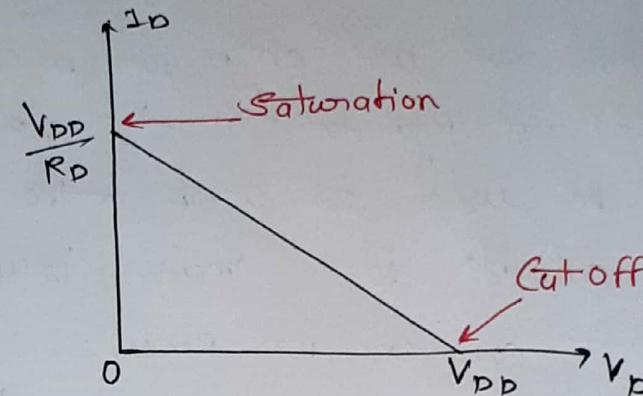
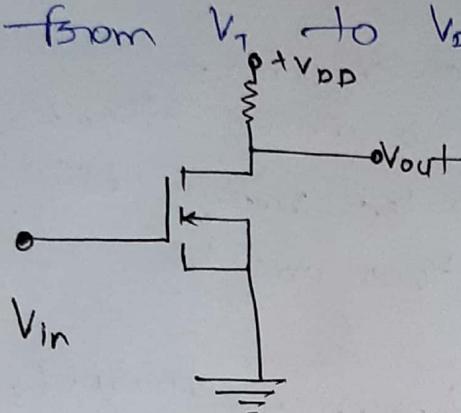
Cmos - it use both p-channel and n-channel device. It has the highest complexity and lower packaging density among the mos families. It possess the important advantage of much lower power dissipation.

Pmos and Nmos digital IC have a greater packing density and are therefore more economical than cmos. Nmos is also about twice as fast as pmos. It has highest application in LSI.

MOSFET logic Circuits

for an n-channel mos, supply voltage is of about +5V. The two voltage level are the function of the threshold voltage V_T . The low level range anywhere from 0 to V_T and the high level range from V_T to V_{DD} .

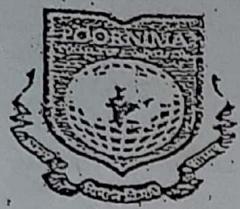
from V_T to V_{DD} ,



(a) mosfet drivers with passive load its load line

In mosfet the fabrication is easier than register. The gate of the upper mosfet is connected to the drain. This mosfet always conduct and behave like the Register R_b . The upper mosfet has a resistance ten times higher than that of the lower mosfet.

Current flows from V_{DD} through the active load Register Q_1 and into Q_1 , Thus the circuit behave as an inverter.

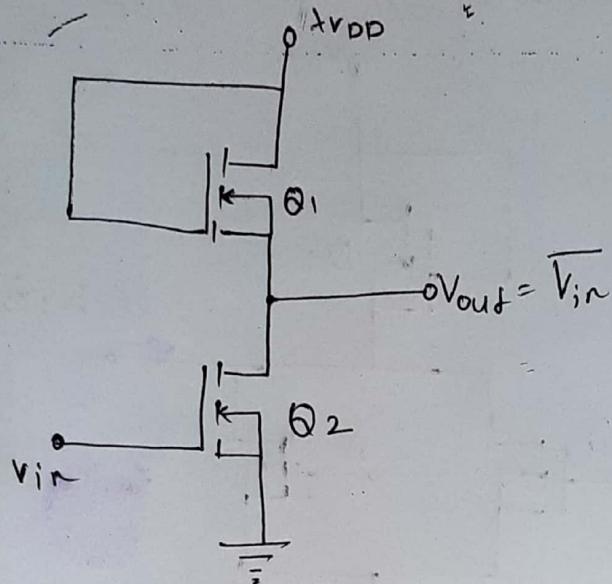


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MOSFET driver with active load

The gate of the upper MOSFET is connected to the drain, this MOSFET always conduct and behave like the Resistor R_D . The upper MOSFET has a resistance ten times greater than the lower MOSFET. When the input is off. Since Q_1 is always ON, the output voltage is at about V_{DD} . When the input voltage is high Q_2 turns ON. Current flows from V_{DD} to the active load Resistor Q_1 and then into Q_2 . Thus the circuit behaves like an inverter circuit.

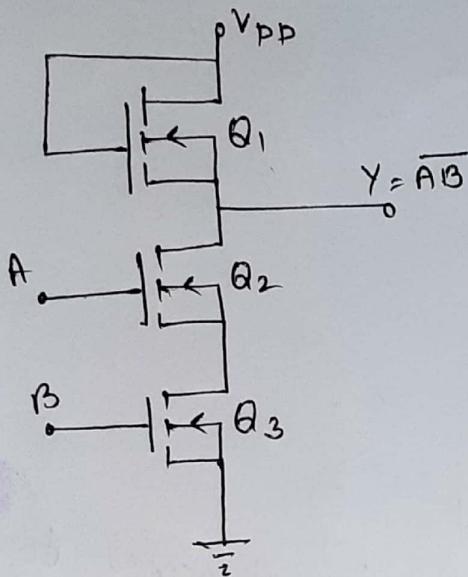
Mos logic Circuits

NAND Gate: — it use three transistor in Series

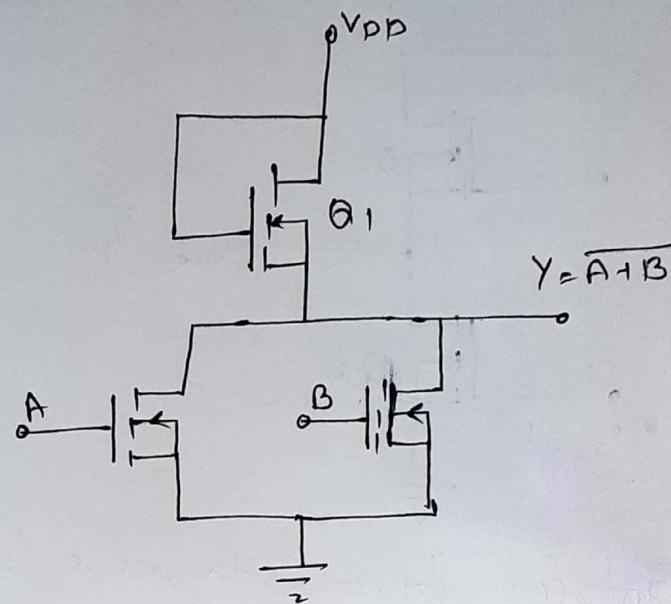
Input A and B be high fall \rightarrow transistor

is conduct and the output become low.

If either of the input is low the corresponding transistor is turned off.



(i) NAND Gate



(ii) NOR Gate

The NOR gate uses two NMOS transistors in parallel circuit. If either of the input is high the corresponding mos transistor conduct and the output is low. If the input one low, both mosfet one off and hence the output is high.



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Diode Transistor logic

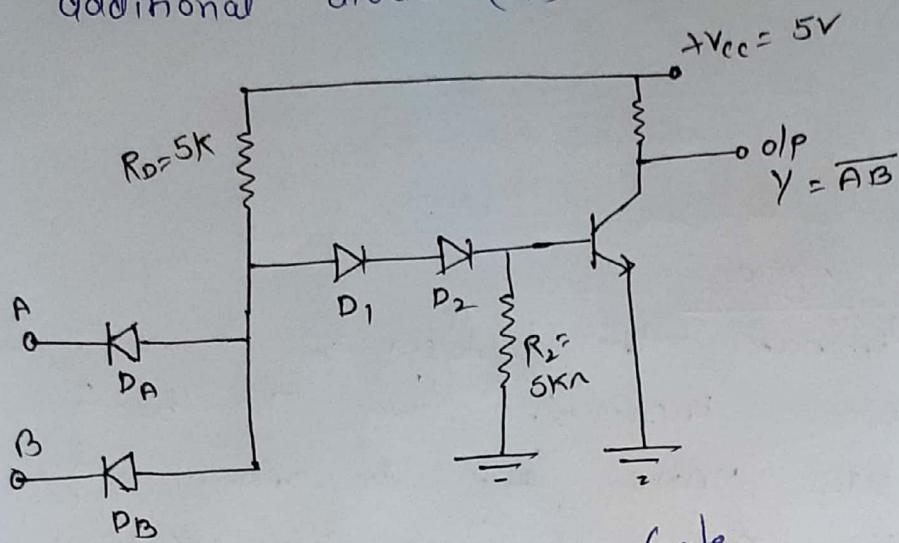
The DTL eliminate the problem of decreasing output voltage with increasing load. The basic circuit of a DTL NAND gate is shown in fig. Two diode in the circuit perform AND operation followed by the transistor. Intran which works as NAND Gate. When both the input at high the diode D_A and D_B one reverse biased. Diode D_1 and D_2 one turned on and hence the output is low. The additional diode increase the noise margin. If any of the input drops to ground potential, the corresponding input diode will conduct and current will flow through the diode and R_D and causing voltage drop at the input of the diode D .

DTL has the following characteristics

Propagation Delay: Turn off delay is longer than the turn on delay.

FAN-OUT: The fan-out is as high as 8, possible with DTL family.

FAN IN → it has fan-in of 8
 Noise immunity additional diode (D_2) connected in series (D_1). The noise immunity is high due to the



Basic DTL NAND Gate

Advantage over TTL

DTL has better noise margin, higher fan out capabilities and faster response than the TTL family. The switching speed and fan-out of the DTL family are improved in the TTL family.