3E1137

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B. Tech. III - Sem. (Main / Back) Exam., Dec. 2019

ESC Computer Science & Engineering

3CS3-04 Digital Electronics

CS, IT

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 (i) In FF clocking –

(a) Hold time is greater than set-up time

(b) Set-up time is greater than hold time

(c) Hold time is before edge triggering

(d) Set-up time is after edge triggering

(ii) A 4-bit binary ripple counter uses flip-flops with propagation delay time of 25ns each. The maximum possible time required for change of state will be –

(a) 25ns

(b) 50ns

(c) 70ns

(d) 100ns

Q.2 (i) A 4-bit modulo- 16 ripple counter uses JK flip-flops. If the propagation delay of each FF is 50ns, the maximum clock frequency that can be used is equal to –

(a) 20 MHz

(b) 10 MHz

(c) 5 MHz

(d) 4 MHz

(ii) What J-K input condition will always set 'Q' upon the occurrence of the active clock transition?

(a) J = 0, K = 0

(b) J = 1, K = 1

(c) J = 1, K= 0

(d) J = 0, K = 1

Q.3 In standard TTL, the "totem pole" stage refers to –

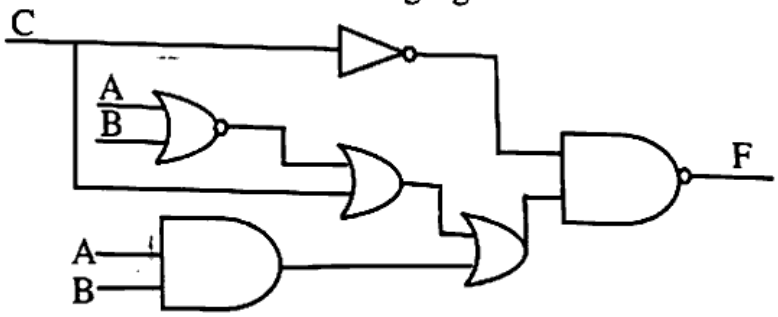
(a) the multi-emitter input stage

(b) the phase splitter

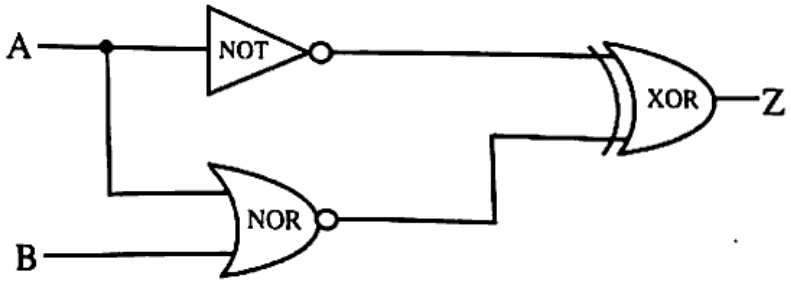
(c) the output buffer

(d) open collector output stage

Q.4 Find the output F in the following figure –



Q.5 Complete the truth table for the combinational circuit shown in the figure –



Q.6 Minimum number of 2-input NAND gates required to implement the function $F=(X'+Y')(Z+W)$ is-

(a) 3

(b) 4

(c) 5

(d) 6

Q.7 CMOS logic has the property of -

(a) Increased capacitance and delay

(b) Decreased area

(c) High noise margin

(d) Low static power dissipation

Q.8 Which TTL logic gate is used for wired ANDing?

Q.9 Which one of the following can be used as parallel to serial converter?

(a) Decoder (b) Multiplexer

(c) Digital counter (d) Demutiplexer

Q.10 Perform the subtraction using 2's complementary arithmetic's –

(i) 11011 – 11001

(ii) 11001 - 11011

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

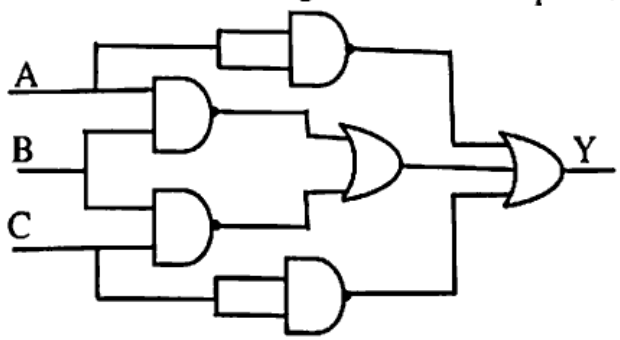
Attempt any five questions

Q.1 Show that: A XNOR B=AB+A'B'=$(AB'+A'B)'$. Write the equation for a 4-input XNOR gate in canonical Sum-of-Products and canonical Product-of-Sum forms. Also construct the corresponding logic diagrams.

Q.2 What is race around condition in JK flip flop? Discuss a method which is commonly used to eliminate the race around condition?

Q.3 (a) What are Universal gates? Why they are known so?

(b) For the logic shown in the figure, find the output 'Y'.



Q.4 Design a 4-bit, Mode-controlled bidirectional shift register using 'SR' flip-flops and explain its working in both directions.

Q.5 (a) Write short note on complementary MOS logic.

(b) (i) What is Fan-in and Fan-out?

(ii) Explain the terms noise margin and gate delays.

Q.6 (a) Represent the number $(-17)_{10}$ in (i) Sign magnitude form (ii) 1's complement representation.

(b) The Boolean expression F = z(w'+y) is a simplified version of the expression: F=(w'+y)(x'+z)(w'+z). Find the Don't care conditions, if any.

Q.7 Design 3-bit synchronous up counter using T flip flop.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 (a) Draw a frequency divider using JK FFs to divide input clock frequency by a factor of 8.

(b) Reduce following Boolean function and then realized the reduced one using NOR gate only. X=A (B'+C') (A+D)

(c) Convert a T Flip-flop into a JK flip-flop.

Q.2 (a) Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates.

(b) Design a 4 bit binary to gray code converter and realize it using logic gates.

Q.3 (a) Draw the voltage profile diagram of a TTL logic gate. Define High noise margin and Low noise margin. Calculate HNM and LNM for a typical TTL gate.

(b) Explain the interfacing concept of a TTL gate driving a CMOS gate with equal power supply voltage.

Q.4 (a) Show that a positive logic NAND gate is the same as a negative logic NOR gate.

(b) Show that the NAND connection is not associative.

(c) Reduce the following equation using Quine McClusky method of minimization F (A,B,C,D) =Σm(0,1,3,4,5,7,10,13,14,15).

Q.5 (a) Discuss a decade counter and its working principle.

(b) Draw an asynchronous 4 bit up-down counter and explain its working.

(c) Using JK flip flops, design a parallel counter which counts in the sequence 000,111,101,110,001,010,000.....
