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MT7612E DATASHEET

802.11a/b/g/n/ac Wi-Fi 2T2R Single Chip

Document Revision History

Revision	Date	Author	Description
0.01	2012/11/15	Ben Lin	Preliminary release
0.02	2012/11/27	Ben Lin	1. Correct the pin definition of pin 58 and pin 68. 2. Revise 2.4 IO control option.
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1 System Overview

1.1 General Descriptions

The MT7612E is a highly integrated single chip which has built in a 2x2 dual-band wireless LAN radio. It supports IEEE 802.11ac draft standard and provides the highest PHY rate up to 867Mbps, offering feature-rich wireless connectivity and reliable throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. MT7612E integrates PA/LNA such that the number of the external components is reduced to minimum. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7612E supports the 802.11i security standard and implements hardware acceleration for TKIP, CCMP, GCMP, and WAPI. The device also supports 802.11e QoS for video, voice, and multimedia applications.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- 20/40MHz crystal clock support with low power operation in sleep mode
- Best-in-class active and idle power consumption performance
- Compact 9mm x 9mm QFN76L package
- Fully compliance with PCIe base specification v1.1 with OBFF, LTR ECN support
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- External serial flash support
- 14 programmable general purpose Input / Output
- 2 configurable LED pins
- Internal thermal sensor for temperature compensation and thermal protection.
- Self calibration

1.2.2 WLAN

- IEEE 802.11 a/b/g/n and 802.11ac draft compliant
- Support 20MHz, 40MHz, 80MHz in 5GHz band, and 20MHz, 40MHz bandwidth in 2.4GHz band
- Dual-band 2T2R mode with data rate up to 867Mbps
- Support 256QAM in 2.4GHz band
- Support STBC, LDPC, MRC, and transmit Beamforming
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- Integrated LNA, PA, and T/R switch.
- Optional external LNA and PA support.

- IEEE 802.11 d/e/h/i/k/r/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- TCP checksum offload
- 802.11 to 802.3 header translation offload
- Supports Wi-Fi Direct
- Per packet transmit power control
- Wake on WLAN
- Conforms to EN300328 V1.8.1 (2012.08) and EN301893 V1.7.1 (2012.06)

1.3 Applications

MT7612E is designed for PCI Express Full/Half Mini Card as well as Next Generation Form Factor (NGFF). It is suitable for the following applications.

- Desktop PC
- Laptop NB
- Tablet NB
- xDSL modem
- AP router

1.4 Block Diagram

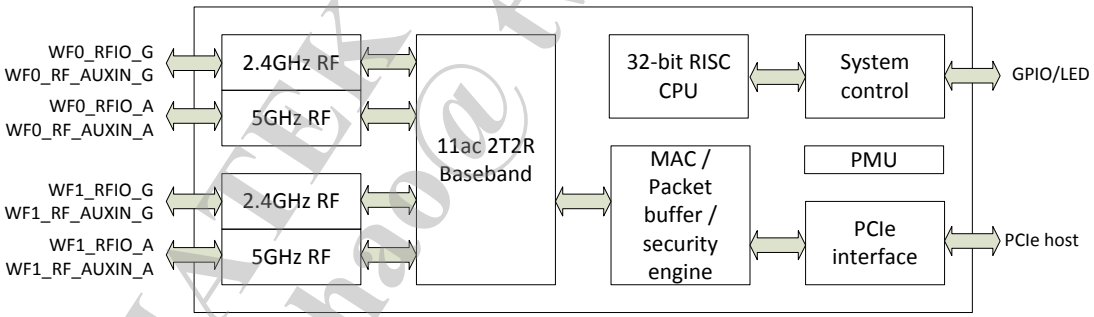


Figure 1 MT7612E block diagram

2 Product Descriptions

2.1 Pin Layout

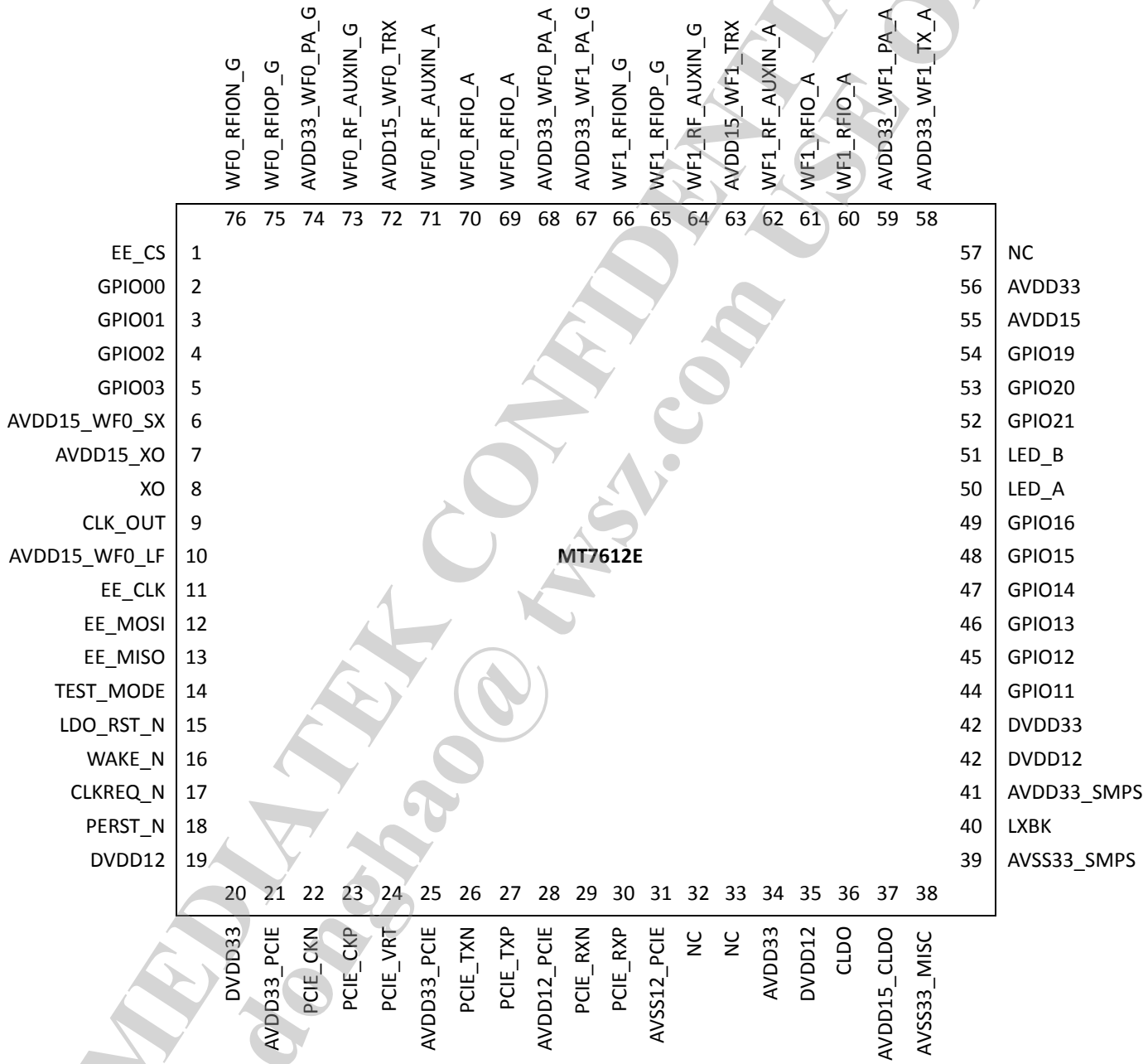


Figure 2 Top view of MT7612E QFN pin-out.

2.2 PIN Description

QFN76	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
15	LDO_RST_N	External system reset active low	N/A	Input	DVDD33
8	XO	Crystal input or external clock input	N/A	Input	AVDD15_XO
PCIe interface					
16	WAKE_N	Request system to wake from the sleep/suspend state	PU	Output	DVDD33
17	CLKREQ_N	Reference clock request signal	PU	Output	DVDD33
18	PERST_N	PCIe functional reset	PU	Input	DVDD33
22	PCIE_CKN	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
23	PCIE_CKP	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
26	PCIE_TXN	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
27	PCIE_TXP	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
29	PCIE_RXN	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
30	PCIE_RXP	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
24	PCIE_VRT	PCIe resister reference	N/A	Analog	
EEPROM/flash interface					
13	EE_MISO	External memory data input / Antenna select	PD	Input	DVDD33
12	EE_MOSI	External memory data output / Antenna select	PD	Output	DVDD33
11	EE_CLK	External clock	PD	Output	DVDD33
1	EE_CS	External chip select	PU	Output	DVDD33
Programmable I/O					
2	GPIO0	Programmable input/output	PD	In/out	DVDD33
3	GPIO1	Programmable input/output	PD	In/out	DVDD33
4	GPIO2	Programmable input/output	PD	In/out	DVDD33
5	GPIO3	Programmable input/output	PD	In/out	DVDD33
44	GPIO11	Programmable input/output	PD	In/out	DVDD33
45	GPIO12	Programmable input/output	PD	In/out	DVDD33
46	GPIO13	Programmable input/output	PD	In/out	DVDD33
47	GPIO14	Programmable input/output	PD	In/out	DVDD33
48	GPIO15	Programmable input/output	PD	In/out	DVDD33
49	GPIO16	Programmable input/output	PU	In/out	DVDD33

45	GPIO19	Programmable input/output	PD	In/out	DVDD33
53	GPIO20	Programmable input/output	PD	In/out	DVDD33
52	GPIO21	Programmable input/output	PD	In/out	DVDD33
LED					
50	LED_A	Programmable open-drain LED controller	PU	Output	DVDD33
51	LED_B	Programmable open-drain LED controller	PU	Output	DVDD33
WIFI radio interface					
60, 61	WF1_RFIO_A	RF a-band RF port	N/A	Input	
62	WF1_RF_AUXIN_A	RF a-band auxiliary RF LNA port	N/A	Output	
64	WF1_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Output	
65	WF1_RFIOP_G	RF g-band RF port	N/A	Input	
66	WF1_RFION_G	RF g-band RF port	N/A	Input	
69, 70	WF0_RFIO_A	RF a-band RF port	N/A	Input	
71	WF0_RF_AUXIN_A	RF a-band auxiliary RF LNA port	N/A	Output	
73	WF0_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Output	
75	WF0_RFIOP_G	RF g-band RF port	N/A	Input	
76	WF0_RFION_G	RF g-band RF port	N/A	Input	
9	CLK_OUT	XTAL buffered clock output	N/A	Output	
PMU/SMPS					
36	CLDO	LDO 1.2V output	N/A	Output	
37	AVDD15_CLDO	Digital LDO 1.5V input	N/A	Input	
41	AVDD33_SMPS	SMPS 3.3V power supply	N/A	Input	
40	LXBK	SMPS 1.5V output	N/A	Output	
Miscellaneous					
14	TEST_MODE	Test mode enable	N/A	Input	DVDD33
Power supplies					
20, 43	DVDD33	Digital 3.3v I/O power supply	N/A	Power	
19, 35, 42	DVDD12	Digital 1.2v core power supply	N/A	Power	
21, 25	AVDD33_PCIE	PCIe 3.3V power supply	N/A	Power	
28	AVDD12_PCIE	PCIe 1.2V power supply	N/A	Power	
58	AVDD33_WF1_TX_A	RF 3.3v power supply	N/A	Power	
59	AVDD33_WF1_PA_A	RF 3.3v power supply	N/A	Power	
67	AVDD33_WF1_PA_G	RF 3.3v power supply	N/A	Power	
68	AVDD33_WF0_PA_A	RF 3.3v power supply	N/A	Power	
74	AVDD33_WF0_PA_G	RF 3.3v power supply	N/A	Power	
34, 56	AVDD33	Analog power supply	N/A	Power	

6	AVDD15_WF0_SX	RF 1.5v power supply	N/A	Power	
7	AVDD15_XO	RF 1.5v power supply	N/A	Power	
10	AVDD15_WF0_LF	RF 1.5v power supply	N/A	Power	
63	AVDD15_WF1_TRX	RF 1.5v power supply	N/A	Power	
72	AVDD15_WF0_TRX	RF 1.5v power supply	N/A	Power	
55	AVDD15	Analog 1.5v power supply	N/A	Power	
31	AVSS12_PCIE	PCIe ground	N/A	Ground	
38	AVSS33_MISC	PMU ground	N/A	Ground	
39	AVSS33_SMPS	PMU ground	N/A	Ground	
32, 33, 57	NC	Reserved	N/A	N/A	
E-PAD	VSS	Ground	N/A	Ground	

Table 1 Pin descriptions

2.3 Strapping option

QFN76	Pin Name	Pin description	Default PU/PD
12	EE_MOSI	EXT_EE_SEL: Pull down	PD
11	EE_CLK	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
47	GPIO14	CHIP_MODE[2]: Pull down	PD
46	GPIO13	CHIP_MODE[1]: Pull down	PD
45	GPIO12	CHIP_MODE[0]: Pull up	PD

Table 2 Strapping option

2.4 IO control option

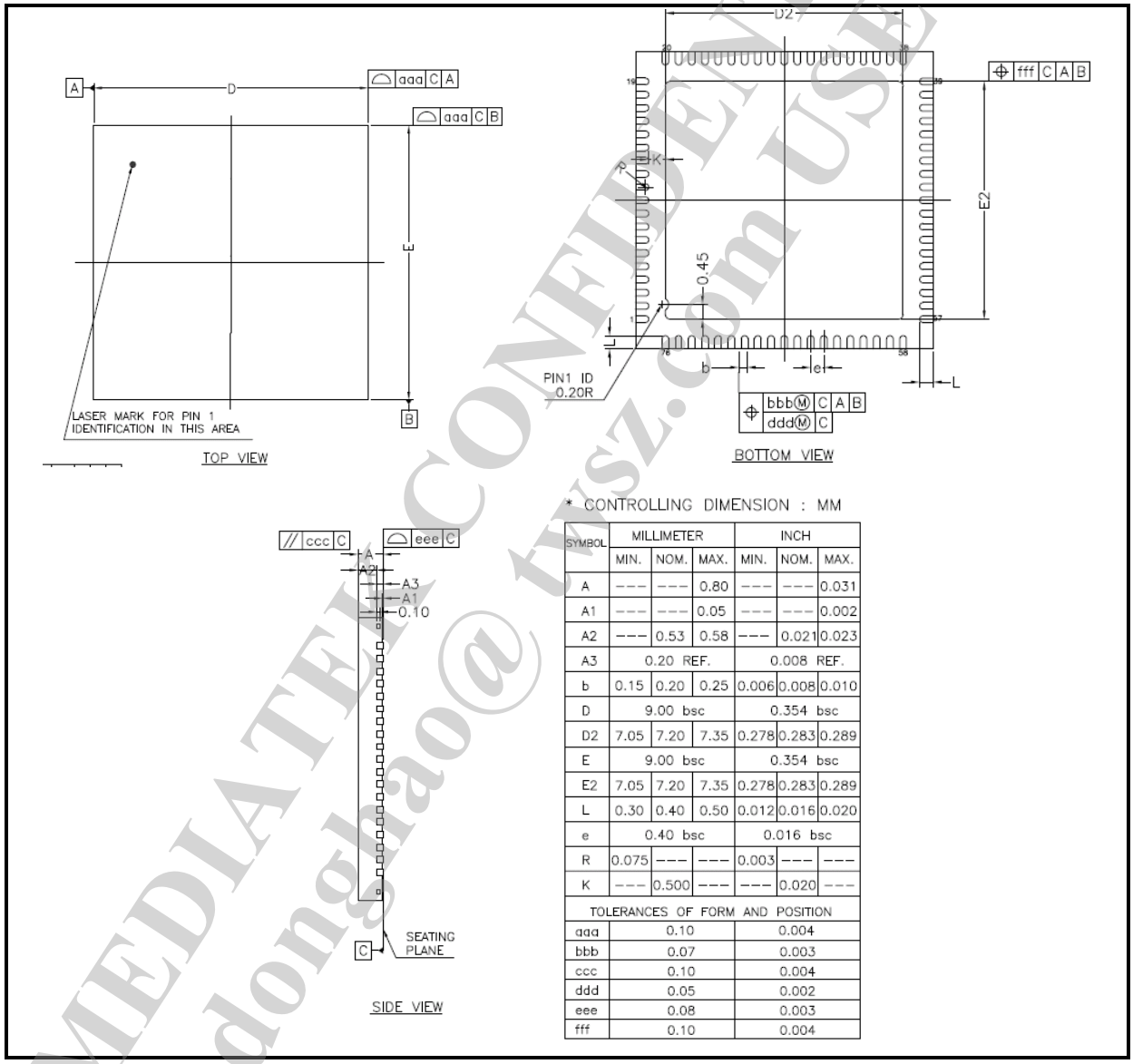
MT7612E provides 14 configurable I/O functions to support diversified applications. It supports external front-end module on dual bands for high power requirement. Open drained I/Os are available for LED.

QFN76	Pin Name	GPIO mode	Default mode	External FEM mode 7	External FEM mode 4	External FEM mode 3
2	GPIO0	GPIO0	Reserved	Reserved	Reserved	Reserved
3	GPIO1	GPIO1	GPIO1	Reserved	GPIO1	Reserved
4	GPIO2	GPIO2	WL_DISABLE	Reserved	WL_DISABLE	WL_DISABLE
5	GPIO3	GPIO3	GPIO3	Reserved	GPIO3	Reserved
44	GPIO11	GPIO11	GPIO11	PA2G_PE1	Reserved	GPIO11
45	GPIO12	GPIO12	GPIO12	PA2G_PE0	Reserved	LED_WL
46	GPIO13	GPIO13	GPIO13	PG5G_PE1	LNA2G5G_PE1	PA2G_PE1
47	GPIO14	GPIO14	GPIO14	PA5G_PE0	LNA2G5G_PE0	PA2G_PE0
48	GPIO15	GPIO15	Reserved	LNA2G5G_PE1	Reserved	Reserved
49	GPIO16	GPIO16	Reserved	LNA2G5G_PE0	Reserved	Reserved

50	LED_A	GPIO17	LED_WL	GPIO17	LED_WL	LNA2G5G_PE1
51	LED_B	GPIO18	LED_B	LED_B	LED_B	LNA2G5G_PE0
54	GPIO19	GPIO19	GPIO19	TRSW_N	TRSW_N	TRSW_N
53	GPIO20	GPIO20	Reserved	TRSW_P	TRSW_P	TRSW_P

Table 3 IO control option

2.5 Package information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.00 bsc			0.354 bsc		
D2	7.05	7.20	7.35	0.278	0.283	0.289
E	9.00 bsc			0.354 bsc		
E2	7.05	7.20	7.35	0.278	0.283	0.289
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
K	---	0.500	---	---	0.020	---

TOLERANCES OF FORM AND POSITION		
aaa	0.10	0.004
bbb	0.07	0.003
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.08	0.003
fff	0.10	0.004

Figure 3 Package outline drawing

2.6 Ordering Information

Part number	Package	Operational temperature range
MT7612EN	9x9x0.8 mm 76-QFN	-10~70°C

Table 4 Ordering information

2.7 TOP Marking Information

MT7612EN : Part number
DDDD : Date code
: Internal control code
BBBBBBB : Lot number

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.5V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 5 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 6 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 7 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
T_J	Maximum Junction Temperature (Plastic Package)	TBD	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	TBD	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	TBD	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	TBD	°C/W

Note:

[1] Half mini-card, 4-layer PCB
[2] 9mm x 9mm QFN76L package

Table 8 Thermal information

3.5 Current consumption

3.5.1 WLAN current consumption

Description	Performance	
	TYP	Unit
Sleep mode	TBD	mA
RX Active, HT40, MCS7	TBD	mA
RX Active, VHT80, MCS9	TBD	mA
RX Power saving, DTIM=1	TBD	mA
RX Listen	TBD	mA
TX HT40, MCS7 @15dBm	TBD	mA
TX VHT80, MCS9 @12dBm	TBD	mA
TX CCK, 11Mbps @19dBm	TBD	mA

Note: All result is measured with internal switching regulator enabled.

Table 9 WLAN Current Consumption

3.6 Wi-Fi RF specification

3.6.1 Wi-Fi RF Block Diagram

The frond-end loss with diplexer:

- 2.4GHz insertion loss is 0.8dB.
- 5GHz insertion loss is 1.7dB.

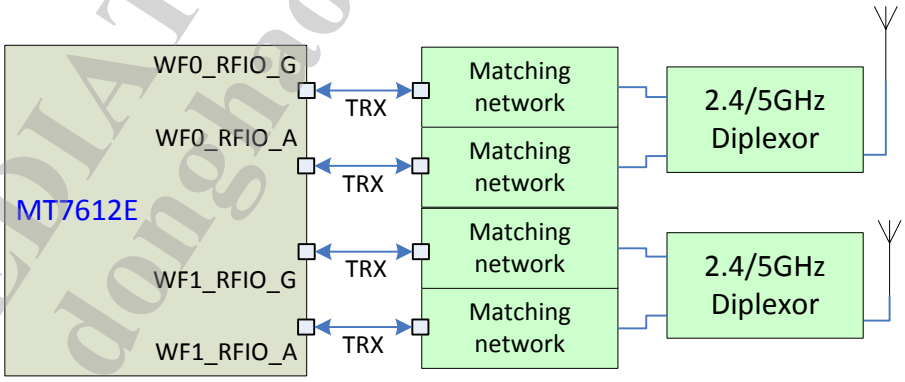


Figure 5 2.4/5GHz RF front-end configuration

3.6.2 Wi-Fi 2.4GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance

		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-98	-	dBm
	2 Mbps CCK	-	-94	-	dBm
	5.5 Mbps CCK	-	-92	-	dBm
	11 Mbps CCK	-	-89	-	dBm
RX sensitivity	6 Mbps OFDM	-	-92.5	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88.5	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
RX Sensitivity BW=20MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-92	-	dBm
	MCS 1	-	-89.5	-	dBm
	MCS 2	-	-88	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-81.5	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-75.5	-	dBm
	MCS 7	-	-74.5	-	dBm
RX Sensitivity BW=40MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-89.5	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-84.5	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-72.5	-	dBm
	MCS 7	-	-71	-	dBm
Maximum Receive Level	11 Mbps CCK	-	-10	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	-	40	-	dBm
	11 Mbps CCK	-	36	-	dBm
	6 Mbps OFDM	-	39	-	dBm
	54 Mbps OFDM	-	22	-	dBm
Receive Adjacent Channel Rejection (HT20)	MCS 0	-	34	-	dBm
	MCS 7	-	9	-	dBm
Receive Adjacent Channel Rejection (HT40)	MCS 0	-	25	-	dBm
	MCS 7	-	9	-	dBm

Table 10 2.4GHz RF receiver specifications

3.6.3 Wi-Fi 2.4GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance

		MIN	TYP	MAX	Unit
Frequency range		2412	-	2484	MHz
Output power	1~11 Mbps CCK	-	20	-	dBm
	6 Mbps OFDM	-	20	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20/HT40, MCS 0	-	20	-	dBm
	HT20/HT40, MCS 7	-	18	-	dBm
TSSI accuracy	Output power variation for close loop control	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Table 11 2.4GHz RF transmitter specifications

3.6.4 Wi-Fi 5GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	GHz
RX sensitivity	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-89	-	dBm
	18 Mbps OFDM	-	-87.5	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	48 Mbps OFDM	-	-76.5	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX Sensitivity BW=40MHz VHT Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-89	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-84.5	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-73.5	-	dBm
	MCS 6	-	-72	-	dBm
	MCS 7	-	-71	-	dBm
	MCS 8	-	-65	-	dBm
	MCS 9	-	-63.5	-	dBm
RX Sensitivity BW=80MHz VHT Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-85.5	-	dBm
	MCS 1	-	-83.5	-	dBm
	MCS 2	-	-81	-	dBm
	MCS 3	-	-77.5	-	dBm
	MCS 4	-	-74	-	dBm
	MCS 5	-	-70	-	dBm
	MCS 6	-	-69	-	dBm
	MCS 7	-	-67	-	dBm
	MCS 8	-	-61.5	-	dBm
	MCS 9	-	-60	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm

Receive Adjacent Channel Rejection (VHT20)	MCS0	-	23	-	dBm
	MCS7	-	2	-	dBm
Receive Adjacent Channel Rejection (VHT40)	MCS 0	-	29	-	dBm
	MCS 7	-	5	-	dBm
Receive Adjacent Channel Rejection (VHT80)	MCS 0	-	26	-	dBm
	MCS 7	-	-3	-	dBm

Table 12 5GHz RF receiver specifications

3.6.5 Wi-Fi 5GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	MHz
Output power	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	15.5	-	dBm
	HT20/HT40, MCS 0	-	18	-	dBm
	HT20/HT40, MCS 7	-	15	-	dBm
	VHT80, MCS0	-	18	-	dBm
	VHT80, MCS9	-	14.5	-	dBm
Output Power Variation over RF frequency	TSSI accuracy	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Table 13 5GHz RF transmitter specifications

3.7 PMU electrical characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
Switching regulator					
Input voltage		2.97	3.3	3.63	V
Output voltage	Default voltage setting in the programmable range[1]	1.5	1.6	1.8	V
Output current		-	-	800	mA
Quiescent current	<1mA load current	-	40	55	uA
Line regulation	3V to 3.6V input voltage range @ no load	-	-	1	%
Load regulation	200mA to 600mA load current	-	-	0.05	mV/mA
Efficiency	300mA load current	-	85	-	%
Over-current Shutdown	Threshold	-	960	-	A
Digital LDO					
Input voltage		1.5	1.6	1.8	V
Output voltage		1.08	1.2	1.32	V

Output current		-	-	650	mA
Quiescent current		-	10	-	uA

Note 1: The programmable range of the output voltage of the switching regulator is 0.8V to 2.3V.

Table 14 PMU electrical characteristics

4 Functional specification

4.1 System

4.1.1 Power Management Unit

Power Management Unit (PMU) contains Low Drop-out Regulators (LDOs), highly efficient switching regulator, and the reference band-gap circuit. The circuits are optimized for quiescent current, drop-out voltage, line/load regulation, ripple rejection, and output noise.

Only one power source is required for MT7612E, The 3.3V power source is directly supplied to the switching regulator, digital I/Os, PCIe PHY, and RF related circuit. It's converted to 1.6V by the switching regulator for low voltage circuits. The built-in digital LDOs and RF LDOs converts 1.6V to 1.2V for digital, RF, PCIe PHY, and BBPLL core circuits.

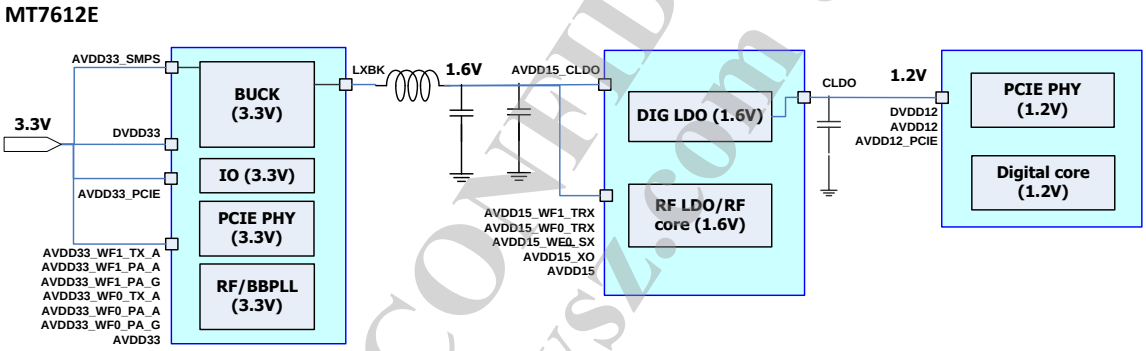


Figure 6 PMU block diagram

The switching regulator integrates the power MOS, and can provide 1A output current driving. It has output current limiting protection to prevent from circuit damage due to abnormal usage. It can reach 80% efficiency when operating at full loading. When the system operates in low power mode, it's turned off by the firmware to reduce the power consumption. It also has low noise spread spectrum operation to reduce the switching noise and the soft-start function.

4.1.2 EFUSE OTP

MT7612E uses embedded Efuse to store device specific configuration information such as MAC addresses, and power control settings.

Below illustrated the major fields defined in the Efuse.

- MAC addresses.
- Wi-Fi country code.
- TSSI parameters, TX power level.
- NIC configuration: RF front-end configuration, LED mode, baseband configuration.

4.1.3 GPIO

MT7612E has GPIO pins with software access. Pins are multiplexed with other functions including the LED control, External RF front-end module control, etc. Each GPIO support internal pull-up/pull-down options as well as driving strength control.

4.2 Host interface architecture

4.2.1 PCI Express

MT7612E supports the high-speed interface which conforms to the PCI Express Base Specification v1.1.
It supports PCIe link power states L0, L0s, L1, and L2. It also supports the new L1 sub-states with CLKREQ ECN as well the capability of Optimized Buffer Flush Fill (OBFF) and Latency Tolerance Reporting (LTR) to provide additional low power modes of operation.
The interface contains all necessary function blocks including transaction layer, data link layer, and physical layer. The standard configuration space and extended configuration space are supported.

4.3 MCU Subsystem

MCU subsystem contains the MCU, internal RAM/ROM and the ROM patch function.
MT7612E uses a 32-bit RISC MCU for low power consumption and efficient use of internal memory.
The MCU controls the host interface, and controls the Wi-Fi hardware.

4.4 Wi-Fi Subsystem

4.4.1 Wi-Fi MAC

MT7612E MAC supports the following features:

- 802.3 to 802.11 header translation offload
- TCP/UDP/IP checksum offload
- Support multiple concurrent clients as an access point
- Support multiple concurrent clients as an repeater
- Shared TX and RX FIFO for maximum throughput
- Aggregate MPDU RX (de-aggregation) and TX (aggregation) support
- Aggregate MSDU support
- Beamforming
  - Explicit Beamforming with support of NDP and Stagger sounding
  - Explicit Beamforming with support of immediate feedback or delayed feedback generation using non-compressed and compressed steering matrix
  - Proprietary Implicit Beamforming using on-chip calibration.
- Transmit rate adaptation
- Transmit power control
- RTS with BW signaling
- CTS with BW signaling in response to RTS with BW signaling

- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP and AES-GCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing

4.4.2 WLAN Baseband

MT7612E baseband supports the following features:

- 11ac stage-1 feature support
  - 20, 40, and 80MHz channels
  - MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
  - MCS8-9 (256QAM, r=3/4 and r=5/6)
  - VHT A-MPDU delimiter for RX and TX for single MPDU
  - Clear Channel Assessment (CCA) on secondary
  - Short Guard Interval
  - STBC support
  - Low Density Parity check (LDPC) coding
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- Dynamic frequency selection (DFS) radar pulse detection

4.4.3 WLAN RF

MT7612E RF supports the following features:

- Integrated 2.4GHz/5GHz PA and LNA
- Integrated 5GHz Balun
- Support 2.4GHz/5GHz external PA and LNA

5 Register

5.1 Memory map

5.1.1 Global View

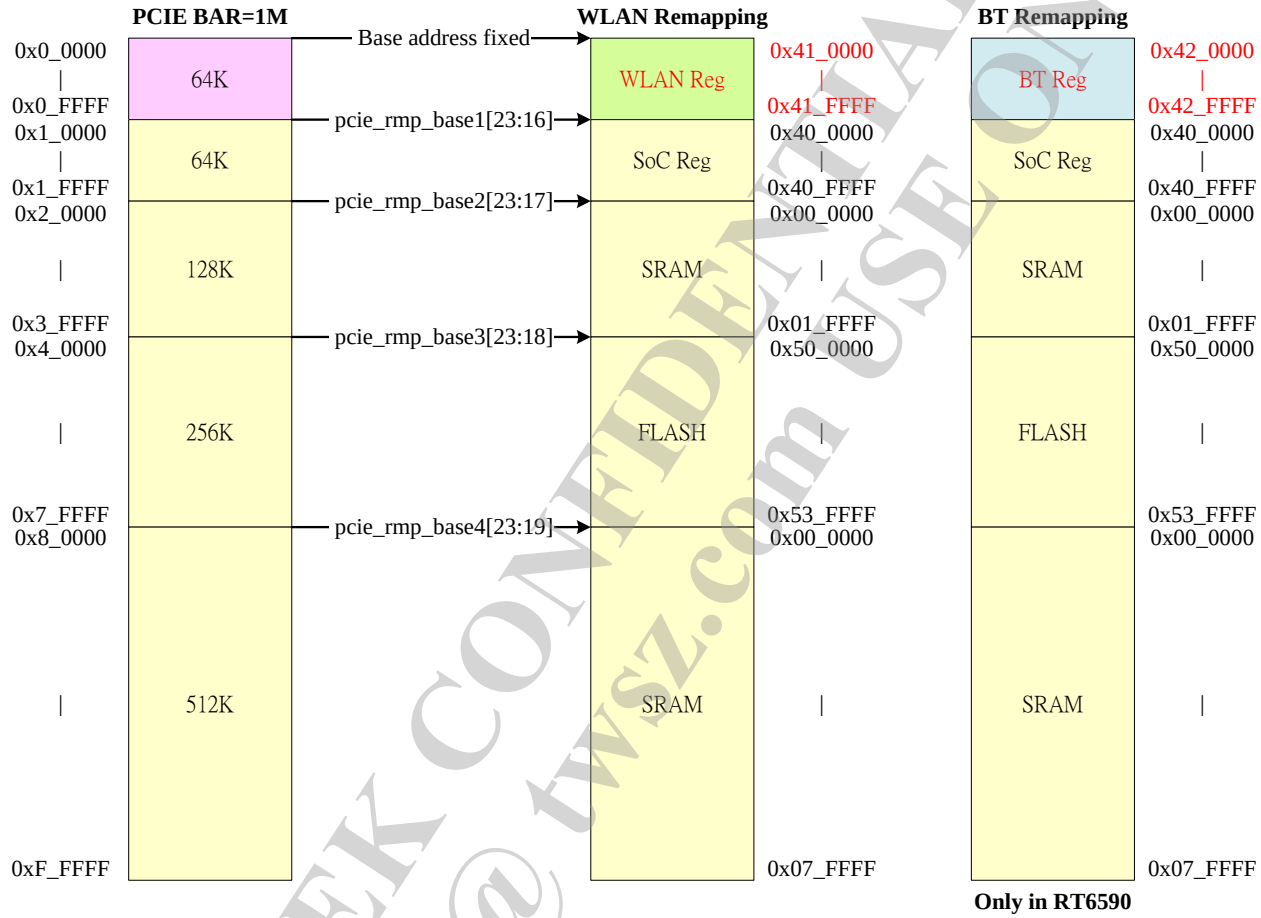
Address	Size	Description	Pbus #
00.0000 – 06.2FFF	396K	ILM-ROM	
06.3000 – 07.FFFF		<<Reserved>>	
08.0000 – 09.FFFF	128K	ILM-RAM	
0A.4000 – 0F.FFFF		<<Reserved>>	
10.0000 – 12.17FF	134K	DLM-RAM	
12.C000 – 3F.FFFF		<<Reserved>>	
40.0000 – 40.01FF	512	SYSCTL	IP08
40.0200 – 40.02FF	256	MCUCTL	IP00
40.0300 – 40.03FF	256	<<Reserved>>	
40.0400 – 40.04FF	256	Timer	IP02
40.0500 – 40.05FF	256	UART-Lite	IP03
40.0600 – 40.06FF	256	<<Reserved>>	
~~40.0700 – 40.07FF~~	~~256~~	~~U2M-PDMA~~	~~IP07~~
40.0800 – 40.0FFF		<<Reserved>>	
40.1000 – 40.9FFF	36K	USB3 MAC/PHY/DMA	IP13
40.A000 – 40.CFFF		<<Reserved>>	
40.D000 – 40.DFFF	4K	Thermal sensor	IP14
40.E000 – 40.EFFF	4K	ROM patch	IP05
40.F000 – 40.FFFF	4K	PCIE Controller	IP06
41.0000 – 41.FFFF	64K	WLAN	
42.0000 – 4F.FFFF	896K	Reserve	
50.0000 – 5F.FFFF	1M	Off-chip SPI FLASH/EEPROM	IP04
60.0000 – 7F.FFFF	2M	Loop code	IP01
80.0000 – 80.FFFF	64K	Reserve	
81.0000 – FF.FFFF		<<Reserved>>	

5.1.2 WLAN 64 K

Address	Size	Description	Pbus #
0000-01FF	512	SYSCTL (remap)	IP08
0200-03FF	512	IF-DMA	IP09
0400-04FF	256	PBF (*)	IP12
0500-06FF	512	TEST (*)	IP12
0700-07FF	256	MCUCTL (remap)	IP00
0800-0BFF	1K	FCE/FCE-PDMA	IP10
0C00-0CFF	256	Data scope	IP12
0D00-0FFF		<<Reserved>>	
1000-1FFF	4K	MAC (*)	IP12
2000-3FFF	8K	BBP	IP11
4000-FFFF	48K	MAC memory (*)	IP12

(*) Share the same Pbus slave.

5.1.3 PCIe view



5.2 Boot mode

boot_mode	Description	Register	Default Value
2'h0	Boot from RAM	ILM_BOOT	0
		DEFAULT_IVB	4'h6
		SPI_ADDR_16B	0
		CPU_ENABLE	1
2'h1	Boot from ROM	ILM_BOOT	1
		DEFAULT_IVB	4'h0
		SPI_ADDR_16B	0
		CPU_ENABLE	1
2'h2	Boot from FLASH	ILM_BOOT	0
		DEFAULT_IVB	4'h5
		SPI_ADDR_16B	0
		CPU_ENABLE	1
2'h3	Boot from EEPROM	ILM_BOOT	0
		DEFAULT_IVB	4'h5
		SPI_ADDR_16B	1
		CPU_ENABLE	1

5.3 System Control Register

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000 0xE001_0000
Reserve	0xF000_0300 0xF001_0000
Andes firmware/TESTIF	0x0040_0000

ASIC_VERSION (offset: 0x0000)

Bits	Type	Name	Description	Init Value
31:16	RO	CHIP_ID	Chip ID	16'h7612
15:8	-	-	reserve	
7:4	RO	HW_ID	HW Version ID	4'h00
3:0	RO	FW_ID	FW Version ID	4'h00

EE_CTRL (offset: 0x0004)

Bits	Type	Name	Description	Init Value
31:5	-	-	Reserved	0
3	RO	EE_DO	EE_DO pin status.	0
2	R/W	EE_DI	Software controlled EE_DI	0
1	R/W	EE_CS	Software controlled EE_CS	0
0	R/W	EE_SCK	Software controlled EE_SCK	0

DBG_CTRL (offset: 0x0008)

Bits	Type	Name	Description	Init Value
31:24	R/W	UTIF_IN_25_18	Utif input bit [25:18]	8'b0
23:16	-	-	Reserved	0
15:9	-	-	Reserved	0
8	R/W	CSR_IO_MODE_EN	1: IO pins can use io_mode in SPI/RBIST strapping mode 0:IO pins in original SPI/RBIST strapping mode	0
7:0	R/W	TEST_CODE	Software controlled debug signal selection	8'h00

DBG_OUT (offset: 0x000C)

Bits	Type	Name	Description	Init Value
31:0	RO	DBG_OUT	Debug output signal	-

DBG_IN (offset: 0x0010)

Bits	Type	Name	Description	Init Value
31:19	-	-	Reserved	0
18	R/W	UTIF_IN_17_0_MODE	1:use register UTIF_IN_17_0 as test_in[17:0] 0:use io[17:0] as test_in[17:0]	0
17:0	R/W	UTIF_IN_17_0	Utif input bit [17:0]	18'b0

BBPL_CTRL0 (offset: 0x0014)

Bits	Type	Name	Description	Init Value
31:30	R/W	RG_WF0_BBPL_RST_DLY_1_0	1.PLL power-on reset timing control 2'b00_ 32*Tref 2'b01_ 64*Tref 2'b10_ 128*Tref 2'b11_ 256*Tref 2.Different DCXO Operation (a)2'b00 for 20MHz DCXO (b)2'b01 for 40MHz DCXO	2'b00
29:28	R/W	RG_WF0_BBPL_PREDIV_1	Pre-divider ratio	2'b00

		_0	2'b00_ /1 2'b01_ /2 2'b10_forbidden 2'b11_ /4	
27:26	R/W	RG_WF0_BBPL_POSDIV_1_0	Post-divider ratio 2'b00_ /1 2'b01_ /2 2'b10_forbidden 2'b11_ /4	2'b00
25:24	R/W	null_1_0	Post-divider ratio 2'b00_ /1 2'b01_ /2 2'b10_forbidden 2'b11_ /4	2'b00
23:19	R/W	RG_WF0_BBPL_RESERVE_4_0		5'b00000
18	R/W	RG_CK_TEST_EN	Testing clock enable 0: disable 1: enable	1'b0
17:16	R/W	RG_WF0_BBPL_TEST_CLK_SEL2_1_0	Testing clock selection 2'b00: TEST_CLK_SEL1<1:0> 2'b01: WF1_RX_ADC_CLK 2'b10: WF1_TX_DAC_CLK 2'b11: WF1_TX_DAC_CLK	2'b00
15:12	R/W	RG_WF0_BBPL_IC_3_0	1.I-path current adjustment MSB 12.5uA 6.25uA 3.125uA LSB 3.125uA 2.Different DCXO Operation (a)4'b0100=6.25uA for 20MHz DCXO (b)4'b0001=3.125uA for40MHz DCXO	4'b0100
11:8	R/W	RG_WF0_BBPL_IR_3_0	1.P-path current adjustment MSB 50uA 25uA 12.5uA LSB 12.5uA 2.Different DCXO Operation (a)4'b1000=50uA for 20MHz DCXO (b)4'b0100=25uA for40MHz DCXO	4'b1000
7:4	R/W	RG_WF0_BBPL_BP_3_0	P-path capacitance adjustment MSB=0.8pF 0.4pF 0.2pF LSB=0.1pF	4'b0100
3:2	R/W	RG_WF0_BBPL_BC_1_0	I-path capacitance adjustment 2'b00_0.5pF 2'b01_1pF 2'b10_1.5pF 2'b11_2pF	2'b11
1:0	R/W	RG_WF0_BBPL_BR_1_0	P-path resistance adjustment 2'b00_140kohm 2'b01_105kohm 2'b10_70kohm 2'b11_35kohm	2'b11

BBPL_CTRL1 (offset: 0x0018)

Bits	Type	Name	Description	Init Value
31	R/W	RG_WF0_BBPL_AUTOK_E	Auto K-Band Enable	1'b1

		N	1'b0_ Disable 1'b1_ Enable	
30	R/W	RG_WF0_BBPL_AUTOK_LOAD	Load Last-Time Auto K-Band Result 1'b0_ Load 1'b1_ Unload	1'b1
29:28	R/W	RG_WF0_BBPL_AUTOK_KS_1_0	Auto K-Band Time Control 2'b00_ 4 ref. clock cycle 2'b01_ 8 ref. clock cycle 2'b10_ 16 ref. clock cycle 2'b11_ 32 ref. clock cycle	2'b11
27:26	R/W	RG_WF0_BBPL_AUTOK_KF_1_0	Auto K-Band Time Control 2'b00_ 8 ref. clock cycle 2'b01_ 16 ref. clock cycle 2'b10_ 32 ref. clock cycle 2'b11_ 64 ref. clock cycle	2'b11
25:24	R/W	RG_WF0_BBPL_AUTOK_PREDIV_1_0	K-Band division ratio control	2'b11
23:16	R/W	RG_WF0_BBPL_BAND_7_0	Manual PLL Band Selection 8'b00000001_ Lowest Band 8'b11111110_ Highest Band	8'b00000000
15:13	R/W	RG_WF0_BBPL_DIVEN_2_0	Time domain cap multiplication ratio 3'd0_ x1 3'd1_ x2 3'd2_ x4 ... 3'd6_ x64	3'b000
12	R/W	RG_WF0_BBPL_MONCK_EN	Monitor clock Enable 1'b0_ Disable 1'b1_ Enable	1'b0
11	R/W	RG_WF0_BBPL_MONVC_EN	Monitor Vctrl Enable 1'b0_ Disable 1'b1_ Enable	1'b0
10	R/W	RG_WF0_BBPL_MONREF_EN	Monitor reference Enable 1'b0_ Disable 1'b1_ Enable	1'b0
9	R/W	RG_WF0_BBPL_VOD_EN	CHP OverDrive Enable 1'b0_ Disable 1'b1_ Enable	1'b0
8	R/W	RG_WF0_BBPL_LVROD_EN	PLL LDO boost enable 1'b0_ Low voltage reference = 1.2V 1'b1_ Low voltage reference from 1.08V to 1.2V	1'b0
7:6	R/W	RG_WF0_BBPL_RESERVE1_1_0	Reserve registers	2'b00
5	R/W	RG_PCIE_BW10M	PCIE MODE LPF BW 0: default 1: PCIE BW 10M	1'b0
4:2	R/W	RG_WF0_BBPL_RESERVE1_2_0	Reserve registers	3'b000
1:0	R/W	RG_WF0_BBPL_TEST_CLK_SEL1_1_0	Testing clock selection 2'b00: PLL_CK 2'b01: FBK_CK 2'b10: REF_CK 2'b11: REF_CK	2'b00

BBPL_CTRL2 (offset: 0x001C)

Bits	Type	Name	Description	Init Value
31:26	-	Reserve	-	-
25	RO	RO_WF0_BBPL_AUTOK_FAIL	Pass signal of Kband	-

24	RO	RO_WF0_BBPL_AUTOK_PASS	Fail signal of Kband	-
23:16	RO	RO_WF0_BBPL_AUTOK_BAND_7_0	Results of Kband	-
15:8	-	Reserve	-	-
7:0	R/W	CSR_BBPL_FBKDIV	FBDIV REF 20MHz: 00110000 (48) REF 40MHz: 00011000 (24) REF 32MHz: 00011110 (30)	8'b00110000

CMB_CTRL (offset: 0x0020)

Bits	Type	Name	Description	Init Value
31:25	-	-	Reserved	-
24	RO	eeload	EE load active signal output	1'b0
23	RO	PLL_LD	BBP PLL lock done	1'b0
22	RO	XTAL_RDY	Xtal ready	1'b0
21:20	R/W		Reserve	2'b01
19	R/W	FOR_CLK_XTAL	0: use pcie(125MHz)/usb(30MHz) as clk_if_src 1:use xtal as clk_if_src	1'b0
18	R/W	GPIO_MODE_LED2	0: GPIO[2] is used as GPIO 1:GPIO[2] is used as MCU LED2	1'b0
17	R/W	GPIO_MODE_LED1	0: GPIO[1] is used as GPIO 1:GPIO[1] is used as MCU LED1	1'b0
16	R/W-	CSR_UART_MODE	0:No Andes UART mode 1:Andes UART mode	1'b0
15:0	R/W	AUX_OPT	Aux control option [0]:0: enable system clock power saving 1: system clock no power saving [1]:0: allow to remove PCIE PHY clock in L1 state 1: always keep PCIE PHY clock on in L1 state [2]:0: allow to remove PCIE PHY clock in D3 state 1: always keep PCIE PHY clock on in D3 state [3]:0: 1: [4]:0: allow to remove PCIE PHY clock despite WLAN on or off 1: allow to remove PCIE PHY clock only when WLAN is off [5]: Reserve [6]:0: 1: [8:7]:PCIE phy rxidle_mode[1:0] [9]:0:PCIE not support stoppable PCIE REFCLK 1.PCIE support stoppable PCIE REFCLK [10]:0:PCIE PHY config by eeprom 1:PCIE PHY config by spi [11]: 0: andes jtag mode (depends on eeprom/efuse value) 1: GPIO mode (depends on eeprom/efuse value) [12]: 0:ANTSEL is used as WLAN TRSW 1: ANTSEL is used as WLAN ANT SEL [13]: PCIE LTR and OBFF function support 0: Not support 1: Support [14]: 0: 1:	EEPROM

			[15]: 0: one antenna mode 1: two antenna mode	

MCU_LED0 → no use

MCU_LED1 → no use

MCU_LED2 →WL_LED

MCU_LED3 → Reserve

EFUSE_CTRL (offset: 0x0024)

Bits	Type	Name	Description	Init Value
31	RO	SEL_EFUSE	Currently used NVM(Non-Volatile Memory) 0: external EEPROM 1: internal e-fuse PROM	0
30	R/W1	EFSROM_KICK	Write it – kick off e-fuse PROM read/write. 0: idle 1: start read/write Read it – busy bit to e-fuse PROM read/write 0: read/write done 1: busy	0
29:26	-		Reserved	0
25:16	R/W	EFSROM_AIN	Address to be read from/written to e-fuse PROM. The address must be 16-byte alignment. (This is to say, the last 4 bits must be 0)	0
15:14	R/W	EFSROM_LDO_ON_TIME	LDO read time (in 128us)	0x2
13:8	R/W	EFSROM_LDO_OFF_TIME	LDO discharge time (in 128us)	0x8
7:6	R/W	EFSROM_MODE	e-fuse PROM access mode: 11: Write in physical view 10: reserved 01: Read in physical view 00: Read in logical view	0
5:0	RO	EFSROM_AOUT	Corresponding usage map entity number to the data read back in logical view	0

RFUSE_DATA0 (offset: 0x0028)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA0	For write: data to be written to e-fuse PROM For read: data read back from e-fuse PROM	0

RFUSE_DATA1 (offset: 0x002C)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA1	For write: data to be written to e-fuse PROM For read: data read back from e-fuse PROM	0

RFUSE_DATA2 (offset: 0x0030)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA2	For write: data to be written to e-fuse PROM For read: data read back from e-fuse PROM	0

RFUSE_DATA3 (offset: 0x0034)

Bits	Type	Name	Description	Init Value
31:0	R/W	EFSROM_DATA3	For write: data to be written to e-fuse PROM For read: data read back from e-fuse PROM	0

EE_CFG0 (offset: 0x0038)

Bits	Type	Name	Description	Init Value

31:25	-	-	Reserved	-
24	RO	CFG_WL_ON_MODE	eFuse WL on mode 0: off 1: on	
23	RO	CFG_AC_ON_MODE	eFuse over write 11AC off mode 0: off 1: on	
22	RO		Reserve	
21:20	RO	CFG_HIF_MODE	eFuse over write HIF 11: U3 10: PCIe+U2 01: PCIe 00: U2	
19	RO	AC_OFF_MODE	11AC off mode 1: off 0: on	bonding opt
18	RO		Reserve	bonding opt
17:16	RO	HIF_MODE	Host Interface Mode 11: U3 10: PCIe+U2 01: PCIe 00: U2	bonding opt
15:0	R/W	ee_cfg0_reg	over write ee_cfg0 0: reserve (directly control by efuse, force U2 mode) 1: reserve 2: Reserve 3: ac on mode 4: wifi on mode 12:5: reserve 15:13: RF front-end setting	16'hFFFF

Reserve (offset: 0x003C)

Reserve (offset: 0x0040)

Reserve (offset: 0x0044)

Reserve (offset: 0x0048)

Reserve (offset: 0x004C)

OLT_CTRL (offset: 0x0050)

Bits	Type	Name	Description	Init Value
31:9	R/W	-	Reserved	-
8	R/W	wifi_olt_scan_mode	wifi olt mode enable	1'b0
7:6	R/W	wifi_olt_mode	wifi olt mode select	2'b0
5	R/W	olt_scan_mode	mbista olt mode	1'b0
4	R/W	ssusb_eq_olt_mode	U3 olt mode enable	1'b0
3	R/W		Reserve	1'b0
2	R/W		Reserve	1'b0
1:0	R/W		Reserve	2'b0

PMU_CTRL0 (offset: 0x0054)

Bits	Type	Name	Description	Init Value
31:30	R/W	RG_BUCK_PFMVH	Burst /PWM mode transition point. High band 00: 600mV 01: 700mV 10: 500mV 11: 400mV	2'b0

29	R/W	RG_BUCK_FPWM	Force-PWM mode selection. 0: normal mode 1: force-PWM mode	1'b0
28	R/W	RG_BUCK_CZADD	Compensation Cap selection (not used)	1'b0
27:26	R/W	RG_BUCK_CSM	Current sensing ratio adjustment. (Current mirror adjust) 00: x2, Rcs ~0.85ohm 01: x3 10: x1.5 11: x2.5	2'b0
25:24	R/W	RG_BUCK_CSR	Current sensing ratio adjustment. (Resister adjust) 00: 65kohm, Rcs ~0.85ohm 01: 55kohm 10: 75kohm 11: 85kohm	2'b0
23:22	R/W	RG_BUCK_CSL	Current limit adjustment 00: 70kohm, ~2.5x OC 01: 60kohm, ~2.9x OC 10: 80kohm, ~2.2x OC 11: 90kohm, ~1.9x OC	2'b0
21:19	R/W	RG_BUCK_CKTRIM	Internal clk frequency calibration	3'b0
18:15	R/W	RG_STUP_RSV	Power-on sequence test mode [3] : Reserved [2] : Force CLDO OFF (including CLDO_STB) [1] : Force Buck OFF [0] : Switch to connect VBG to PAD_TEST. 1: connect; 0: disconnect	4'b0
14	R/W	RG_FORCE_OT_OFF	Force the OT (Over Temperature) OFF 0 : Normal 1 : Force OFF	1'b0
13	R/W	RG_THRCMP_TEST_EN	Enable the test mode of the thermal comparator 0 : Normal mode 1 : Can test thermal comparator's threshold by applying input voltage via PALDO_FB pin. To see the comparator's output, check QI_STARTUP_A2D_RSV<3>.	1'b0
12	R/W	RG_BIAS_GEN_FORCE_TM	Force the IBIAS/VBIAS Generator ON in the Testmode 0 : Normal 1 : Force ON	1'b0
11:8	R/W	RG_IBIAS_SEL	Internal reference current tuning (IGEN of PMU, Iref~2.5uA) 0000 : Iref x 8/20 (~1uA) 0001 : Iref x 9/20 (~1.125uA) 0010 : Iref x 10/20 (~1.25uA) 0011 : Iref x 11/20 (~1.375uA) 0100 : Iref x 8/20 x 8/9 (~0.89uA) 0101 : Iref x 9/20 x 8/9 (~1uA) 0110 : Iref x 10/20 x 8/9 (~1.11uA) 0111 : Iref x 11/20 x 8/9 (~1.22uA) 1000 : Iref x 8/20 x 8/10 (~0.8uA) 1001 : Iref x 9/20 x 8/10 (~0.9uA) 1010 : Iref x 10/20 x 8/10 (~1uA) 1011 : Iref x 11/20 x 8/10 (~1.1uA) 1100 : Iref x 8/20 x 8/11 (~0.73uA) 1101 : Iref x 9/20 x 8/11 (~0.82uA) 1110 : Iref x 10/20 x 8/11 (~0.91uA) 1111 : Iref x 11/20 x 8/11 (~1uA)	4'b0
7:5	R/W	RG_VREF_BG	Reference voltage fine tuning according to VBG 000 : initial setting (assume VBG=1.21V) 001 : plus 2% (assume VBG=1.23V) 010 : plus 4% (assume VBG=1.25V) 011 : plus 6% (assume VBG=1.27V)	3'b0

			100 : minus 0% (assume VBG=1.21V) 101 : minus 6% (assume VBG=1.15V) 110 : minus 4% (assume VBG=1.17V) 111 : minus 2% (assume VBG=1.19V)	
4	R/W	RG_BGOSC_ENB	Enable Oscillator in Bandgap Block 0: enable 1: disable	1'b0
3	R/W	RG_FORCE_BGCK	Force bandgap chopper clock 0 : Use internal BG clock 1 : Use "RG_EXT_BGCK" as the chopping clock input	1'b0
2:0	R/W	RG_VBG_SEL	Bandgap T.C. Fine Tuning 000: Initial Setting 001: Plus 1 Step 010: Plus 2 Step 011: Plus 3 Step 100: Minus 0 Step 101: Minus 1 Step 110: Minus 2 Step 111: Minus 3 Step	3'b0

PMU_CTRL1 (offset: 0x0058)

Bits	Type	Name	Description	Init Value
31:27	R/W	RG_BUCK_VOSEL[4:0]	VOUT selection, 0.825V ~ 1.8V tunable, 25mV/step 000000: 0.825V 000011: 0.9V 000111: 1.0V 001011: 1.1V 001111: 1.2V 010011: 1.3V 010111: 1.4V 011011: 1.5V 011101: 1.55V 011111: 1.6V (default) 100001: 1.65V 100011: 1.7V 100111: 1.8V	5'h1F
26:24	R/W	RG_BUCK_RZSEL	Compensation Resistor selection. 000: 420kohm 001: 210kohm 010: 260kohm 011: 310kohm 100: 520kohm 101: 620kohm 110: 720kohm 111: 820kohm	3'b0
23	R/W	RG_BUCK_NDIS_ENB	Discharge function ENB 0: discharging enable 1: discharging disable	1'b0
22:20	R/W	RG_BUCK_MASEL	Slope compensation selection. [0]: +0.5uA [1]: -1uA [2]: +2uA	3'b0
19	R/W	RG_BUCK_GMSEL	Error amp. Gm selection.	1'b0
18:17	R/W	RG_BUCK_CSOS	Current sense DC offset settings.	2'b0
16:9	R/W	RG_BUCK_RSV	Reserved register [3]: VCS test mode [5:4]: Test mode selection [6]: Test mode enable	8'b0
8:7	R/W	RG_BUCK_ZXOS	Offset setting for Zero-cross detection.	2'b0

6	R/W	RG_BUCK_ZXPDN	Zero-cross detection power-down. 0: ZX detect enable 1: ZX detection off	1'b0
5:4	R/W	RG_BUCK_SLEWN	Slew rate for LX falling edge	2'b0
3:2	R/W	RG_BUCK_SLEW	Slew rate for LX raising edge	2'b0
1:0	R/W	RG_BUCK_PFMVL	Burst /PWM mode transition point. Low band 00: 500mV 01: 600mV 10: 400mV 11: 350mV	2'b0

PMU_CTRL2 (offset: 0x005C)

Bits	Type	Name	Description	Init Value
31	R/W	QI_CKEXT_RDY	External clock ready flag. 0: not ready, internal clk will be used 1: external clk ready. Use ext. clk and internal clk off.	1'b0
30	R/W	NI_CLDO_MODE	low power mode enable 0: normal mode 1: low power mode	1'b0
29:28	R/W	RG_RSV_ELDOS	reserve register for ELDOS	2'b0
27	R/W	RG_ELDO_REMOTE_SENSE	ELDO Remote sense function selection, 0: local sense 1: remote sense	1'b0
26	R/W	RG_ELDO_TBST_EN	RG_ELDO_TBST_EN=RG_LDO25_LARGEA DC enhance=> accuracy enhance	1'b0
25	R/W	RG_ELDO_NDIS_EN	ELDO NDIS Enable	1'b1
24:19	R/W	RG_ELDO_VOSEL	RG_ELDO_VOSEL[5:0]=LDO25_TUNE<5:0> ELDO output voltage Level Adjustment 6`b110000=2.16v 6`b110001=2.22v 6`b110010=2.28v 6`b110011=2.34v 6`b110100=2.40v 6`b110101=2.46v 6`b110110=2.52v 6`b110111=2.58v 6`b111000=264v 6`b111001=2.72v 6`b111010=2.80v 6`b111011=2.84v	6'h35
18:15	R/W	RG_RSV_CLDOS	reserve register for CLDO	4'b0
14	R/W	RG_CLDO_BIST_EN	BIST EN 0: disable; 1:enable	1'b0
13	R/W	RG_CLDO_NDIS_EN	POWER DOWN NMOS Enable 1: enable 0: disable	1'b0
12:8	R/W	RG_CLDO_CAL	Voltage Calibration (keep dropout voltage >=0.3V) 5b'01010: 1.42V 5b'01001: 1.40V 5b'01000: 1.38V 5b'00111: 1.36V 5b'00110: 1.32V 5b'00101: 1.3V 5b'00100: 1.28V 5b'00011: 1.26V 5b'00010 1.24V 5b'00001: 1.22V 5b'00000: 1.2V	5'b0

			5b'11111 1.18V 5b'11110: 1.16V 5b'11101: 1.14V 5b'11100 1.12V 5b'11011: 1.10V 5b'11010: 1.08V 5b'11001: 1.06V 5b'11000:1.04V 5b'10111: 1.02V 5b'10110: 1.00V 5b'10101: 0.98V 5b'10100: 0.96V 5b'10011: 0.94V 5b'10010: 0.92V 5b'10001: 0.90V 5b'10000: 0.88V	
7:5	R/W	RG_ABIST_SEL	ABIST selection for test mode. 000: default, BUCK normal mode others: for LDOs PM measurement	3'b0
4:1	R/W	RG_BUCK_VOCAL	VOUT calibration. 0000: default value 0001: +0.78% 0010: +1.56% 0011: +2.34% 0100: +3.13% 0101: +3.91% 0110: +4.69% 0111: +5.47% 1111: -0.78% 1110: -1.56% 1101: -2.34% 1100: -3.13% 1011: -3.91% 1010: -4.69% 1001: -5.47% 1000: -6.25%	4'b0
0	R/W	RG_BUCK_VOSEL[5]		1'b0

PMU_STATUS (offset: 0x0060)

Bits	Type	Name	Description	Init Value
31:8	RO	PMU_STATUS		-
11	RO	qi_cldo_rsv		-
10	RO	ni_buck_tmsig		-
9	RO	qi_buck_oc		-
8	RO	qi_cldo_rsv		-
7:4	RO	qi_startup_a2d_rsv		-
3	RO	qi_bg_rdy		-
2	RO	qi_por		-
1	RO	qi_uv		-
0	RO	qi_pmu_rst		-

MISC_CTRL (offset: 0x0064)

Bits	Type	Name	Description	Init Value
31	RO	RBIST_DW_EN	RBIST download enable signal	0
30	RO	PERST_N	PCIE PERST_N input pin readout	0
29	RO	XTAL_SEL_20	Xtal 20MHz selection after boot strapping 0:40 MHz Xtal 1:20MHz Xtal	Bootstrap
28	RO	EXT_EE_SEL	External EE selection after boot strapping	Bootstrap

			0: select internal EFUS 1: select external EEPROM	
27:24	RO	CHIP_MODE	Chip mode after boot strapping 000:Normal Boot from RAM 001:Normal Boot from ROM 010:Normal Boot from Serial Flash (USB mode only) 011:Normal Boot from Serial EEPROM (USB mode only) 100:SPI mode 101: Scan mode + bypass PLL 110: Test mode 111: Test mode + bypass PLL	Bootstrap
23	R/W	EN_CLK_IFDMA_WIFI	CLK enable signal of clk_ifdma_wifi	1'b1
22	R/W	CSR_IFDMA_RST	IFDMA SW reset	1'b0
21	R/W	CSR_FCE_RST	FCE SW reset	1'b0
20	R/W	CSR_WLAN_RST	WLAN_CORE(MAC/PBF/SEC) SW reset	1'b0
19	R/W	CSR_WL_PATH_RST	ALL WLAN function (BBP/MAC/PBF/SEC/FCE/IFDMA) SW reset	1'b0
18	R/W	CSR_BBP_RST	BBP SW reset	1'b1
17	R/W	CSR_U3DMA_RST	U3DMA SW reset	1'b0
16:11	R/W	-	Reserved for low power control in E3	6'h3F
10	R/W	csr_if_slow_en	Enable clk_if_slow_en=1 (clk_if_slow run in sys_clk)	1'b0
9	R/W	csr_bypass_ini	For rbist test, bypass power on sequence and jump to rbist procedure. 1: bypass 0: normal	1'b0
8	R/W	Csr_sel_93c66	0: access external 25060 through register 0x04 1: access external 93C66 through register 0x04	1'b1
7:6	-	-	Reserved	-
5	R/W	CRS_USB_REF_F20M_CKEN	for gating usb_ref_f20m_clk 9/10 cycle in E3	1'b0
4	R/W	CSR_CHIP_RST_N	for whole chip reset in E3	1'b1
3	R/W	PHYA scan mode	use utif to test PHYA scan	1'b0
2:1	R/W	CSR_WAKEUP_OPT	Register control of wakeup_opt	2'b0
0	R/W	CSR_WAKEUP_N	Register control of wakeup_n	1'b0

PCIE_SPI (offset: 0x0078)

Bits	Type	Name	Description	Init Value
31	R/W	PCIE_SOC_SPI_MODE	0:Use utif pins for PCIE SPI 1:Use SOC pci host controller for PCIE SPI	1'b0
30	R/W	PCIE_PROBE_MODE	0:Use PCIE internal cfg idx as probe idx 1:Use CSR_PROBE_IDX as probe idx	1'b0
29:16	-	-	Reserved	-
15:8	R/W	CSR_PROBE_IDX1	PCIE probe idx1 selection register	14'h900
7:0	R/W	CSR_PROBE_IDX0	PCIE probe idx0 selection register	10'h0a0

*Reserved for PCIE PHY test

FFT_OUT (offset: 0x007c)

Bits	Type	Name	Description	Init Value
31:0	RO	-	Reserved	-

WLAN_FUN_CTRL (offset: 0x0080)

Bits	Type	Name	Description	Init Value
31:10	-	-	Reserved	-
9	R/W	therm_cken	thermal ctl clock enable	1'b1
8	R/W	therm_rst	thermal ctl sw reset	1'b0
7	R/W	WAKE_HOST_F0	Wakeup host for WLAN	1'b0
6	R/W	INV_ANT_SEL	Invert ANT_SEL_P/ANT_SEL_N	1'b0
5	R/W	FRC_WL_ANT_SEL	Force WLAN_ANT_SEL output 1: WLAN_ANT_SEL = 1	1'b0

			0: WLAN_ANT_SEL controlled by H/W	
4	R/W	PCIE_APP0_CLK_REQ	PCIE function0 (WLAN) clock request	1'b0
3	R/W	csr_f20m_cken	enable 20Mhz clock source	1'b1
2	R/W	WLAN_RESET_RF	Reset WLAN_RF	1'b0
1	R/W	WLAN_CLK_EN	WLAN clock enable	1'b1
0	R/W	WLAN_EN	WLAN function enable	1'b0

WLAN_FUN_INFO (offset: 0x0084)

Bits	Type	Name	Description	Init Value
31:0	R/W	WLAN_FUN_INFO	WLAN function information (R/W by driver)	32'h00

AUX_TIMER0 (offset: 0x0088)

Bits	Type	Name	Description	Init Value
31	R/W	AUX_TIMER0_EN	Enable AUX_TIMER0 1: enable aux timer, load timer value to counter and start down count Uint: Xtal enable: 1 us Xtal disabled: 1/F_OSC	1'h00
30:24	R/O	NA	Unused	7'h00
23:0	R/W	AUX_TIMER0_VALUE	AUX Timer0 load value	24'h00

AUX_TIMER1 (offset: 0x008C)

Bits	Type	Name	Description	Init Value
31	R/W	AUX_TIMER1_EN	Enable AUX_TIMER1 1: enable aux timer, load timer value to counter and start down count Uint: Xtal enable: 1 us Xtal disabled: 1/F_OSC	1'h00
30:24	R/O	NA	Unused	7'h00
23:0	R/W	AUX_TIMER1_VALUE	AUX Timer1 load value	24'h00

RBIST_START_ADDR (offset: 0x0090)

Bits	Type	Name	Description	Init Value
31:0	R/W	RBIST_START_ADDR	RBIST WR/RD start address	32'b0

AUX_MS_TMR (offset: 0x0094)

Bits	Type	Name	Description	Init Value
31:0	RO	AUX_MS_TIMER	For every 1ms , it strigger interrupt to mcusys, in the mean while, increase 1 for every 1ms to register out.	32'h00

XTAL_CAL (offset: 0x0098)

Bits	Type	Name	Description	Init Value
31	R/O	XTAL_DET_VLD	Xtal calibration counter valid, clalibration done	1'h00
30:27	-	-	-	-
26:25	-	REF_CNT_SEL	Reference clk counter value set: 0:0.5M 1:1M 2:2M 3:2M	2'b01
24	R/W	XTA_DET_EN	Enable xtal calirbation	1'b0
23:21	-	-	-	-
20:0	R/O	XTAL_COUNTER	Xtal counter value	21'h00

Reserve (offset: 0x00B4)

US_TMR (offset: 0x00B8)

Bits	Type	Name	Description	Init Value
31	R/W	US_TIMER_EN	US counter enable	1'b1

30:0	RO	US_TIMER	US counter value	32'h00

Reserve (offset: 0x00C0)

Reserve (offset: 0x00C4)

LMP_TIMER0 (offset: 0x00C8)

Bits	Type	Name	Description	Init Value
31	R/W	TIMER0_EN	Enable LMP_TIMER0 1: enable timer 0, 0: disable LMP_TIMER0 In single shot mode, it will be auto cleared by H/W when counter stops. In auto reload mode, it can only be cleared by S/W. When set to '1', the download counter is decremented by one every 1 us. An interrupt is generated when the counter reaches '1'. When set to '0', the down counter is stopped but not cleared nor reloaded.	1'h0
30	R/WC	TIMER0_IRQ	Interrupt status of LMP_TIMER0. When down counter reaches '1', this bit is set to '1'. S/W writes '1' to clear	1'h0
29	R/W	TIMER0_LOAD	Write: 1: load TIMER0_VALUE into the down counter 0: do not load TIMER0_VALUE into down counter When clear interrupt status, set this bit to '0'. Read: Always returns '0' when read.	1'h0
28	R/W	TIMER0_MODE	1: auto reload mode 0: single shot mode	1'h0
27:24	R/O	NA	Unused	4'h0
23:16	R/W	IRQ_COUNT	Increased by 1 for each TIMER0_IRQ S/W can also write to this register (e.g. to clear to 0)	8'h00
15:0	R/W	TIMER0_VALUE	Timer 0 load value	16'h00

LMP_TIMER1 (offset: 0x00CC)

Bits	Type	Name	Description	Init Value
31	R/W	TIMER1_EN	Enable LMP_TIMER1 1: enable timer 1, 0: disable LMP_TIMER1 In single shot mode, it will be auto cleared by H/W when counter stops. In auto reload mode, it can only be cleared by S/W. When set to '1', the download counter is decremented by one every 1 us. An interrupt is generated when the counter reaches '1'. When set to '0', the down counter is stopped but not cleared nor reloaded.	1'h0
30	R/WC	TIMER1_IRQ	Interrupt status of LMP_TIMER1. When down counter reaches '1', this bit is set to '1'. S/W writes '1' to clear	1'h0
29	R/W	TIMER1_LOAD	Write: 1: load TIMER1_VALUE into the down counter 0: do not load TIMER1_VALUE into down counter When clear interrupt status, set this bit to '0' Read: Always returns '0' when read.	1'h0
28	R/W	TIMER1_MODE	1: auto reload mode	1'h0

			0: single shot mode	
27:26	R/O	NA	Unused	2'h0
25:0	R/W	TIMER1_VALUE	Timer 1 load value	26'h00

CSR_LTR_MAX_LAT_F0 (offset: 0x00D0)

Bits	Type	Name	Description	Init Value
31:29	-	-	Reserved	-
28:26	RO	MAX_NSNP_LAT_SCL	Max No-Snoop Latency Scale reported by function 0 of PCIe controller.	3'h0
25:16	RO	MAX_NSNP_LAT	Max No-Snoop Latency Value reported by function 0 of PCIe controller.	10'h0
15:13	-	-	Reserved	-
12:10	RO	MAX_SNP_LAT_SCL	Max Snoop Latency Scale reported by function 0 of PCIe controller.	3'h0
9:0	RO	MAX_SNP_LAT	Max Snoop Latency Value reported by function 0 of PCIe controller.	10'h0

CSR_LTR_MAX_LAT_F1 (offset: 0x00D4)

Bits	Type	Name	Description	Init Value
31:29	-	-	Reserved	-
28:26	RO	MAX_NSNP_LAT_SCL	Max No-Snoop Latency Scale reported by function 1 of PCIe controller.	3'h0
25:16	RO	MAX_NSNP_LAT	Max No-Snoop Latency Value reported by function 1 of PCIe controller.	10'h0
15:13	-	-	Reserved	-
12:10	RO	MAX_SNP_LAT_SCL	Max Snoop Latency Scale reported by function 1 of PCIe controller.	3'h0
9:0	RO	MAX_SNP_LAT	Max Snoop Latency Value reported by function 1 of PCIe controller.	10'h0

CSR_LTR_OBFF_CTRL (offset: 0x00D8)

Bits	Type	Name	Description	Init Value
31:28	-	-	Reserved	-
27	RO	LTR_M_SUPPORT	LTR Mechanism Support in PCIe capability register 0 : Not support 1 : Support	1'h1
26	RO	OBFF_SUPPORT	OBFF function Support in PCIe capability register 0 : Not support 1 : Both WAKE# and Message are supported	1'h1
25:24	R/W	OBFF_TRG_MODE	OBFF Trigger Mode 00 : No trigger mode 01 : Triggered by FCE queue level 10 : Triggered by Timer expired 11 : Reserved	2'h0
23:16	R/W	OBFF_EXPR_TIMER	OBFF Expired Timer The actual timer value is (OBFF_EXPR_TIMER * OBFF_TIMER_SCL) us. 0 here means that instant expired, no more accumulation.	8'h0
15	-	-	Reserved	-
14:12	R/W	OBFF_TIMER_SCL	OBFF Timer Scale 000 : expire timer unit is 1us 001 : expire timer unit is 2us 010 : expire timer unit is 4us 011 : expire timer unit is 8us 100 : expire timer unit is 20us 101 : expire timer unit is 40us 110 : expire timer unit is 80us 111 : expire timer unit is 160us	3'h0
11	R/W	OBFF_MSG_CPUACT_EN	OBFF Message for CPU Active Enable 0 : disable re-active PCIe function when receiving OBFF message for CPU Active. 1 : enable re-active PCIe function when receiving OBFF message for	1'b1

			CPU Active.	
10	R/W	OBFF_MSG_OBFF_INTR	OBFF Message for OBFF Interrupt Enable 0 : disable PCIe interrupt function when receiving OBFF message for OBFF. 1 : enable re-active PCIe interrupt function when receiving OBFF message for OBFF.	1'b1
9	R/W	OBFF_MSG_OBFF_DMA	OBFF Message for OBFF DMA Enable 0 : disable PCIe DMA when receiving OBFF message for OBFF. 1 : enable re-active PCIe DMA when receiving OBFF message for OBFF.	1'b1
8	R/W	OBFF_MSG_IDLE	OBFF Message for IDLE Enable 0 : disable suspend PCIe function when receiving OBFF message for OBFF. 1 : enable suspend PCIe function when receiving OBFF message for OBFF.	1'b1
7:6	RO	OBFF_EN	OBFF Enable support (Platform dependent) 00 : OBFF not support. 01 : OBFF supported using Message signaling only. 10 : OBFF supported using WAKE# signaling only. 11 : OBFF supported using WAKE# and Message signaling.	2'h3
5	R/W	OBFF_REQID_CMP_EN	OBFF Message Request ID Compare Enable 0 : disable OBFF message request ID comparison with ID of function 0. 1 : enable OBFF message request ID comparison with ID of function 0.	1'h1
4	R/W	LTR_MSG_FRC_UPDT	LTR Message Force Update Let LTR message update immediately. SW must assert this bit after LTR message ready, and de-assert later.	1'h0
3:1	R/W	LTR_FUNC_NUM	LTR Message Function Number 000 : for WIFI 001 : Reserve Others : reserved	3'h0
0	RO	LTR_M_EN	LTR Mechanism Enable (Platform dependent) It is reported by PCIe controller for LTR operation on the current platform.	1'h0

CSR_LTR_MSG (offset: 0x00DC)

Bits	Type	Name	Description	Init Value
31	R/W	NSNP_LTR_MSG_REQ	No-Snoop LTR Message Requirement	1'h0
30:29	-	-	Reserved	-
28:26	R/W	NSNP_LAT_SCL	No-Snoop Latency Scale 000 : time unit is 1ns 001 : time unit is 32ns 010 : time unit is 1,024ns 011 : time unit is 32,768ns 100 : time unit is 1.048,576ns 101 : time unit is 33,554,432ns others : reserved	3'h0
25:16	R/W	NSNP_LAT	No-Snoop Latency	10'h0
15	R/W	SNP_LTR_MSG_REQ	Snoop LTR Message Requirement	1'h0
14:13	-	-	Reserved	-
12:10	R/W	SNP_LAT_SCL	Snoop Latency Scale 000 : time unit is 1ns 001 : time unit is 32ns 010 : time unit is 1,024ns 011 : time unit is 32,768ns 100 : time unit is 1.048,576ns 101 : time unit is 33,554,432ns others : reserved	3'h0

9:0	R/W	SNP_LAT	Snoop Latency	10'h0

Reserve (offset: 0xf4)

Reserve (offset: 0xf8)

Reserve (offset: 0xfc)

XO_CTRL0 (offset: 0x0100)

Bits	Type	Name	Description	Init Value
31:19	-	-	-	
18	RO	xo_lpm_en	1: in low power mode 0: in normal mode	
17	RO	xo_ready	xo ready 1: ready for change mode 0: not ready for change mode	
16	RO	rc_xo_ready	read then clean flag for xo ready	
15:5	-	-	-	
4:3	R/W	xo_slow_mode	adjust the timer to x1~x4 0: x1, 1:x2, 2:x3, 3:x4	2'b00
2	R/W	xo_manual_lpm_on	xo_manual_lpm=1'b1 then can on/off manually	1'b0
1	R/W	xo_manual_lpm	on/off the low power mode manually	1'b0
0	R/W	xo_seq_en	start XO power on sequence	1'b0

XO_CTRL1 (offset: 0x0104)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_temp1	change mode value for temp1 step	32'b?

XO_CTRL2 (offset: 0x0108)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_temp2	change mode value for temp2 step	32'b?

XO_CTRL3 (offset: 0x010C)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_temp3	change mode value for temp3 step	32'b?

XO_CTRL4 (offset: 0x0110)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_final	change mode value for final step	32'b?

XO_CTRL5 (offset: 0x0114)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_test1	xo_test1	32'b?
14:8	R/W	c2 value	default is 7'd60, increase frequency down, decrease frequency up	7'h60
7:0	R/W	xo_seq_test1	xo_test1	32'b?

XO_CTRL6 (offset: 0x0118)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_seq_test2	xo_test2	32'b?
14:8	R/W	c2 manual control	manual mode 7'b111_1111	7'b0
7:0	R/W	xo_seq_test2	xo_test2	32'b?

XO_CTRL6 (offset: 0x011C)

Bits	Type	Name	Description	Init Value
31:0	R/W	xo_ctrl		32'b?

REG_IO_MODE0 (offset: 0x0120)

Bits	Type	Name	Description	Init Value
31:0	R/W	Reg_io_mode0	Change the IO function in Normal mode or SPI/RBIST mode and	32'b0

			reg_io_mode_en(0x80[8])=1 Reg_io_mode0[3:0]=>reg_io_mode_00[3:0] … Reg_io_mode0[31:28]=>reg_io_mode_07[3:0]	

REG_IO_MODE 1 (offset: 0x0124)

Bits	Type	Name	Description	Init Value
31:0	R/W	Reg_io_mode1	Change the IO function in Normal mode or SPI/RBIST mode and reg_io_mode_en(0x80[8])=1 Reg_io_mode1[3:0]=>reg_io_mode_08[3:0] … Reg_io_mode1[31:28]=>reg_io_mode_15[3:0]	32'b0

REG_IO_MODE 2 (offset: 0x0128)

Bits	Type	Name	Description	Init Value
31	R/W	MUX_UART_EN	Enable uart/uart-lite pin mux signals	1b0
300	R/W	Reg_io_mode2	Change the IO function in Normal mode or SPI/RBIST mode and reg_io_mode_en(0x80[8])=1 Reg_io_mode2[3:0]=>reg_io_mode_16[3:0] … Reg_io_mode2[19:16]=>reg_io_mode_20[3:0]	31b0

MBISTA_SETTING (offset: 0x012C)

Bits	Type	Name	Description	Init Value
31:16	R/W	mbist_background	control all of the mbista background	16'h55AA
15:0	R/W	mbist_bsel	control all of the byte select	16'hFFFF

WIFI_RF_CTL (offset: 0x0130)

Bits	Type	Name	Description	Init Value
31:26	-	-	Reserved for E3 desense debug used.	-
25	W/R	u3_ana_f20m_clk		1'b1
24	W/R	error_handling_en		1'b0
23:20	-	-	Reserved	-
19	R/W	MAC_SEL_AUX		1'b0
18	R/W	DA_WF0_BBPL_ROOTCLK_SEL		1'b1
17	R/W	DA_EN_WF0_BBPL_EN	PLL Enable 1'b0: Disable 1'b1: Enable	1'b0
16	R/W	DA_EN_WF0_BBPL_CLDO		1'b1
15	-	-	Reserved	-
14	R/W	WF1 in 2G		1'b0
13	R/W	DA_EN_WF1_ADDA_LDO		1'b0
12	R/W	DA_EN_WF1_ABB_LDO		1'b0
11	R/W	DA_EN_WF1_AFE		1'b0
10	R/W	DA_EN_WF1_RFDIG_CLDO	PLL digital part LDO from digital side 1'b0: from RFDIGI LDO (V13_RFDIG) 1'b1: from digital side (DVDD)	1'b1
9	R/W	DA_EN_WF1_RFDIGLDO		1'b0
8	R/W	DA_EN_WF1_BG		1'b0
7	-	-	Reserved	-
6	R/W	WF0 in 2G		1'b0
5	R/W	DA_EN_WF0_ADDA_LDO		1'b0
4	R/W	DA_EN_WF0_ABB_LDO		1'b0
3	R/W	DA_EN_WF0_AFE		1'b0
2	R/W	DA_EN_WF0_RFDIG_CLDO	PLL digital part LDO from digital side 1'b0: from RFDIGI LDO (V13_RFDIG) 1'b1: from digital side (DVDD)	1'b1
1	R/W	DA_EN_WF0_RFDIGLDO		1'b0

0	R/W	DA_EN_WF0_BG		1'b0

SLPCTL_CTRL0 (offset: 0x013C)

Bits	Type	Name	Description	Init Value
31:13	-	-	Reserved	-
12:8	R/W	PMU_CLDO_SETP2	set RG_CLDO_CAL value in step2 (1.08V)	5'b11010
7:5	-	-	Reserved	-
4:0	R/W	PMU_CLDO_SETP1	set RG_CLDO_CAL value in step1 (1.14V)	5'b11101

SLPCTL_CTRL1 (offset: 0x0140)

Bits	Type	Name	Description	Init Value
31:28	RO	ST_SLPCTL	State of SLPCTL state machine 4'h0: Active 4'h4: Sleep	4'h0
27	-	-	Reserved	-
26	R/W	PCIE_MANUAL_RB	PCIe RAM manual reset	1'b1
25	R/W	HIF_MEM_RB	Reset HIF RAM.	1'b1
24	R/W		Reserve	1'b1
23:19	-	-	Reserved	-
18	R/W	PCIE_MANUAL_PD	PCIe RAM manual power down mode	1'b0
17	R/W	HIF_MEM_PD	Power down HIF RAM.	1'b0
16	R/W		Reserve	1'b0
15:12	-	-	Reserved	-
11:0	R/W	SLPCTL_CFG	SLPCTL state machine control [0]: Enable state machine [1]: Trigger state machine to sleep [2]: Trigger state machine to wakeup [3]: MCU ROM force mode [4]: Disable MCU clock when sleep [5]: Power down MCU ROM when sleep [6]: Reserved [7]: Enter XTAL low power mode when sleep [8]: Enter PMU low voltage mode when sleep [9]: MCU ROM 0-192KB PD in force mode [10]: MCU ROM 192-396KB PD in force mode [11] MCU ROM RB in force mode	12'h0

Reserve (offset: 0x00144)

WL_MTC_CTRL (offset: 0x00148)

Bits	Type	Name	Description	Init Value
31:28	RO	ST_WL_MTC	State of WL_MTC state machine 4'h0: power-down 4'h1: power-up	
27	R/W	TSO_MEM_RB	Reset down TSO RAM.	1'b1
26	R/W	FCE_MEM_RB	Reset down FCE RAM.	1'b1
25	R/W	PBF_MEM_RB	Reset PBF RAM	1'b1
24	R/W	BBP_MEM_RB	Power down BBP RAM.	1'b1
23	-	-	Reserved	-
22	R/W	TSO_MEM_PD	Power down TSO RAM.	1'b1
21	R/W	FCE_MEM_PD	Power down FCE RAM.	1'b1
20	R/W	PBF_MEM_PD	Power down PBF RAM	1'b1
19:16	R/W	BBP_MEM_PD	Power down BBP RAM.	4'h1
15:14	-	-	Reserved	-
13	RO	WL_MTC_PWR_ACK_S	WL_MTC_PWR_ACK_S signal	1'b0

12	RO	WL_MTC_PWR_ACK	WL_MTC_PWR_ACK signal	1'b0
11:0	R/W	WL_MTC_CFG	WIFI MTCMOS state machine control [0]: Power-up WIFI MTCMOS [1]: Power-down WIFI MTCMOS [2]: WIFI MTCMOS and MEM signals force mode [3]: Reserved [4]: WL_MTC_RSTB value in force mode [5]: WL_MTC_ISO value in force mode [6]: WL_MTC_PWR_ON value in force mode [7]: WL_MTC_PWR_ON_S value in force mode [8]: WL_MEM_SLEEPB value in force mode [9]: WL_MEM_ISO value in force mode [11:10]: Reserved	12'h0

CLK_ENABLE (offset: 0x0014C)

Bits	Type	Name	Description	Init Value
31:16	R/W		[16]: f32k_clk enable [17]: f1m_clk enable [18]: f2m_clk enable [19]: f240m_clk enable [20]: f320m_clk enable [23:21]: reserve [24]: mcusys_sel 0:from wifi pll, 1: Reserve [25]: xo_clk_sel 0:xtal frequence. 1:xtal frequence/2 [26]: sys_clk_sel, system clock select in force mode 1: 32KHz clock, 0: Xtal clock [31:27]: reserve	16'h0007
15:8	R/W	PUM_LV_TIMER		8''h14
7:4	R/W	MTC_TIMER	MTCMOS control signal timer. Unit: 31.25us.	4'h0
3:0	R/W	PLL_TIMER	PLL count down timer for SLPCTL. Unit:31.25us	4'h0

Reserve (offset: 0x0150)

Reserve (offset: 0x0154)

Reserve (offset: 0x0158)

Reserve (offset: 0x015C)

Reserve (offset: 0x0160)

Reserve (offset: 0x0164)

Register allocation table

PTA_CNT_MODE	2'b00	2'b01	2'b10,2'b11
0x150	wl_fail_pri[31:0]	wl_fail_pri_tx[31:0]	Bt_fail_pri[7:0], wl_fail_pri_tx[23:0]
0x154	wl_fail_abt[31:0]	wl_fail_abt_tx[31:0]	Bt_fail_pri[15:8], wl_fail_abt_tx[23:0]
0x158	wl_pass[31:0]	wl_pass_tx[31:0]	Bt_fail_abt[7:0], wl_pass_tx[23:0]
0x15c	bt_fail_pri[31:0]	wl_fail_pri_rx[31:0]	Bt_fail_abt[15:8], wl_fail_pri_rx[23:0]
0x160	bt_fail_abt[31:0]	wl_fail_abt_rx[31:0]	Bt_pass[7:0], wl_fail_abt_rx[23:0]
0x164	bt_pass[31:0]	wl_pass_rx[31:0]	Bt_pass[15:8], wl_pass_rx[23:0]

Delsel0(offset: 0x01A0)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel0	SRAM delay select	32'b0

Delsel1(offset: 0x01A4)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel1	SRAM delay select	32'b0

Delsel2(offset: 0x01A8)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel2	SRAM delay select	32'b0

Delsel3(offset: 0x01AC)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel3	SRAM delay select	32'b0

Delsel4(offset: 0x01B0)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel4	SRAM delay select	32'b0

Delsel5(offset: 0x01B4)

Bits	Type	Name	Description	Init Value
31:0	R/W	delsel5	SRAM delay select	32'b0

GPIO_OEN (offset: 0x01B8)

Bits	Type	Name	Description	Init Value
31:24	R/W	GPO[19:12] as LED	1'b0 switch to LED one by on, GPIO[19:12] mapping to {LED[3:0],LED[3:0]}	8'hFF
23:22	-	-	reserve	
21:0	R/W	gpio_oen[21:0]	GPIO oen	21'h1FFFFF

GPO (offset: 0x01BC)

Bits	Type	Name	Description	Init Value
31:22	-	-	reserve	
21:0	R/W	gpo[21:0]	GPO	21'h0

GPI (offset: 0x01C0)

Bits	Type	Name	Description	Init Value
31:22	-	-	reserve	
21:0	R	gpi[21:0]	GPI	21'h0

CIDCFG (offset: 0x01C4)

Bits	Type	Name	Description	Init Value
31:0	R	cidcfg[20:0]	CIDCFG	21'h1FFFFF

IOCFG_ISE (offset: 0x01C8)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_ise[20:0]	IO config ISE for each (AGPIO) pin.	21'h1FFFFF

IOCFG_R1 (offset: 0x01CC)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_r1[20:0]	IO config R1 for each (floating IO pad) pin.	21'b0

IOCFG_R0 (offset: 0x01D0)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_r0[20:0]	IO config R0 for each (floating IO pad) pin.	21'b0

IOCFG_PDPU (offset: 0x01D4)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_pdpu[20:0]	IO config pull up/down for each (floating IO pad) pin.	21'b0

IOCFG_PU (offset: 0x01D8)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_pu[20:0]	IO config pull up for each pin.	21'h00001

IOCFG_PD (offset: 0x01DC)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_pd[20:0]	IO config pull down for each pin.	21'h007980

IOCFG_E8 (offset: 0x01E0)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_e8[20:0]	IO config driving strengh for each pin.	21'h1FFFFF

E8	E4	Driving
0	0	4mA
0	1	8mA
1	0	12mA
1	1	16mA

IOCFG_E4 (offset: 0x01E4)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_e4[20:0]	IO config driving strengh for each pin.	21'h1FFFFF

E8	E4	Driving
0	0	4mA
0	1	8mA
1	0	12mA
1	1	16mA

IOCFG_SMT (offset: 0x01E8)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_smt[20:0]	IO config SMT for each pin.	21'b0

IOCFG_SR (offset: 0x01EC)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_sr[20:0]	IO config Slew Rate for each pin. 0: Fast, 1:Slow	21'b0

IOCFG_RDSEL1 (offset: 0x01F0)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_rdsel1[20:0]	IO config RDSEL1 for each pin.	21'b0

IOCFG_RDSEL0 (offset: 0x01F4)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_rdsel0[20:0]	IO config RDSEL0 for each pin.	21'b0

IOCFG_TDSEL1 (offset: 0x01F8)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_tdsel1[20:0]	IO config TDSEL1 for each pin.	21'b0

IOCFG_TDSEL0 (offset: 0x01FC)

Bits	Type	Name	Description	Init Value
31:0	R/W	gpiocfg_tdsel0[20:0]	IO config TDSEL0 for each pin.	21'b0

5.4 MCUSYS registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE001_0000
Reserve	0xF001_0000
Andes firmware/TESTIF	0x0040_0000

Note: For PCIe WLAN driver, 0xE001_0200 also map to 0xE000_0700.

5.4.1 MCUCTL registers

BOOT_MODE (offset: 0x0200, default: 0x0)

Bits	Type	Name	Description	Initial value
31:2	-	-	Reserved	-
1:0	RO	BOOT_MODE	Boot mode For boot from RAM, initial value is 2'h0. For boot from ROM, initial value is 2'h1. For boot from FLASH, initial value is 2'h2. For boot from EEPROM, initial value is 2'h3.	-

CPU_CTL (offset: 0x0204, default: 0x6801)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:20	R/W	DEFAULT_IVB	Bit [23:20] of default program counter value after reset. For boot from RAM, initial value is 4'h6. For boot from ROM, initial value is 4'h0. For boot from FLASH/EEPROM, initial value is 4'h5.	-
19:16	-	-	Reserved	-
15:12	R/W	EDLM_SIZE	Data local memory size. 0: 4KB 1: 8KB 2: 16KB 3: 32KB 4: 64KB 5: 128KB 6: 256KB 7: 512KB 8: 1MB 9: 1KB 10: 2KB 11-15: reserved	4'h6
11:8	R/W	EILM_SIZE	Instruction local memory size.	4'h8
7:1	-	-	Reserved	-
0	R/W	ILM_BOOT	0: Boot from front-side-bus 1: Boot from ILM For boot from ROM, initial value is 1. For boot from RAM/FLASH/EEPROM, initial value is 0.	-

CLOCK_CTL (offset: 0x0208, default: 0x0F0000)

Bits	Type	Name	Description	Initial value
31:20	-	-	Reserved	-
19	R/W		Reserve	1'b1
18	R/W		Reserve	1'b1
17	R/W		Reserve	1'b1
16	R/W		Reserve	1'b1
15	-	-	Reserved	-
14	R/W	TEST_MODE_SEL_XTAL	0: In RBIST test mode, select PLL as bus clock. 1: In RBIST test mode, select XTAL as bus clock. This bit has no function in normal mode.	1'b0
13	R/W	CK_GATE_CPU	CPU clock gating	1'b0
12	R/W	BUS_CLK_SEL	0: Select sys_clk as bus clock 1: Select pll_clk as bus clock	1'b0
11	-	-	Reserved	-
10:8	R/W	CK_MASK	Mask CPU/FCE/bus clock cycles for clock division. 0: no mask, no clock division n: mask n cycles in 8 clock cycles, n=1~7.	4'h0
7	R/W		Reserve	1'b0
6	R/W	CK_GATE_DSCOPE	Data scope clock gating	1'b0
5	R/W	CK_GATE_U2M	USB-to-MCU PDMA clock gating	1'b0
4	R/W	CK_GATE_FCE	FCE clock gating	1'b0
3	R/W	CK_GATE_FLH	Flash controller clock gating	1'b0
2	R/W	CK_GATE_UARTLITE	UART-Lite clock gating	1'b0
1	R/W	CK_GATE_TIMER	Timer clock gating	1'b0
0	R/W	~~CK_GATE_GDMA~~	~~GMDA clock gating~~ Reserved	1'b0

RESET_CTL (offset: 0x020C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	-
9	WO	CPU_RESET_PULSE	Write 1 to trigger CPU reset pulse. Auto-cleared.	1'b0
8	R/W	CPU_ENABLE	CPU enable For boot from RAM, initial value is 0. For boot from ROM/FLASH/EEPROM, initial value is 1.	-
7	-	-	Reserved	-
6	R/W	SW_RESET_DSCOPE	Data scope software reset	1'b0
5	R/W	SW_RESET_U2M	USB-to-MCU PDMA software reset	1'b0
4	R/W	SW_RESET_FCE	FCE software reset	1'b0
3	R/W	SW_RESET_FLH	Flash controller software reset	1'b0
2	R/W	SW_RESET_UARTLITE	UART-Lite software reset	1'b0
1	R/W	SW_RESET_TIMER	Timer software reset	1'b0
0	R/W	~~SW_RESET_GDMA~~	~~GMDA software reset~~ Reserved	1'b0

INT_STS (offset: 0x0210, default: 0x0)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	-
17	RO	INT_STS_RBUS	RBUS interrupt status	1'b0
16	RO	INT_STS_LEVEL	Level-trigger interrupt status	1'b0
15	RO	INT_STS_GPIO	GPIO interrupt status	1'b0
14	RO	INT_STS_UARTLITE	UART-Lite interrupt status	1'b0
13	RO	INT_STS_TIMER1	Timer 1 interrupt status	1'b0
12	RO	INT_STS_TIMER0	Timer 0 interrupt status	1'b0
11	RO	~~INT_STS_DMA_CH3~~	~~GMDA channel 3 interrupt status~~ Reserved	1'b0
10	RO	~~INT_STS_DMA_CH2~~	~~GMDA channel 2 interrupt status~~ Reserved	1'b0
9	RO	~~INT_STS_DMA_CH1~~	~~GMDA channel 1 interrupt status~~ Reserved	1'b0
8	RO	~~INT_STS_DMA_CH0~~	~~GMDA channel 0 interrupt status~~ Reserved	1'b0
7	-	-	Reserved	-
~~6~~	~~RO~~	~~INT_STS_BT_PDMA~~	~~BT PDMA interrupt status~~ Reserved	1'b0
~~5~~	~~RO~~	~~INT_STS_U2M~~	~~USB to MCU interrupt status~~ Reserved	1'b0
~~4~~	~~RO~~	~~INT_STS_BT_PBF~~	~~BT PBF interrupt status~~ Reserved	1'b0
~~3~~	~~RO~~	~~INT_STS_BT_LC~~	~~BT LC interrupt status~~ Reserved	1'b0
~~2~~	~~RO~~	~~INT_STS_USB~~	~~USB interrupt status~~ Reserved	1'b0
~~1~~	~~RO~~	~~INT_STS_FCE~~	~~FCE interrupt status~~ Reserved	1'b0
~~0~~	~~RO~~	~~INT_STS_PBF~~	~~PBF interrupt status~~ Reserved	1'b0

INT_ENA (offset: 0x0214, default: 0x0)

Bits	Type	Name	Description	Initial value
31:18	-	-	Reserved	-
17	R/W	INT_ENA_RBUS	RBUS interrupt enable	1'b0
16	R/W	INT_ENA_LEVEL	Level-trigger interrupt enable	1'b0
15	R/W	INT_ENA_GPIO	GPIO interrupt enable	1'b0
14	R/W	INT_ENA_UARTLITE	UART-Lite interrupt enable	1'b0
13	R/W	INT_ENA_TIMER1	Timer 1 interrupt enable	1'b0
12	R/W	INT_ENA_TIMER0	Timer 0 interrupt enable	1'b0
11	R/W	~~INT_ENA_DMA_CH3~~	~~GMDA channel 3 interrupt enable~~ Reserved	1'b0
10	R/W	~~INT_ENA_DMA_CH2~~	~~GMDA channel 2 interrupt enable~~ Reserved	1'b0
9	R/W	~~INT_ENA_DMA_CH1~~	~~GMDA channel 1 interrupt enable~~ Reserved	1'b0
8	R/W	~~INT_ENA_DMA_CH0~~	~~GMDA channel 0 interrupt enable~~ Reserved	1'b0
7	-	-	Reserved	
~~6~~	~~R/W~~	~~INT_ENA_BT_PDMA~~	~~BT PDMA interrupt enable~~ Reserved	1'b0
~~5~~	~~R/W~~	~~INT_ENA_U2M~~	~~USB to MCU interrupt enable~~ Reserved	1'b0
~~4~~	~~R/W~~	~~INT_ENA_BT_PBF~~	~~BT PBF interrupt enable~~ Reserved	1'b0
~~3~~	~~R/W~~	~~INT_ENA_BT_LC~~	~~BT LC interrupt enable~~ Reserved	1'b0
~~2~~	~~R/W~~	~~INT_ENA_USB~~	~~USB interrupt enable~~ Reserved	1'b0
~~1~~	~~R/W~~	~~INT_ENA_FCE~~	~~FCE interrupt enable~~ Reserved	1'b0
~~0~~	~~R/W~~	~~INT_ENA_PBF~~	~~PBF interrupt enable~~ Reserved	1'b0

INT_LEVEL (offset: 0x0218, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	R/W	INT_LEVEL	Write 1 to trigger interrupt. Write 0 to clear.	8'b0

INT_RBUS (offset: 0x021C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	-
5	R/W	INT_RBUS5	RBUS master #5 zero length interrupt status. Write 1 to clear.	1'b0
4	R/W	INT_RBUS4	RBUS master #4 zero length interrupt status. Write 1 to clear.	1'b0
3	R/W	INT_RBUS3	RBUS master #3 zero length interrupt status. Write 1 to clear.	1'b0
2	R/W	INT_RBUS2	RBUS master #2 (FCE-PDMA) zero length interrupt status. Write 1 to clear.	1'b0
1	R/W	INT_RBUS1	RBUS master #1 (PCIE) zero length interrupt status. Write 1 to clear.	1'b0
0	R/W	INT_RBUS0	RBUS master #0 (TEST-IF) zero length interrupt status. Write 1 to clear.	1'b0

PERI_CTL (offset: 0x0220, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:20	R/W	SPI_BADDR	Bit [23:20] of SPI base address	4'b0
19:12	-	-	Reserved	
11:8	R/W	MCU_DBG_SEL	Select MCU debug port	4'b0
7:5	-	-	Reserved	-
4	R/W	MUX_SEL_UART	Select UART-Lite/GPIO mux 0: GPIO[13:12] I/O pins function as GPIO 1: GPIO[12] I/O pin function as UART-Lite RXD GPIO[13] I/O pin function as UART-Lite TXD	1'b0
3	RO	FLASH_ACCESS	FLASH controller in operation, select I/O pins. 0: SPI I/O pins used by EE_CSR 1: SPI I/O pins used by FLASH controller	1'b0
2	R/W	SPI_SCK_INV	SPI FLASH clock inverse mode 0: data transition at spi_sck falling edge 1: data transition at spi_sck rising edge	1'b0
1	R/W	SPI_SCK_HSPD	SPI FLASH high speed mode 0: spi_sck = clk_bus / 4 1: spi_sck = clk_bus / 2	1'b1
0	R/W	SPI_ADDR_16B	SPI FLASH 16-bit address mode 0: SPI 24-bit address (FLASH) 1: SPI 16-bit address (EEPROM) For boot from RAM/ROM/FLASH, initial value is 0. For boot from EEPROM, initial value is 1.	-

SPI_READOUT (offset: 0x0224, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	RO	SPI_READOUT	SPI command mode read data	32'b0

COM_REG0 (offset: 0x0230, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	R/W	COM_REG0	Common register	32'b0

COM_REG1 (offset: 0x0234, default: 0x0)

Bits	Type	Name	Description	Initial

				value
31:0	R/W	COM_REG1	Common register	32'b0

COM_REG2 (offset: 0x0238, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	R/W	COM_REG2	Common register	32'b0

COM_REG3 (offset: 0x023c, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	R/W	COM_REG3	Common register	32'b0

PCIE_REMAP_BASE1 (offset: 0x0240, default: 0x4000000)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	
23:16	R/W	PCIE_RMP_BASE1	PCIE remap base address 1 bit [23:16]	8'h40
15:0	-	-	Reserved	

PCIE_REMAP_BASE2 (offset: 0x0244, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	
23:17	R/W	PCIE_RMP_BASE2	PCIE remap base address 2 bit [23:17]	7'h0
16:0	-	-	Reserved	

PCIE_REMAP_BASE3 (offset: 0x0248, default: 0x500000)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	
23:18	R/W	PCIE_RMP_BASE3	PCIE remap base address 3 bit [23:18]	6'h14
17:0	-	-	Reserved	

PCIE_REMAP_BASE4 (offset: 0x024c, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	
23:19	R/W	PCIE_RMP_BASE4	PCIE remap base address 4 bit [23:19]	5'h0
18:0	-	-	Reserved	

GPI_INT_MODE (offset: 0x0258, default: 0x0)

Bits	Type	Name	Description	Initial value
31:30	R/W	GPI15_INT_MODE	USB suspend interrupt mode. 0: no trigger 1: falling edge trigger	2'b0

			2: rising edge trigger 3: both falling and rising edge trigger	
29:28	R/W	GPI14_INT_MODE	AUX timer 1 done interrupt mode.	2'b0
27:26	R/W	GPI13_INT_MODE	AUX timer 0 done interrupt mode.	2'b0
25:24	R/W	GPI12_INT_MODE	PMU to CPU wakeup_ok interrupt mode.	2'b0
23:22	R/W	GPI11_INT_MODE	AUX ms timer done interrupt mode.	2'b0
21:20	R/W	GPI10_INT_MODE	GPI10 interrupt mode.	2'b0
19:18	R/W	GPI09_INT_MODE	GPI09 interrupt mode.	2'b0
17:16	R/W	GPI08_INT_MODE	GPI08 interrupt mode.	2'b0
15:14	R/W	GPI07_INT_MODE	GPI07 interrupt mode.	2'b0
13:12	R/W	GPI06_INT_MODE	GPI06 interrupt mode.	2'b0
11:10	R/W	GPI05_INT_MODE	GPI05 interrupt mode.	2'b0
9:8	R/W	GPI04_INT_MODE	GPI04 interrupt mode.	2'b0
7:6	R/W	GPI03_INT_MODE	GPI03 interrupt mode.	2'b0
5:4	R/W	GPI02_INT_MODE	GPI02 interrupt mode.	2'b0
3:2	R/W	GPI01_INT_MODE	GPI01 interrupt mode.	2'b0
1:0	R/W	GPI00_INT_MODE	GPI00 interrupt mode.	2'b0

GPI_INT_STS (offset: 0x025C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	-
15:0	R/W1C	GPI_INT_STS	GPI interrupt status. Write 1 to clear.	16'b0

GPI_DEBOUNCE_0 (offset: 0x260, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	R/W	GPI3_DBC_PRD	GPIO3 input de-bouncing period.	8'b0
23:16	R/W	GPI2_DBC_PRD	GPIO2 input de-bouncing period.	8'b0
15:8	R/W	GPI1_DBC_PRD	GPIO1 input de-bouncing period.	8'b0
7:0	R/W	GPI0_DBC_PRD	GPIO0 input de-bouncing period. 0 means no de-bouncing, keep original input signal. N means input bouncing less then (N+1)x2 us will be filtered.	8'b0

GPI_DEBOUNCE_1 (offset: 0x264, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	R/W	GPI7_DBC_PRD	GPIO7 input de-bouncing period.	8'b0
23:16	R/W	GPI6_DBC_PRD	GPIO6 input de-bouncing period.	8'b0
15:8	R/W	GPI5_DBC_PRD	GPIO5 input de-bouncing period.	8'b0
7:0	R/W	GPI4_DBC_PRD	GPIO4 input de-bouncing period.	8'b0

GPI_DEBOUNCE_2 (offset: 0x268, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:16	R/W	GPI10_DBC_PRD	GPIO10 input de-bouncing period.	8'b0
15:8	R/W	GPI9_DBC_PRD	GPIO9 input de-bouncing period.	8'b0
7:0	R/W	GPI8_DBC_PRD	GPIO8 input de-bouncing period.	8'b0

CPU_STANDBY (offset: 0x26C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	-
4	RO	STANDBY_STS	CPU standby status. 0: normal mode 1: standby mode	1'b0
3:1	-	-	Reserved	-
0	WSC	STANDBY_REQ	Write 1 to request CPU enter standby mode. It's the same behavior as instruction "STANDBY with subtype wake_grant", wait for wakeup_ok and interrupt to resume. Auto-cleared.	1'b0

LED_CTRL (offset: 0x0270, default: 0x0)

Bits	Type	Name	Description	Initial value
31	WSC	LED3_KICK	A pulse to enable the LED3 control setting	1'b0
30:27	-	-	Reserved	-
26	R/W	LED3_ TX_BLINK_MODE	LED3 MAC TX blinking enable	1'b0
25	R/W	LED3_POL	LED3 polarity 0: active high 1:active low	1'b0
24	R/W	LED3_RPY_MODE	LED3 Replay mode indication (Only available when S1 exists)	1'b0
23	WSC	LED2_KICK	A pulse to enable the LED2 control setting	1'b0
22:19	-	-	Reserved	-
18	R/W	LED2_ TX_BLINK_MODE	LED2 MAC TX blinking enable	1'b0
17	R/W	LED2_POL	LED2 polarity 0: active high 1:active low	1'b0
16	R/W	LED2_RPY_MODE	LED2 Replay mode indication (Only available when S1 exists)	1'b0
15	WSC	LED1_KICK	A pulse to enable the LED1 control setting	1'b0
14:11	-	-	Reserved	-
10	R/W	LED1_ TX_BLINK_MODE	LED1 MAC TX blinking enable	1'b0
9	R/W	LED1_POL	LED1 polarity 0: active high 1:active low	1'b0
8	R/W	LED1_RPY_MODE	LED1 Replay mode indication (Only available when S1 exists)	1'b0
7	WSC	LED0_KICK	A pulse to enable the LED0 control setting	1'b0
6:3	-	-	Reserved	-
2	R/W	LED0_ TX_BLINK_MODE	LED0 MAC TX blinking enable	1'b0
1	R/W	LED0_POL	LED0 polarity 0: active high 1:active low	1'b0
0	R/W	LED0_RPY_MODE	LED0 Replay mode indication (Only available when S1 exists)	1'b0

LED_TX_BLINK_0 (offset: 0x0274, default: 0x03070307)

Bits	Type	Name	Description	Initial value
31:24	R/W	LED1_TX_ OFF_TIME	LED1 TX blinking on period (unit:10ms)	8'h3
23:16	R/W	LED1_TX_ ON_TIME	LED1 TX blinking off period (unit:10ms)	8'h7
15:8	R/W	LED0_TX_ OFF_TIME	LED0 TX blinking on period (unit:10ms)	8'h3
7:0	R/W	LED0_TX_ ON_TIME	LED0 TX blinking off period (unit:10ms)	8'h7

LED_TX_BLINK_1 (offset: 0x0278, default: 0x03070307)

Bits	Type	Name	Description	Initial value

31:24	R/W	LED3_TX_ OFF_TIME	LED3 TX blinking on period (unit:10ms)	8'h3
23:16	R/W	LED3_TX_ ON_TIME	LED3 TX blinking off period (unit:10ms)	8'h7
15:8	R/W	LED2_TX_ OFF_TIME	LED2 TX blinking on period (unit:10ms)	8'h3
7:0	R/W	LED2_TX_ ON_TIME	LED2 TX blinking off period (unit:10ms)	8'h7

LED0_S0 (offset: 0x027C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	R/W	LED0_ S0_OFF_TIME	LED0 state0 led off period (unit:10ms)	8'h0
23:16	R/W	LED0_ S0_ON_TIME	LED0 state0 led on period (unit:10ms)	8'h0
15:8	R/W	LED0_S0_ LASTING_TIME	LED0 state0 lasting period (unit:10ms)	16'h0

LED0_S1 (offset: 0x0280, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	R/W	LED0_ S1_OFF_TIME	LED0 state1 led off period (unit:10ms)	8'h0
23:16	R/W	LED0_ S1_ON_TIME	LED0 state1 led on period (unit:10ms)	8'h0
15:8	R/W	LED0_S1_ LASTING_TIME	LED0 state1 lasting period (unit:10ms)	16'h0

LED1_S0 (offset: 0x0284, default: 0x0)

LED1_S1 (offset: 0x0288, default: 0x0)

LED2_S0 (offset: 0x028C, default: 0x0)

LED2_S1 (offset: 0x0290, default: 0x0)

LED3_S0 (offset: 0x0294, default: 0x0)

LED3_S1 (offset: 0x0298, default: 0x0)

SEMAPHORE_00 (offset: 0x2B0, default: 0x1)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	-
0	W1S/RC	SMPH_00	The semaphore bit is used to protect common usage registers, to prevent from 2 driver/firmware write the same register and cause racing problem. Read return data 1 means got the permission. Write 1 to set, read to clear. Working scenario: (ex. to protect ant_sel register) Semaphore bit default value is 1. Before setting ant_sel, WIFI driver has to read semaphore bit and got 1, means it get the permission. After read operation, the semaphore bit is auto cleared to 0.	1'b1

SEMAPHORE_01 (offset: 0x2B4, default: 0x1)

SEMAPHORE_02 (offset: 0x2B8, default: 0x1)

SEMAPHORE_03 (offset: 0x2BC, default: 0x1)

SEMAPHORE_04 (offset: 0x2C0, default: 0x1)

SEMAPHORE_05 (offset: 0x2C4, default: 0x1)

SEMAPHORE_06 (offset: 0x2C8, default: 0x1)

SEMAPHORE_07 (offset: 0x2CC, default: 0x1)

SEMAPHORE_08 (offset: 0x2D0, default: 0x1)

SEMAPHORE_09 (offset: 0x2D4, default: 0x1)

SEMAPHORE_10 (offset: 0x2D8, default: 0x1)

SEMAPHORE_11 (offset: 0x2DC, default: 0x1)

SEMAPHORE_12 (offset: 0x2E0, default: 0x1)

SEMAPHORE_13 (offset: 0x2E4, default: 0x1)

SEMAPHORE_14 (offset: 0x2E8, default: 0x1)

SEMAPHORE_15 (offset: 0x2EC, default: 0x1)

5.4.2 ROM patch registers

PATCH_ADDR_0 (offset: 0xE000, default: 0x0)

Bits	Type	Name	Description	Initial value
31:19	-	-	Reserved	-
18:0	R/W	PATCH_ADDR_0	Patch address for entry 0	19'h0

PATCH_DEST_0 (offset: 0xE004, default: 0x0)

Bits	Type	Name	Description	Initial value
31:22	-	-	Reserved	-
21:0	R/W	DEST_ADDR_0	Destination address for entry 0	2'h0

PATCH_ADDR_1 (offset: 0xE008, default: 0x0)

PATCH_DEST_1 (offset: 0xE00C, default: 0x0)

(Total 64 patch entries)

PATCH_ADDR_63 (offset: 0xE1F8, default: 0x0)

PATCH_DEST_63 (offset: 0xE1FC, default: 0x0)

PATCH_ENABLE_0 (offset: 0xE200, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	R/W	PATCH_ENABLE_0	Patch enable for entry 31-0.	32'h0

PATCH_ENABLE_1 (offset: 0xE204, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	R/W	PATCH_ENABLE_1	Patch enable for entry 63-32.	32'h0

5.4.3 Timer registers

TMRSTAT (offset: 0x0400, default: 0x0)

Bits	Type	Name	Description	Initial value
31:6	-	-	Reserved	26'b0
5	WSC	TMR1RST	Timer 1 Reset Writing a '1' to this bit will reset the Timer 1 to 0xFFFF if in free-running mode, or the value specified in the TMR1LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
4	WSC	TMR0RST	Timer 0 Reset Writing a '1' to this bit will reset Timer 0 to 0xFFFF if in free-running mode, or the value specified in the TMR0LOAD register in all other modes. Writing a '0' to this bit has no effect. Reading this bit will return a '0'.	1'b0
3:2	-	-	Reserved	2'b0
1	R/W1C	TMR1INT	Timer 1 Interrupt Status This bit is set if Timer 1 has expired. The Timer 1 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0
0	R/W1C	TMR0INT	Timer 0 Interrupt Status This bit is set if Timer 0 has expired. The Timer 0 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.	1'b0

TMR0LOAD (offset: 0x0410, default: 0x0)

Bits	Type	Name	Description	Initial value
31:16	R-	-	Reserved	16'b0
15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	16'b0

TMR0VAL (offset: 0x0414, default: 0xFFFF)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

TMR0CTL (offset: 0x0418, default: 0x0)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0
14:8	-	-	Reserved	15'b0
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0
6	-	-	Reserved	1'b0
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running: counts from FFFF to 0000 and then reloads FFFF and continues counting. 1: Periodic: counts from LOAD to 0000 and then reloads LOAD and continues counting. 2: Time-out: counts from LOAD to 0000 and then reloads LOAD but resets the enable bit. 3: Time-out	1'b0
3:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. Value / Timer Clock Frequency 0 / System clock 1 / System clock / 4 2 / System clock / 8 3 / System clock / 16 . / . . / . 14 / System clock / 32768 15 / System clock /65536 **Note:** The pre-scale value should not be changed unless the timer is disabled.	4'b0

TMR1LOAD (offset: 0x0420, default: 0x0)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	TMRLOAD[15:0]	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.	16'b0

TMR1VAL (offset: 0x0424, default: 0xFFFF)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	RO	TMRVAL[15:0]	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	16'hffff

TMR1CTL (offset: 0x0428, default: 0x0)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15	R/W	TESTEN	Reserved for Test This bit should be written with a zero	1'b0
14:8	-	-	Reserved	7'b0
7	R/W	ENABLE	Timer Enable 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	1'b0
6	-	-	Reserved	1'b0
5:4	R/W	MODE[1:0]	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Watchdog	1'b0
3:0	R/W	PRESCALE[3:0]	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. Value / Timer Clock Frequency 0 / System clock 1 / System clock / 4 2 / System clock / 8 3 / System clock / 16 . / . . / . 14 / System clock / 32768 15 / System clock / 65536 Note: The pre-scale value should not be changed unless the timer is disabled.	4'b0

5.4.4 UART-Lite registers

RBR (offset: 0x0500, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	RBR[7:0]	Receive Buffer Data Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received.	8'b0

TBR (offset: 0x0504, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	RO	THR[7:0]	Transmit Buffer Data Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	8'b0

IER (offset: 0x0508, default: 0x0)

Bits	Type	Name	Description	Initial value
31:3	-	-	Reserved	29'b0
2	R/W	ELSI	Enable Receiver Line Status Interrupt 1: Enable line status (OE, PE, FE, and BI) interrupts. 0: Disable line status (OE, PE, FE, and BI) interrupts.	1'b0
1	R/W	ETBEI	Enable Transmitter Buffer Line Status Interrupt 1: Enable transmit buffer empty (THRE) interrupt. 0: Disable transmit buffer empty (THRE) interrupt.	1'b0
0	R/W	ERBFI	Enable Receiver Buffer FullInterrupt 1: Enable data ready (DR) or character time-out interrupt. 0: Disable data ready (DR) or character time-out interrupt.	1'b0

IIR (offset: 0x050C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:6	RO	FIFOES [1:0]	FIFOs Enabled Status FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.	1'b0
5:4	-	-	Reserved	2'b0
3:1	RO	INTID[2:0]	Interrupt Identifier Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below.	3'b0

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>ID</th><th>Priority</th><th>Type</th><th>Source</th></tr>
<tr><td>7</td><td></td><td>Undefined</td><td></td></tr>
<tr><td>6</td><td></td><td>Receiver Timed Out</td><td></td></tr>
<tr><td>5</td><td></td><td>Undefined</td><td></td></tr>
<tr><td>4</td><td></td><td>Undefined</td><td></td></tr>
<tr><td>3</td><td>1</td><td>Receiver Line Status</td><td>OE,PE,F E,BI</td></tr>
<tr><td>2</td><td>2</td><td>Receiver Buffer Full</td><td>DR(FIFOENA=0)</td></tr>
<tr><td>1</td><td>3</td><td>Transmit buffer Empty</td><td>THRE</td></tr>
<tr><td>0</td><td>4</td><td>Modem Status</td><td>DCTD,DD SR, RI, DCD</td></tr>
</table>
If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register.
See also “Interrupt Priorities”.
</td><td></td></tr>
<tr><td>0</td><td>RO</td><td>INTPEND</td><td>Interrupt Pending
0: An interrupt bit is set and is not masked.
1: No interrupts are pending.</td><td>1’b1</td></tr>
</table>

FCR (offset: 0x0510, default: 0x0)

<table>
<tr><th>Bits</th><th>Type</th><th>Name</th><th>Description</th><th>Initial value</th></tr>
<tr><td>31:8</td><td>-</td><td>-</td><td>Reserved</td><td>24’b0</td></tr>
<tr><td>7:6</td><td>R/W</td><td>RXTRIG [1:0]</td><td>Receiver Trigger Level
The data ready interrupt (DR) will be asserted when the receiver buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:
<table>
<tr><th>RXTRIG</th><th>Trigger Level</th></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>8</td></tr>
<tr><td>3</td><td>14</td></tr>
</table>
Note: This register is not used if the receive FIFO is disabled.</td><td>2’b0</td></tr>
<tr><td>5:4</td><td>R/W</td><td>TXTRIG[1:0]</td><td>Transmitter Trigger Level
The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:
<table>
<tr><th>TXTRIG</th><th>Trigger Level</th></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>8</td></tr>
<tr><td>3</td><td>12</td></tr>
</table></td><td>2’b0</td></tr>
<tr><td>3</td><td>R/W</td><td>DMAMODE</td><td>Enable DMA transfers</td><td>1’b0</td></tr>
</table>

			This bit is writeable and readable, but has no other hardware function.	
2	WO	TXRST	Transmitter FIFO Reset Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.	1'b0
1	WO	RXRST	Receive FIFO Reset Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.	1'b0
0	R/W	FIFOENA	0: The Transmit and Receive FIFOs have the effective depth of one character. 1: The Transmit and Receive FIFOs are enabled. Note: The FIFO status and data are automatically cleared when this bit is changed.	1'b0

LCR (offset: 0x0514, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	R/W	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	2'b0
6	R/W	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to '0'. Transmitter otherwise operates normally.	2'b0
5	R/W	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity if forced to '1'.	1'b0
4	R/W	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is '1'). 1: Even parity selected (checksum, including parity is '0'). Note: This bit is ignored if the PEN bit is '0'.	1'b0
3	R/W	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	1'b0
2	R/W	STB	Stop Bit Select 0: 1 stop bit is transmitted and received. 1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.	1'b0
1:0:	R/W	WLS[1:0]	Word Length Select 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	2'b0

MCR (offset: 0x0518, default: 0x0)

Bits	Type	Name	Description	Initial value
31:5	-	-	Reserved	24'b0
4	R/W	LOOP	Loop-back Mode Enable 0: Normal Operation.	1'b0

			1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal are connected to RXD internally.	
3:0	RO	Reserved	Reserved	7'b0

LSR (offset: 0x051C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7	RO	ERINFIFO	The FIFO contains data which had a parity or framing error This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.	2'b0
6	RO	TEMT	Transmitter Empty This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the **TBR** register.	1'b1
5	RO	THRE	Transmitter Holding Register Empty This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the **TBR** register.	1'b1
4	RO	BI	Break Interrupt This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received.	1'b1
3	RO	FE	Framing Error This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.	1'b1
2	RO	PE	Parity Error This bit is set if the received parity is different from the expected value.	1'b0
1	RO	OE	Overrun Error This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.	1'b0
0	RO	DR	Data Ready This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.	1'b0

DL (offset: 0x0528, default: 0x0001)

Bits	Type	Name	Description	Initial value
31:16	-	-	Reserved	16'b0
15:0	R/W	DL[15:0]	Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: baud rate = system clock frequency / (DL * 16). Note: In standard 16550 implementation, this register is	16'h0001

			accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.	

DLLO (offset: 0x052C, default: 0x01)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLLO[7:0]	This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	8'b1

DLHI (offset: 0x0530, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	24'b0
7:0	R/W	DLHI[7:0]	This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	8'b0

IFCTL (offset: 0x0534, default: 0x0)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	31'b0
0	R/W	IFCTL	Open Collector Mode Control. This register controls if the UART Lite TXD output functions in open collector mode or is always driven. When set to '0', the output is always driven with the value of the transmit data signal. When set to a '1', the TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high.	1'b0

5.4.5 Data Scope registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Andes firmware/TESTIF	0x0041_0000

DSCOPE_CTL (offset: 0x0C00, default: 0x0)

Bits	Type	Name	Description	Initial value
31:17	-	-	Reserved	-
16	R/W		Reserve	1'b0
15:10	-	-	Reserved	-
9	WSC	DSC_STOP	Write 1 to stop data scope, auto-cleared pulse.	1'b0
8	WSC	DSC_START	Write 1 to start data scope, auto-cleared pulse.	1'b0
7:6	-	-	Reserved	-
5:4	R/W	DSC_MODE	Data scope mode. 0: reserved 1: capture/record mode (capture RX, record TX) 2: playback mode (playback TX) 3: loopback mode (playback TX + capture RX)	2'b0
3:0	R/W	IQ_FORMAT	IQ format [0]: DAC0/ADC0 is active [1]: DAC1/ADC1 is active [2]: 0: 8bit, 1: 10bit [3]: Reserved	4'b0

DSCOPE_STS (offset: 0x0C04, default: 0x0)

Bits	Type	Name	Description	Initial value
31:19	-	-	Reserved	-
18	RO	LBK_ENABLE	Loopback enable status	1'b0
17	RO	PBK_ENABLE	Playback enable status	1'b0
16	RO	CAP_ENABLE	Capture enable status	1'b0
15	-	-	Reserved	-
14:0	RO	CAP_START_ADDR	Start address of captured data. Unit: byte. Captured data starts at byte address 0x418000+CAP_START_ADDR. Set 0x410400[18:16]=3'h1 before access RAM0 (32KB). Set 0x410400[18:16]=3'h2 before access RAM1 (32KB). Set 0x410400[18:16]=3'h3 before access RAM2 (32KB).	15'b0

CAP_CTL (offset: 0x0C08, default: 0x400)

Bits	Type	Name	Description	Initial value
31:21	-	-	Reserved	-
20	WSC	MAN_TRIG	Write 1 to trigger data capture, auto-cleared pulse.	1'b0
19:15	-	-	Reserved	-
14:0	R/W	TRIG_OFFSET	Start address offset before trigger point. Unit: byte.	15'h400

PBK_CTL (offset: 0x0C0C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	-
23:16	R/W	PBK_LOOP_GAP	Gap between each playback loop. Unit: us.	8'b0
15:12	-	-	Reserved	-
11:0	R/W	PBK_LOOP_CNT	Playback loop count. 0 means endless loop. In loopback mode, the hardware starts capture and playback at the same time, and auto trigger in the beginning of the last playback round. In loopback mode, do not support PBK_LOOP_CNT = 0 or 1.	12'b0

PBK_END_ADDR (offset: 0x0C10, default: 0x7FFC)

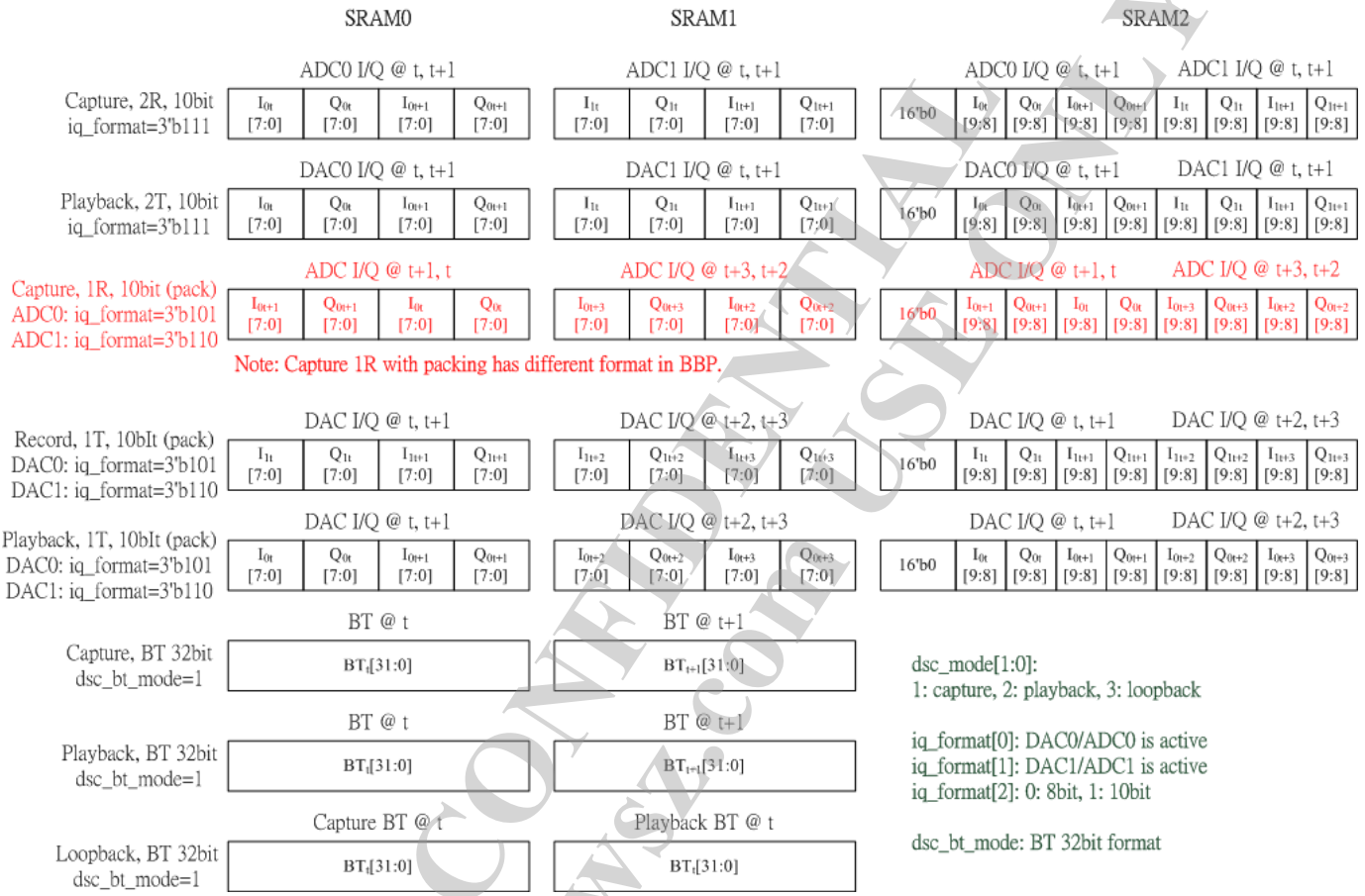
Bits	Type	Name	Description	Initial value
31:15	-	-	Reserved	-
14:0	R/W	PBK_END_ADDR	End address of playback data. Unit: byte. Playback data ends at byte address 0x418000+PBK_END_ADDR. Set 0x410400[18:16]=3'h1 before access RAM0 (32KB). Set 0x410400[18:16]=3'h2 before access RAM1 (32KB). Set 0x410400[18:16]=3'h3 before access RAM2 (32KB).	15'h7FFC

CAP_HEAD_ADDR (offset: 0x0C14, default: 0x0)

Bits	Type	Name	Description	Initial value
31:15	-	-	Reserved	-
14:0	R/W	CAP_HEAD_ADDR	Head address of capture. Unit: byte.	15'h0

CAP_END_ADDR (offset: 0x0C18, default: 0x7FFC)

Bits	Type	Name	Description	Initial value
31	R/W	CAP_END_EN	0: Capture stops when RAM full. 1: Capture stops when RAM address = CAP_END_ADDR.	1'b0
30:15	-	-	Reserved	-
14:0	R/W	CAP_END_ADDR	End address of capture. Unit: byte.	15'h7FFC



5.4.6 U3DMA registers

U3_FLOW_CTRL (offset: 0x9010, default: 0x03FC_03FC)

Bits	Type	Name	Description	Init Value
31:28	RO	-	Reserved	4'h0
27:18	R/W	OUT_IDLE_TIMER_LMT	Valid when FORCE _OUT_FLOW_CTL is set to 0. There is a timer used to calculate the FSM idle lasting time. When this timer meets OUT_IDLE_TIMER_LMT, the rx_active signal would de-assert. Unit: 1us	10'h0
17	R/W	OUT_FLOW_CTL_REG	0 : force to set rx_active = 0 1 : force to set rx_active = 1	1'h0
16	R/W	FORCE _OUT_FLOW_CTL	Set 1 to put OUT flow control to register force mode. When this it set, rx_active signal is controlled by OUT_FLOW_CTL_REG.	1'h0
15:12	RO	-	Reserved	4'h0
11:2	R/W	IN_IDLE_TIMER_LMT	Valid when FORCE _IN_FLOW_CTL is set to 0. There is a timer used to calculate the FSM idle lasting time. When this timer meets IN_IDLE_TIMER_LMT, the tx_active signal would de-assert. Unit: 1us	10'h0
1	R/W	IN_FLOW_CTL_REG	0 : force to set tx_active = 0 1 : force to set tx_active = 1	1'h0
0	R/W	FORCE _IN_FLOW_CTL	Set 1 to put IN flow control to register force mode. When this it set, tx_active signal is controlled by IN_FLOW_CTL_REG.	1'h0

U3DMA_RESET (offset: 0x9014, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	26'h0
7	R/W	UDMA_RESET	Write 1 then write 0 to reset U3DMA	1'h0
6	R/W	WL_TX_RESET	Write 1 then write 0 to reset WL TX module	1'h0
5	R/W	WL_RX_RESET	Write 1 then write 0 to reset WL RX module	1'h0
4	R/W	EP3OUT_RESET	Write 1 then write 0 to reset EP3OUT module	1'h0
3	R/W	EP3IN_RESET	Write 1 then write 0 to reset EP3IN module	1'h0
2	R/W	EP2OUT_RESET	Write 1 then write 0 to reset EP2OUT module	1'b0
1	R/W	EP2IN_RESET	Write 1 then write 0 to reset EP2IN module	1'h0
0	R/W	EP1IN_RESET	Write 1 then write 0 to reset EP1IN module	1'h0

U3DMA_WLCFG (offset: 0x9018, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	RO	WL_TX_BUSY	0 : Idle 1 : busy	1'h0
30	RO	WL_RX_BUSY	0 : Idle 1 : busy	1'h0
29:24	RO	-	Reserved	6'h0
23	R/W	WL_TX_EN	WLAN UDMA TX Enable	1'h0
22	R/W	WL_RX_EN	WLAN UDMA RX Enable	1'b0
21	R/W	WL_RX_AGG_EN	WLAN UDMA RX Aggregation Function Enable	1'h0
20	R/W	WL_LPK_EN	WLAN U3DMA loopback mode enable	1'h0
19	R/W	WL_TX_CLEAR	WLAN UDMA UDMA TX Clear	1'h0
18	R/W	WL_RX_MPSZ_PAD0	Padding 1DW if the length of IN data is with maxima packet size	1'h0
15:8	R/W	WL_RX_AGG_LMT	WLAN UDMA RX Aggregation Limit	8'h0
7:0	R/W	WL_RX_AGG_TO	WLAN UDMA RX Aggregation Time-Out Value Unit:1us	8'h0

Reserve (offset: 0x901C, default: 0x0000_0000)

Reserve (offset: 0x9020, default: 0x0000_0000)

Reserve (offset: 0x9024, default: 0x0000_0000)

M_EP1IN_PORT(offset: 0x9030, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	24'h0
7:0	WO	M_EP1IN_PORT	MCU EP1IN PORT	8'h0

EP1IN_CTRL(offset: 0x9034, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5	RO	-	Reserved	27'h0
4	RO	EP1IN_BUSY	0 : Idle 1 : busy	1'h0
3	RO	EP1IN_NOT_FULL	0 : full 1 : not_full	1'h0
2	WO	EP1IN_PKTEND_ZLP	MCU writes 1 when one packet ends with zero length packets, auto-clear	1'b0
1	WO	EP1IN_PKTEND	MCU writes 1 when one packet ends, auto-clear	1'h0
0	RO	-	Reserved	1'h0

M_EP2IN_PORT(offset: 0x9040, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	24'h0
7:0	WO	M_EP2IN_PORT	MCU EP2IN PORT	8'h0

EP2IN_CTRL(offset: 0x9044, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5	RO	-	Reserved	27'h0
4	RO	EP2IN_BUSY	0 : Idle 1 : busy	1'h0
3	RO	EP2IN_NOT_FULL	0 : full 1 : not_full	1'h0
2	WO	EP2IN_PKTEND_ZLP	MCU writes 1 when one packet ends with zero length packets, auto-clear	1'b0
1	WO	EP2IN_PKTEND	MCU writes 1 when one packet ends, auto-clear	1'h0
0	R/W	EP2IN_MCU_MODE	0 : DMA mode 1 : MCU mode	1'h0

M_EP2OUT_PORT(offset: 0x9050, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	24'h0
7:0	RO	M_EP2OUT_PORT	MCU EP2OUT_PORT	8'h0

EP2OUT_CTRL(offset: 0x9054, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5	RO	-	Reserved	27'h0
4	RO	EP2OUT_BUSY	0 : Idle 1 : busy	1'h0
3	RO	EP2OUT_NOT_EMPTY	0 : empty 1 : empty	1'h0
2	RO	-	Reserved	1'b0
1	WO	EP2OUT_PKTEND	MCU writes 1 when one packet ends, auto-clear	1'h0
0	R/W	EP2OUT_MCU_MODE	0 : DMA mode 1 : MCU mode	1'h0

M_EP3IN_PORT(offset: 0x9060, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	24'h0
7:0	WO	M_EP3IN_PORT	MCU EP3IN_PORT	8'h0

EP3IN_CTRL(offset: 0x9064, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5	RO	-	Reserved	27'h0
4	RO	EP3IN_BUSY	0 : Idle 1 : busy	1'h0
3	RO	EP3IN_NOT_FULL	0 : full 1 : not_full	1'h0
2	WO	EP3IN_PKTEND_ZLP	MCU writes 1 when one packet ends with zero length packets, auto-clear	1'b0
1	WO	EP3IN_PKTEND	MCU writes 1 when one packet ends, auto-clear	1'h0
0	R/W	EP3IN_MCU_MODE	0 : VFIFO mode 1 : MCU mode	1'h0

M_EP3OUT_PORT(offset: 0x9070, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:8	RO	-	Reserved	24'h0
7:0	RO	M_EP3OUT_PORT	MCU EP3OUT_PORT	8'h0

EP3OUT_CTRL(offset: 0x9074, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5	RO	-	Reserved	27'h0
4	RO	EP3OUT_BUSY	0 : Idle 1 : busy	1'h0
3	RO	EP3OUT _NOT_EMPTY	0 : empty 1 : empty	1'h0
2	RO	-	Reserved	1'b0
1	WO	EP3OUT _PKTEND	MCU writes 1 when one packet ends, auto-clear	1'h0
0	R/W	EP3OUT_MCU_MODE	0 : VFIFO mode 1 : MCU mode	1'h0

STOP_ DP_OUT (offset: 0x9080, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:26	RO	-	Reserved	6'h0
25	R/W	DROP_EP9OUT	Drop EP9OUT packets from USB FIFO	1'h0
24	R/W	DROP_EP8OUT	Drop EP8OUT packets from USB FIFO	1'h0
23	R/W	DROP_EP7OUT	Drop EP7OUT packets from USB FIFO	1'h0
22	R/W	DROP_EP6OUT	Drop EP6OUT packets from USB FIFO	1'h0
21	R/W	DROP_EP5OUT	Drop EP5OUT packets from USB FIFO	1'h0
20	R/W	DROP_EP4OUT	Drop EP4OUT packets from USB FIFO	1'h0
19	R/W	DROP_EP3OUT	Drop EP3OUT packets from USB FIFO	1'h0
18	R/W	DROP_EP2OUT	Drop EP2OUT packets from USB FIFO	1'h0
17:10	RO	-	Reserved	8'h0
9	R/W	STOP_EP9OUT	Stop EP9OUT packets from USB FIFO	1'h0
8	R/W	STOP_EP8OUT	Stop EP8OUT packets from USB FIFO	1'h0
7	R/W	STOP_EP7OUT	Stop EP7OUT packets from USB FIFO	1'h0
6	R/W	STOP_EP6OUT	Stop EP6OUT packets from USB FIFO	1'h0
5	R/W	STOP_EP5OUT	Stop EP5OUT packets from USB FIFO	1'h0
4	R/W	STOP_EP4OUT	Stop EP4OUT packets from USB FIFO	1'h0
3	R/W	STOP_EP3OUT	Stop EP3OUT packets from USB FIFO	1'b0
2	R/W	STOP_EP2OUT	Stop EP2OUT packets from USB FIFO	1'h0
1:0	RO	-	Reserved	1'h0

STOP_DP_IN (offset: 0x9088, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:20	RO	-	Reserved	12'h0
19	R/W	EP5IN_STOP_WITH_ZLP	Send ZLP to drop current packet for EP5IN	1'h0
18	R/W	EP4IN_STOP_WITH_ZLP	Send ZLP to drop current packet for EP4IN	1'h0
19	R/W	EP3IN_STOP_WITH_ZLP	Send ZLP to drop current packet for EP3IN	1'h0
18	R/W	EP2IN_STOP_WITH_ZLP	Send ZLP to drop current packet for EP2IN	1'h0
17	R/W	EP1IN_STOP_WITH_ZLP	Send ZLP to drop current packet for EP1IN	1'h0
16:14	RO	-	Reserved	3'h0
13	R/W	DROP_EP5IN	Drop EP5IN packets to USB FIFO	1'h0
12	R/W	DROP_EP4IN	Drop EP4IN packets to USB FIFO	1'h0
11	R/W	DROP_EP3IN	Drop EP3IN packets to USB FIFO	1'h0
10	R/W	DROP_EP2IN	Drop EP2IN packets to USB FIFO	1'h0
9	R/W	DROP_EP1IN	Drop EP1IN packets to USB FIFO	1'h0
8:6	RO	-	Reserved	1'h0
5	R/W	STOP_EP5IN	Stop EP5IN packets to USB FIFO	1'h0
4	R/W	STOP_EP4IN	Stop EP4IN packets to USB FIFO	1'h0
3	R/W	STOP_EP3IN	Stop EP3IN packets to USB FIFO	1'h0
2	R/W	STOP_EP2IN	Stop EP2IN packets to USB FIFO	1'b0
1	R/W	STOP_EP1IN	Stop EP1IN packets to USB FIFO	1'h0
0	RO	-	Reserved	1'h0

WL_TX_DBG (offset: 0x9100)

WL_RX_DBG (offset: 0x9110)

Reserve (offset: 0x9120)

Reserve (offset: 0x9130)

Reserve (offset: 0x9140)

Reserve (offset: 0x9150)

Reserve (offset: 0x9160)

ARB_DBG (offset: 0x9170)

PRB_SEL (offset: 0x9200, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:24	RO	-	Reserved	8'h0
23:16	R/W	prb_idx	Probe index	8'h0
15:8	R/W	prb_sub_idx_g0	Probe sub-index group0	8'h0
7:0	R/W	prb_sub_idx_g1	Probe sub-index group1	8'h0

MISC (offset: 0x9210, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:1	RO	-	Reserved	31'h0
0	R/W	u3_suspendm	USB3 suspendm signal	1'h0

5.5 IF_DMA registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Reserve	N/A
Andes firmware/TESTIF	0x0041_0000

PDMA_INT_STA (offset: 0x0200, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	-	-	Reserved	-
27	R/W1C	TX_DLY_INT	Summary of the whole WPDMA TX related interrupts Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
26	R/W1C	RX_DLY_INT	Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
25	-	-	Reserved	-
24	R/W1C	MAC_INT_4	MAC interrupt 4: GP timer interrupt	1'h0
23	R/W1C	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	1'h0
22	R/W1C	MAC_INT_2	MAC interrupt 2: TX status interrupt	1'h0
21	R/W1C		Reserve	1'h0
20	R/W1C		Reserve	1'h0
19	R/W1C	MCU_CMD_INT	MCU command interrupt	1'h0
18	RO	ANY_COHERENT	When TX_COHERENT or RX_COHERENT is on, this bit is set	1'h0
17	R/W1C	TX_COHERENT	TX_DMA finds data coherent event when checking ddone bit Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
16	R/W1C	RX_COHERENT	RX_DMA finds data coherent event when checking ddone bit Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
15:14	-	-	Reserved	-
13	R/W1C	TX_DONE_INT9	TX Queue#9 packet transmit interrupt Write 1 to clear the interrupt	1'h0
12	R/W1C	TX_DONE_INT8	TX Queue#8 packet transmit interrupt Write 1 to clear the interrupt	1'h0
11	R/W1C	TX_DONE_INT7	TX Queue#7 packet transmit interrupt Write 1 to clear the interrupt	1'h0
10	R/W1C	TX_DONE_INT6	TX Queue#6 packet transmit interrupt Write 1 to clear the interrupt	1'h0
9	R/W1C	TX_DONE_INT5	TX Queue#5 packet transmit interrupt Write 1 to clear the interrupt	1'h0
8	R/W1C	TX_DONE_INT4	TX Queue#4 packet transmit interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
7	R/W1C	TX_DONE_INT3	TX Queue#3 packet transmit interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
6	R/W1C	TX_DONE_INT2	TX Queue#2 packet transmit interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
5	R/W1C	TX_DONE_INT1	TX Queue#1 packet transmit interrupt Write 1 to clear the interrupt	1'h0

			Read to get the raw interrupt status	
4	R/W1C	TX_DONE_INT0	TX Queue#0 packet transmit interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
3:2	-	-	Reserved	-
1	R/W1C	RX_DONE_INT1	RX Queue#1 packet receive interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0
0	R/W1C	RX_DONE_INT0	RX Queue#0 packet receive interrupt Write 1 to clear the interrupt Read to get the raw interrupt status	1'h0

PDMA_INT_MSK (offset: 0x0204, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	-	-	Reserved	-
27	R/W	TX_DLY_INT_MSK	Summary of the whole WPDMA TX related interrupts	1'h0
26	R/W	RX_ DLY_INT_MSK	Summary of the whole WPDMA RX related interrupts	1'h0
25	-	-	Reserved	-
24	R/W	MAC_INT4_EN	MAC interrupt 4: GP timer interrupt	1'h0
23	R/W	MAC_INT3_EN	MAC interrupt 3: Auto wakeup interrupt	1'h0
22	R/W	MAC_INT2_EN	MAC interrupt 2: TX status interrupt	1'h0
21	R/W	MAC_INT1_EN	MAC interrupt 1: Pre-TBTT interrupt	1'h0
20	R/W	MAC_INT0_EN	MAC interrupt 0: TBTT interrupt	1'h0
19	R/W	MCU_CMD_INT_MSK	MCU command interrupt enable	1'h0
18	R/W	ANY_COHERENT_EN	Enable for TX_DMA or RX_DMA data coherent interrupt	1'h0
17	R/W	TX_COHERENT_EN	Enable for TX_DMA data coherent interrupt	1'h0
16	R/W	RX_COHERENT_EN	Enable for RX_DMA data coherent interrupt	1'h0
15:14	-	-	Reserved	-
13	R/W	TX_DONE_INT_MSK9	TX Queue#9 packet transmit interrupt	1'h0
12	R/W	TX_DONE_INT_MSK8	TX Queue#8 packet transmit interrupt	1'h0
11	R/W	TX_DONE_INT_MSK 7	TX Queue#7 packet transmit interrupt	1'h0
10	R/W	TX_DONE_INT_MSK 6	TX Queue#6 packet transmit interrupt	1'h0
9	R/W	TX_DONE_INT_MSK5	TX Queue#5 packet transmit interrupt	1'h0
8	R/W	TX_DONE_INT_MSK4	TX Queue#4 packet transmit interrupt	1'h0
7	R/W	TX_DONE_INT_MSK 3	TX Queue#3 packet transmit interrupt	1'h0
6	R/W	TX_DONE_INT_MSK 2	TX Queue#2 packet transmit interrupt	1'h0
5	R/W	TX_DONE_INT_MSK 1	TX Queue#1 packet transmit interrupt	1'h0
4	R/W	TX_DONE_INT_MSK 0	TX Queue#0 packet transmit interrupt	1'h0
3:2	-	-	Reserved	-
1	R/W	RX_DONE_INT_MSK1	RX Queue#1 packet receive interrupt	1'h0
0	R/W	RX_DONE_INT_MSK0	RX Queue#0 packet receive interrupt	1'h0

WPDMA_GLO_CFG (offset: 0x0208, default: 0x4000_0450)

Bits	Type	Name	Description	Init Value
31	R/W	RX_2B_OFFSET		1'h0
30	R/W	CLK_GATE_DIS	PDMA Clock Gated Function Disable 0: normal function 1: disable clock gated function	1'h1
29:16			Reserved	14'h0
10	R/W	MULTI_DMA_EN	MULTI-ISSUE DMA Enable	1'h1

			0: Disable 1: Enable	
9:8	R/W		Reserved	2'h0
7	R/W	BIG_ENDIAN	The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.	1'h0
6	R/W	TX_WB_DDONE	0 :Disable TX_DMA writing back DDONE into TXD 1 : Enable TX_DMA writing back DDONE into TXD	1'h1
5:4	R/W		Reserve	2h1
3	R	RX_DMA_BUSY	1 : RX_DMA is busy 0 : RX_DMA is not busy	1'h0
2	R/W	RX_DMA_EN	1 : Enable RX_DMA 0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.)	1'h0
1	R	TX_DMA_BUSY	1 : TX_DMA is busy 0 : TX_DMA is not busy	1'h0
0	R/W	TX_DMA_EN	1 : Enable TX_DMA 0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)	1'h0

WPDMA_RST_PTR (offset: 0x020C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:18	-	-	Reserved	-
17	W1C	RST_DRX_IDX1	Write 1 to reset to RX_DMARX_IDX1 to 0	1'b0
16	W1C	RST_DRX_IDX0	Write 1 to reset to RX_DMARX_IDX0 to 0	1'b0
15:10	-	-	Reserved	-
9	W1C	RST_DTX_IDX9	Write 1 to reset to TX_DMATX_IDX9 to 0	1'b0
8	W1C	RST_DTX_IDX8	Write 1 to reset to TX_DMATX_IDX8 to 0	1'b0
7	W1C	RST_DTX_IDX7	Write 1 to reset to TX_DMATX_IDX7 to 0	1'b0
6	W1C	RST_DTX_IDX6	Write 1 to reset to TX_DMATX_IDX6 to 0	1'b0
5	W1C	RST_DTX_IDX5	Write 1 to reset to TX_DMATX_IDX5 to 0	1'b0
4	W1C	RST_DTX_IDX4	Write 1 to reset to TX_DMATX_IDX4 to 0	1'b0
3	W1C	RST_DTX_IDX3	Write 1 to reset to TX_DMATX_IDX3 to 0	1'b0
2	W1C	RST_DTX_IDX2	Write 1 to reset to TX_DMATX_IDX2 to 0	1'b0
1	W1C	RST_DTX_IDX1	Write 1 to reset to TX_DMATX_IDX1 to 0	1'b0
0	W1C	RST_DTX_IDX0	Write 1 to reset to TX_DMATX_IDX0 to 0	1'b0

WPDMA_DELAY_INT_CFG (offset: 0x0210, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	R/W	TX_DLY_INT_EN	1: Enable TX delayed interrupt mechanism. 0: Disable TX delayed interrupt mechanism	1'h0
30:24	R/W	TX_MAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or greater than the value specified here or interrupt pending time reach the limit (See below), a Final TX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'h0
23:16	R/W	TX_MAX_PTIME	Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or greater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or greater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'h0
15	R/W	RX_DLY_INT_EN	1: Enable RX delayed interrupt mechanism. 0: Disable RX delayed interrupt mechanism.	1'h0

14:8	R/W	RX_MAX_PINT	Specified Max # of pended interrupts. When the # of pended interrupts equal or greater than the value specified here or interrupt pending time reach the limit (See below), a Final RX_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'h0
7:0	R/W	RX_MAX_PTIME	Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or greater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or greater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'h0

WMM_AIFSN_CFG (offset: 0x0214, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	R/W	AIFSN7	WMM parameter AIFSN7	4'h0
27:24	R/W	AIFSN6	WMM parameter AIFSN6	4'h0
23:20	R/W	AIFSN5	WMM parameter AIFSN5	4'h0
19:16	R/W	AIFSN4	WMM parameter AIFSN4	4'h0
15:12	R/W	AIFSN3	WMM parameter AIFSN3	4'h0
11:8	R/W	AIFSN2	WMM parameter AIFSN2	4'h0
7:4	R/W	AIFSN1	WMM parameter AIFSN1	4'h0
3:0	R/W	AIFSN0	WMM parameter AIFSN0	4'h0

WMM_CW_MIN_CFG (offset: 0x0218, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	R/W	CW_MIN7	WMM parameter Cw_min7	4'h0
27:24	R/W	CW_MIN6	WMM parameter Cw_min6	4'h0
23:20	R/W	CW_MIN5	WMM parameter Cw_min5	4'h0
19:16	R/W	CW_MIN4	WMM parameter Cw_min4	4'h0
15:12	R/W	CW_MIN3	WMM parameter Cw_min3	4'h0
11:8	R/W	CW_MIN2	WMM parameter Cw_min2	4'h0
7:4	R/W	CW_MIN1	WMM parameter Cw_min1	4'h0
3:0	R/W	CW_MIN0	WMM parameter Cw_min0	4'h0

WMM_CW_MAX_CFG (offset: 0x021C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	R/W	CW_MAX7	WMM parameter Cw_max7	4'h0
27:24	R/W	CW_MAX6	WMM parameter Cw_max6	4'h0
23:20	R/W	CW_MAX5	WMM parameter Cw_max5	4'h0
19:16	R/W	CW_MAX4	WMM parameter Cw_max4	4'h0
15:12	R/W	CW_MAX3	WMM parameter Cw_max3	4'h0
11:8	R/W	CW_MAX2	WMM parameter Cw_max2	4'h0
7:4	R/W	CW_MAX1	WMM parameter Cw_max1	4'h0
3:0	R/W	CW_MAX0	WMM parameter Cw_max0	4'h0

WMM_TXOP_CFG0 (offset: 0x0220, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:16	R/W	WMM_TXOP1	WMM parameter TXOP1	16'h0
15:0	R/W	WMM_TXOP0	WMM parameter TXOP0	16'h0

WMM_TXOP_CFG1 (offset: 0x0224, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:16	R/W	WMM_TXOP3	WMM parameter TXOP3	16'h0
15:0	R/W	WMM_TXOP2	WMM parameter TXOP2	16'h0

WMM_TXOP_CFG2 (offset: 0x0228, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:16	R/W	WMM_TXOP5	WMM parameter TXOP5	16'h0
15:0	R/W	WMM_TXOP4	WMM parameter TXOP4	16'h0

WMM_TXOP_CFG3 (offset: 0x022C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:16	R/W	WMM_TXOP7	WMM parameter TXOP7	16'h0
15:0	R/W	WMM_TXOP6	WMM parameter TXOP6	16'h0

WMM_CTRL (offset: 0x0230, default: 0x0004_1040)

Bits	Type	Name	Description	Init Value
31	R/W	WMM_CH_SEL	WMM Channel Select 0: select channel 0 1: select channel 1	1'h0
30:28			Reserved	3'h0
27:24	R/W	CFG_SCH_RMP_EN	Configuration Scheduler Re-Mapping Enable [3]: switching ring 3 from channel 0 to channel 1 [2]: switching ring 2 from channel 0 to channel 1 [1]: switching ring 1 from channel 0 to channel 1 [0]: switching ring 0 from channel 0 to channel 1	4'h0
23:20			Reserved	4'h0
19:15	R/W	WMM1_RG2_TXQMA	WMM 1 Ready 2 to TX Queue Mapping	5'h8
14:10	R/W	WMM0_RG2_TXQMA	WMM 0 Ready 2 to TX Queue Mapping	5'h4
9:5	R/W	WMM_RG1_TXQMA	WMM 0/1 Ready 1 to TX Queue Mapping	5'h2
4:0	R/W	WMM_RG0_TXQMA	WMM 0/1 Ready 0 to TX Queue Mapping [4]: mapping to CT queue [3]: mapping to queue 3 [2]: mapping to queue 2 [1]: mapping to queue1 [0]: mapping to queue0 If all these 4 bits are de-asserted (all zero), there is no further queue ready mapping to current group ready. This means that the current TX queue always sends out.	5'h0

MCU_CMD (offset: 0x0234, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	MCU_CMD	MCU Command CPU command register. Internal CPU writes this register will trigger MCU command interrupt (0x0200 bit 9) to host.	32'h0

PDMA_DBG (offset: 0x0244, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:28	R/W	PDMA_DBG_IDX	PDMA Debug Index	4'h0

27	R/W	PDMA_DBG_SEL	PDMA Debug Selection 0: Debug index is controlled by UTIF 1: Debug index is controlled by bit[31:28]	1'h0
26:18	R		Reserved	9'h0
17:0	R	PDMA_DBG	PDMA Debug Signals	18'h0

TSO_CTRL (offset: 0x0250, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:19	R		Reserved	13'h0
18	R/W	TSO_WR_LEN_EN	TSO Write TXWI MPDU total byte count function enable 0: TXWI MPDU total byte count is written by FCE 1: TXWI MPDU total byte count is written by TSO	1'h0
17	R/W	TSO_SEG_EN	Enable TSO_SEG module(1:enable 0:disable) Partial TSO mode(TSO_SEG is disabled)	1'h0
16	R/W	TSO_EN	Enable TCP Segment Offload(1:enable 0:disable)	1'h0
15:12	R/W	RXWI_LEN	RXWI length sized by double word. (4'b1: 1DW, 4'b2: 2DW…)	4'h0
11:8	R/W	RX_L2_FIX_LEN	Fixed Rx l2 header length sizes by double word (4'b1: 1DW, 4'b2: 2DW…)	4'h0
7:4	R/W	TXWI_LEN	TXWI length sized by double word. (4'b1: 1DW, 4'b2: 2DW…)	4'h0
3:0	R/W	TX_L2_FIX_LEN	Fixed Tx l2 header length sizes by double word (4'b1: 1DW, 4'b2: 2DW…)	4'h0

WPDMA_TX_RING0_CTRL0 (offset: 0x0300, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring0 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING0_CTRL1 (offset: 0x0304, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring0.	12'h0

WPDMA_TX_RING0_CTRL2 (offset: 0x0308, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING0_CTRL3 (offset: 0x030C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING1_CTRL0 (offset: 0x0310, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring1 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING1_CTRL1 (offset: 0x0314, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring1.	12'h0

WPDMA_TX_RING1_CTRL2 (offset: 0x0318, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING1_CTRL3 (offset: 0x031C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING2_CTRL0 (offset: 0x0320, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring2 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING2_CTRL1 (offset: 0x0324, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring2.	12'h0

WPDMA_TX_RING2_CTRL2 (offset: 0x0328, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING2_CTRL3 (offset: 0x032C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING3_CTRL0 (offset: 0x0330, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring3 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING3_CTRL1 (offset: 0x0334, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring3.	12'h0

WPDMA_TX_RING3_CTRL2 (offset: 0x0338, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING3_CTRL3 (offset: 0x033C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING4_CTRL0 (offset: 0x0340, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring4 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING4_CTRL1 (offset: 0x0344, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring4.	12'h0

WPDMA_TX_RING4_CTRL2 (offset: 0x0348, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING4_CTRL3 (offset: 0x034C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING5_CTRL0 (offset: 0x0350, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring5 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING5_CTRL1 (offset: 0x0354, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring5.	12'h0

WPDMA_TX_RING5_CTRL2 (offset: 0x0358, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING5_CTRL3 (offset: 0x035C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING6_CTRL0 (offset: 0x0360, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring6 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING6_CTRL1 (offset: 0x0364, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring6.	12'h0

WPDMA_TX_RING6_CTRL2 (offset: 0x0368, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING6_CTRL3 (offset: 0x036C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING7_CTRL0 (offset: 0x0370, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring7 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING7_CTRL1 (offset: 0x0374, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring7.	12'h0

WPDMA_TX_RING7_CTRL2 (offset: 0x0378, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING7_CTRL3 (offset: 0x037C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0

11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING8_CTRL0 (offset: 0x0380, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring8 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING8_CTRL1 (offset: 0x0384, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring8.	12'h0

WPDMA_TX_RING8_CTRL2 (offset: 0x0388, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING8_CTRL3 (offset: 0x038C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_TX_RING9_CTRL0 (offset: 0x0390, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of TX_Ring9 (4-DWORD aligned address)	32'h0

WPDMA_TX_RING9_CTRL1 (offset: 0x0394, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of TXD count in TXD_Ring9.	12'h0

WPDMA_TX_RING9_CTRL2 (offset: 0x0398, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next TXD CPU wants to use	12'h0

WPDMA_TX_RING9_CTRL3 (offset: 0x039C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next TXD DMA wants to use	12'h0

WPDMA_RX_RING0_CTRL0 (offset: 0x03C0, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of RXD Ring #0 (GE ports). It should be a	32'h0

			4-DWORD aligned address	

WPDMA_RX_RING0_CTRL1 (offset: 0x03C4, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of RXD count in RXD Ring #0.	12'h0

WPDMA_RX_RING0_CTRL2 (offset: 0x03C8, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next RXD CPU wants to allocate to RXD Ring #0.	12'h0

WPDMA_RX_RING0_CTRL3 (offset: 0x03CC, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address.	12'h0

WPDMA_RX_RING1_CTRL0 (offset: 0x03D0, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BASE_PTR	Point to the base address of RXD Ring #1 (GE ports). It should be a 4-DWORD aligned address	32'h0

WPDMA_RX_RING1_CTRL1 (offset: 0x03D4, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	MAX_CNT	The maximum number of RXD count in RXD Ring #1.	12'h0

WPDMA_RX_RING1_CTRL2 (offset: 0x03D8, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	CPU_IDX	Point to the next RXD CPU wants to allocate to RXD Ring #1.	12'h0

WPDMA_RX_RING1_CTRL3 (offset: 0x03DC, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:12	R		Reserved	20'h0
11:0	R/W	DMA_IDX	Point to the next RXD DMA wants to use in FDS Ring#1. It should be a 4-DWORD aligned address.	12'h0

5.6 WLAN PBF registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Reserve	N/A
Andes firmware/TESTIF	0x0041_0000

SYS_CTRL (offset: 0x0400,default :0x00080000)

Bits	Type	Name	Description	Init Value
31:25	-	-	Reserved	
24	R/W	CSR_TEST_EN	Test enable	1'b0
23:22	R/W	MAC_CLKSEL	00: non-idle MAC clock is 160MHz 01: non-idle MAC clock is 120MHz 10: non-idle MAC clock is 80MHz 11: non-idle MAC clock is 40MHz	2'b00
21:20	R/W	PWRSV_EN	MAC idle power saving mode enable 00: disable MAC idle power-saving 01: MAC clock will be 120MHz when MAC is idle and MAC_CLKSEL is 2'b00 or 2'b01; MAC clock will be 80MHz when MAC is idle and MAC_CLKSEL is 2'b10; MAC clock will be 40MHz when MAC is idle and MAC_CLKSEL is 2'b11 10: MAC clock will be 80MHz when MAC is idle and MAC_CLKSEL is 2'b00 or 2'b01 or 2'b10; MAC clock will be 40MHz when MAC is idle and MAC_CLKSEL is 2'b11 11: MAC clock will be 40MHz when MAC is idle [MAC clock table] PWRSV_EN / MAC_CLKSEL 00 01 10 11 00 160M 120M 80M 40M 01 120M 120M 80M 40M 10 80M 80M 80M 40M 11 40M 40M 40M 40M	2'b00
19	R/W	SHRM_SEL	Shared memory selection 0: address 0x8000 – 0xFFFF mapping to packet buffer memory 1: address 0x8000 – 0xFFFF mapping to shared memory	1
18:16	R/W	PBF_MSEL	Packet buffer memory access selection. 000: address 0x8000 – 0xFFFF mapping to 1st 32kB of packet buffer. 001: address 0x8000 – 0xFFFF mapping to 2nd 32kB of packet buffer. 010: address 0x8000 – 0xFFFF mapping to 3rd 32kB of packet buffer. 011: address 0x8000 – 0xFFFF mapping to 4th 32kB of packet buffer. 100: address 0x8000 – 0xFFFF mapping to 5th 32kB of packet buffer. Others: Reserved	0
15:12	-	-	Reserved	
11	R/W	PBF_CLKEN	PBF clock enable.	0
10	R/W	MAC_CLK_EN	MAC clock enable.	0

9:4			Reserved	
3	R/W	PBF_RESET	PBF hardware reset. Write '1' to put PBF into reset state.	0
2	R/W	MAC_RESET	MAC hardware reset. Write '1' to put MAC into reset state.	0
1:0	-	-	Reserved	

PBF_CFG (offset: 0x0404,default : 0x000000F5)

Bits	Type	Name	Description	Init Value
31:28	R/W	TX3Q_PKT_NUM	Maximum packet number of TX3 OUT Queue	4'd7
27:24	R/W	TX2Q_PKT_NUM	Maximum packet number of TX2 OUT Queue	4'd7
23:20	R/W	TX1Q_PKT_NUM	Maximum packet number of TX1 OUT Queue	4'd7
19:16	R/W	TX0Q_PKT_NUM	Maximum packet number of TX0 OUT Queue	4'd2
15:14			Reserved	
13	R/W	TX3_OUTQ_EN	TX3 Out Queue enable	1'b1
12	R/W	TX2_OUTQ_EN	TX2 Out Queue enable	1'b1
11	R/W	TX1_OUTQ_EN	TX1 Out Queue enable	1'b1
10	R/W	TX0_OUTQ_EN	TX0 Out Queue enable	1'b1
9	R/W	PBF_CAP_MODE	Data scope mode. When set, 64K PBF buffer will be used for data scope.	0
8	R/W	RX_DROP_MODE	Rx drop mode. When set, PBF will drop Rx packet before into DMA. 0: normal mode 1: drop mode	0
7:5	R/W	NULL2_SEL	NULL2 frame buffer selection (reuse beacon buffer). 0: use beacon #8 buffer (address set by 0x424[7:0]) 1: use beacon #9 buffer (address set by 0x424[15:8]) 2: use beacon #10 buffer (address set by 0x424[23:16]) 3: use beacon #11 buffer (address set by 0x424[31:24]) 4: use beacon #12 buffer (address set by 0x428[7:0]) 5: use beacon #13 buffer (address set by 0x428[15:8]) 6: use beacon #14 buffer (address set by 0x428[23:16]) 7: use beacon #15 buffer (address set by 0x428[31:24])	3'h7
4	R/W	RX0Q_EN	Rx0Q enable	1
3	R/W	TX3Q_EN	Tx3Q enable	0
2	R/W	TX2Q_EN	Tx2Q enable	1
1	R/W	TX1Q_EN	Tx1Q enable	0
0	R/W	TX0Q_EN	Tx0Q enable	1

TX_MAX_PCNT (offset: 0x0408,default :0x1F3F9F9F)

Bits	Type	Name	Description	Init Value
31:24	R/W	MAX_TX3Q_PCNT	Maximum buffer page count of Tx3Q.	8'h1f
23:16	R/W	MAX_TX2Q_PCNT	Maximum buffer page count of Tx2Q.	8'h9f
15:8	R/W	MAX_TX1Q_PCNT	Maximum buffer page count of Tx1Q.	8'h1f
7:0	R/W	MAX_TX0Q_PCNT	Maximum buffer page count of Tx0Q.	8'h1f

RX_MAX_PCNT (offset: 0x040C,default :0x0000009F)

Bits	Type	Name	Description	Init Value
31:8	-	-	Reserved	
7:0	R/W	MAX_RX0Q_PCNT	Maximum buffer page count of Rx0Q.	8'h9f

BUF_CTRL (offset:0x0410,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:5			Reserved	

19:16	R/W		Reserve	0
15:14	R		Reserved	
13	W1C	NULL9_KICK	Kick out NULL9 frame. This bit will be cleared after NULL3 frame is transmitted.	0
12	W1C	NULL8_KICK	Kick out NULL8 frame. This bit will be cleared after NULL3 frame is transmitted.	0
11	W1C	NULL7_KICK	Kick out NULL7 frame. This bit will be cleared after NULL3 frame is transmitted.	0
10	W1C	NULL6_KICK	Kick out NULL6 frame. This bit will be cleared after NULL3 frame is transmitted.	0
9	W1C	NULL5_KICK	Kick out NULL5 frame. This bit will be cleared after NULL3 frame is transmitted.	0
8	W1C	NULL4_KICK	Kick out NULL4 frame. This bit will be cleared after NULL3 frame is transmitted.	0
7:5			Reserved	
4	W1C	BUF_RESET	Buffer reset.	0
3	W1C	NULL3_KICK	Kick out NULL3 frame. This bit will be cleared after NULL3 frame is transmitted.	0
2	W1C	NULL2_KICK	Kick out NULL2 frame. This bit will be cleared after NULL2 frame is transmitted.	0
1	W1C	NULL1_KICK	Kick out NULL1 frame. This bit will be cleared after NULL1 frame is transmitted.	0
0	W1C	NULL0_KICK	Kick out NULL0 frame. This bit will be cleared after NULL0 frame is transmitted.	0

MCU_INT_STA (offset:0x0414,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	MAC_INT_15	MAC interrupt 15: Beacon of my BSS is dropped	0
30	R/W	MAC_INT_14	MAC interrupt 14: Beacon of my BSS has uc2me frame	0
29	R/W	MAC_INT_13	MAC interrupt 13: Beacon of my BSS has bc/mc frame	0
28	R/W	MAC_INT_12	MAC interrupt 12: Beacon of my BSS content changes	0
27	R/W	MAC_INT_11	MAC interrupt 11: Beacon of my BSS2 is received	0
26	R/W	MAC_INT_10	MAC interrupt 10: Beacon of my BSS1 is received	0
25	R/W	MAC_INT_9	MAC interrupt 9: Beacon of my BSS0 is received	0
24	R/W	MAC_INT_8	MAC interrupt 8: RX QoS CF-Poll interrupt	0
23	R/W	MAC_INT_7	MAC interrupt 7: TXOP early termination interrupt	0
22	R/W	MAC_INT_6	MAC interrupt 6: TXOP early timeout interrupt	0
21	R/W	MAC_INT_5	MAC interrupt 5: No BSS0 Beacon received within Beacon expect window	0
20	R/W	MAC_INT_4	MAC interrupt 4: GP timer interrupt	0
19	R/W	MAC_INT_3	MAC interrupt 3: Auto wakeup interrupt	0
18	R/W	MAC_INT_2	MAC interrupt 2: TX status interrupt	0
17	R/W	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt	0
16	R/W	MAC_INT_0	MAC interrupt 0: TBTT interrupt	0
15			Reserved	
~~14~~	~~R/W~~	~~EAP_INT~~	~~EAP interrupt~~	~~0~~
~~13~~	~~R/W~~	~~BB_AGC_ULP_INT~~	~~BBP AGC ULP interrupt~~	~~0~~
12	R/W	BB_RADAR_INT	BBP detects radar tones interrupt	0
11	R/W		Reserve	0
10	R/W		Reserve	0
9	R/W		Reserve	0
8	R/W	MRX0_INT	MAC to RX0Q frame transfer complete interrupt.	0
7	R/W	BCNTX_INT	Beacon frame Tx complete interrupt.	0
6	R/W	N2TX_INT	NULL2 frame Tx complete interrupt.	0
5	R/W	N1TX_INT	NULL1 frame Tx complete interrupt.	0
4	R/W	N0TX_INT	NULL0 frame Tx complete interrupt.	0

3	R/W	MTX3_INT	TX3Q to MAC frame transfer complete interrupt.	0
2	R/W	MTX2_INT	TX2Q to MAC frame transfer complete interrupt.	0
1	R/W	MTX1_INT	TX1Q to MAC frame transfer complete interrupt.	0
0	R/W	MTX0_INT	TX0Q to MAC frame transfer complete interrupt.	0

***This register is only for internal MCU**

MCU_INT_ENA (offset:0x0418,default :0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	MAC_INT15_EN	MAC interrupt 15 enable	0
30	R/W	MAC_INT14_EN	MAC interrupt 14 enable	0
29	R/W	MAC_INT13_EN	MAC interrupt 13 enable	0
28	R/W	MAC_INT12_EN	MAC interrupt 12 enable	0
27	R/W	MAC_INT11_EN	MAC interrupt 11 enable	0
26	R/W	MAC_INT10_EN	MAC interrupt 10 enable	0
25	R/W	MAC_INT9_EN	MAC interrupt 9 enable	0
24	R/W	MAC_INT8_EN	MAC interrupt 8 enable	0
23	R/W	MAC_INT7_EN	MAC interrupt 7 enable	0
22	R/W	MAC_INT6_EN	MAC interrupt 6 enable	0
21	R/W	MAC_INT5_EN	MAC interrupt 5 enable	0
20	R/W	MAC_INT4_EN	MAC interrupt 4 enable	0
19	R/W	MAC_INT3_EN	MAC interrupt 3 enable	0
18	R/W	MAC_INT2_EN	MAC interrupt 2 enable	0
17	R/W	MAC_INT1_EN	MAC interrupt 1 enable	0
16	R/W	MAC_INT0_EN	MAC interrupt 0 enable	0
15:13			Reserved	
12	R/W	RADAR_INT_EN	BBP detects radar tones interrupt enable	0
11	R/W	MAC_INT18_EN	MAC interrupt 18 enable	0
10	R/W	MAC_INT17_EN	MAC interrupt 17 enable	0
9	R/W	MAC_INT16_EN	MAC interrupt 16 enable	0
8	R/W	MRX0_INT_EN	MAC to RX0Q frame transfer complete interrupt enable.	0
7	R/W	BCNTX_INT_EN	Beacon frame Tx complete interrupt enable.	0
6	R/W	N2TX_INT_EN	NULL2 frame Tx complete interrupt enable.	0
5	R/W	N1TX_INT_EN	NULL1 frame Tx complete interrupt enable.	0
4	R/W	N0TX_INT_EN	NULL0 frame Tx complete interrupt enable.	0
3	R/W	MTX3_INT_EN	TX3Q to MAC frame transfer complete interrupt enable.	0
2	R/W	MTX2_INT_EN	TX2Q to MAC frame transfer complete interrupt enable.	0
1	R/W	MTX1_INT_EN	TX1Q to MAC frame transfer complete interrupt enable.	0
0	R/W	MTX0_INT_EN	TX0Q to MAC frame transfer complete interrupt enable.	0

***This register is only for internal MCU**

BCN_OFFSET0 (offset: 0x041C,default :0xECE8E4E0)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN3_OFFSET	Beacon #3 address offset in shared memory. Unit is 64 byte.	8'hec
23:16	R/W	BCN2_OFFSET	Beacon #2 address offset in shared memory. Unit is 64 byte.	8'he8
15:8	R/W	BCN1_OFFSET	Beacon #1 address offset in shared memory. Unit is 64 byte.	8'he4
7:0	R/W	BCN0_OFFSET	Beacon #0 address offset in shared memory. Unit is 64 byte.	8'he0

BCN_OFFSET1 (offset: 0x0420,default :0xFCF8F4F0)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN7_OFFSET	Beacon #7 address offset in shared memory. Unit is 64 byte.	8'hfc
23:16	R/W	BCN6_OFFSET	Beacon #6 address offset in shared memory. Unit is 64 byte.	8'hf8

15:8	R/W	BCN5_OFFSET	Beacon #5 address offset in shared memory. Unit is 64 byte.	8'hf4
7:0	R/W	BCN4_OFFSET	Beacon #4 address offset in shared memory. Unit is 64 byte.	8'hf0

BCN_OFFSET2 (offset: 0x0424,default :0x0C080400)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN11_OFFSET	Beacon #11 address offset in shared memory. Unit is 64 byte.	8'h0c
23:16	R/W	BCN10_OFFSET	Beacon #10 address offset in shared memory. Unit is 64 byte.	8'h08
15:8	R/W	BCN9_OFFSET	Beacon #9 address offset in shared memory. Unit is 64 byte.	8'h04
7:0	R/W	BCN8_OFFSET	Beacon #8 address offset in shared memory. Unit is 64 byte.	8'h00

BCN_OFFSET3 (offset: 0x0428,default :0x1C181410)

Bits	Type	Name	Description	Init Value
31:24	R/W	BCN15_OFFSET	Beacon #15 address offset in shared memory. Unit is 64 byte.	8'h1c
23:16	R/W	BCN14_OFFSET	Beacon #14 address offset in shared memory. Unit is 64 byte.	8'h18
15:8	R/W	BCN13_OFFSET	Beacon #13 address offset in shared memory. Unit is 64 byte.	8'h14
7:0	R/W	BCN12_OFFSET	Beacon #12 address offset in shared memory. Unit is 64 byte.	8'h10

RXQ_STA (offset: 0x0430,default :0x00000022)

Bits	Type	Name	Description	Init Value
31:24	-	-	Reserved	
23:16	RO	RX0Q_PCNT	Page count in RxQ	8'h00
15:8	-	-	Reserved	
7:0	RO	R0Q_STA	Rx0Q status	8'h22

TXQ_STA (offset: 0x0434,default :0x22020202)

Bits	Type	Name	Description	Init Value
31:24	RO	TX3Q_STA	Tx3Q status	8'h02
23:16	RO	TX2Q_STA	Tx2Q status	8'h02
15:8	RO	TX1Q_STA	Tx1Q status	8'h02
7:0	RO	TX0Q_STA	Tx0Q status	8'h02

TXRXQ_PCNT (offset: 0x0438,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:24	RO	TX3Q_PCNT	Page count in Tx3Q	8'h00
23:16	RO	TX2Q_PCNT	Page count in Tx2Q	8'h00
15:8	RO	TX1Q_PCNT	Page count in Tx1Q	8'h00
7:0	RO	TX0Q_PCNT	Page count in Tx0Q	8'h00

PBF_DBG (offset: 0x043C,default :0x00000FE)

Bits	Type	Name	Description	Init Value
31:8			Reserved	
7:0	RO	FREE_PCNT	Free page count	8'hFE

MCU_INT2_ST (offset:0x0450,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:22	R		Reserved	0
21	R/W	MAC_INT_24	MAC interrupt 24: Probe Response of my BSS2 is received	0
20	R/W	MAC_INT_23	MAC interrupt 23: Probe Response of my BSS1 is received	0
19	R/W	MAC_INT_22	MAC interrupt 22: Probe Response of my BSS0 is received	0
18	R/W	MAC_INT_21	MAC interrupt 21: TBTT1 interrupt	0

17	R/W	MAC_INT_20	MAC interrupt 20: Pre-TBTT1 interrupt	0
16	R/W	MAC_INT_19	MAC interrupt 19: No BSS1 Beacon received within Beacon expect window	0
15:7	R		Reserved	0
6	R/W	N9TX _INT	NULL9 frame Tx complete interrupt.	0
5	R/W	N8TX _INT	NULL8 frame Tx complete interrupt.	0
4	R/W	N7TX _INT	NULL7 frame Tx complete interrupt.	0
3	R/W	N6TX _INT	NULL6 frame Tx complete interrupt.	0
2	R/W	N5TX_INT	NULL5 frame Tx complete interrupt.	0
1	R/W	N4TX_INT	NULL4 frame Tx complete interrupt.	0
0	R/W	N3TX_INT	NULL3 frame Tx complete interrupt.	0

***This register is only for internal MCU**

MCU_INT2_EN (offset:0x0454,default :0x00000000)

Bits	Type	Name	Description	Init Value
31:22	R		Reserved	0
21	R/W	MAC_INT24_EN	MAC interrupt 24 enable	0
20	R/W	MAC_INT23_EN	MAC interrupt 23 enable	0
19	R/W	MAC_INT22_EN	MAC interrupt 22 enable	0
18	R/W	MAC_INT21_EN	MAC interrupt 21 enable	0
17	R/W	MAC_INT20_EN	MAC interrupt 20 enable	0
16	R/W	MAC_INT19_EN	MAC interrupt 19 enable	0
15:7	R		Reserved	0
6	R/W	N9TX_INT_EN	NULL9 frame Tx complete interrupt enable.	0
5	R/W	N8TX_INT_EN	NULL8 frame Tx complete interrupt enable.	0
4	R/W	N7TX_INT_EN	NULL7 frame Tx complete interrupt enable.	0
3	R/W	N6TX _INT_EN	NULL6 frame transfer complete interrupt enable.	0
2	R/W	N5TX _INT_EN	NULL5 frame transfer complete interrupt enable.	0
1	R/W	N4TX _INT_EN	NULL4 frame transfer complete interrupt enable.	0
0	R/W	N3TX _INT_EN	NULL3 frame transfer complete interrupt enable.	0

5.7 RFCTRL registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Reserve	N/A
Andes firmware/TESTIF	0x0041_0000

RF_CSR_CFG (offset: 0x0500, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0			Reserved	

RF_BYPASS_0 (offset: 0x0504, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	R/W	BYPASS_dacclk_on1	When set, RF control signals come from the corresponding bit in RF_SETTING instead of MAC/BBP in normal operation mode	0
30	R/W	BYPASS_dacclk_on0	Same as the above	0
29	R/W	BYPASS_dac_on1	Same as the above	0
28	R/W	BYPASS_dac_on0	Same as the above	0
27	R/W	BYPASS_dac10_freq	Same as the above	0
26	R/W	BYPASS_adcclk_on1	Same as the above	0
25	R/W	BYPASS_adcclk_on0	Same as the above	0
24	R/W	BYPASS_adc9_stby1	Same as the above	0
23	R/W	BYPASS_adc9_on1	Same as the above	0
22	R/W	BYPASS_adc9_stby0	Same as the above	0
21	R/W	BYPASS_adc9_on0	Same as the above	0
20	R/W	BYPASS_adc9_freq	Same as the above	0
19	R/W	BYPASS_trsw_ant1	Same as the above	0
18	R/W	BYPASS_trsw_ant0	Same as the above	0
17	R/W	BYPASS_addac_ldo_en	Same as the above	0
16	R/W	BYPASS_pa_mode	Same as the above	0
15	R/W	BYPASS_ant_sel	Same as the above	0
14	R/W	BYPASS_pa_pe_a1	Same as the above	0
13	R/W	BYPASS_pa_pe_g1	Same as the above	0
12	R/W	BYPASS_pa_pe_a0	Same as the above	0
11	R/W	BYPASS_pa_pe_g0	Same as the above	0
10	R/W	BYPASS_xlna1_en	Same as the above	0
9	R/W	BYPASS_xlna0_en	Same as the above	0
8	R/W	BYPASS_lna_pe_a1	Same as the above	0
7	R/W	BYPASS_lna_pe_g1	Same as the above	0
6	R/W	BYPASS_lna_pe_a0	Same as the above	0
5	R/W	BYPASS_lna_pe_g0	Same as the above	0
4	R/W	BYPASS_rftx_pe	Same as the above	0
3	R/W	BYPASS_rfrx_pe	Same as the above	0
2	R/W	BYPASS_rfpll_pe	Same as the above	0
1	R/W	BYPASS_rf_pe	Same as the above	0
0	R/W	BYPASS_rfldo0_en	Same as the above	0

RF_BYPASS_1 (offset: 0x0508, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:9			Reserved	
8	R/W	BYPASS_tssi_on	When set, RF control signals come from the corresponding bit in RF_SETTING instead of MAC/BBP in normal operation mode	0
~~7~~	~~R/W~~	~~BYPASS_tx_gainatt1~~	~~Same as the above~~	~~0~~

6	R/W	BYPASS_tx_gcrf1	Same as the above	0
~~5~~	~~R/W~~	~~BYPASS_tx_gainatt0~~	~~Same as the above~~	~~0~~
4	R/W	BYPASS_tx_gcrf0	Same as the above	0
3	R/W	BYPASS_rf_vga1	Same as the above	0
2	R/W	BYPASS_rf_lna1	Same as the above	0
1	R/W	BYPASS_rf_vga0	Same as the above	0
0	R/W	BYPASS_rf_lna0	Same as the above	0

RF_SETTING_0 (offset: 0x050C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:29			Reserved	
28	R/W	SET_adcclk_on1	Set control on adcclk_on1	0
27	R/W	SET_adcclk_on0	Set control on adcclk_on0	0
26	R/W	SET_adc9_stby1	Set control on adc9_stby1	0
25	R/W	SET_adc9_on1	Set control on adc9_on1	0
24	R/W	SET_adc9_stby0	Set control on adc9_stby0	0
23	R/W	SET_adc9_on0	Set control on adc9_on0	0
22:21	R/W	SET_adc9_freq	Set control on adc9_freq	0
20	R/W	SET_trsw_ant1	Set control on trsw_ant1	0
19	R/W	SET_trsw_ant0	Set control on trsw_ant0	0
18	R/W	SET_addac_ldo_en	Set control on addac_ldo_en	0
17:16	R/W	SET_pa_mode	Set control on pa_mode	0
15	R/W	SET_ant_sel	Set control on ant_sel	0
14	R/W	SET_pa_pe_a1	Set control on pa_pe_a1	0
13	R/W	SET_pa_pe_g1	Set control on pa_pe_g1	0
12	R/W	SET_pa_pe_a0	Set control on pa_pe_a0	0
11	R/W	SET_pa_pe_g0	Set control on pa_pe_g0	0
10	R/W	SET_xlna1_en	Set control on xlna1_en	0
9	R/W	SET_xlna0_en	Set control on xlna0_en	0
8	R/W	SET_lna_pe_a1	Set control on lna_pe_a1	0
7	R/W	SET_lna_pe_g1	Set control on lna_pe_g1	0
6	R/W	SET_lna_pe_a0	Set control on lna_pe_a0	0
5	R/W	SET_lna_pe_g0	Set control on lna_pe_g0	0
4	R/W	SET_rftx_pe	Set control on rftx_pe	0
3	R/W	SET_rfrx_pe	Set control on rfrx_pe	0
2	R/W	SET_rfpll_pe	Set control on rfpll_pe	0
1	R/W	SET_rf_pe	Set control on rf_pe	0
0	R/W	SET_rfldo0_en	Set control on rfldo0_en	0

RF_SETTING_1 (offset: 0x0510, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31	R/W	SET_tssi_on	Set control on tssi_on	0
30			Reserved	
~~29:28~~	~~R/W~~	~~SET_tx_gainatt1~~	~~Set control on tx_gainatt1[1:0]~~	~~0~~
27:24	R/W	SET_tx_gcrf1	Set control on tx_gcrf1[3:0]	0
~~21:20~~	~~R/W~~	~~SET_tx_gainatt0~~	~~Set control on tx_gainatt0[1:0]~~	~~0~~
19:16	R/W	SET_tx_gcrf0	Set control on tx_gcrf0[3:0]	0
15:10	R/W	SET_rf_vga1	Set control on rf_vga1[5:0]	0
9:8	R/W	SET_rf_lna1	Set control on rf_lna1[1:0]	0
7:2	R/W	SET_rf_vga0	Set control on rf_vga0[5:0]	0
1:0	R/W	SET_rf_lna0	Set control on rf_lna0[1:0]	0

RF_SETTING_2 (offset: 0x0514, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:5			Reserved	
4	R/W	SET_dacclk_on1	Set control on dacclk_on1	0
3	R/W	SET_dacclk_on0	Set control on dacclk_on0	0
2	R/W	SET_dac_on1	Set control on dac_on1	0
1	R/W	SET_dac_on0	Set control on dac_on0	0
0	R/W	SET_dac10_freq	Set control on dac10_freq	0

RF_MISC (offset: 0x0518, default: 0x0000_0001)

Bits	Type	Name	Description	Init Value
31:5			Reserved	
4	R/W	ext_pa_en_g1	1'b1: enable external G band PA, 1'b0: disable external G band PA	0
3	R/W	ext_pa_en_a1	1'b1: enable external A band PA, 1'b0: disable external A band PA	0
2	R/W	ext_pa_en_g0	1'b1: enable external G band PA, 1'b0: disable external G band PA	0
1	R/W	ext_pa_en_a0	1'b1: enable external A band PA, 1'b0: disable external A band PA	0
0	R/W	Addac_ldo_adc9_en	When set, adc9_on0 will enable addac_ldo_en in normal WLAN enable mode ; otherwise, adc9_on0 won't enable addac_ldo_en	1

RF_BSI_CKDIV (offset: 0x0520, default: 0x0000_0002)

Bits	Type	Name	Description	Init Value
31:5			Reserved	
4:0	R/W	ckdiv	SPI clock setting SPI clock rate = 160MHz/(ckdiv*2), ckdiv = 5'd0 & 5'd1 are illegal. Default is 5'd2, SPI clock rate = 40MHz	5'd2

RF_BSI_WDATA (offset: 0x0524, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	R/W	BSI_WDATA	Write data for parallel to serial	0

RF_BSI_ACCESS (offset: 0x0528, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:17			Reserved	
16	R/W	WF_SEL	1'b0: WF0 select 1'b1: WF1 select	0
15:14	RO	BSI_ST	FSM state	0
13	RO	BSI_BUSY	Busy state indication	0
12	R/W	BSI_WHRL	1'b0: for read function 1'b1: for write function	0
11:0	R/W	BSI_ADDR	Address for read/write	0

RF_BSI_RDATA (offset: 0x052C, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:0	RO	BSI_RDATA	Read data for seral to parallel	0

RF_RFDIGI_RST (offset: 0x0530, default: 0x0000_0000)

Bits	Type	Name	Description	Init Value
31:4			Reserved	
3	R/W	WF1_RFDIGI_CR_RSTB	WF1 RFDIGI CR reset Low active reset, default at reset	0
2	R/W	WF1_RFDIGI_RSTB	WF1 RFDIGI reset Low active reset, default at reset	0
1	R/W	WF0_RFDIGI_CR_RSTB	WF0 RFDIGI CR reset Low active reset, default at reset	0
0	R/W	WF0_RFDIGI_RSTB	WF0 RFDIGI reset Low active reset, default at reset	0

5.8 FCE/FCE PDMA registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Reserve	N/A
Andes firmware/TESTIF	0x0041_0000

FCE_and_PSE_control (offset:0x0800,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:12	-	-	reserved	20'b0
11:8	R/W	dbg_sel	debug output select.	4'b0000
7:5	-	-	reserved	3'b0
4	-	reserved	-	1'b0
3	-	reserved	-	1'b0
2	RO	pse_rdy	PSE and FCE is initialized and is ready for work (page_cnt contents is valid)	1'b0
1	WSC	fce_rst	FCE reset pulse issued and is applied to FCE.	1'b0
0	R/W	fce_en	FCE enable. FCE halt and stay in current status if this bit is low.	1'b0

FCE_Parameters (offset:0x0804,default:0xf6255f0f)

Bits	Type	Name	Description	Init Value
31:24	R/W	px_1q_only	define which port only to use one queue. bit31: reserved bit30: set for f0 port bit29: set for vt port bit28: set for vr port bit27: set for h port bit26: set for ct port bit25: set for cr port bit24: set for w port	8'b111101 10
23:20	R/W	LLC_len	LLC length in double word. Used for skipping the gap between L2 header and LLC. LLC abuts with L3 header.	4'd2
19:16	R/W	txwi_len	length of TX wireless MAC information in double word	4'd5
15:12	R/W	rxwi_len	length of RX wireless MAC information in double word	4'd5
11:8	R/W	rx_L2_hd_sz	length of RX L2 header in double word	4'd15
7:4	-	-	reserved	4'b0
3:0	R/W	tx_802_11_L2_hd_sz	length of 802.11 TX L2 header in double word	4'd15

Checksum_Offload (offset:0x0808,default:0x00000200)

Bits	Type	Name	Description	Init Value
31:11	-	-	reserved	21'b0
10	R/W	stamp_seq_num_en	"0", leave L2 sequence number intact."1", refer to WCID field in TXWI then increment WLAN sequence number from sequence number memory.	1'b0
9	R/W	cso_bigendian	define the word's endian of the final DW	1'b1
8	R/W	cso_en	checksum offload enable	1'b0
7	R/W	tx_ipv6_en	IPv6 search next_header for TCP/UDP checksum generation enable	1'b0
6	R/W	tx_ipv4_cs_gen	generate IPv4 header checksum	1'b0
5	R/W	tx_tcp_cs_gen	generate TCP checksum	1'b0
4	R/W	tx_udp_cs_gen	generate UCP checksum	1'b0
3	R/W	rx_ipv6_en	IPv6 search next_header for TCP/UDP checksum enable	1'b0
2	R/W	rx_ipv4_cs_en	IPv4 header checksum enable	1'b0
1	R/W	rx_tcp_cs_en	TCP checksum enable	1'b0
0	R/W	rx_udp_cs_en	UDP checksum enable	1'b0

L2_stuffing (offset:0x080c,default:0x03ff0233)

Bits	Type	Name	Description	Init Value
31:26	-	-	reserved	6'b0
25:24	R/W	other_port	for MAC info bit31to0 are all zero. 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
23:16	R/W	auto_length_en	For each port, Auto packet length calculate enable.	8'hFF
15:8	R/W	ts_cmd_qsel_en	For each port, TS command packet Qsel enable.	8'd2
7:6	-	-	reserved	2'b0
5	R/W	mvinf_byte_swp	swap byte during move info.	1'b1
4	R/W	fs_wr_mpdu_len_en	H for write mpdu length	1'b1
3	R/W	tx_L2_de_stuffing_en	parse 802.11 L2 header then remove stuffed DW and handover correct L2 to WMAC	1'b0
2	R/W	rx_L2_stuffing_en	parse 802.11 L2 header from WMAC frames then stuff double words to fit rx_L2_hd_sz	1'b0
1	R/W	QoS_L2_en	QoS control field support	1'b1
0	R/W	HT_L2_en	the 802.11 frame header can contain HT control field	1'b1

RX_classification_bit_enable_control (offset:0x0810,default:0x00001fff)

Bits	Type	Name	Description	Init Value
31:0	R/W	rxctr_en	bit enable for MAC info.	32'h00001FFF

RX_classification_configuration_0 (offset:0x0814,default:0xffffffff)

Bits	Type	Name	Description	Init Value
31:26	R/W	bit15to13_port	for MAC info bit15to13,each info is controled by two bit register. 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	6'h3F
25:24	R/W	WAMSDU_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host. The priority is discard, cpu, virtual cpu port then host.	2'b11
23:22	R/W	AMSDU_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
21:20	R/W	MIC_err_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
19:18	R/W	ICV_err_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
17:16	R/W	CRC_err_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
15:14	R/W	MYBSS_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
13:12	R/W	BC_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
11:10	R/W	MC_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
9:8	R/W	UC2ME_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
7:6	R/W	FRAG_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
5:4	R/W	NULL_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
3:2	R/W	DATA_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
1:0	R/W	BA_port	00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11

RX_classification_configuration_1 (offset:0x0818,default:0xffffffff)

Bits	Type	Name	Description	Init Value
31:26	R/W	bit31to28_port	for MAC info bit31to29,each info is controled by two bit register. 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	8'hFF
25:24	R/W	ACT_WANTED_port	Specified Action frame port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
23:22	R/W	DEAUTH_port	Deauthentication frame port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
21:20	R/W	DIS_ASSO_port	Disassociation frame port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
19:18	R/W	BEACON_port	Beacon frame port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
17:16	R/W	PRB_RSP_port	Probe Reponse frame port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
15:14	R/W	SW_FCTYPE1_port	SW specified frame type1 port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
13:12	R/W	SW_FCTYPE0_port	SW specified frame type0 port config : 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	2'b11
11:0	R/W	Bit23to16_port	for MAC info bit21to16,each info is controled by two bit register. 00 to discard, 01 to cpu, 10 to virtual cpu port, 11 to host.	16'hFFFF

FCE_flow_control_interrupt_reason (offset:0x081c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7	R/W1C	pse_px_rx_int_7	f1 port pause timeout interrupt occurs during free-page level under f1_fp_lth and enq_level over f1_hth.	1'b0
6	R/W1C	pse_px_rx_int_6	f0 port pause timeout interrupt occurs during free-page level under f0_fp_lth and enq_level over f0_hth.	1'b0
5	R/W1C	pse_px_rx_int_5	vt port pause timeout interrupt occurs during free-page level under vt_fp_lth and enq_level over vt_hth.	1'b0
4	R/W1C	pse_px_rx_int_4	vr port pause timeout interrupt occurs during free-page level under vr_fp_lth and enq_level over vr_hth.	1'b0
3	R/W1C	pse_px_rx_int_3	h port pause timeout interrupt occurs during free-page level under h_fp_lth and enq_level over h_hth.	1'b0
2	R/W1C	pse_px_rx_int_2	ct port pause timeout interrupt occurs during free-page level under ct_fp_lth and enq_level over ct_hth.	1'b0
1	R/W1C	pse_px_rx_int_1	cr port pause timeout interrupt occurs during free-page level under cr_fp_lth and enq_level over cr_hth.	1'b0
0	R/W1C	pse_px_rx_int_0	w pause timeout interrupt occurs during free-page level under w_fp_lth and enq_level over w_hth.	1'b0

FCE_flow_control_interrupt_enable (offset:0x0820,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	pse_px_rx_int_en	interrupt enable for above address.	8'b0

WLAN_port_flow_control_1 (offset:0x0824,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	w_hth	in-use page count shmidt trigger high threshold for WLAN port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	w_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	w_fq_hth	in-use free page count shmidt trigger high threshold for WLAN port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0

6:0	R/W	w_fq_lth	shmidt trigger low threshold.	7'd40

WLAN_port_flow_control_2 (offset:0x0828,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	w_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	w_int_time	interrupt for pause process and time out.	7'd64

WLAN_TX_queue_throttle_threshold (offset:0x082c,default:0x30303030)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	w_q3_thr	interrupt for w port queue3 pause process and time out.	7'd48
23	-	-	reserved	1'b0
22:16	R/W	w_q2_thr	interrupt for w port queue2 pause process and time out.	7'd48
15	-	-	reserved	1'b0
14:8	R/W	w_q1_thr	interrupt for w port queue1 pause process and time out.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	w_q0_thr	interrupt for w port queue0 pause process and time out.	7'd48

CPU_RX_port_flow_control_1 (offset:0x0830,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	cr_hth	in-use page count shmidt trigger high threshold for Cr port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	cr_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	cr_fq_hth	in-use free page count shmidt trigger high threshold for Cr port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	cr_fq_lth	shmidt trigger low threshold.	7'd40

CPU_RX_port_flow_control_2 (offset:0x0834,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	cr_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	cr_int_time	interrupt for pause process and time out.	7'd64

CPU_TX_port_flow_control_1 (offset:0x0838,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	ct_hth	in-use page count shmidt trigger high threshold for Ct port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	ct_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	ct_fq_hth	in-use free page count shmidt trigger high threshold for Ct port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	ct_fq_lth	shmidt trigger low threshold.	7'd40

CPU_TX_port_flow_control_2 (offset:0x083c,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	ct_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	ct_int_time	interrupt for pause process and time out.	7'd64

CPU_TX_queue_throttle_threshold (offset:0x0840,default:0x30303030)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	ct_q3_thr	interrupt for ct port queue3 pause process and time out.	7'd48
23	-	-	reserved	1'b0
22:16	R/W	ct_q2_thr	interrupt for ct port queue2 pause process and time out.	7'd48
15	-	-	reserved	1'b0
14:8	R/W	ct_q1_thr	interrupt for ct port queue1 pause process and time out.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	ct_q0_thr	interrupt for ct port queue0 pause process and time out.	7'd48

Host_port_flow_control_1 (offset:0x0844,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	h_hth	in-use page count shmidt trigger high threshold for host port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	h_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	h_fq_hth	in-use free page count shmidt trigger high threshold for host port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	h_fq_lth	g trigger low threshold.	7'd40

Host_port_flow_control_2 (offset:0x0848,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	h_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	h_int_time	interrupt for pause process and time out.	7'd64

Virtual_CPU_RX_port_flow_control_1 (offset:0x084c,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	vr_hth	in-use page count shmidt trigger high threshold for Vr port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	vr_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	vr_fq_hth	in-use free page count shmidt trigger high threshold for Vr port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	vr_fq_lth	shmidt trigger low threshold.	7'd40

Virtual_CPU_RX_port_flow_control_2 (offset:0x0850,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	vr_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	vr_int_time	interrupt for pause process and time out.	7'd64

Virtual_CPU_TX_port_flow_control_1 (offset:0x0854,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	vt_hth	in-use page count shmidt trigger high threshold for Vt port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	vt_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	vt_fq_hth	in-use free page count shmidt trigger high threshold for Vt port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	vt_fq_lth	shmidt trigger low threshold.	7'd40

Virtual_CPU_TX_port_flow_control_2 (offset:0x0858,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	vt_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	vt_int_time	interrupt for pause process and time out.	7'd64

Free0_page_port_flow_control_1 (offset:0x085c,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	f0_hth	in-use page count shmidt trigger high threshold for free page port.when there are too many to-be-processed pages, this port will pause the incoming port.	7'd96
23	-	-	reserved	1'b0
22:16	R/W	f0_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	f0_fq_hth	in-use free page count shmidt trigger high threshold for free page port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	f0_fq_lth	shmidt trigger low threshold.	7'd40

Free0_page_port_flow_control_2 (offset:0x0860,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	f0_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	f0_int_time	interrupt for pause process and time out.	7'd64

Free1_page_port_flow_control_1 (offset:0x0864,default:0x60402c28)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	f1_hth	in-use page count shmidt trigger high threshold for free page port.when	7'd96

			there are too many to-be-processed pages, this port will pause the incoming port.	
23	-	-	reserved	1'b0
22:16	R/W	f1_lth	shmidt trigger low threshold.	7'd64
15	-	-	reserved	1'b0
14:8	R/W	f1_fq_hth	in-use free page count shmidt trigger high threshold for free page port.when there are too few to-be-processed pages, this port will pause the incoming port.	7'd44
7	-	-	reserved	1'b0
6:0	R/W	f1_fq_lth	shmidt trigger low threshold.	7'd40

Free1_page_port_flow_control_2 (offset:0x0868,default:0x00003040)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	f1_int_pcnt	interrupt for page counter.	7'd48
7	-	-	reserved	1'b0
6:0	R/W	f1_int_time	interrupt for pause process and time out.	7'd64

virtual_cpu_port_next_page_query (offset:0x086c,default:0x00010000)

Bits	Type	Name	Description	Init Value
31:17	-	-	reserved	15'b0
16	RO	free_q_vld	virtual cpu port current free pages area can be allocated	1'b1
15	-	-	reserved	1'b0
14:8	R/W	qry_cur_pg	query next page number from this page number by writing this register.	7'b0
7	-	-	reserved	1'b0
6:0	RO	ret_nxt_pg	next page number	7'b0

virtual_cpu_port_memory_alloc (offset:0x0870,default:0x00000004)

Bits	Type	Name	Description	Init Value
31:16	-	-	reserved	16'b0
15	R/W	insert_after	let new page link after cur_end_pg_num	1'b0
14:8	R/W	cur_end_pg_num	if insert_after is high, free_pg_num will be the next page of the page specified in this field	7'b0
7	-	-	reserved	1'b0
6:0	RO	free_pg_num	virtual cpu port current front free page number. Be noted that the allocation is completed automatically when writing any field in this register. The number of the newly allocated page can be read out through this field. If the wish page is the front page of a newly dreated list, set insert_after as "L" with a don't care value of cur_end_pg_num.	7'h4

virtual_cpu_port_access_page (offset:0x0874,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:15	-	-	reserved	17'b0
14:8	R/W	read_acc_pg	virtual cpu port current access page number	7'b0
7	-	-	reserved	1'b0
6:0	R/W	write_acc_pg	virtual cpu port current access page number	7'b0

PSE_memory (offset:0x0880-0x08ff,default:unknown)

cpu direct access to PSE memory with read_acc_pg when read, with write_acc_pg when write

tx_virtual_cpu_port_input_queue_query (offset:0x0900,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:20	-	-	reserved	12'b0
19:16	RO	tx_Vi_q_vld	virtual cpu port current front page number is valid	4'b0
15	-	-	reserved	1'b0
14:8	RO	tx_Vi_front_pg	virtual cpu port current front page number	7'b0
7:2	-	-	reserved	6'b0

1:0	R/W	tx_Vi_q_id	write this queue ID to get the front page number of this queue	2'b0

tx_virtual_cpu_port_enqueue_control (offset:0x0904,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	tx_Ve_enq_pl_start	enqueue page list start.	7'b0
23	-	-	reserved	1'b0
22:16	R/W	tx_Ve_enq_pl_end	enqueue page list end.	7'b0
15	-	-	reserved	1'b0
14:8	R/W	tx_Ve_enq_pl_cnt	enqueue page list count.	7'b0
7:6	-	-	reserved	2'b0
5:3	R/W	tx_Ve_enq_pid	enqueue to which port.	3'b0
2:0	R/W	tx_Ve_enq_qid	enqueue to which queue. Be noted that the enqueuing is completed automatically when writing any field in this register.	3'b0

tx_virtual_cpu_port_dequeue_control (offset:0x0908,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	tx_Vi_deq_pl_start	dequeue page list start.	7'b0
23	-	-	reserved	1'b0
22:16	R/W	tx_Vi_deq_pl_end	dequeue page list end.	7'b0
15	-	-	reserved	1'b0
14:8	R/W	tx_Vi_deq_pl_cnt	dequeue page list count.	7'b0
7:2	-	-	reserved	6'b0
1	R/W	tx_Vi_deq_cnt_release	Only active at tx_Vi_deq_to_free_q=1'b0. Set high to release local page cnt.	1'b0
0	R/W	tx_Vi_deq_to_free_q	'1' to dequeue from the current queue and free the page list to the free queue; '0' to dequeue from the current queue and then cpu hold the memory pages (not belonging to any queue) for later enqueuing to tx virtual cpu port by writing to 'tx virtual cpu port enqueue control' register. Be noted that the dequeuing is completed automatically when writing any field in this register.	1'b0

rx_virtual_cpu_port_input_queue_query (offset:0x090c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:20	-	-	reserved	12'b0
19:16	RO	rx_Vi_q_vld	virtual cpu port current front page number is valid	4'b0
15	-	-	reserved	1'b0
14:8	RO	rx_Vi_front_pg	virtual cpu port current front page number	7'b0
7:2	-	-	reserved	6'b0
1:0	R/W	rx_Vi_qid	write this queue ID to get the front page number of this queue id	2'b0

rx_virtual_cpu_port_enqueue_control (offset:0x0910,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	rx_Ve_enq_pl_start	enqueue page list start.	7'b0
23	-	-	reserved	1'b0
22:16	R/W	rx_Ve_enq_pl_end	enqueue page list end.	7'b0
15	-	-	reserved	1'b0
14:8	R/W	rx_Ve_enq_pl_cnt	enqueue page list count.	7'b0
7:6	-	-	reserved	2'b0
5:3	R/W	rx_Ve_enq_pid	enqueue to which port.	3'b0
2:0	R/W	rx_Ve_enq_qid	enqueue to which queue. Be noted that the dequeuing is completed automatically when writing any field in this register.	3'b0

rx_virtual_cpu_port_dequeue_control (offset:0x0914,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	-	-	reserved	1'b0
30:24	R/W	rx_Vi_deq_pl_start	dequeue page list start.	7'b0
23	-	-	reserved	1'b0
22:16	R/W	rx_Vi_deq_pl_end	dequeue page list end.	7'b0
15	-	-	reserved	1'b0
14:8	R/W	rx_Vi_deq_pl_cnt	dequeue page list count.	7'b0
7:2	-	-	reserved	6'b0
1	R/W	rx_Vi_deq_cnt_release	Only active at rx_Vi_deq_to_free_q=1'b0. Set high to release local page cnt.	1'b0
0	R/W	rx_Vi_deq_to_free_q	'1' to dequeue from the current queue and free the page list to the free queue;'0' to dequeue from the current queue and then the cpu hold the memory pages (not belonging to any queue) for later enqueuing to rx virtual cpu port by writing to 'rx virtual cpu port enqueue control' register. Be noted that the dequeuing is completed automatically when writing any field in this register.	1'b0

tx_cpu_port_to_FCE_base_pointer (offset:0x0980,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	tx_ts_base_ptr	point to the base address of in "to switch descriptor" ring 0 (4-DWORD aligned address)	32'b0

tx_cpu_port_to_FCE_max_descriptor_count (offset:0x0984,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_ts_max_cnt	the maximum number of "to switch descriptor" count in "to switch descriptor" ring 0	8'b0

tx_cpu_port_to_FCE_cpu_descriptor_index (offset:0x0988,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_ts_ctx_idx	point to the next "to switch descriptor" that CPU wants to use	8'b0

tx_cpu_port_to_FCE_dma_descriptor_index (offset:0x098c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_ts_dtx_idx	point to the next "to switch descriptor" that DMA wants to use	8'b0

rx_cpu_port_to_FCE_base_pointer (offset:0x0990,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	rx_ts_base_ptr	point to the base address of in "to switch descriptor" ring 1 (4-DWORD aligned address)	32'b0

rx_cpu_port_to_FCE_max_descriptor_count (offset:0x0994,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_ts_max_cnt	the maximum number of "to switch descriptor" count in "to switch descriptor" ring 1	8'b0

rx_cpu_port_to_FCE_cpu_descriptor_index (offset:0x0998,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_ts_ctx_idx	point to the next "to switch descriptor" that CPU wants to use	8'b0

rx_cpu_port_to_FCE_dma_descriptor_index (offset:0x099c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_ts_dtx_idx	point to the next "to switch descriptor" that DMA wants to use	8'b0

tx_cpu_port_from_FCE_base_pointer (offset:0x09a0,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	tx_fs_base_ptr	point to the base address of in "from switch descriptor" ring 0 (4-DWORD aligned address)	32'b0

tx_cpu_port_from_FCE_max_descriptor_count (offset:0x09a4,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_fs_max_cnt	the maximum number of "from switch descriptor" count in "from switch descriptor" ring 0	8'b0

tx_cpu_port_from_FCE_cpu_descriptor_index (offset:0x09a8,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_fs_ctx_idx	point to the next "from switch descriptor" wants to use	8'b0

tx_cpu_port_from_FCE_dma_descriptor_index (offset:0x09ac,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	tx_fs_dtx_idx	point to the next "from switch descriptor" that DMA wants to use	8'b0

rx_cpu_port_from_FCE_base_pointer (offset:0x09b0,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W	rx_fs_base_ptr	point to the base address of in "from switch descriptor" ring 1 (4-DWORD aligned address)	32'b0

rx_cpu_port_from_FCE_max_descriptor_count (offset:0x09b4,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_fs_max_cnt	the maximum number of "from switch descriptor" count in "from switch descriptor" ring 1	8'b0

rx_cpu_port_from_FCE_cpu_descriptor_index (offset:0x09b8,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_fs_ctx_idx	point to the next "from switch descriptor" that CPU wants to use	8'b0

rx_cpu_port_from_FCE_dma_descriptor_index (offset:0x09bc,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	R/W	rx_fs_dtx_idx	point to the next "from switch descriptor" that DMA wants to use	8'b0

FCE_PDMA_information (offset:0x09c0,default:0x28000202)

Bits	Type	Name	Description	Init Value
31:28	RO	version	PDMA version	4'h2
27:24	RO	index_width	-	4'h8
23:16	RO	base_ptr_width	-	8'b0
15:8	RO	ts_ring_num	-	8'h2
7:0	RO	fs_ring_num	-	8'h2

FCE_PDMA_global_configuration (offset:0x09c4,default:0x40000040)

Bits	Type	Name	Description	Init Value
31	R/W	rx_2b_offset	-	1'b0
30	R/W	clkgate_byp	-	1'b1
29	R/W	byte_swap	-	1'b0
28:8	-	-	reserved	21'b0
7	R/W	big_endian	The endian mode selection. DMA applies the endian rule to convert payload and TS/FS FCEINFO. DMA won't apply endian rule to register or descriptor. '1' for big endian. '0' for little endian.	1'b0
6	R/W	tx_wb_ddone	'0' to disable TS_DMA writing back DDONE into TSD. '1' to enable TS_DMA writing back DDONE into TSD	1'b1

5:4	R/W		Reserve	2'b00
3	RO	fs_dma_busy	'1', FS_DMA is busy; '0', FS_DMA is not busy	1'b0
2	R/W	fs_dma_en	'1' to enable FS_DMA; '0' to disable FS_DMA (when disabled, FS_DMA will finish the current receiving packet, then stop.)	1'b0
1	RO	ts_dma_busy	'1' TS_DMA is busy '0', TS_DMA is not busy	1'b0
0	R/W	ts_dma_en	'1' to enable TS_DMA; '0' to disable TS_DMA (when disabled, TS_DMA will finish the current sending packet, then stop.)	1'b0

PDMA_reset_index (offset:0x09c8,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	R/W1C	pdma_rst_idx	reserved to zero	32'b0

Delay_Interrupt_Configuration (offset:0x09cc,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	ts_dly_int_en	\"1\" to enable TS delayed interrupt mechanism. \"0\" to disable TS delayed interrupt mechanism.	1'b0
30:24	R/W	ts_max_pint	Specify max number of pended interrupts. When the number of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TS_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
23:16	R/W	ts_max_ptime	Specified max pending time for the internal TS_DONE_INT0-1. When the pending time equal or grater TSMAX_PTIME x 20us or the number of pended TS_DONE_INT0-5 equal or grater than TSMAX_PINT (see above), an Final TS_DLY_INT is generated Set to 0 will disable pending interrupt time check	8'b0
15	R/W	fs_dly_int_en	\'1\' to enable FS delayed interrupt mechanism. \'0\' to disable FS delayed interrupt mechanism.	1'b0
14:8	R/W	fs_max_pint	Specified max number of pended interrupts.When the number of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final FS_DLY_INT is generated. Set to 0 will disable pending interrupt count check	7'b0
7:0	R/W	fs_max_ptime	Specified Max pending time for the internal FS_DONE_INT. When the pending time equal or grater FSMAX_PTIME x 20us or , the number of pended FS_DONE_INT equal or grater than FSMAX_PCNT (see above), an Final FS_DLY_INT is generated . Set to 0 will disable pending interrupt time check	8'b0

Reserved (offset:0x09d0,default:0x00000002)

Bits	Type	Name	Description	Init Value

PDMA_interrupt_status (offset:0x09e0,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W1C	fs_coherence_int	Ingress packet (packets come from FCE switch) DMA finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
30	R/W1C	fs_dly_int	Summary of the whole from FCE packet related interruptsWrite 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
29	R/W1C	ts_coherence_int	Egress packet (packets are forwarded to FCE switch) finds data coherent event when checking ddone bit. Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
28	R/W1C	ts_dly_int	Summary of the whole to FCE packet related interrupts Write 1 to clear the interrupt.	1'b0

			Read to get the raw interrupt status	
27	-	-	reserved	1'b0
26	R/W1C	pse_pause_too_long_int	PSE engine paused due to few FCE memory pages, see register "FCE flow control interrupr reason"	1'b0
25	R/W1C	virtual_port_rx_int	some packets are enqueued to virtual port when RX	1'b0
24	R/W1C	virtual_port_tx_int	some packets are enqueued to virtual port when TX	1'b0
23:18	-	-	reserved	6'b0
17	R/W1C	cr_fs_done_int	packet from wmac receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
16	R/W1C	ct_fs_done_int	packet from host receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
15:2	-	-	reserved	14'b0
1	R/W1C	cr_ts_done_int	packet to host receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0
0	R/W1C	ct_ts_done_int	packet to wmac receive interrupt Write 1 to clear the interrupt. Read to get the raw interrupt status	1'b0

PDMA_interrupt_enable (offset:0x09e8,default:0x00000000)

Bits	Type	Name	Description	Init Value
31	R/W	fs_coherence_int_en	enable Ingress packet coherent event when checking ddone bit.	1'b0
30	R/W	fs_dly_int_en	whole from FCE packet related interrupts enable	1'b0
29	R/W	ts_coherence_int_en	enable Egress packet coherent event when checking ddone bit	1'b0
28	R/W	ts_dly_int_en	whole to FCE packet related interrupts enable	1'b0
27	-	reserved	-	1'b0
26	R/W	pse_pause_too_long_int_en	PSE engine paused due to resources deadlock interrupt enable	1'b0
25	R/W	virtual_port_rx_int_en	when set to "H", issue an interrupt to embedded CPU when any ports enqueue packets to virtual port when RX	1'b0
24	R/W	virtual_port_tx_int_en	when set to "H", issue an interrupt to embedded CPU when any ports enqueue packets to virtual port when TX	1'b0
23:18	-	reserved	-	6'b0
17	R/W	cr_fs_done_int_en	from wmac receive packet interrupt enable	1'b0
16	R/W	ct_fs_done_int_en	from host receive packet interrupt enable	1'b0
15:8	-	reserved	-	8'b0
7:2	-	reserved	-	6'b0
1	R/W	cr_ts_done_int_en	to host transmit packet interrupt enable	1'b0
0	R/W	ct_ts_done_int_en	to wmac transmit packet interrupt enable	1'b0

Reserved (offset:0x0a00,default:0x00000000)

Bits	Type	Name	Description	Init Value

Reserved (offset:0x0a04,default:0x00000000)

Bits	Type	Name	Description	Init Value

Reserved (offset:0x0a08,default:0x00000000)

Bits	Type	Name	Description	Init Value

virtual_port_free_queue_page_count_snap_shot (offset:0x0a0c,default:0x0000007b)

Bits	Type	Name	Description	Init Value
31:8	-	-	reserved	24'b0
7:0	RO	pse_fq_pcnt	-	8'h7b

wmac_port_used_page_count_per_queue (offset:0x0a10,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	w_pse_qx_pcnt	-	32'b0

cpu_rx_port_used_page_count_per_queue (offset:0x0a14,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	cr_pse_qx_pcnt	-	32'b0

cpu_tx_port_used_page_count_per_queue (offset:0x0a18,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	ct_pse_qx_pcnt	-	32'b0

host_port_used_page_count_per_queue (offset:0x0a1c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	h_pse_qx_pcnt	-	32'b0

rx_virtual_cpu_port_used_page_count_per_queue (offset:0x0a20,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	vr_pse_qx_pcnt	-	32'b0

tx_virtual_cpu_port_used_page_count_per_queue (offset:0x0a24,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	vt_pse_qx_pcnt	-	32'b0

free0_port_used_page_count_per_queue (offset:0x0a28,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	f0_pse_qx_pcnt	-	32'b0

free1_port_used_page_count_per_queue (offset:0x0a2c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:0	RO	f1_pse_qx_pcnt	-	32'b0

per_port_total_used_page_count_1 (offset:0x0a30,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:24	RO	f1_pse_pcnt	total page count (include all queue) in f1 port	8'b0
23:16	RO	f0_pse_pcnt	total page count (include all queue) in f0 port	8'b0
15:8	RO	h_pse_pcnt	total page count (include all queue) in h port	8'b0
7:0	RO	w_pse_pcnt	total page count (include all queue) in w port	8'b0

per_port_total_used_page_count_2 (offset:0x0a34,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:24	RO	ct_pse_pcnt	total page count (include all queue) in ct port	8'b0
23:16	RO	cr_pse_pcnt	total page count (include all queue) in cr port	8'b0
15:8	RO	vt_pse_pcnt	total page count (include all queue) in vt port	8'b0
7:0	RO	vr_pse_pcnt	total page count (include all queue) in vr port	8'b0

per_port_pause_enable_control_1 (offset:0x0a38,default:0x0000000a)

Bits	Type	Name	Description	Init Value
31:24	R/W	f1_pause_en	enable which port can pause f1 port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00000000
23:16	R/W	f0_pause_en	enable which port can pause f0 port bit7: reserved bit6: f0 port bit5: vt port	8'b00000000

			bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	
15:8	R/W	h_pause_en	enable which port can pause h port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00000000
7:0	R/W	w_pause_en	enable which port can pause w port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00001010

per_port_pause_enable_control_2 (offset:0x0a3c,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:24	R/W	ct_pause_en	enable which port can pause ct port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00000000
23:16	R/W	cr_pause_en	enable which port can pause cr port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00000000
15:8	R/W	vt_pause_en	enable which port can pause vt port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port bit1: cr port bit0: w port	8'b00000000
7:0	R/W	vr_pause_en	enable which port can pause vr port bit7: reserved bit6: f0 port bit5: vt port bit4: vr port bit3: h port bit2: ct port	8'b00000000

			bit1: cr port bit0: w port	

Manual_pause_control (offset:0x0a40,default:0x00000000)

Bits	Type	Name	Description	Init Value
31:14	-	-	reserved	18'b0
13	R/W	free1_fs_pause	cpu can pause free port from-switch state machine to do diagnosis	1'b0
12	R/W	free0_fs_pause	cpu can pause free port from-switch state machine to do diagnosis	1'b0
11	R/W	H_fs_pause	cpu must pause h port from-switch state machine to get a free page	1'b0
10	R/W	ct_fs_pause	cpu can pause ct port from switch state machine to do diagnosis	1'b0
9	R/W	cr_fs_pause	cpu can pause cr port from-switch state machine to do diagnosis	1'b0
8	R/W	W_fs_pause	cpu must pause w port from-switch state machine to get a free page	1'b0
7:6	-	-	reserved	2'b0
5	R/W	free0_ts_pause	cpu can pause free port to-switch state machine to do diagnosis	1'b0
4	R/W	free1_ts_pause	cpu can pause free port to-switch state machine to do diagnosis	1'b0
3	R/W	H_ts_pause	cpu must pause h port to-switch state machine to get a free page	1'b0
2	R/W	ct_ts_pause	cpu can pause ct port to-switch state machine to do diagnosis	1'b0
1	R/W	cr_ts_pause	cpu can pause cr port to-switch state machine to do diagnosis	1'b0
0	R/W	W_ts_pause	cpu must pause w port to-switch state machine to get a free page	1'b0

Reserved (offset:0x0a64,default:0x0000007e)

Bits	Type	Name	Description	Init Value

Reserved (offset:0x0a68,default:0x00000028)

Bits	Type	Name	Description	Init Value

Reserved (offset:0x0a6c,default:0x00000003)

Bits	Type	Name	Description	Init Value

5.9 WLAN MAC registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE000_0000
Reserve	N/A
Andes firmware/TESTIF	0x0041_0000

5.9.1 MAC System configuration registers (offset:0x1000)

ASIC_VER_ID (offset:0x1000, default :0x7612_XXXX)

Bits	Type	Name	Description	Initial value
31:16	R	VER_ID	ASIC version ID	16'h7612
15:0	R		Reserved	16'hXXXX

MAC_SYS_CTRL (offset:0x1004, default :0x0000_0003)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15	R/W	DIS_VHT_MODE	Disable VHT Mode If enable "Disable VHT Mode," VHT downgrades to HT Mix Mode BW80 downgrades to BW40 MCS8/9 downgrades to MCS7	0
14:12	R/W	WLAN_ACT_MASK	Bit12: TX is reported as WLAN active Bit13: RX is reported as WLAN active Bit14: SIFS is reported as WLAN active 0: disable 1: enable	0
11:8	R/W		Reserve	0
7	R/W	RX_TS_EN	Write 32-bit hardware RX timestamp instead of (RXWI->RSSI), and write (RXWI->RSSI) instead of (RXWI->SNR). Note: For QA RX sniffer mode only. 1: enable 0: disable	0
6	R/W	WLAN_HALT_EN	Enable external WLAN halt control signal 1: enable 0: disable	0
5	R/W	PBF_LOOP_EN	Packet buffer loop back enable (TX->RX) 1: enable 0: disable	0
4	R/W	CONT_TX_TEST	Continuous TX production test; override MAC_RX_EN, MAC_TX_EN 1: enable 0: disable	0
3	R/W	MAC_RX_EN	MAC RX enable 1: enable 0: disable	0
2	R/W	MAC_TX_EN	MAC TX enable 1: enable 0: disable	0
~~1~~	~~R/W~~	~~BBP_HRST~~	~~BBP hard reset~~ ~~1: BBP in reset state 0: BBP in normal state~~ ~~Note: Whole BBP including BBP registers will be reset.~~ Move to 0x0064 bit[18] Reserved	~~1~~
0	R/W	MAC_SRST	MAC soft-reset	1

			1: MAC in reset state 0: MAC in normal state Note: MAC registers and tables will NOT be reset.	

Note: MAC hard-reset is outside the scope of MAC registers.

MAC_ADDR_DW0 (offset:0x1008, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	MAC_ADDR_3	MAC address byte3	0
23:16	R/W	MAC_ADDR_2	MAC address byte2	0
15:8	R/W	MAC_ADDR_1	MAC address byte1	0
7:0	R/W	MAC_ADDR_0	MAC address byte0	0

MAC_ADDR_DW1 (offset:0x100C, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	MAC_ADDR_5	MAC address byte5	0
7:0	R/W	MAC_ADDR_4	MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC_BSSID0_DW0 (offset:0x1010, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	BSSID0_3	BSSID0 byte3	0
23:16	R/W	BSSID0_2	BSSID0 byte2	0
15:8	R/W	BSSID0_1	BSSID0 byte1	0
7:0	R/W	BSSID0_0	BSSID0 byte0	0

MAC_BSSID0_DW1 (offset: 0x1014, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26:24	R/W	MULTI_BSSID_BYTE_SEL	Multiple BSSID index byte selection (only for New BSSID mode) 0: use MAC address byte0 bit[5:2] as BSSID index 1: use MAC address byte1 bit[3:0] as BSSID index 2: use MAC address byte2 bit[3:0] as BSSID index 3: use MAC address byte3 bit[3:0] as BSSID index 4: use MAC address byte4 bit[3:0] as BSSID index 5: use MAC address byte5 bit[3:0] as BSSID index	0
23	R/W	MULTI_BCN_NUM_B3	Multiple BSSID Beacon number bit3 Use together with MULTI_BCN_NUM	0
22	R/W	MULTI_BSSID_MODE_B2	Multiple BSSID mode bit2 Use together with MULT_BSSID_MODE	0
21	R/W	NEW_MULTI_BSSID_MODE	New multiple BSSID mode 0: disable, 1: enable When enabled, set MAC address byte0-bit1 to 1 as local administration bit for multiple BSSID addresses.	0

20:18	R/W	MULTI_BCN_NUM	Multiple BSSID Beacon number 0: one back-off beacon 1-7: SIFS-burst beacon count	0
17:16	R/W	MULTI_BSSID_MODE	Multiple BSSID mode In multiple-BSSID AP mode, BSSID shall be the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode. The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 as BSS index) 2: 4-BSSID mode (byte5.bit1:0 as BSS index) 3: 8-BSSID mode (byte5.bit2:0 as BSS index)	0
15:8	R/W	BSSID0_5	BSSID0 byte5	0
7:0	R/W	BSSID0_4	BSSID0 byte4	0

MAX_LEN_CFG (offset: 0x1018, default: 0x000A_7FFF)

Bits	Type	Name	Description	Initial value
31:22	R		Reserved	0
21:20	R/W	MAX_MPDU_LEN_EXT	Maximum MPDU length extension Use together with MAX_MPDU_LEN as MSB extension to represent a 14-bit maximum MPDU length.	0
19:16	R/W	MIN_MPDU_LEN	Minimum MPDU length (unit: bytes) MAC will drop the MPDU if the length is less than this limitation. Applied only in MAC RX.	10
15	R		Reserved	0
14:12	R/W	MAX_PSDU_LEN	Maximum PSDU length (power factor) 0: 2^13 = 8K bytes 1: 2^14 = 16K bytes 2: 2^15 = 32K bytes 3: 2^16 = 64K bytes 4: 2^17 = 128K bytes 5: 2^18 = 256K bytes 6: 2^18 = 512K bytes 7: 2^18 = 1024K bytes MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX.	7
11:0	R/W	MAX_MPDU_LEN	Maximum MPDU length (unit: bytes) MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.	4095

BBP_CSR_CFG (offset: 0x101C, default: 0x0008_0000)

~~Bits~~	~~Type~~	~~Name~~	~~Description~~	~~Initial value~~
~~31:20~~	~~R~~		~~Reserved~~	~~0~~
~~19~~	~~R/W~~	~~BBP_RW_MODE~~	~~BBP Register R/W mode~~ ~~1: parallel mode~~ ~~0: serial mode~~	~~1~~
~~18~~	~~R/W~~	~~BBP_PAR_DUR~~	~~BBP Register parallel R/W pulse width~~ ~~0: pulse width = 62.5ns~~ ~~1: pulse width = 112.5ns~~	~~0~~

			Note: Please set BBP_PAR_DUR=1 in 802.11J mode	
17	R/W	BBP_CSR_KICK	Write - kick BBP register read/write 0: do nothing 1: kick read/write process Read - Polling BBP register read/write progress 0: idle 1: busy	0
16	R/W	BBP_CSR_RW	0: Write 1: Read	0
15:8	R/W	BBP_ADDR	BBP register ID 0 for R0, 1 for R1, and so on.	0
7:0	R/W	BBP_DATA	Write - Data written to BBP Read - Data read from BBP	0

RF_CSR_CFG0 (offset: 0x1020, default: 0x1600_0000)

Bits	Type	Name	Description	Initial value
31	R/W	RF_REG_CTRL	Write: 1 - RF_REG0/1/2 to RF chip Read: 0 – idle, 1 - busy	0
30	R/W	RF_LE_SEL	RF_LE selection 0:RF_LE0 activate 1:RF_LE1 activate	0
29	R/W	RF_LE_STBY	RF_LE standby mode 0: RF_LE is high when standby 1: RF_LE is low when standby	0
28:24	R/W	RF_REG_WIDTH	RF register bit width	22
23:0	R/W	RF_REG_0	RF register0 ID and content	0

RF_CSR_CFG1 (offset: 0x1024, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	RF_DUR	Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycle (37.5usec) 1: 5 system clock cycle (62.5usec)	0
23:0	R/W	RF_REG_1	RF register1 ID and content	0

RF_CSR_CFG2 (offset: 0x1028, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:0	R/W	RF_REG_2	RF register2 ID and content	0

Note: Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

LED_CFG (offset: 0x102C, default: 0x0003_1E46)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	LED_POL	LED polarity 0: active low 1: active high	0
29:28	R/W	Y_LED_MODE	Yellow LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
27:26	R/W	G_LED_MODE (LED_RDYA_N)	Green LED mode 0: off 1: blinking upon TX	0

			2: periodic slow blinking 3: always on	
25:24	R/W	R_LED_MODE	Red LED mode 0: off 1: blinking upon TX 2: periodic slow blinking 3: always on	0
23:22	R		Reserved	0
21:16	R/W	SLOW_BLK_TIME	Slow blinking period (unit: 1sec)	3
15:8	R/W	LED_OFF_TIME	TX blinking off period (unit: 1ms)	30
7:0	R/W	LED_ON_TIME	TX blinking on period (unit: 1ms)	70

*MAC LED_CFG is unused function for LED mode

AMPDU_MAX_LEN_20M1S (offset: 0x1030, default: 0xffff_ffff)

Bits	Type	Name	Description	Initial value
31:28	R/W	AMPDU_MAX_BW20_MCS7	Maximum AMPDU for BW20 HT/VHT 1SS MCS7*	15
27:24	R/W	AMPDU_MAX_BW20_MCS6	Maximum AMPDU for BW20 HT/VHT 1SS MCS6*	15
23:20	R/W	AMPDU_MAX_BW20_MCS5	Maximum AMPDU for BW20 HT/VHT 1SS MCS5*	15
19:16	R/W	AMPDU_MAX_BW20_MCS4	Maximum AMPDU for BW20 HT/VHT 1SS MCS4*	15
15:12	R/W	AMPDU_MAX_BW20_MCS3	Maximum AMPDU for BW20 HT/VHT 1SS MCS3*	15
11:08	R/W	AMPDU_MAX_BW20_MCS2	Maximum AMPDU for BW20 HT/VHT 1SS MCS2*	15
07:04	R/W	AMPDU_MAX_BW20_MCS1	Maximum AMPDU for BW20 HT/VHT 1SS MCS1*	15
03:00	R/W	AMPDU_MAX_BW20_MCS0	Maximum AMPDU for BW20 HT/VHT 1SS MCS0*	15

Note1: Per MCS maximum A-MPDU length = 2^(AMPDU_MAX – 5) bytes, for example, set to 15 means maximum A-MPDU length is 1024KB

Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

Note3: BW40/80, HT MCS8-15, VHT 2SS is automatically double by hardware.

AMPDU_MAX_LEN_20M1S_256QAM (offset: 0x1034, default: 0x0000_0077)

Bits	Type	Name	Description	Initial value
31:08	R		Reserved	0
07:04	R/W	AMPDU_MAX_BW20_MCS9	Maximum AMPDU for BW20 VHT 1SS MCS9*	7
03:00	R/W	AMPDU_MAX_BW20_MCS8	Maximum AMPDU for BW20 VHT 1SS MCS8*	7

Note1: Per MCS maximum A-MPDU length = 2^(AMPDU_MAX – 5) bytes, for example, set to 15 means maximum A-MPDU length is 1024KB

Note2: The value applied together with 0x1018 MAX_PSDU_LEN.

Note3: BW40/80, VHT 2SS is automatically double by hardware.

Bits	Type	Name	Description	Initial value
31:07	R		Reserved	0
06	R/W	FORCE_BA_WINSIZE_EN	Enable forced BA window size over BA window size value in TXWI 0: disable, 1: enable	0
05:00	R/W	FORCE_BA_WINSIZE	Forced BA window size	0

AMPDU_BA_WINSIZE (offset: 0x1040, default: 0x0000_0000)

TX_AGG_GAP (offset: 0x1050, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:11	R		Reserved	0
10:0	R/W	AGG_GAP	A-MPDU Tx is gated until the time elapsed is longer than AGG_GAP and no more MPDU has arrived (unit : us)	0

TX_AGG_THRES (offset: 0x1054, default: 0x1000_4000)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0
29:24	R/W	AGG_NUM_THRES	A-MPDU Tx is gated until the MPDU frame number are larger than AGG_NUM_THRES	16
23:20	R		Reserved	0
19:0	R/W	AGG_LEN_THRES	A-MPDU Tx is gated until the A-MPDU byte length is larger than AGG_LEN_THRES (unit : byte)	16384

MAC_BSSID0_AID (offset:0x1060, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:12	R		Reserved	0
11:0	R/W	BSSID0_AID	AID of BSSID0	0

EXT_SYM_CFG (offset: 0x1064, default: 0x0000_0003)

Bits	Type	Name	Description	Initial value
31:0	R		Reserved	3

TX_WCID_DROP_MASK0 (offset: 0x106C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK0-31	Directly drop TX frame of specific WCID Bit0=WCID0, bit1=WCID1,… bit31=WCID31 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1070, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK32-63	Directly drop TX frame of specific WCID Bit0=WCID32, bit1=WCID33,… bit31=WCID63 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1074, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK64-95	Directly drop TX frame of specific WCID Bit0=WCID64, bit1=WCID65,… bit31=WCID95 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1078, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK96-127	Directly drop TX frame of specific WCID Bit0=WCID96, bit1=WCID97,… bit31=WCID127 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x107C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK128-159	Directly drop TX frame of specific WCID Bit0=WCID128, bit1=WCID129,… bit31=WCID159 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1080, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK160-191	Directly drop TX frame of specific WCID Bit0=WCID160, bit1=WCID161,… bit31=WCID191 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1084, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK192-223	Directly drop TX frame of specific WCID Bit0=WCID192, bit1=WCID193,… bit31=WCID223 0: disable, 1:enable	0

TX_WCID_DROP_MASK0 (offset: 0x1088, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	TX_WCID_DROP_MASK224-255	Directly drop TX frame of specific WCID Bit0=WCID224, bit1=WCID225,… bit31=WCID255 0: disable, 1:enable	0

TX_BCN_BYPASS_MASK (offset: 0x108C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R/W		Reserved	0
15:0	R/W	TX_BCN_DROP_MASK0-15	Directly bypass TX Beacon frame of specific Beacon Bit0=1st Beacon, bit1=2nd Beacon,… bit15=16th Beacon 0: disable, 1:enable	0

AP_CLIENT_BSSID0_L (offset: 0x1090, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID0_3	AP client BSSID0 byte3	0
23:16	R/W	APC_BSSID0_2	AP client BSSID0 byte2	0
15:8	R/W	APC_BSSID0_1	AP client BSSID0 byte1	0
7:0	R/W	APC_BSSID0_0	AP client BSSID0 byte0	0

AP_CLIENT_BSSID0_H (offset: 0x1094, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	APC_BSSID_EN	Enable AP client mode (occupy BSSIDX8-16 of multiple BSSID mode) 0: disable, 1:enable	0
15:8	R/W	APC_BSSID0_5	AP client BSSID0 byte5	0
7:0	R/W	APC_BSSID0_4	AP client BSSID0 byte4	0

AP_CLIENT_BSSID1_L (offset: 0x1098, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID1_3	AP client BSSID1 byte3	0
23:16	R/W	APC_BSSID1_2	AP client BSSID1 byte2	0
15:8	R/W	APC_BSSID1_1	AP client BSSID1 byte1	0
7:0	R/W	APC_BSSID1_0	AP client BSSID1 byte0	0

AP_CLIENT_BSSID1_H (offset: 0x109C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:	R/W	BSSID1_EN	Refer BSSID1 as my BSSID when AP-Cliend Mode is disabled 0: disable 1: enable	0
30:27	R		Reserved	0
26:16	R/W	BSSSID1_AID	AID of BSSID1	0
15:8	R/W	BSSID1_5	BSSID1 byte5	0
7:0	R/W	BSSID1_4	BSSID1 byte4	0

AP_CLIENT_BSSID2_L (offset: 0x10A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID2_3	AP client BSSID2 byte3	0
23:16	R/W	APC_BSSID2_2	AP client BSSID2 byte2	0
15:8	R/W	APC_BSSID2_1	AP client BSSID2 byte1	0
7:0	R/W	APC_BSSID2_0	AP client BSSID2 byte0	0

AP_CLIENT_BSSID2_H (offset: 0x10A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:	R/W	BSSID2_EN	Refer BSSID2 as my BSSID when AP-Cliend Mode is disabled 0: disable 1: enable	0
30:27	R		Reserved	
26:16	R/W	BSSSID2_AID	AID of BSSID2	0
15:8	R/W	BSSID2_5	BSSID2 byte5	0
7:0	R/W	BSSID2_4	BSSID2 byte4	0

AP_CLIENT_BSSID3_L (offset: 0x10A8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID3_3	AP client BSSID3 byte3	0
23:16	R/W	APC_BSSID3_2	AP client BSSID3 byte2	0
15:8	R/W	APC_BSSID3_1	AP client BSSID3 byte1	0
7:0	R/W	APC_BSSID3_0	AP client BSSID3 byte0	0

AP_CLIENT_BSSID3_H (offset: 0x10AC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID3_5	AP client BSSID3 byte5	0
7:0	R/W	APC_BSSID3_4	AP client BSSID3 byte4	0

AP_CLIENT_BSSID4_L (offset: 0x10B0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID4_3	AP client BSSID4 byte3	0
23:16	R/W	APC_BSSID4_2	AP client BSSID4 byte2	0
15:8	R/W	APC_BSSID4_1	AP client BSSID4 byte1	0
7:0	R/W	APC_BSSID4_0	AP client BSSID4 byte0	0

AP_CLIENT_BSSID4_H (offset: 0x10B4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID4_5	AP client BSSID4 byte5	0
7:0	R/W	APC_BSSID4_4	AP client BSSID4 byte4	0

AP_CLIENT_BSSID5_L (offset: 0x10B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID5_3	AP client BSSID5 byte3	0
23:16	R/W	APC_BSSID5_2	AP client BSSID5 byte2	0
15:8	R/W	APC_BSSID5_1	AP client BSSID5 byte1	0
7:0	R/W	APC_BSSID5_0	AP client BSSID5 byte0	0

AP_CLIENT_BSSID5_H (offset: 0x10BC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID5_5	AP client BSSID5 byte5	0
7:0	R/W	APC_BSSID5_4	AP client BSSID5 byte4	0

AP_CLIENT_BSSID6_L (offset: 0x10C0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID6_3	AP client BSSID6 byte3	0
23:16	R/W	APC_BSSID6_2	AP client BSSID6 byte2	0
15:8	R/W	APC_BSSID6_1	AP client BSSID6 byte1	0
7:0	R/W	APC_BSSID6_0	AP client BSSID6 byte0	0

AP_CLIENT_BSSID6_H (offset: 0x10C4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	APC_BSSID6_5	AP client BSSID6 byte5	0
7:0	R/W	APC_BSSID6_4	AP client BSSID6 byte4	0

AP_CLIENT_BSSID7_L (offset: 0x10C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	APC_BSSID7_3	AP client BSSID7 byte3	0
23:16	R/W	APC_BSSID7_2	AP client BSSID7 byte2	0
15:8	R/W	APC_BSSID7_1	AP client BSSID7 byte1	0
7:0	R/W	APC_BSSID7_0	AP client BSSID7 byte0	0

AP_CLIENT_BSSID7_H (offset: 0x10CC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value

31:16	R		Reserved	0
15:8	R/W	APC_BSSID7_5	AP client BSSID7 byte5	0
7:0	R/W	APC_BSSID7_4	AP client BSSID7 byte4	0

Reserve (offset: 0x10D0, default: 0x04E2_00FA)

Reserve (offset: 0x10D4, default: 0x0010_D3FF)

5.9.2 MAC Timing Control Registers (offset:0x1100)

XIFS_TIME_CFG (offset:0x1100, default :0x33A4_100A)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	
29	R/W	BB_RXEND_EN	BB_RX_END signal enable Refer BB_RX_END signal from BBP RX logic to start SIFS defer. 0: disable 1: enable	1
28:20	R/W	EIFS_TIME	EIFS time (unit: 1us) EIFS is the defer time after reception of a CRC error packet. After deferring EIFS, the normal back-off process may proceed.	314
19:16	R/W	OFDM_XIFS_TIME	Delayed OFDM SIFS time compensator (unit: 1us) When BB_RX_END from BBP is a delayed version the SIFS deferred will be (OFDM_SIFS_TIME - OFDM_XIFS_TIME)	4
15:8	R/W	OFDM_SIFS_TIME	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_TIME	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note1: EIFS = SIFS + ACK @ 1Mbps + DIFS = 10us (SIFS) + 192us (long preamble) + 14*8us (ACK) + 50us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

Note2: EIFS is not applied if MAC is a TXOP initiator that owns the channel.

Note3: EIFS is not started if AMPDU is only partial corrupted.

Caution: It is recommended that both (CCK_SIFS_TIME) and (OFDM_SIFS_TIME) are no less than TX/RX transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF_SLOT_CFG (offset:0x1104, default : 0x0000_0214)

Bits	Type	Name	Description	Initial value
31:12	R/W		Reserved	
11:8	R/W	CC_DELAY_TIME	Channel clear delay (unit: 1-us) This value specifies TX guard time after channel is clear.	2
7:0	R/W	SLOT_TIME	Slot time (unit: 1-us) This value specifies the slot boundary after deferring SIFS time. Note: Default 20us is for 11b/g. 11a and 11g-short-slot-mode	20

			is 9us.	

NAV_TIME_CFG (offset:0x1108, default :0x0000_8000)

Bits	Type	Name	Description	Initial value
31	W1C	NAV_UPD	NAV timer manual update command 0: Do nothing 1: Update NAV timer with NAV_UPD_VAL	0
30:16	R/W	NAV_UPD_VAL	NAV timer manual update value (unit: 1us)	0
15	R/W	NAV_CLR_EN	NAV timer auto-clear enable When enabled, MAC will auto clear NAV timer after the reception of CF-End frame from previous NAV holder STA. 0: disable 1: enable	1
14:0	R	NAV_TIMER	NAV timer (unit: 1us) The timer is set by other STA and will auto countdown to zero. The STA who set the NAV timer is called the NAV holder. When NAV timer is nonzero, MAC will not send any packet.	0

CH_TIME_CFG (offset:0x110C, default: 0x0000_001E)

Bits	Type	Name	Description	Initial value
31:12	R		Reserved	0
11:10	R/W	MDRDY_CNT_CLR_CFG	Media Ready Counter Clear Config 0: No Clear 1: Read Clear 2:Write Clear 3:Reserved	0
9:8	R/W	CH_TIMER_CLR_CFG	Channel Busy/Idle Timer Clear Config 0: No Clear 1: Read Clear 2:Write Clear 3:Reserved	0
7	R		Reserved	0
6	R/W	CCA_RC_EN	CCA Timer auto clear when register read. 0: disable 1: enable	0
5	R/W	MDRDY_CNT_EN	Media Ready Counter, up count while receiving 802.11 frame. 0: disable 1: enable	0
4	R/W	EIFS_AS_CH_BUSY	Count EIFS as channel busy 0: disable 1: enable	1
3	R/W	NAV_AS_CH_BUSY	Count NAV as channel busy 0: disable 1: enable	1
2	R/W	RX_AS_CH_BUSY	Count RX busy as channel busy 0: disable 1: enable	1
1	R/W	TX_AS_CH_BUSY	Count TX busy as channel busy 0: disable 1: enable	1
0	R/W	CH_STA_TIMER_EN	Channel statistic timer enable 0: disable 1: enable	0

PBF_LIFE_TIMER (offset:0x1110, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	PBF_LIFE_TIMER	TX/RX MPDU timestamp timer (free run) Unit: 1us	0

BCN_TIME_CFG (offset:0x1114, default: 0x00000640)

Bits	Type	Name	Description	Initial value
31:24	R/W	TSF_INS_COMP	TSF insertion compensation value (unit: 1us) When inserting TSF, add this value with local TSF timer as the TX timestamp.	0

23:21	R		Reserved	0
20	R/W	BCN_TX_EN	BEACON frame TX enable When enabled, MAC sends BEACON frame at TBTT interrupt. 0: disable 1: enable	0
19	R/W	TBTT_TIMER_EN	TBTT timer enable When enabled, TBTT interrupt will be issued periodically with period specified in (BCN_INTVAL). 0: disable 1: enable	0
18:17	R/W	TSF_SYNC_MODE	Local 64-bit TSF timer synchronization mode 00: disable 01: (STA infra-structure mode) Upon the reception of BEACON frame from associated BSS, local TSF is always updated with remote TSF. 10: (STA ad-hoc mode) Upon the reception of BEACON frame from associated BSS, local TSF is updated with remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) SYNC with nobody	0
16	R/W	TSF_TIMER_EN	Local 64-bit TSF timer enable When enabled, TSF timer will re-start from zero. 0: disable 1: enable	0
15:0	R/W	BCN_INTVAL	BEACON interval (unit: 64us) This value specified the interval between Maximum beacon interval is about 4sec.	1600

TBTT_SYNC_CFG (offset:0x1118, default: 0x0042_2010)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:20	R/W	BCN_CWMIN	Beacon transmission CWMIN after TBTT interrupt (unit: slot)	4
19:16	R/W	BCN_AIFSN	Beacon transmission AIFSN after TBTT interrupt (unit: slot)	2
15:8	R/W	BCN_EXP_WIN	Beacon expecting window duration (unit: 64us) The window starts from TBTT interrupt. The phase of “TBTT interrupt train” will NOT be adjusted by the beacon arrived within the window.	32
7:0	R/W	TBTT_ADJUST	IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us. In IBSS mode (Ad hoc), if consecutive TX beacon failures (or consecutive success) happened, TBTT timer will adjust it phase to meet the external Ad hoc TBTT time.	16

TX_TSF_TIMER_DW0 (offset:0x111C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	TX_TSF_TIMER_DW0	Local TX TSF timer LSB 32 bits (unit: 1us)	0

TX_TSF_TIMER_DW1 (offset:0x1120, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	TX_TSF_TIMER_DW1	Local TX TSF timer MSB 32 bits (unit: 1us)	0

TBTT_TIMER (offset:0x1124, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16:0	R	TBTT_TIMER	TBTT Timer (unit: 64us) The time remains till next TBTT. When TBTT_TIMER_EN is enabled, the timer will down count	0

			from BCN_INTVAL to zero. When TBTT_TIMER_EN is disabled, the timer will stay in zero.	

INT_TIMER_CFG (offset:0x1128, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R/W	GP_TIMER	Period of general purpose interrupt timer (Unit: 64us)	0
15:0	R/W	PRE_TBTT_TIMER	Pre-TBTT interrupt time (unit: 64us) The value specified the interrupt timing before TBTT interrupt.	0

INT_TIMER_EN (offset:0x112C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31	R/W	TBTT_EARLY_ADJ_EN	Auto-adjust TBTT while the BSS0 Beacon is received beyond expected window. 0: disable 1: enable	0
30:28	R		Reserved	0
27:16	R/W	TBTT_EARLY_ADJ_TIME	While the BSS0 Beacon is received beyond expected window. Adjust the TBTT ahead of TBTT_EARLT_ADJ_TIME of this Beacon. (unit: 1us)	0
15:2	R		Reserved	0
1	R/W	GP_TIMER_EN	Periodic general purpose interrupt timer enable 0: disable 1: enable	0
0	R/W	PRE_TBTT_INT_EN	Pre-TBTT interrupt enable 0: disable 1: enable	0

CH_IDLE_STA (offset:0x1130, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	RC	CH_IDLE_TIME	Channel idle time (unit: 1us)	0

In application, the channel busy time can be derived by the equation:

CH_BUSY_TIME = host polling period – CH_IDLE_TIME

CH_BUSY_STA (offset:0x1134, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/RC	CH_BUSY_TIME	Channel busy time (unit: 1us)	0

EXT_CH_BUSY_STA (offset:0x1138, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/RC	EXT_CH_BUSY_TIME	Extension Channel busy time (unit: 1us)	0

BBP_IPI_TIMER (offset:0x113C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	BBP_IPI_KICK	Write 1: Kick-off the measurement of BBP IPI Read 1: BBP IPI enabled, 0: BBP IPI disabled	0
15:0	R/W	BBP_IPI_TIMER	Measurement period of BBP IPI (unit: 1.024ms)	0

ED_CCA_TIMER (offset:0x1140, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/RC	ED_PD_CCA_TIMER	Primary ED/PD CCA Channel busy time (unit: 1us)	0

MDRDY_CNT (offset:0x1144, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/RC	MDRDY_CNT	Media Ready Counter, up count while receiving 802.11	0

			frame.	

TBTT2RXBCN0_Timer (offset:0x1148, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31	R/W	TBTT2RXBCN0_EN	Enable TBTT2RXBCN TIMER	0
30:18	R		Reserved	0
17:0	R	TBTT2RXBCN TIMER	Timer interval between BSS0 TBTT to Beacon received (unit : us)	0

TSF_CTRL (offset:0x114C, default: 0x0000_0080)

Bits	Type	Name	Description	Initial value
31:8	R		Reserved	0
7	R/W	TXRX0_TSF_BSS_SYNC	Local TX TSF Sync with RX0 TSF when the TSF_SYNC_MODE is set to STA infra-structure mode. 0: disable 1: enable	1
6	R/W	PRBRSP_UPD_TSF2_EN	When receives probe response from BSS2, update Rx2 TSF 0: disable 1: enable	0
5	R/W	PRBRSP_UPD_TSF1_EN	When receives probe response from BSS1, update Rx1 TSF 0: disable 1: enable	0
4	R/W	PRBRSP_UPD_TSF0_EN	When receives probe response from BSS0, update Rx0 TSF 0: disable 1: enable	0
3	R		Reserved	0
2	R/W	RX2_TSF_TIMER_EN	Local 64-bit Rx2 TSF timer enable When enabled, Rx2 TSF timer will re-start from zero. 0: disable 1: enable	0
1	R/W	RX1_TSF_TIMER_EN	Local 64-bit Rx1 TSF timer enable When enabled, Rx2 TSF timer will re-start from zero. 0: disable 1: enable	0
0	R/W	RX0_TSF_TIMER_EN	Local 64-bit Rx0 TSF timer enable When enabled, Rx2 TSF timer will re-start from zero. 0: disable 1: enable	0

RX0_TSF_TIMER_DW0 (offset:0x1150, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX0_TSF_TIMER_DW0	Local Rx0 TSF timer LSB 32 bits (unit: 1us)	0

RX0_TSF_TIMER_DW1 (offset:0x1154, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX0_TSF_TIMER_DW1	Local Rx0 TSF timer MSB 32 bits (unit: 1us)	0

RX1_TSF_TIMER_DW0 (offset:0x1158, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX1_TSF_TIMER_DW0	Local Rx1 TSF timer LSB 32 bits (unit: 1us)	0

RX1_TSF_TIMER_DW1 (offset:0x115C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX1_TSF_TIMER_DW1	Local Rx1 TSF timer MSB 32 bits (unit: 1us)	0

RX2_TSF_TIMER_DW0 (offset:0x1160, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX2_TSF_TIMER_DW0	Local Rx2 TSF timer LSB 32 bits (unit: 1us)	0

RX2_TSF_TIMER_DW1 (offset:0x1164, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	RX2_TSF_TIMER_DW1	Local Rx2 TSF timer MSB 32 bits (unit: 1us)	0

TIM_CTRL (offset:0x1180, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R	Reserved		
15	R/W	EN_TIM7DCNT	Enable TIM7_DCNT 1'b1: TIM7 OFFSET down counts when TIM7 event happens 1'b0: TIM7 OFFSET doesn't down count when TIM7 event happens	0
14	R/W	EN_TIM6DCNT	Enable TIM6_DCNT 1'b1: TIM6 OFFSET down counts when TIM6 event happens 1'b0: TIM6 OFFSET doesn't down count when TIM6 event happens	0
13	R/W	EN_TIM5DCNT	Enable TIM5_DCNT 1'b1: TIM5 OFFSET down counts when TIM5 event happens 1'b0: TIM5 OFFSET doesn't down count when TIM5 event happens	0
12	R/W	EN_TIM4DCNT	Enable TIM4_DCNT 1'b1: TIM4 OFFSET down counts when TIM4 event happens 1'b0: TIM4 OFFSET doesn't down count when TIM4 event happens	0
11	R/W	EN_TIM3DCNT	Enable TIM3_DCNT 1'b1: TIM3 OFFSET down counts when TIM3 event happens 1'b0: TIM3 OFFSET doesn't down count when TIM3 event happens	0
10	R/W	EN_TIM2DCNT	Enable TIM2_DCNT 1'b1: TIM2 OFFSET down counts when TIM2 event happens 1'b0: TIM2 OFFSET doesn't down count when TIM2 event happens	0
9	R/W	EN_TIM1DCNT	Enable TIM1_DCNT 1'b1: TIM1 OFFSET down counts when TIM1 event happens 1'b0: TIM1 OFFSET doesn't down count when TIM1 event happens	0
8	R/W	EN_TIM0DCNT	Enable TIM0_DCNT 1'b1: TIM0 OFFSET down counts when TIM0 event happens 1'b0: TIM0 OFFSET doesn't down count when TIM0 event happens	0
7	R/W	EN_TIM7	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
6	R/W	EN_TIM6	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
5	R/W	EN_TIM5	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
4	R/W	EN_TIM4	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
3	R/W	EN_TIM3	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
2	R/W	EN_TIM2	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0
1	R/W	EN_TIM1	Enable TIM0	0

Bits	Type	Name	Description	Initial value
31	R/W	TBTT_TIMER1_EN	TBTT timer1 enable When enabled, TBTT1 interrupt will be issued periodically with period specified in (BCN1_INTVAL). 0: disable	0
30	R/W	PRE_TBTT1_INT_EN	Pre-TBTT1 interrupt enable 0: disable 1: enable	0
29	R/W	TBTT1_EARLY_ADJ_EN	Auto-adjust TBTT1 while the BSS1 Beacon is received beyond expected window. 0: disable 1: enable	0
28	R/W	TBTT2RXBCN1_EN	Enable TBTT2RXBCN1 TIMER 0: disable 1: enable	0
27:24	R		Reserved	0
23:16	R/W	BCN1_EXP_WIN	BSS1 Beacon expecting window duration (unit: 64us)	00

			1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	
0	R/W	EN_TIM0	Enable TIM0 1'b1: kick TIM0 frame when tim0_offset 1'b0: doesn't kick TIM0 frame when tim0_offset	0

TIM_OFFSET01 (offset:0x1184, default: 0x00000)

Bits	Type	Name	Description	Initial value
31:16	R	TIM1_OFFSET	Offset between TIM1 and TBTT(unit: us)	0
15:0	R/W	TIM0_OFFSET	Offset between TIM0 and TBTT(unit: us)	0

TIM_OFFSET23 (offset:0x1188, default: 0x00000)

Bits	Type	Name	Description	Initial value
31:16	R	TIM3_OFFSET	Offset between TIM3 and TBTT(unit: us)	0
15:0	R/W	TIM2_OFFSET	Offset between TIM2 and TBTT(unit: us)	0

TIM_OFFSET45 (offset:0x118C, default: 0x00000)

Bits	Type	Name	Description	Initial value
31:16	R	TIM5_OFFSET	Offset between TIM5 and TBTT(unit: us)	0
15:0	R/W	TIM4_OFFSET	Offset between TIM4 and TBTT(unit: us)	0

TIM_OFFSET67 (offset:0x1190, default: 0x00000)

Bits	Type	Name	Description	Initial value
31:16	R	TIM7_OFFSET	Offset between TIM7 and TBTT(unit: us)	0
15:0	R/W	TIM6_OFFSET	Offset between TIM6 and TBTT(unit: us)	0

TBTT1_TIME_CFG (offset:0x1194, default: 0x00000)

			The window starts from TBTT1 interrupt. The phase of "TBTT1 interrupt train" will NOT be adjusted by the beacon arrived within the window.	
15:0	R/W	BCN1_INTVAL	BSS1 BEACON interval (unit: 64us) This value specified the interval between Maximum beacon interval is about 4sec.	00

INT_TIMER_CFG (offset:0x1198, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	PRE_TBTT1_TIMER	Pre-TBTT 1interrupt time (unit: 64us) The value specified the interrupt timing before TBTT1 interrupt.	0

INT1_TIMER_EN (offset:0x119C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
30:12	R		Reserved	0
11:0	R/W	TBTT_EARLY_ADJ_TIME	While the BSS1 Beacon is received beyond expected window. Adjust the TBTT ahead of TBTT1_EARLT_ADJ_TIME of this Beacon. (unit: 1us)	0

TBTT2RXBCN1_Timer (offset:0x11A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:18	R		Reserved	0
17:0	R	TBTT2RXBCN1 TIMER	Timer interval between BSS1 TBTT to Beacon received (unit : us)	0

TBTT1_TIMER (offset:0x11A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16:0	R	TBTT1_TIMER	TBTT1 Timer (unit: 64us) The time remains till next BSS1 TBTT. When TBTT1_TIMER_EN is enabled, the timer will down count from BCN1_INTVAL to zero. When TBTT1_TIMER_EN is disabled, the timer will stay in zero.	0

5.9.3 MAC Power save configuration registers (offset:0x1200)

MAC_STATUS_REG (offset:0x1200, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R	RX_STATUS	RX status 0: Idle 1: Busy	0
0	R	TX_STATUS	TX status 0: Idle 1: Busy	0

PWR_PIN_CFG (offset:0x1204, default: 0x0000_000A)

Bits	Type	Name	Description	Initial value
31:4	R		Reserved	0
3	R/W	IO_ADDA_PD	AD/DA power down	1
2	R/W	IO_PLL_PD	PLL power down (obsolete, no function)	0
1	R/W	IO_RA_PE	RA_PE (obsolete, no function)	1

0	R/W	IO_RF_PE	RF_PE (obsolete, no function)	0

AUTO_WAKEUP_CFG (offset:0x1208, default: 0x0000_0014)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15	R/W	AUTO_WAKEUP_EN	Auto wakeup interrupt enable Auto wakeup interrupt will be issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target TBTT. 0: disable 1: enable Note: Please make sure TBTT_TIMER_EN is enabled.	0
14:8	R/W	SLEEP_TBTT_NUM	Number of sleeping TBTT	0
7:0	R/W	WAKEUP_LEAD_TIME	Auto wakeup lead time (unit: 1TU=1024us)	20

AUX_CLK _CFG (offset: 0x120C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:1	R		Reserved	0
0	R/W	AUX_CLK_EN	Aux Clock enable 0: disable, 1: enable	0

MIMO_PS_CFG (offset: 0x1210, default: 0x0000_0002)

Bits	Type	Name	Description	Initial value
31:5	R		Reserved	0
4	R/W	RX_STBY_POL	RF RX standby polarity 0: high active, 1: low active	0
3	R/W	MMPS_RF_EN	RF MIMO power save mode 0: disable, 1: enable	0
2:1	R/W	MMPS_RX_ANT_NUM	Number of RX antenna in MIMO power save mode 0 : 1R. 1: 2R. 2,3 : Reserved.	1
0	R/W	MMPS_BB_EN	BB MIMO power save mode 0: disable, 1: enable	0

BB_PA_MODE_CFG0 (offset: 0x1214, default: 0x0100_55ff)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0x0
29:28	R/W	BB_PA_MODE_VHT1SS/2SS 9	Defined as the note below	0x0
27:26	R/W	BB_PA_MODE_VHT1SS/2SS 8	Defined as the note below	0x0
25:24	R/W	BB_PA_MODE_MCS32	Defined as the note below	0x1
23:22	R/W	BB_PA_MODE_OFDM54	Defined as the note below	0x0
21:20	R/W	BB_PA_MODE_OFDM48	Defined as the note below	0x0
19:18	R/W	BB_PA_MODE_OFDM36	Defined as the note below	0x0
17:16	R/W	BB_PA_MODE_OFDM24	Defined as the note below	0x0
15:14	R/W	BB_PA_MODE_OFDM18	Defined as the note below	0x1
13:12	R/W	BB_PA_MODE_OFDM12	Defined as the note below	0x1
11:10	R/W	BB_PA_MODE_OFDM9	Defined as the note below	0x1
9:8	R/W	BB_PA_MODE_OFDM6	Defined as the note below	0x1
7:6	R/W	BB_PA_MODE_CCK11	Defined as the note below	0x3
5:4	R/W	BB_PA_MODE_CCK5	Defined as the note below	0x3

3:2	R/W	BB_PA_MODE_CCK2	Defined as the note below	0x3
1:0	R/W	BB_PA_MODE_CCK1	Defined as the note below	0x3

Note: 00 – OFDM EVM limited, 01 – OFDM Mask limited, 10 – CCK EVM limited, 11 – CCK Mask limited

BB_PA_MODE_CFG1 (offset: 0x1218, default: 0x0055_0055)

Bits	Type	Name	Description	Initial value
31:30	R/W	BB_PA_MODE_HT15 / VHT2SS 7	Defined as the note below	0x0
29:28	R/W	BB_PA_MODE_HT14 / VHT2SS 6	Defined as the note below	0x0
27:26	R/W	BB_PA_MODE_HT13 / VHT2SS 5	Defined as the note below	0x0
25:24	R/W	BB_PA_MODE_HT12 / VHT2SS 4	Defined as the note below	0x0
23:22	R/W	BB_PA_MODE_HT11 / VHT2SS 3	Defined as the note below	0x1
21:20	R/W	BB_PA_MODE_HT10/ VHT2SS 2	Defined as the note below	0x1
19:18	R/W	BB_PA_MODE_HT 9 / VHT2SS 1	Defined as the note below	0x1
17:16	R/W	BB_PA_MODE_HT 8 / VHT2SS 0	Defined as the note below	0x1
15:14	R/W	BB_PA_MODE_HT 7 / VHT1SS 7	Defined as the note below	0x0
13:12	R/W	BB_PA_MODE_HT 6 / VHT1SS 6	Defined as the note below	0x0
11:10	R/W	BB_PA_MODE_HT 5 / VHT1SS 5	Defined as the note below	0x0
9:8	R/W	BB_PA_MODE_HT 4 / VHT1SS 4	Defined as the note below	0x0
7:6	R/W	BB_PA_MODE_HT 3 / VHT1SS 3	Defined as the note below	0x1
5:4	R/W	BB_PA_MODE_HT 2 / VHT1SS 2	Defined as the note below	0x1
3:2	R/W	BB_PA_MODE_HT 1 / VHT1SS 1	Defined as the note below	0x1
1:0	R/W	BB_PA_MODE_HT 0/ VHT1SS 0	Defined as the note below	0x1

Note: 00 – OFDM EVM limited, 01 – OFDM Mask limited, 10 – CCK EVM limited, 11 – CCK Mask limited

RF_PA_MODE_CFG0 (offset: 0x121C, default: 0x0100_55ff)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0x0
29:28	R/W	RF_PA_MODE_VHT1SS/2SS 9	Defined as the note below	0x0
27:26	R/W	RF_PA_MODE_VHT1SS/2SS 8	Defined as the note below	0x0
25:24	R/W	RF_PA_MODE_MCS32	Defined as the note below	0x1
23:22	R/W	RF_PA_MODE_OFDM54	Defined as the note below	0x0
21:20	R/W	RF_PA_MODE_OFDM48	Defined as the note below	0x0
19:18	R/W	RF_PA_MODE_OFDM36	Defined as the note below	0x0
17:16	R/W	RF_PA_MODE_OFDM24	Defined as the note below	0x0
15:14	R/W	RF_PA_MODE_OFDM18	Defined as the note below	0x1
13:12	R/W	RF_PA_MODE_OFDM12	Defined as the note below	0x1
11:10	R/W	RF_PA_MODE_OFDM9	Defined as the note below	0x1
9:8	R/W	RF_PA_MODE_OFDM6	Defined as the note below	0x1
7:6	R/W	RF_PA_MODE_CCK11	Defined as the note below	0xf
5:4	R/W	RF_PA_MODE_CCK5	Defined as the note below	0xf
3:2	R/W	RF_PA_MODE_CCK2	Defined as the note below	0xf
1:0	R/W	RF_PA_MODE_CCK1	Defined as the note below	0xf

Note: 00 – OFDM EVM limited, 01 – OFDM Mask limited, 10 – CCK EVM limited, 11 – CCK Mask limited

RF_PA_MODE_CFG1 (offset: 0x1220, default: 0x0055_0055)

Bits	Type	Name	Description	Initial

				value
31:30	R/W	RF_PA_MODE_HT15 / VHT2SS 7	Defined as the note below	0x0
29:28	R/W	RF_PA_MODE_HT14 / VHT2SS 6	Defined as the note below	0x0
27:26	R/W	RF_PA_MODE_HT13 / VHT2SS 5	Defined as the note below	0x0
25:24	R/W	RF_PA_MODE_HT12 / VHT2SS 4	Defined as the note below	0x0
23:22	R/W	RF_PA_MODE_HT11 / VHT2SS 3	Defined as the note below	0x1
21:20	R/W	RF_PA_MODE_HT10 / VHT2SS 2	Defined as the note below	0x1
19:18	R/W	RF_PA_MODE_HT 9 / VHT2SS 1	Defined as the note below	0x1
17:16	R/W	RF_PA_MODE_HT 8 / VHT2SS 0	Defined as the note below	0x1
15:14	R/W	RF_PA_MODE_HT 7 / VHT1SS 7	Defined as the note below	0x0
13:12	R/W	RF_PA_MODE_HT 6 / VHT1SS 6	Defined as the note below	0x0
11:10	R/W	RF_PA_MODE_HT 5 / VHT1SS 5	Defined as the note below	0x0
9:8	R/W	RF_PA_MODE_HT 4 / VHT1SS 4	Defined as the note below	0x0
7:6	R/W	RF_PA_MODE_HT 3 / VHT1SS 3	Defined as the note below	0x1
5:4	R/W	RF_PA_MODE_HT 2 / VHT1SS 2	Defined as the note below	0x1
3:2	R/W	RF_PA_MODE_HT 1 / VHT1SS 1	Defined as the note below	0x1
1:0	R/W	RF_PA_MODE_HT 0/ VHT1SS 0	Defined as the note below	0x1

Note: 00 – OFDM EVM limited, 01 – OFDM Mask limited, 10 – CCK EVM limited, 11 – CCK Mask limited

FAST_CH_SW (offset: 0x1224, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:28	R	Reserved		0x0
27:8	R/W		Reserve	0x0
7:3	R	Reserved		0x0
1	R/W	SW_UNLOCK_REQ	1’b1: PBF unlocks on-going packets and PBF does not dequeue this packet. Auto clear after write.	1’b0
0	R/W	FORCE_PS	1’b1 : force ps bit to 1’b1 of all packets in out queue	1’b0

PAMODE_PWR_ADJ0 (offset: 0x1228, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	PA_MODE3_PWR_ADJ0	Power adjustment for Tx0 when rf pa mode = 3. (8 bit Signed value, Unit : 0.25dB)	0x0
23:16	R/W	PA_MODE2_PWR_ADJ0	Power adjustment for Tx0 when rf pa mode = 2. (8 bit Signed value, Unit : 0.25dB)	0x0
15:8	R/W	PA_MODE1_PWR_ADJ0	Power adjustment for Tx0 when rf pa mode = 1. (8 bit Signed value, Unit : 0.25dB)	0x0
7:0	R/W	PA_MODE0_PWR_ADJ0	Power adjustment for Tx0 when rf pa	0x0

			mode = 0. (8 bit Signed value, Unit : 0.25dB)	

PAMODE_PWR_ADJ1 (offset: 0x122C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	PA_MODE3_PWR_ADJ1	Power adjustment for Tx1 when rf pa mode = 3. (8 bit Signed value, Unit : 0.25dB)	0x0
23:16	R/W	PA_MODE2_PWR_ADJ1	Power adjustment for Tx1 when rf pa mode = 2. (8 bit Signed value, Unit : 0.25dB)	0x0
15:8	R/W	PA_MODE1_PWR_ADJ1	Power adjustment for Tx1 when rf pa mode = 1. (8 bit Signed value, Unit : 0.25dB)	0x0
7:0	R/W	PA_MODE0_PWR_ADJ1	Power adjustment for Tx1 when rf pa mode = 0. (8 bit Signed value, Unit : 0.25dB)	0x0

Reserve (offset: 0x123C, default: 0x0000_0000)

Reserve (offset: 0x1240, default: 0x0000_0000)

Reserve (offset: 0x1244, default: 0x0000_0000)

Reserve (offset: 0x1248, default: 0x0000_0000)

Reserve (offset: 0x124C, default: 0x0000_0000)

Reserve (offset: 0x1250, default: 0x0000_0000)

Reserve (offset: 0x1254, default: 0x0000_0000)

Reserve (offset: 0x1258, default: 0x0000_0000)

Reserve (offset: 0x125C, default: 0x0000_0000)

Reserve (offset: 0x1260, default: 0x0000_0000)

Reserve (offset: 0x1264, default: 0x8000_8000)

Bits	Type	Name	Description	Initial value
31	R/W	DACCLK1_EN_ON	Set dac clk1 en always on. 1. Enable 0. Disable	0x1
30:24	R/W	DLY_DACCLK1_DIS	Delay of dac clk1 en deassertion	0x0
23				
22:16	R/W	DLY_DACCLK0_EN	Delay of dac clk0 en assertion	0x0
15	R/W	DACCLK0_EN_ON	Set dac clk0 en always on. 1. Enable 0. Disable	0x1
14:8	R/W	DLY_DACCLK0_DIS	Delay of dac clk0 en deassertion	0x0
7	R	Reserved		
6:0	R/W	DLY_DACCLK0_EN	Delay of dac clk0 en assertion	0x0

Note1: The timing unit is 0.25us.

ADCCLK_EN_DLY_CFG (offset: 0x1268, default: 0x8000_8000)

Bits	Type	Name	Description	Initial value
31	R/W	ADCCLK1_EN_ON	Set adc clk1 en always on. 1. Enable 0. Disable	0x1
30:24	R/W	DLY_ADCCLK1_DIS	Delay of adc clk1 en deassertion	0x0

23	R	Reserved		
22:16	R/W	DLY_ADCCLK1_EN	Delay of adc clk1 en assertion	0x0
15	R/W	ADCCLK0_EN_ON	Set adc clk0 en always on. 1. Enable 0. Disable	0x1
14:8	R/W	DLY_ADCCLK0_DIS	Delay of adc clk0 en deassertion	0x0
7	R	Reserved		
6:0	R/W	DLY_ADCCLK0_EN	Delay of adc clk0 en assertion	0x0

Note1: The timing unit is 0.25us.

Reserve (offset: 0x126C, default: 0x0000_0000)

Reserve (offset: 0x1270, default: 0x0000_0000)

Reserve (offset: 0x1274, default: 0x0000_0000)

Reserve (offset: 0x1278, default: 0x0000_0000)

Reserve (offset: 0x127C, default: 0x0000_0000)

PAMODE_DBG (offset: 0x1280, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:6	R	Reserved		0
5	R/W	RF_PA_MODE_DBG_EN	Enable bypass RF_PAMODE [1:0] value	0x0
4	R/W	BB_PA_MODE_DBG_EN	Enable bypass BB_PAMODE [1:0] value	0x0
3:2	R/W	RF_PA_MODE_DBG	bypass RF_PAMODE [1:0] value	0x0
1:0	R/W	BB_PA_MODE_DBG	bypass BB_PAMODE [1:0] value	0x0

5.9.4 MAC TX configuration registers (offset: 0x1300)

EDCA_AC0_CFG (BE) (offset: 0x1300, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC0_CWMAX	AC0 CWMAX (unit: power of 2)	7
15:12	R/W	AC0_CWMIN	AC0 CWMIN (unit: power of 2)	3
11:8	R/W	AC0_AIFSN	AC0 AIFSN (unit: # of slot time)	2
7:0	R/W	AC0_TXOP	AC0 TXOP limit (unit: 32us)	0

EDCA_AC1_CFG (BK) (offset: 0x1304, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC1_CWMAX	AC1 CWMAX (unit: power of 2)	7
15:12	R/W	AC1_CWMIN	AC1 CWMIN (unit: power of 2)	3
11:8	R/W	AC1_AIFSN	AC1 AIFSN (unit: # of slot time)	2
7:0	R/W	AC1_TXOP	AC1 TXOP limit (unit: 32us)	0

EDCA_AC2_CFG (VI) (offset: 0x1308, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC2_CWMAX	AC2 CWMAX (unit: power of 2)	7
15:12	R/W	AC2_CWMIN	AC2 CWMIN (unit: power of 2)	3
11:8	R/W	AC2_AIFSN	AC2 AIFSN (unit: # of slot time)	2
7:0	R/W	AC2_TXOP	AC2 TXOP limit (unit: 32us)	0

EDCA_AC3_CFG (VO) (offset: 0x130C, default: 0x0007_3200)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19:16	R/W	AC3_CWMAX	AC3 CWMAX (unit: power of 2)	7
15:12	R/W	AC3_CWMIN	AC3 CWMIN (unit: power of 2)	3
11:8	R/W	AC3_AIFSN	AC3 AIFSN (unit: # of slot time)	2
7:0	R/W	AC3_TXOP	AC3 TXOP limit (unit: 32us)	0

EDCA_TID_AC_MAP (offset: 0x1310, default: 0000_FA14)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:14	R/W	TID7_AC_MAP	AC value as TID=7	3
13:12	R/W	TID6_AC_MAP	AC value as TID=6	3
11:10	R/W	TID5_AC_MAP	AC value as TID=5	2
9:8	R/W	TID4_AC_MAP	AC value as TID=4	2
7:6	R/W	TID3_AC_MAP	AC value as TID=3	0
5:4	R/W	TID2_AC_MAP	AC value as TID=2	1
3:2	R/W	TID1_AC_MAP	AC value as TID=1	1
1:0	R/W	TID0_AC_MAP	AC value as TID=0	0

Note: default according 802.11e Table 20.23—User priority to Access Category mappings

TX_PWR_CFG_0 (offset: 0x1314, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_OFDM_12	TX power for OFDM 12M/18M	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_OFDM_6	TX power for OFDM 6M/9M	0x00
15:14	R/W		Reserved	0
13:8	R/W	TX_PWR_CCK_5	TX power for CCK5.5M/11M	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_CCK_1	TX power for CCK1M/2M	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_1 (offset: 0x1318, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_MCS_2	TX power for HT MCS=2,3, VHT 1SS MCS=2,3	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_MCS_0	TX power for HT MCS=0,1, VHT 1SS MCS=0,1	0x00
15:14	R/W		Reserved	0
13:8	R/W	TX_PWR_OFDM_48	TX power for OFDM 48M	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_OFDM_24	TX power for OFDM 24M/36M	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_2 (offset: 0x131C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_MCS_10	TX power for HT MCS=10,11 , VHT 2SS MCS=2,3	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_MCS_8	TX power for HT MCS=8,9 , VHT 2SS MCS=0,1	0x00
15:14	R/W		Reserved	0

13:8	R/W	TX_PWR_MCS_6	TX power for HT MCS=6, VHT 1SS MCS=6	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_MCS_4	TX power for HT MCS=4,5, VHT 1SS MCS=4,5	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_3 (offset: 0x1320, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_STBC_2	TX power for HT/VHT STBC MCS=2, 3	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_STBC_0	TX power for HT/VHT STBC MCS=0, 1	0x00
15:14	R/W		Reserved	0
13:8	R/W	TX_PWR_MCS_14	TX power for HT MCS=14 , VHT 2SS MCS=6	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_MCS_12	TX power for HT MCS=12,13 , VHT 2SS MCS=4,5	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_4 (offset: 0x1324, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:14	R/W		Reserved	0
13:8	R/W	TX_PWR_STBC_6	TX power for HT/VHT STBC MCS=6	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_STBC_4	TX power for HT/VHT STBC MCS=4, 5	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_7 (offset: 0x13D4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_VHT_2SS_MCS_9	TX power for VHT 2SS MCS=9	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_MCS_7	TX power for HT MCS=7, VHT 1SS MCS=7	0x00
15:14	R/W		Reserved	0
13:8	R/W	TX_PWR_VHT_2SS_MCS_8	TX power for VHT 2SS MCS=8	0x00
7:6	R/W		Reserved	0
5:0	R/W	TX_PWR_OFDM_54	TX power for OFDM 54	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_8 (offset: 0x13D8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_VHT_1SS_MCS_9	TX power for VHT 1SS MCS=9	0x00
23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_VHT_1SS_MCS_8	TX power for VHT 1SS MCS=8	0x00
15:6	R/W		Reserved	0
5:0	R/W	TX_PWR_MCS_15	TX power for HT MCS=15, , VHT 2SS MCS7	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PWR_CFG_9 (offset: 0x13DC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R/W		Reserved	0
29:24	R/W	TX_PWR_VHT_1SS_MCS_9	TX power for VHT STBC MCS=9	0x00

23:22	R/W		Reserved	0
21:16	R/W	TX_PWR_VHT_1SS_MCS_8	TX power for VHT STBC MCS=8	0x00
15:6	R/W		Reserved	0
5:0	R/W	TX_PWR_STBC_7	TX power for HT/VHT STBC MCS=7	0x00

※The Tx power is 6 bit signed 2's complement value. The unit is 0.5dB. Range : -16dB ~ 15.5dB

TX_PIN_CFG (offset: 0x1328, default: 0x0015_0F0F)

Bits	Type	Name	Description	Initial value
31:20	R	Reserved		0
21	R/W	RF_RXON_POL	RF_RXON polarity	0
20	R/W	RF_RXON_EN	RF_RXON enable	1
19	R/W	TRSW_POL	TRSW_EN polarity	0
18	R/W	TRSW_EN	TRSW_EN enable	1
17	R/W	RFTR_POL	RF_TR polarity	0
16	R/W	RFTR_EN	RF_TR enable	1
15	R/W	LNA_PE_G1_POL	LNA_PE_G1 polarity	0
14	R/W	LNA_PE_A1_POL	LNA_PE_A1 polarity	0
13	R/W	LNA_PE_G0_POL	LNA_PE_G0 polarity	0
12	R/W	LNA_PE_A0_POL	LNA_PE_A0 polarity	0
11	R/W	LNA_PE_G1_EN	LNA_PE_G1 enable	1
10	R/W	LNA_PE_A1_EN	LNA_PE_A1 enable	1
9	R/W	LNA_PE_G0_EN	LNA_PE_G0 enable	1
8	R/W	LNA_PE_A0_EN	LNA_PE_A0 enable	1
7	R/W	PA_ON_G1_POL	PA_ON_G1 polarity	0
6	R/W	PA_ON_A1_POL	PA_ON_A1 polarity	0
5	R/W	PA_ON_G0_POL	PA_ON_G0 polarity	0
4	R/W	PA_ON_A0_POL	PA_ON_A0 polarity	0
3	R/W	PA_ON_G1_EN	PA_ON_G1 enable	1
2	R/W	PA_ON_A1_EN	PA_ON_A1 enable	1
1	R/W	PA_ON_G0_EN	PA_ON_G0 enable	1
0	R/W	PA_ON_A0_EN	PA_ON_A0 enable	1

TX_BAND_CFG (offset: 0x132C, default: 0x0000_0004)

Bits	Type	Name	Description	Initial value
31:3	R	Reserved		0
2	R/W	5G_BAND_SEL_N	5G band selection PIN (complement of 5G_BAND_SEL_P)	1
1	R/W	5G_BAND_SEL_P	5G band selection PIN	0
0	R/W	TX_BAND_SEL	0: use lower 40Mhz band in 20Mhz TX 1: use upper 40Mhz band in 20Mhz TX	0

Note1: TX_BAND_SEL is effective only when TX/RX bandwidth control register R4 of BBP is set to 40Mhz.

TX_SW_CFG0 (offset: 0x1330, default: 0x0000_0404)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_TXON_EN	Delay of RF WF_TXON assertion	0x0
23:16	R/W	DLY_TRSW_EN	Delay of TR_SW_P assertion	0x0
15:8	R/W	DLY_PAON_EN	Delay of PA_ON assertion	0x4
7:0	R/W	DLY_TXPE_EN	Delay of BB TX_PE assertion	0x4

Note1: The timing unit is 0.25us.

Note2: SIFS_TIME should compensate with DLY_TXPE_EN.

TX_SW_CFG1 (offset: 0x1334, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
23:16	R/W	DLY_TXON_DIS	Delay of RF WF_TXON de-assertion	0x0
15:8	R/W	DLY_TRSW_DIS	Delay of TR_SW de-assertion	0x0
7:0	R/W	DLY_PAON_DIS	Delay of PA_ON de-assertion	0x0

Note1: The timing unit is 0.25us.

Note2: The delay is started from TX_END event of BBP.

Note3: BB TX_PE is de-asserted automatically as last data byte passed to BBP.

TX_SW_CFG2 (offset: 0x1338, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	DLY_LNA_EN	Delay of LNA* assertion	0x0
23:16	R/W	DLY_LNA_DIS	Delay of LNA* de-assertion	0x0
15:8	R/W	DLY_DAC_EN	Delay of DAC_PE assertion	0x0
7:0	R/W	Reserved		0x0

Note1: The timing unit is 0.25us.

TXOP_THRES_CFG (offset: 0x133C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_REM_THRES	Remaining TXOP threshold, unit: 32us As the remaining TXOP is less than the threshold, the TXOP is passed silently.	0
23:16	R/W	CF_END_THRES	CF-END threshold, unit: 32us As the remaining TXOP is greater than the threshold, the CF-END will be send to release the remaining TXOP reserved by long NAV. Set 0xFF to disable CF_END transmission.	0
15:8	R/W	RDG_IN_THRES	RX RDG threshold, unit: 32us As the remaining TXOP (specified in the duration field of the RX frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0
7:0	R/W	RDG_OUT_THRES	TX RDG threshold, unit: 32us As the remaining TXOP is greater than or equal to the threshold, RDG in the TX frame may be set to one.	0

TXOP_CTRL_CFG (offset: 0x1340, default: 0x0400_243F)

Bits	Type	Name	Description	Initial value
31:24	R/W	EXT_CCA_MUTE	Extension CCA de-glitch time window (unit: usec)	4
23:21	R		Reserved	0
20	R/W	ED_CCA_EN	Primary 20 ED/PD CCA blocking TX 0: disable, 1: enable	0
19:16	R/W	EXT_CW_MIN	Cwmin for extension channel backoff When EXT_CCA_EN is enabled, 40Mhz transmission will be suppressed to 20Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: Cwmin=0, disable.	0
15:8	R/W	EXT_CCA_DLY	Extension CCA signal delay time (unit: usec)	36

			Create delayed version of extension CCA signal reference time for extension channel IFS. Default: (ofdm SIFS) + (long slot time) = 16+20 = 36 (us)	
7	R/W	EXT_CCA_EN	Extension CCA reference enable When transmit in 40Mhz mode, defer until extension CCA is also clear. 0: disable 1: enable	0
6	R/W	LSIG_TXOP_EN	L-SIG TXOP protection enable Extension of mix mode L-SIG protection range to following ACK/CTS.	0
5:0	R/W	TXOP_TRUN_EN	TXOP truncation enable Bit5: reserved Bit4: truncation for MIMO power save RTS/CTS Bit3: truncation for user TXOP mode Bit2: truncation for TX rate group change Bit1: truncation for AC change Bit0: TXOP timeout truncation 0: disable 1: enable	0x3F

TX_RTS_CFG (offset: 0x1344, default: 0x00FF_FF07)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
24	R/W	RTS_FBK_EN	RTS rate fallback enable	0
23:8	R/W	RTS_THRES	RTS threshold (unit: byte) MPDU or AMPDU with length greater than RTS threshold will be protected with RTS/CTS exchange at the beginning of the TXOP.	65535
7:0	R/W	RTS_RTY_LIMIT	Auto RTS retry limit	7

TX_TIMEOUT_CFG (offset: 0x1348, default: 0x010F_0A90)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
24	R/W	ACKTO_END_TXOP	Ends TXOP when TX ack timeout 1'b1: enable 1'b0:disable	1
23:16	R/W	TXOP_TIMEOUT	TXOP timeout value for TXOP truncation (Unit: us) Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	15
15:8	R/W	RX_ACK_TIMEOUT	RX ACK/CTS timeout value for TX procedure (Unit: us) Note: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: For 20us long slot time.	10
7:4	R/W	MPDU_LIFE_TIME	TX MPDU expiration time Expiration time = 2^(9+MPDU_LIFE_TIME) us Default value is 2^(9+9) ~= 256ms	9
3:0	R		Reserved	0

TX_RTY_CFG (offset: 0x134C, default: 0x4BB8_0407)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30	R/W	TX_AUTOFB_EN	TX retry PHY rate auto fallback enable 0: disable 1: enable	1

29	R/W	AGG_RTY_MODE	Aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	0
28	R/W	NAG_RTY_MODE	Non-aggregate MPDU retry mode 0: expired by retry limit 1: expired by MPDU life timer	0
27:16	R/W	LONG_RTY_THRES	Long retry threshold MPDU with length over this threshold is applied with long retry limit.	3000
15:8	R/W	LONG_RTY_LIMIT	Long retry limit	4
7:0	R/W	SHORT_RTY_LIMIT	Short retry limit	7

TX_LINK_CFG (offset: 0x1350, default: 0x007f_0020)

Bits	Type	Name	Description	Initial value
31:24	R	REMOTE_MFS	Remote MCS feedback sequence number	*
23:16	R	REMOTE_MFB	Remote MCS feedback	0x7F
15:13	R		Reserved	0
12	R/W	TX_CFACK_EN	Piggyback CF-ACK enable 0: disable 1: enable	0
11	R/W	TX_RDG_EN	RDG TX enable 0: disable 1: enable	0
10	R/W	~~TX_MRQ_EN~~ TX_EXT_ED_REF_DIS	~~MCS request TX enable~~ ~~0: disable 1: enable~~ Disable reference secondary channel's ED_CCA for the following Tx case : RDG, SIFS Tx, PIFS Reverse Tx, while Tx BW > 20M 0: Reference ED_CCA 1: Don't reference ED CCA	0
9	R/W	~~REMOTE_UMFS_EN~~ TX_ED_REF_DIS	~~Remote un-solicit MFB enable~~ ~~0: do not apply remote un-solicit MFB (MFS=7)~~ ~~1: apply un-solicit MFB~~ Disable reference primary channel's ED_CCA for the following Tx case : CFACK, RDG, SIFS Tx, PIFS Reverse Tx 0: Reference ED_CCA 1: Don't reference ED CCA	0
8	R/W	~~TX_MFB_EN~~ TXOP_BURST_ED_REF_EN	~~TX apply remote MFB~~ ~~0: disable 1: enable~~ While under TxOP burst, reference ED_CCA to halt Tx until ED_CCA deasserted. 0: Disable 1: Enable	0
7:0	R/W	REMOTE_MFB_LITETIME	Remote MFB life time Unit: 32us	32

VHT_HT_FBK_CFG0 (offset: 0x1354, default: 0x6543_2100)

Bits	Type	Name	Description	Initial value
31:28	R/W	VHT_HT_MCS7_FBK	Auto fall back MCS as HT MCS =7, VHT 1SS MCS7	6
27:24	R/W	VHT_HT_MCS6_FBK	Auto fall back MCS as HT MCS =6, VHT 1SS MCS6	5
23:20	R/W	VHT_HT_MCS5_FBK	Auto fall back MCS as HT MCS =5, VHT 1SS MCS5	4
19:16	R/W	VHT_HT_MCS4_FBK	Auto fall back MCS as HT MCS =4, VHT 1SS MCS4	3
15:12	R/W	VHT_HT_MCS3_FBK	Auto fall back MCS as HT MCS =3, VHT 1SS MCS3	2
11:8	R/W	VHT_HT_MCS2_FBK	Auto fall back MCS as HT MCS =2, VHT 1SS MCS2	1
7:4	R/W	VHT_HT_MCS1_FBK	Auto fall back MCS as HT MCS =1, VHT 1SS MCS1	0
3:0	R/W	VHT_HT_MCS0_FBK	Auto fall back MCS as HT MCS =0, VHT 1SS MCS0	0

Note1. For VHT, bit[3] = fall back NSS, bit[2:0] =fall back MCS.

VHT_HT_FBK_CFG1 (offset: 0x1358, default: 0xEDCB_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	VHT_HT_MCS15_FBK	Auto fall back MCS as HT MCS =15, VHT 2SS MCS7	14
27:24	R/W	VHT_HT_MCS14_FBK	Auto fall back MCS as HT MCS =14, VHT 2SS MCS6	13
23:20	R/W	VHT_HT_MCS13_FBK	Auto fall back MCS as HT MCS =13, VHT 2SS MCS5	12
19:16	R/W	VHT_HT_MCS12_FBK	Auto fall back MCS as HT MCS =12, VHT 2SS MCS4	11
15:12	R/W	VHT_HT_MCS11_FBK	Auto fall back MCS as HT MCS =11, VHT 2SS MCS3	10
11:8	R/W	VHT_HT_MCS10_FBK	Auto fall back MCS as HT MCS =10, VHT 2SS MCS2	9
7:4	R/W	VHT_HT_MCS9_FBK	Auto fall back MCS as HT MCS =9, VHT 2SS MCS1	8
3:0	R/W	VHT_HT_MCS8_FBK	Auto fall back MCS as HT MCS =8, VHT 2SS MCS0	8

Note1. The MCS is a fallback stopping state, as the fallback MCS is the same as current MCS.

Note2. HT TX PHY rates will not fallback to legacy PHY rates.

Note3. For VHT, bit[3] = fall back NSS, bit[2:0] =fall back MCS.

LG_FBK_CFG0 (offset: 0x135C, default: 0xEDCB_A988)

Bits	Type	Name	Description	Initial value
31:28	R/W	OFDM7_FBK	Auto fall back MCS as previous TX rate is OFDM 54Mbps.	14
27:24	R/W	OFDM6_FBK	Auto fall back MCS as previous TX rate is OFDM 48Mbps.	13
23:20	R/W	OFDM5_FBK	Auto fall back MCS as previous TX rate is OFDM 36Mbps.	12
19:16	R/W	OFDM4_FBK	Auto fall back MCS as previous TX rate is OFDM 24Mbps.	11
15:12	R/W	OFDM3_FBK	Auto fall back MCS as previous TX rate is OFDM 18Mbps.	10
11:8	R/W	OFDM2_FBK	Auto fall back MCS as previous TX rate is OFDM 12Mbps.	9
7:4	R/W	OFDM1_FBK	Auto fall back MCS as previous TX rate is OFDM 9Mbps.	8
3:0	R/W	OFDM0_FBK	Auto fall back MCS as previous TX rate is OFDM 6Mbps.	8

VHT_LG_FBK_CFG1 (offset: 0x1360, default: 0x8787_2100)

Bits	Type	Name	Description	Initial value
31:28	R/W	VHT_2SS_MCS9_FBK	Auto fall back 2SS MCS as VHT 2SS MCS =9	8
27:24	R/W	VHT_2SS_MCS8_FBK	Auto fall back 2SS MCS as VHT 2SS MCS =8	7
23:20	R/W	VHT_1SS_MCS9_FBK	Auto fall back 1SS MCS as VHT 1SS MCS =9	8
19:16	R/W	VHT_1SS_MCS8_FBK	Auto fall back 1SS MCS as VHT 1SS MCS =8	7
15:12	R/W	CCK3_FBK	Auto fall back MCS as previous TX rate is CCK 11Mbps.	2
11:8	R/W	CCK2_FBK	Auto fall back MCS as previous TX rate is CCK 5.5Mbps.	1
7:4	R/W	CCK1_FBK	Auto fall back MCS as previous TX rate is CCK 2Mbps.	0
3:0	R/W	CCK0_FBK	Auto fall back MCS as previous TX rate is CCK 1Mbps.	0

Note1. Bit3 of each legacy fallback rate is selection of OFDM/CCK. 0=CCK, 1=OFDM.

Note1. For VHT MCS 8,9 , bit[3:0] =fall back MCS, only fallback to the same NSS

CCK_PROT_CFG (offset: 0x1364, default: 0x0010_0003)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	CCK_RTSTH_EN	RTS threshold enable on CCK TX 0: disable 1: enable	0
25:20	R/W	CCK_TXOP_ALLOW	CCK TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX	1

			Bit20: allow CCK TX	
19:18	R/W	CCK_PROT_NAV	TXOP protection type for CCK TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	CCK_PROT_CTRL	Protection control frame type for CCK TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	CCK_PROT_RATE	Protection control frame rate for CCK TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

OFDM_PROT_CFG (offset: 0x1368, default: 0x0020_0003)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	OFDM_RTSTH_EN	RTS threshold enable on OFDM TX 0: disable 1: enable	0
25:20	R/W	OFDM_PROT_TXOP	OFDM TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	2
19:18	R/W	OFDM_PROT_NAV	TXOP protection type for OFDM TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	OFDM_PROT_CTRL	Protection control frame type for OFDM TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	OFDM_PROT_RATE	Protection control frame rate for OFDM TX (Including RTS/CTS-to-self/CF-END) Default: CCK 11M	0x0003

MM20_PROT_CFG (offset: 0x136C, default: 0x0040_2004)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM20_RTSTH_EN	RTS threshold enable on MM20 TX 0: disable 1: enable	0
25:20	R/W	MM20_PROT_TXOP	MM20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX	4

			Bit20: allow CCK TX	
19:18	R/W	MM20_PROT_NAV	TXOP protection type for MM20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM20_PROT_CTRL	Protection control frame type for MM20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM20_PROT_RATE	Protection control frame rate for MM20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x2004

MM40_PROT_CFG (offset: 0x1370, default: 0x0080_2084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	MM40_RTSTH_EN	RTS threshold enable on MM40 TX 0: disable 1: enable	0
25:20	R/W	MM40_PROT_TXOP	MM40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	8
19:18	R/W	MM40_PROT_NAV	TXOP protection type for MM40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	MM40_PROT_CTRL	Protection control frame type for MM40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	MM40_PROT_RATE	Protection control frame rate for MM40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x2084

GF20_PROT_CFG (offset: 0x1374, default: 0x0100_2004)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF20_RTSTH_EN	RTS threshold enable on GF20 TX 0: disable 1: enable	0
25:20	R/W	GF20_PROT_TXOP	GF20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX	16

			Bit21: allow OFDM TX Bit20: allow CCK TX	
19:18	R/W	GF20_PROT_NAV	TXOP protection type for GF20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF20_PROT_CTRL	Protection control frame type for GF20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF20_PROT_RATE	Protection control frame rate for GF20 TX (Including RTS/CTS-to-self/CF-END) Default: OFDM 24M	0x2004

GF40_PROT_CFG (offset: 0x1378, default: 0x0200_2084)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0
26	R/W	GF40_RTSTH_EN	RTS threshold enable on GF40 TX 0: disable 1: enable	0
25:20	R/W	GF40_PROT_TXOP	GF40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	16
19:18	R/W	GF40_PROT_NAV	TXOP protection type for GF40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	GF40_PROT_CTRL	Protection control frame type for GF40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	GF40_PROT_RATE	Protection control frame rate for GF40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x2084

EXP_CTS_TIME (offset: 0x137C, default: 0x0038_013A)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_CTS_TIME	Expected time for OFDM CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps CTS	56
15	R		Reserved	0
14:0	R/W	EXP_CCK_CTS_TIME	Expected time for CCK CTS response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps CTS	314

EXP_ACK_TIME (offset: 0x1380, default: 0x0024_00CA)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0
30:16	R/W	EXP_OFDM_ACK_TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 6Mbps ACK preamble	36
15	R		Reserved	0
14:0	R/W	EXP_CCK_ACK_TIME	Expected time for OFDM ACK response (unit: 1us) Used for outgoing NAV setting. Default: SIFS + 1Mbps ACK preamble	202

HT_FBK_TO_LEGACY (offset: 0x1384, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:13	R		Reserved	0
12	R/W	RTS_FBK_TO_LEGACY_EN	RTS TX rate fallback to legacy OFDM/CCK 0: disable, 1: enable	0
11:8	R/W	RTS_FBK_TO_LEGACY_RATE	Target legacy OFDM/CCK rate for RTS to fallback from MCS0 B3: 0: CCK, 1, OFDM B2:B0: Legacy MCS	0
7:5	R		Reserved	0
4	R/W	HT_FBK_TO_LEGACY_EN	TX rate fallback from HT/VHT rate to legacy OFDM/CCK 0: disable, 1: enable	0
3:0	R/W	HT_FBK_TO_LEGACY_RATE	Target legacy OFDM/CCK rate for HT/VHT to fallback from MCS0 B3: 0: CCK, 1, OFDM B2:B0: Legacy MCS	0

TX_MPDU_ADJ_INT (offset: 0x1388, default: 0x0101_0101)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_MPDU_ADJ_INT3	MPDU TX rate adjustment interval at TX fallback leve-3 (unit: number of MPDU)	1
23:16	R/W	TX_MPDU_ADJ_INT2	MPDU TX rate adjustment interval at TX fallback leve-2 (unit: number of MPDU)	1
15:8	R/W	TX_MPDU_ADJ_INT1	MPDU TX rate adjustment interval at TX fallback leve-1 (unit: number of MPDU)	1
7:0	R/W	TX_MPDU_ADJ_INT0	MPDU TX rate adjustment interval at TX fallback leve-0 (unit: number of MPDU)	1

TX_AMPDU_ADJ_INT (offset: 0x138C, default: 0x0101_0101)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_AMPDU_ADJ_INT3	AMPDU TX rate adjustment interval at TX fallback leve-3 (unit: number of MPDU)	1
23:16	R/W	TX_AMPDU_ADJ_INT2	AMPDU TX rate adjustment interval at TX fallback leve-2 (unit: number of MPDU)	1
15:8	R/W	TX_AMPDU_ADJ_INT1	AMPDU TX rate adjustment interval at TX fallback leve-1 (unit: number of MPDU)	1
7:0	R/W	TX_AMPDU_ADJ_INT0	AMPDU TX rate adjustment interval at TX fallback leve-0 (unit: number of MPDU)	1

TX_MPDU_UP_DOWN_THRES (offset: 0x1390, default: 0x1000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24:16	R/W	TX_MPDU_UP_THRES	MPDU TX fallback level upgrade threshold by packet error rate (unit: 1/256 %)	256
15:9	R		Reserved	0

8:0	R/W	TX_MPDU_DOWN_THRES	MPDU TX fallback level downgrade threshold by packet error rate (unit: 1/256 %)	0

TX_AMPDU_UP_DOWN_THRES (offset: 0x1394, default: 0x1000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24:16	R/W	TX_AMPDU_UP_THRES	AMPDU TX fallback level upgrade threshold by packet error rate (unit: 1/256 %)	256
15:9	R		Reserved	0
8:0	R/W	TX_AMPDU_DOWN_THRES	AMPDU TX fallback level downgrade threshold by packet error rate (unit: 1/256 %)	0

TX_FBK_LIMIT (offset: 0x1398, default: 0x0003_1010)

Bits	Type	Name	Description	Initial value
31:19	R		Reserved	0
18	R/W	TX_RATE_LUT_EN	Copy TX rate from per WCID lookup table when TXWI.TXLUT is also set to 1. 0: disable, 1: enable	0
17	R/W	TX_AMPDU_UP_CLEAR	AMPDU Directly upgrade to level-0 0: disable, 1: enable	1
16	R/W	TX_MPDU_UP_CLEAR	MPDU Directly upgrade to level-0 0: disable, 1: enable	1
15:8	R/W	TX_AMPDU_FBK_LIMIT	AMPDU TX fallback level limitation (unit: # of level)	16
7:0	R/W	TX_MPDU_FBK_LIMIT	MPDU TX fallback level limitation(unit: # of level)	16

TX_SW_CFG0 (offset: 0x139C, default: 0x0000_0404)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0x0
15:8	R/W	DLY_EN_LOFT	Delay of Enable LOFT	0x4
7:0	R/W	DLY_DIS_LOFT	Delay of Disble LOFT	0x4

Note1: The timing unit is 0.25us.

TX0_RF_GAIN_CORRECT (offset: 0x13A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0x00
29:24	R/W	GAIN_CORR_3	TX Gain Correction when RF_ALC[3:2]==3. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
23:22	R		Reserved	0x00
21:16	R/W	GAIN_CORR_2	TX Gain Correction when RF_ALC[3:2]==2. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
15:14	R		Reserved	0x00
13:8	R/W	GAIN_CORR_1	TX Gain Correction when RF_ALC[3:2]==1. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
7:6	R		Reserved	0x00
5:0	R/W	GAIN_CORR_0	TX Gain Correction when RF_ALC[3:2]==0. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00

TX1_RF_GAIN_CORRECT (offset: 0x13A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0x00
29:24	R/W	GAIN_CORR_3	TX Gain Correction when RF_ALC[3:2]==3. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
23:22	R		Reserved	0x00
21:16	R/W	GAIN_CORR_2	TX Gain Correction when RF_ALC[3:2]==2. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
15:14	R		Reserved	0x00
13:8	R/W	GAIN_CORR_1	TX Gain Correction when RF_ALC[3:2]==1. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00
7:6	R		Reserved	0x00
5:0	R/W	GAIN_CORR_0	TX Gain Correction when RF_ALC[3:2]==0. Unit: 0.1 dB, Range: -3.2dB ~ 3.1dB	0x00

TX_ALC_CFG_2 (offset: 0x13A8, default: 0x2216_0A00)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0x00
30:24	R/W	THRES_A0	Unsighed Tx0Target Gain Threshold-A. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x22
23	R		Reserved	0x00
22:16	R/W	THRES_B0	Unsighed Tx0Target Gain Threshold-B. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x16
15	R		Reserved	0x00
14:8	R/W	THRES_C0	Unsighed Tx0Target Gain Threshold-B. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x0A
7:6	R		Reserved	0x00
5:0	R/W	TX1_TEMP_COMP	TX1 power temperature compensation Format: 6-bit, signed value Unit: 0.5dB, Range: -10 ~ 10dB	0x00

TX_ALC_CFG_3 (offset: 0x13AC, default: 0x2216_0A74)

Bits	Type	Name	Description	Initial value
31	R		Reserved	0x00
30:24	R/W	THRES_A1	Unsighed Tx1 Target Gain Threshold-A. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x22
23	R		Reserved	0x00
22:16	R/W	THRES_B1	Unsighed Tx1 Target Gain Threshold-B. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x16
15	R		Reserved	0x00
14:8	R/W	THRES_C1	Unsighed Tx1 Target Gain Threshold-B. Unit: 0.5dB, Range: 0dB ~ 31.5dB	0x0A
7	R		Reserved	0x00
6:4	R/W	CCK PWR OFST	Power offset when Tx CCK (Unsigned. Unit : 1dB)	0x7
3	R		Reserved	0x00
2:0	R/W	DAC PWR BO	DAC Power backoff (Unsigned. Unit : 1dB)	0x4

TX_ALC_CFG_0 (offset: 0x13B0, default: 0x2F2F_1B1B)

Bits	Type	Name	Description	Initial value
31:30	R		Reserved	0x00
29:24	R/W	TX_ALC_LIMIT_1	TX1 ALC upper limit Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x2F
23:22	R		Reserved	0x00
21:16	R/W	TX_ALC_LIMIT_0	TX0 ALC upper limit Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x2F
15:14	R		Reserved	0x00
13:8	R/W	TX_ALC_CH_INIT_1	TX1 channel initial transmission gain Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x1B
7:6	R		Reserved	0x00
5:0	R/W	TX_ALC_CH_INIT_0	TX0 channel initial transmission gain Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x1B

TX_ALC_CFG_1 (offset: 0x13B4, default: 0x8904_0000)

Bits	Type	Name	Description	Initial value
31	R/W	ROS_BUSY_EN	Defer TX procedure if ROS is busy 0: disable, 1: enable	0x01
30	R/W	~~RF_TOS_ENABLE~~	~~RF TOS calibration enable~~ ~~0: disable, 1: enable~~	0x00
29:24	R/W	RF_TOS_TIMEOUT	RF_TOS_EN de-assertion timeout value if RF_TOS_DONE Is missing Unit: 0.25 usec	0x09
23:22	R		Reserved	0x1
21:20	R		Reserved	0x1
19	R/W	DIG_TX_MCS_PWR	Use Digital power to contribute all Tx MCS Power.	0x00
18:16	R/W	RF_TOS_DLY	RF_TOS_EN assertion delay after de-assertion of PA_PE Unit: 0.25 usec	0x04
15:12	R/W	TX1_GAIN_FINE	TX1 gain fine adjustment Format: 4-bit, signed value Unit: 0.1dB, Range: -0.8 ~ 0.7dB	0x00
11:8	R/W	TX0_GAIN_FINE	TX0 gain fine adjustment Format: 4-bit, signed value Unit: 0.1dB, Range: -0.8 ~ 0.7dB	0x00
7:6	R		Reserved	0x00
5:0	R/W	TX0_TEMP_COMP	TX0 power temperature compensation Format: 6-bit, signed value Unit: 0.5dB, Range: -10 ~ 10dB	0x00

TX_ALC_DBG_1 (offset: 0x13B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial

				value
31	R/W	TX_MCS_PWR_DBG_EN	TX MCS power debug enable 0: disable, 1: enable	0x00
30:24	R/W	TX_MCS_PWR_DBG	TX MCS power debug value	0x00
23	R/W	TX_ALC_REQ_DBG	TX ALC requested debug mode enable 0: disable, 1: enable	0x00
22:16	R/W	TX_ALC_REQ_DBG	TX ALC requested debug value Applied when TX_ALC_REQ_DBG_EN = 1	0x00
15	R		Reserved	0x00
15	R/W	TX_ALC_ADJ_DBG_EN	TX ALC adjustment debug enable 0: disable, 1: enable	0x00
14:8	R/W	TX_ALC_ADJ_DBG	TX ALC adjustment debug value Applied to	0x00
7:6	R		Reserved	0x00
5	R/W	RF_GAINATT_DBG	TX ALC RF gain attenuation debug value Applied to RF when TX_ALC_RF_DBG_EN is set to 1.	0x00
4	R/W	TX_ALC_RF_DBG_EN	TX ALC RF control pin debug enable 0: disable, 1: enable	0x00
3:0	R/W	TX_ALC_RF_DBG	TX ALC RF TX power debug value Applied to RF when TX_ALC_RF_DBG_EN is set to 1.	0x00

TX_ ALC_MONITOR (offset: 0x13BC, default: 0xXXXX_XXXX)

Bits	Type	Name	Description	Initial value
31	R/W	TX_ALC_IDX	Select TX Index 0: Monitor Tx0 ALC 1: Monitor Tx1 ALC	0x00
30:24	R	TX_MCS_PWR	Per Rate Tx MCS Power	0xXX
23	R		Reserved	0x00
22:16	R	TX_ALC_REQ	TX ALC Requset[6:0]	0xXX
15	R		Reserved	0x00
14:8	R	TX_ALC_REQ_ADJ	TX ALC Req Saturated[6:0]	0xXX
7:4	R	TXWI_PWR_ADJ	TXWI_PWR_ADJ	0xXX
3:0	R	RF_TX_ALC	GCRF[3:0] to RF	0xXX

TX_ALC_CFG_4 (offset: 0x13C0, default: 0x8000_0606)

Bits	Type	Name	Description	Initial value
31:29	R/W	WL_LOWGAIN_CH_EN	Use TX0/TX1_CH_LOWGAIN as ch_init power when wl_lowgain asserts.	0x1
30	R			
29:24	R/W	TX1_CH_LOWGAIN	TX1 channel wl_lowgain when wl_lowgain asserts Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x00

23:22	R		Reserved	0x00
21:16	R/W	TX0_CH_LOWGAIN	TX0 channel wl_lowgain Format: 6-bit, unsigned value Unit: 0.5dB, Range: 0 ~ 23.5dB	0x00
15:14	R		Reserved	0x00
13:8	R/W	GAIN_MIN_1	RF Tx1 minimum gain, (Unit : 0.5dB) Range=-16dB~15.5dB (Gain_max=Gain_Min+24dB)	0x6
7:6	R		Reserved	0x00
5:0	R/W	GAIN_MIN_0	RF Tx0 minimum gain, (Unit : 0.5dB) Range=-16dB~15.5dB (Gain_max=Gain_Min+24dB)	0x6

TX_ALC_CFG_5 (offset: 0x13C4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31	R/W	PA_MODE_ADJ_DIS	Discard pa_mode_pwr_adj in TxALC	0x0
30	R/W	PA_MODE_ADJ_DBG_EN	pa_mode_pwr_adj dbg mode enable	0x0
29:28	R/W	PA_MODE_ADJ_DBG	pa_mode_pwr_adj dbg value	0x0
27:16	R		Reserved	0x00
15	R/W	WL_LOWGAIN_ADJ_EN	Reduce relative gain when wl_lowgain 0: Disable. 1:Enable	0x00
14:13	R		Reserved	0x00
12:8	R/W	PWR_MAC_ADJ1	Tx1 Relative gain Unit: 0.5dB, Range: -8dB ~ 7dB	0x00
7:5	R		Reserved	0x00
4:0	R/W	PWR_MAC_ADJ0	Tx0 Relative gain Unit: 0.5dB, Range: -8dB ~ 7dB	0x00

TX_ALC_VGA3 (offset: 0x13C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:29	R		Reserved	0x00
28:24	R/W	TX1_ALC_VGA2	Gain compensation for TX1 target gain > Threshold B Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6dB	0x00
23:21	R		Reserved	0x00
20:16	R/W	TX0_ALC_VGA2	Gain compensation for TX0 target gain > Threshold B Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6dB	0x00
15:13	R		Reserved	0x00
12:8	R/W	TX1_ALC_VGA3	Gain compensation for TX1 target gain > Threshold A Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6dB	0x00
7:5	R		Reserved	0x00
4:0	R/W	TX0_ALC_VGA3	Gain compensation for TX0 target gain > Threshold A Format: 5-bit, un-signed value	0x00

			Unit: 0.5 dB, Range: 0-6dB	

TX_AC_RTY_LIMIT (offset: 0x13CC, default: 0x0707_0707)

Bits	Type	Name	Description	Initial value
31:24	R/W	TX_AC3_RTY_LIMIT	AC3 QoS-Data frame TX retry limit	7
23:16	R/W	TX_AC2_RTY_LIMIT	AC2 QoS-Data frame TX retry limit	7
15:8	R/W	TX_AC1_RTY_LIMIT	AC1 QoS-Data frame TX retry limit	7
7:0	R/W	TX_AC0_RTY_LIMIT	AC0 QoS-Data frame TX retry limit	7

TX_AC_FBK_SPEED (offset: 0x13D0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:2	R		Reserved	0
1	R/W	TX_AC_FBK_SPEED_EN	Apply per AC TX fallback speed parameters	0
0	R/W	TX_AC_RTY_LIMIT_EN	Apply per AC TX retry limit parameters 0: disable, 1: enable	0

TX_PROT_CFG6 (offset: 0x13E0, default: 0xE3F0_2004)

Bits	Type	Name	Description	Initial value
31:29	R/W	VHT20_PROT_TXOP	VHT20 TXOP allowance (0: disallow, 1: allow) Bit31: allow VHT80 TX Bit30: allow VHT40 TX Bit29: allow VHT20 TX	0x7
28	R/W	VHT20_DYN_CBW	RTS use dynamic channel bandwidth when TX signaling mode is turned on 0: static, 1: dynamic	0
27	R/W	VHT20_RTS_TA_SIGNAL	RTS TA signaling mode on VHT20 TX 0: disable, 1: enable	0
26	R/W	VHT20_RTS_THRES_EN	RTS threshold enable on VHT20 TX 0: disable, 1: enable	0
25:20	R/W	VHT20_PROT_TXOP	VHT20 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	0x3F
19:18	R/W	VHT20_PROT_NAV	TXOP protection type for VHT20 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	VHT20_PROT_CTRL	Protection control frame type for VHT20 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	VHT20_PROT_RATE	Protection control frame rate for VHT20 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x2004

TX_PROT_CFG7 (offset: 0x13E4, default: 0xE3F0_2084)

Bits	Type	Name	Description	Initial value
31:29	R/W	VHT40_PROT_TXOP	VHT40 TXOP allowance (0: disallow, 1: allow) Bit31: allow VHT80 TX Bit30: allow VHT40 TX Bit29: allow VHT20 TX	0x7

28	R/W	VHT40_DYN_CBW	RTS use dynamic channel bandwidth when TX signaling mode is turned on 0: static, 1: dynamic	0
27	R/W	VHT40_RTS_TA_SIGNAL	RTS TA signaling mode on VHT40 TX 0: disable, 1: enable	0
26	R/W	VHT40_RTS_THRES_EN	RTS threshold enable on VHT40 TX 0: disable, 1: enable	0
25:20	R/W	VHT40_PROT_TXOP	VHT40 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	0x3F
19:18	R/W	VHT40_PROT_NAV	TXOP protection type for VHT40 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	VHT40_PROT_CTRL	Protection control frame type for VHT40 TX 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0
15:0	R/W	VHT40_PROT_RATE	Protection control frame rate for VHT40 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x2084

TX_PROT_CFG8 (offset: 0x13E8, default: 0xE3F0_2104)

Bits	Type	Name	Description	Initial value
31:29	R/W	VHT80_PROT_TXOP	VHT80 TXOP allowance (0: disallow, 1: allow) Bit31: allow VHT80 TX Bit30: allow VHT40 TX Bit29: allow VHT20 TX	0x7
28	R/W	VHT80_DYN_CBW	RTS use dynamic channel bandwidth when TX signaling mode is turned on 0: static, 1: dynamic	0
27	R/W	VHT80_RTS_TA_SIGNAL	RTS TA signaling mode on VHT80 TX 0: disable, 1: enable	0
26	R/W	VHT80_RTS_THRES_EN	RTS threshold enable on VHT80 TX 0: disable, 1: enable	0
25:20	R/W	VHT80_PROT_TXOP	VHT80 TXOP allowance (0: disallow, 1: allow) Bit25: allow GF-40 TX Bit24: allow GF-20 TX Bit23: allow MM-40 TX Bit22: allow MM-20 TX Bit21: allow OFDM TX Bit20: allow CCK TX	0x3F
19:18	R/W	VHT80_PROT_NAV	TXOP protection type for VHT80 TX 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0
17:16	R/W	VHT80_PROT_CTRL	Protection control frame type for VHT80 TX 0: None 1: RTS/CTS	0

			2: CTS-to-self 3: Reserved (None)	
15:0	R/W	VHT80_PROT_RATE	Protection control frame rate for VHT80 TX (Including RTS/CTS-to-self/CF-END) Default: duplicate OFDM 24M	0x2014

PIFS_TX_CFG (offset: 0x13EC, default: 0x0006_07D0)

Bits	Type	Name	Description	Initial value
31:20	R		Reserved	0
19	R/W	PIFS_REV_TX_FORCE	Force per packet PIFS reverse TX mode, ignore TXWI.PIFSTX bit.	0
18	R/W	PIFS_REV_TX_EN	Enable PIFS reverse TX mode 0: disable, 1: enable	1
17:16	R/W	PIFS_REV_TX_SLOT	PIFS slot count	2
15:0	R/W	PIFS_REV_TX_THRES	Only AMPDU/MPDU with length less than this threshold is able to do PIFS reverse direction TX after a successful ACK transmission	2000

TX_PROT_RTY_LIMIT (offset: 0x13F0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W		Reserve	0
7:1	R		Reserved	
0	R/W	PROT_RTY_LIMIT_EN	Enable the protection frame retry limit by PROT_RTY_LIMIT	0

TX_ALC_DBG (offset: 0x13F4, default: 0xXXXX_XXXX)

Bits	Type	Name	Description	Initial value
31	R/W	TX_ALC_DBG_IDX	Tx ALC Debug Index 0: Tx0 Report 1: Tx1 Report	0x0
30	R	TX_BB_INT4	BBP Integer power bit 4, use together with TX_BB_INT3_0	0xXX
29:24	R	TX_ALC_TAR_GAIN	Tx ALC target gain. Unit : 0.5dBm	0xXX
23:16	R	TX_ALC_REQ_PAMODE	Tx ALC request gain with PA Mode Adj	0xXX
15:8	R	ALC_DIG_WO_FINE	Tx ALC digital power without gain_fine factor. Unit : 0.5dB	0xXX
7:4	R	TX_BB_INT3_0	BBP Integer power bit 3~0. Unit : 1dB (Range = -16dB~15dB, value 0 = -16dB)	0xXX
3:0	R	TX_BB_FRAC	BBP frac power bit 3~0. Unit = 0.1dB (Range = 0dB~0.9dB)	0xXX

5.9.5 MAC RX configuration registers (offset: 0x1400)

RX_FILTR_CFG (offset: 0x1400, default: 0x0001_5F9F)

Bits	Type	Name	Description	Initial value
31:17	R		Reserved	0
16	R/W	DROP_CTRL_RSV	Drop reserve control subtype	1
15	R/W	DROP_BAR	Drop BAR	0
14	R/W	DROP_BA	Drop BA	1
13	R/W	DROP_PSPOLL	Drop PS-Poll	0
12	R/W	DROP_RTS	Drop RTS	1

11	R/W	DROP_CTS	Drop CTS	1
10	R/W	DROP_ACK	Drop ACK	1
9	R/W	DROP_CFEND	Drop CF-END	1
8	R/W	DROP_CFACK	Drop CF-END + CF-ACK	1
7	R/W	DROP_DUPL	Drop duplicated frame	1
6	R/W	DROP_BC	Drop broadcast frame	0
5	R/W	DROP_MC	Drop multicast frame	0
4	R/W	DROP_VER_ERR	Drop 802.11 version error frame	1
3	R/W	DROP_NOT_MYBSS	Drop frame that is not my BSSID	1
2	R/W	DROP_UC_NOME	Drop not to me unicast frame	1
1	R/W	DROP_PHY_ERR	Drop physical error frame	1
0	R/W	DROP_CRC_ERR	Drop CRC error frame	1

Note: 1: enable, 0: disable.

AUTO_RSP_CFG (offset: 0x1404, default: 0x0000_0007)

Bits	Type	Name	Description	Initial value
31:9	R		Reserved	0
8	R/W	CTS_BYPASS_EXTCCA	Duplicate legacy CTS response bypass extension CCA check 0: disable, 1: enable	0
7	R/W	CTRL_PWR_BIT	Power bit value in control frame	0
6	R/W	BAC_ACK_POLICY	BA frame -> BAC -> Ack policy bit value	0
5	R/W	CTRL_WRAP_EN	ACK/CTS Control Wrapper frame auto-responding enable 0: disable 1: enable	0
4	R/W	CCK_SHORT_EN	CCK short preamble auto response enable 0: disable 1: enable	0
3	R/W	CTS_40M_REF	In duplicate legacy CTS response mode, refer to extension CCA to decide duplicate or not. 0: disable 1: enable	0
2	R/W	CTS_40M_MODE	Duplicate legacy CTS response mode 0: disable 1: enable	1
1	R/W	BAC_ACKPOLICY_EN	BAC ACK policy bit enable 0: disable; don't care this bit 1: enable; no BA auto responding upon reception of BAR with no ACK policy	1
0	R/W	AUTO_RSP_EN	Auto responder enable	1

LEGACY_BASIC_RATE (offset: 0x1408, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31: 12	R/W		Reserved	0
11: 0	R/W	LEGACY_BASIC_RATE	Legacy basic rate bit mask Bit0: 1 Mbps is basic rate Bit1: 2 Mbps is basic rate Bit2: 5.5 Mbps is basic rate Bit3: 11 Mbps is basic rate Bit4: 6 Mbps is basic rate Bit5: 9 Mbps is basic rate Bit6: 12 Mbps is basic rate Bit7: 18 Mbps is basic rate Bit8: 24 Mbps is basic rate	0

			Bit9: 36 Mbps is basic rate Bit10: 48 Mbps is basic rate Bit11: 54 Mbps is basic rate 0: disable 1: enable	

HT_BASIC_RATE (offset: 0x140C, default: 0x8200_8000)

Bits	Type	Name	Description	Initial value
31: 16	R/W	STBC_BASIC_RATE	The definition is the same as that in PHY rate format.	0x8200
15:0	R/W	HT_BASIC_RATE	The definition is the same as that in PHY rate format.	0x8000

HT_CTRL_CFG (offset: 0x1410, default: 0x0000_0100)

Bits	Type	Name	Description	Initial value
31: 9	R		Reserved	0
8: 0	R/W	HT_CTRL_THRES	Remaining TXOP threshold for HT control frame auto responding (unit: us)	256

SIFS_COST_CFG (offset: 0x1414, default: 0x0000_100A)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:8	R/W	OFDM_SIFS_COST	OFDM SIFS time (unit: 1us) Applied after OFDM TX/RX.	16
7:0	R/W	CCK_SIFS_COST	CCK SIFS time (unit: 1us) Applied after CCK TX/RX.	10

Note: The OFDM_SIFS_COST and CCK_SIFS_COST are used only for duration field calculation. It will not affect the responding timing.

RX_PARSER_CFG (offset: 0x1418, default: 0x0FFF_0000)

Bits	Type	Name	Description	Initial value
31:28	R		Reserved	
27:16	R/W	LSIG_LEN_THRES	When the length in L-SIG is longer than this threshold, the L-SIG TXOP will not be applied as NAV channel reservation.	4095
15:02	R		Reserved	
1	R/W	RX_LSIG_TXOP_EN	Respect LSIG-TXOP as channel reservation 0: disable 1: enable	0
0	R/W	NAV_ALL_EN	Set NAV for all received frames 0: disable (unicast to me frame will not set the NAV) 1: enable	0

EXT_CCA_CFG (offset: 0x141C, default: 0x0000_FFE4)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:12	R/W	ED_CCA_MASK	Mask of ED CCA0-3 0: on, 1: off The ED/PD CCA0-3 is: (PD_CCA[3:0] & PD_CCA_MASK[3:0]) || (ED_CCA[3:0] & ED_CCA_MASK[3:0])	0xF
11:8	R/W	PD_CCA_MASK	Mask of PD CCA0-3 0: on, 1: off The ED/PD CCA0-3 is: (PD_CCA[3:0] & PD_CCA_MASK[3:0]) || (ED_CCA[3:0] & ED_CCA_MASK[3:0])	0xF
7:6	R/W	ED_PD_CCA3_SELECT	ED/PD CCA3 select Select from ED/PD CCA0-3 as secondary40* CCA	0x3
5:4	R/W	ED_PD _CCA2_SELECT	ED/PD CCA2 select Select from ED/PD CCA0-3 as secondary40 CCA	0x2
3:2	R/W	ED_PD _CCA1_SELECT	ED/PD CCA1 select Select from ED/PD CCA0-3 as secondary20 CCA	0x1
1:0	R/W	ED_PD _CCA0_SELECT	ED/PD CCA0 select Select from ED/PD CCA0-3 as primary20 ED/PD CCA	0x0

RXINFO_FCTYPE_CFG (offset: 0x142C, default: 0x0B00_0000)

Bits	Type	Name	Description	Initial value
31:24	R.W	RX_ACTION_CATEGORY	Specify Action frame Cateogry to be indicated in RXINFO. Default : TIM Frame	0xB
23:16	R/W	RX_ACTION_ACTION	Specify Action frame Action field to be indicated in RXINFO Default : TIM Frame	0x0
15	R/W	RXINFO23_FCTYPE_EN	Filter Frame Control type,subtype and set flag in RXINFO [23]	0x0
14	R		Reserved	0x0
13:10	R/W	RXINFO23_FC_SUB_TYPE	Frame Control Subtype to filter in RXINFO bit[23]	0x0
9:8	R/W	RXINFO23_FC_TYPE	Frame Control Type to filter in RXINFO bit[23] 00 : Mgmt 01 : Control 10 : Data	0x0
7	R/W	RXINFO22_FCTYPE_EN	Filter Frame Control type,subtype and set flag in RXINFO [22]	0x0
6	R		Reserved	0x0
5:2	R/W	RXINFO22_FC_SUB_TYPE	Frame Control Subtype to filter in RXINFO bit[22]	0x0
1:0	R/W	RXINFO22_FC_TYPE	Frame Control Type to filter in RXINFO bit[22] 00 : Mgmt 01 : Control 10 : Data	0x0

BCN_FIL_CFG0 (offset: 0x1430, default: 0x0900_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	P2P_OUI_TYPE	Specify OUI TYPE for P2P IE	0x09
23:19	R		Reserved	0x0
18	R/W	BCN_MONITOR_RST_EN	Enable Beacon Monitor Report reset when Rx Beacon start	0
17	R/W	BCN_MONITOR_EN	Enable Beacon Monitor Report in BCN_MONITOR CR	0
16	R/W	BCN_HASH16_WR_EN	Beacon hash16 value update by new value if compare fail 0 : Disable, the hash16 value of BSSIDX won't be updated even if hash16 compare fail. 1 : Enable, the hash16 value of BSSIDX will be updated if hash16 compare fail.	0x0
15	R/W	BCN_IE_WHITE_EN	Disgard Beacon IE listed in whitelist 0 : Disable 1: Enable	0x0
14	R/W	BCN_IE_BLACK_EN	Check Beacon IE listed in blacklist 0 : Disable 1: Enable	0x0
13	R/W	BCN_CON_CHK_EN_BSS2	Check Beacon content from BSSID2 0 : Disable 1: Enable	0x0
12	R/W	BCN_CON_CHK_EN_BSS1	Check Beacon content from BSSID1	0x0

			0 : Disable 1: Enable	
11	R/W	BCN_CON_CHK_EN_BSS0	Check Beacon content from BSSID0 0 : Disable 1: Enable	0x0
10	R/W	BCN_TIM_PARSE_EN_BSS2	Parsing the BSSID2 Beacon TIM IE for buffered UC2ME/BC/MC frame. 0 : Disable, the MAC will not parse the TIM and the Beacon from BSSID will always be received. 1 : Enable, the MAC will parse the TIM and indicate if UC2ME or BC/MC is buffered.	0x0
9	R/W	BCN_TIM_PARSE_EN_BSS1	Parsing the BSSID1 Beacon TIM IE for buffered UC2ME/BC/MC frame. 0 : Disable, the MAC will not parse the TIM and the Beacon from BSSID will always be received. 1 : Enable, the MAC will parse the TIM and indicate if UC2ME or BC/MC is buffered.	0x0
8	R/W	BCN_TIM_PARSE_EN_BSS0	Parsing the BSSID0 Beacon TIM IE for buffered UC2ME/BC/MC frame. 0 : Disable, the MAC will not parse the TIM and the Beacon from BSSID will always be received. 1 : Enable, the MAC will parse the TIM and indicate if UC2ME or BC/MC is buffered.	0x0
7:4	R		Reserved	0x0
3	R/W	IE_HT_PCO_PHASE_SKIP_BSS2	Skip checking the PCO_PHASE bit of IE “HT OPERATION” IE of Beacon from BSSID2 Beacon. 0 : Always check the PCO_PHASE bit 1 : Don’t check the PCO_PHASE bit	0x0
2	R/W	IE_HT_PCO_PHASE_SKIP_BSS1	Skip checking the PCO_PHASE bit of IE “HT OPERATION” IE of Beacon from BSSID1 Beacon. 0 : Always check the PCO_PHASE bit 1 : Don’t check the PCO_PHASE bit	0x0
1	R/W	IE_HT_PCO_PHASE_SKIP_BSS0	Skip checking the PCO_PHASE bit of IE “HT OPERATION” IE of Beacon from BSSID0 Beacon. 0 : Always check the PCO_PHASE bit 1 : Don’t check the PCO_PHASE bit	0x0
0	R/W	DROP_BCN_EN	Drop Beacon which pass TIM parsing and content check 0 : Disable 1: Enable	0x0

BCN_FIL_CFG1 (offset: 0x1434, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	BCN_IE_WHITE_LIST_3	Always discard the IE ID while check Beacon content	0x0
23:16	R/W	BCN_IE_WHITE_LIST_2	Always discard the IE ID while check Beacon content	0x0
15:8	R/W	BCN_IE_WHITE_LIST_1	Always discard the IE ID while check Beacon content	0x0
7:0	R/W	BCN_IE_WHITE_LIST_0	Always discard the IE ID while check Beacon content	0x0

BCN_FIL_CFG2 (offset: 0x1438, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	BCN_IE_BLACK_LIST_3	Always check the IE ID while check Beacon content	0x0
23:16	R/W	BCN_IE_BLACK_LIST_2	Always check the IE ID while check Beacon content	0x0
15:8	R/W	BCN_IE_BLACK_LIST_1	Always check the IE ID while check Beacon content	0x0
7:0	R/W	BCN_IE_BLACK_LIST_0	Always check the IE ID while check Beacon content	0x0

BCN_FIL_CFG3 (offset: 0x143C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R/W	BCN_HASH16_BSS1	Hash16 value of BSS1 Beacon, auto-updated by Beacon filter or manually writable by SW	0x0
15:0	R/W	BCN_HASH16_BSS0	Hash16 value of BSS0 Beacon, auto-updated by Beacon filter or	0x0

			manually writable by SW	

BCN_FIL_CFG4 (offset: 0x1440, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:0	R/W	BCN_HASH16_BSS2	Hash16 value of BSS2 Beacon, auto-updated by Beacon filter or manually writable by SW	0x0

BCN_MONITOR (offset: 0x1444, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R	BCN_MONITOR	Rx Beacon Monitor result	0x0

TX_SW_CFG2 (offset: 0x1478, default: 0x000C_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	
15:8	R/W	DLY_RF_RXON	Delay of RF WF_RXON assertion	0x0
7:0	R/W	DLY_BB_RXPE	Delay of BB_RXPE assertion	0x0

Note1: The timing unit is 0.25us.

MAC_ADDR_EXT_EN (offset: 0x147C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:1	R		Reserved	0x0
0	R/W	MAC_ADDR_EXT_EN	Enable Extended MAC Address	0x0

MAC_ADDR_EXT0_31_0 (offset: 0x1480, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT0_31_0	Extended MAC Address0 bit 31~0	0x0

MAC_ADDR_EXT0_47_32 (offset: 0x1484, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT0_47_32	Extended MAC Address0 bit 47~32	0x0

MAC_ADDR_EXT1_31_0 (offset: 0x1488, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT1_31_0	Extended MAC Address1 bit 31~0	0x0

MAC_ADDR_EXT1_47_32 (offset: 0x148C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT1_47_32	Extended MAC Address1 bit 47~32	0x0

MAC_ADDR_EXT2_31_0 (offset: 0x1490, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT2_31_0	Extended MAC Address2 bit 31~0	0x0

MAC_ADDR_EXT2_47_32 (offset: 0x1494, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT2_47_32	Extended MAC Address2 bit 47~32	0x0

MAC_ADDR_EXT3_31_0 (offset: 0x1498, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT3_31_0	Extended MAC Address3 bit 31~0	0x0

MAC_ADDR_EXT3_47_32 (offset: 0x149C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT3_47_32	Extended MAC Address3 bit 47~32	0x0

MAC_ADDR_EXT4_31_0 (offset: 0x14A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT4_31_0	Extended MAC Address4 bit 31~0	0x0

MAC_ADDR_EXT4_47_32 (offset: 0x14A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT4_47_32	Extended MAC Address4 bit 47~32	0x0

MAC_ADDR_EXT5_31_0 (offset: 0x14A8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT5_31_0	Extended MAC Address5 bit 31~0	0x0

MAC_ADDR_EXT5_47_32 (offset: 0x14AC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT5_47_32	Extended MAC Address5 bit 47~32	0x0

MAC_ADDR_EXT6_31_0 (offset: 0x14B0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT6_31_0	Extended MAC Address6 bit 31~0	0x0

MAC_ADDR_EXT6_47_32 (offset: 0x14B4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT6_47_32	Extended MAC Address6 bit 47~32	0x0

MAC_ADDR_EXT7_31_0 (offset: 0x14B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT7_31_0	Extended MAC Address7 bit 31~0	0x0

MAC_ADDR_EXT7_47_32 (offset: 0x14BC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT7_47_32	Extended MAC Address7 bit 47~32	0x0

MAC_ADDR_EXT8_31_0 (offset: 0x14C0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT8_31_0	Extended MAC Address8 bit 31~0	0x0

MAC_ADDR_EXT8_47_32 (offset: 0x14C4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT8_47_32	Extended MAC Address8 bit 47~32	0x0

MAC_ADDR_EXT9_31_0 (offset: 0x14C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT9_31_0	Extended MAC Address9 bit 31~0	0x0

MAC_ADDR_EXT9_47_32 (offset: 0x14CC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT9_47_32	Extended MAC Address9 bit 47~32	0x0

MAC_ADDR_EXT10_31_0 (offset: 0x14D0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT10_1_0	Extended MAC Address10 bit 31~0	0x0

MAC_ADDR_EXT10_47_32 (offset: 0x14D4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT10_47_32	Extended MAC Address10 bit 47~32	0x0

MAC_ADDR_EXT11_31_0 (offset: 0x14D8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT11_31_0	Extended MAC Address11 bit 31~0	0x0

MAC_ADDR_EXT11_47_32 (offset: 0x14DC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT11_47_32	Extended MAC Address11 bit 47~32	0x0

MAC_ADDR_EXT12_31_0 (offset: 0x14E0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT12_31_0	Extended MAC Address12 bit 31~0	0x0

MAC_ADDR_EXT12_47_32 (offset: 0x14E4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT12_47_32	Extended MAC Address12 bit 47~32	0x0

MAC_ADDR_EXT13_31_0 (offset: 0x14E8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT13_31_0	Extended MAC Address13 bit 31~0	0x0

MAC_ADDR_EXT13_47_32 (offset: 0x14EC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT13_47_32	Extended MAC Address13 bit 47~32	0x0

MAC_ADDR_EXT14_31_0 (offset: 0x14F0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT14_31_0	Extended MAC Address14 bit 31~0	0x0

MAC_ADDR_EXT14_47_32 (offset: 0x14F4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT14_47_32	Extended MAC Address14 bit 47~32	0x0

MAC_ADDR_EXT15_31_0 (offset: 0x14F8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	MAC_ADDR_EXT15_31_0	Extended MAC Address15 bit 31~0	0x0

MAC_ADDR_EXT15_47_32 (offset: 0x14FC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	R/W	MAC_ADDR_EXT15_47_32	Extended MAC Address15 bit 47~32	0x0

5.9.6 MAC Security Configuration Registers (offset:0x1500)

TX_SEC_CNT0 (offset:0x1500, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_SEC_ERR_CNT	TX SEC packet error count	0

15:0	RC	TX_SEC_CPL_CNT	TX SEC packet complete count	0

RX_SEC_CNT0 (offset:0x1504, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16			Reserved	0
15:0	RC	RX_SEC_CPL_CNT	RX SEC packet complete count	0

CCMP_FC_MUTE (offset:0x1508, default: 0xC78F_C78f)

Bits	Type	Name	Description	Initial value
31:16	R/W	HT_CCMP_FC_MUTE	HT rate CCMP FC mute	0xc78f
15:0	R/W	LG_CCMP_FC_MUTE	Legacy rate CCMP FC mute	0xc78f

PN_PAD_MODE (offset:0x150C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:2			Reserved	0
1	R/W	TX_MPDU_16K_LEN	Allow TX MPDU length in TXWI > 4095 Byte 0 : Disable 1 : Enable	0
0	R/W	PN_PAD_MODE	Padding IV/EIV in RX MPDU when packet is decrypted 0 : Disable 1: Enable	0

5.9.7 MAC HCCA/PSMP CSR (offset:0x1600)

TXOP_HLDR_ADDR0 (offset:0x1600, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	TXOP_HOL_3	TXOP holder MAC address byte3	0
23:16	R/W	TXOP_HOL_2	TXOP holder MAC address byte2	0
15:8	R/W	TXOP_HOL_1	TXOP holder MAC address byte1	0
7:0	R/W	TXOP_HOL_0	TXOP holder MAC address byte0	0

TXOP_HLDR_ADDR1 (offset:0x1604, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R/W	TXOP_HOL_5	TXOP holder MAC address byte5	0
7:0	R/W	TXOP_HOL_4	TXOP holder MAC address byte4	0

Note: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

TXOP_HLDR_ET (offset:0x1608, default :0x0000_0000)

Bits	Type	Name	Description	Initial value
31:25	R		Reserved	0
24	R/W	AMPDU_ACC_EN	Accumulate AMPDU enable 0: disable, 1: enable	0
23:19	R/W	TX_DMA_TIMEOUT	When AMPDU_ACC_EN is enabled: Wait at most (TX_DMA_TIMEOUT * 32) usec for the MPDU for aggregation	0
18	R/W	TX_FBK_THRES_EN	Transmission MCS fallback threshold enable 0: disable, 1: enable	0
17:16	R/W	TX_FBK_THRES	When TX_FBK_THRES_EN is enabled, fallback when 0: less than 25% in AMPDU are success.	0

			1: less than 50% in AMPDU are success. 2: less than 75% in AMPDU are success. 3: less than 100% in AMPDU are success.	
15:5	R		Reserved	0
4	R/W	PAPE_MAP	When PAPE_MAP1S_EN is enabled: 0: only turn on PAPE0 for 1S transmission 1: only turn on PAPE1 for 1S transmission	0
3	R/W	PAPE_MAP1S_EN	Turn on only on PAPE in 1S transmission 0: disable, 1: enable	0
2	R/W	TX_BCN_HIPRI_DIS	Disable high priority beacon transmisson 1: disable, 0: enable	0
1	R/W	TX40M_BLK_EN	Block 40Mhz transmission as extension CCA is busy 0: disable, 1: enable	0
0	R/W	PER_RX_RST_EN	Baseband RX_PE per RX reset enable 0: disable, 1: enable	0

QOS_CFPOLL_RA_DW0 (offset:0x160C, default :0xXXXX_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R	CFPOLL_A1_BYTE3	Byte3 of A1 of received QoS Data (+) CF-Poll frame	X
23:16	R	CFPOLL_A1_BYTE2	Byte2 of A1 of received QoS Data (+) CF-Poll frame	X
15:8	R	CFPOLL_A1_BYTE1	Byte1 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE0	Byte0 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_A1_DW1 (offset:0x1610, default :0x0000_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
16	R	CFPOLL_A1_TOME	1: QoS CF-Poll to me 0: Qos CF-Poll not to me	X
15:8	R	CFPOLL_A1_BYTE5	Byte5 of A1 of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_A1_BYTE4	Byte4 of A1 of received QoS Data (+) CF-Poll frame	X

QOS_CFPOLL_QC (offset:0x1614, default :0x0000_XXXX)

Bits	Type	Name	Description	Initial value
31:24	R		Reserved	0
15:8	R	CFPOLL_QC_BYTE1	Byte1 of QC of received QoS Data (+) CF-Poll frame	X
7:0	R	CFPOLL_QC_BYTE0	Byte0 of QC of received QoS Data (+) CF-Poll frame	X

Note: CFPOLL_RA_DW0, CFPOLL_RA_DW1, and CFPOLL_QC are updated after the reception of QoS Data (+) CF-Poll frame and RX QoS CF-Poll interrupt (RX_QOS_CFPOLL_INT) is launched then.

EAP_INDEX (offset:0x1618, default : 0x0000_0000)

~~Bits~~	~~Type~~	~~Name~~	~~Description~~	~~Initial value~~
~~31:0~~	~~R/W~~	~~EAP_INDEX~~	~~EAP control register index~~ ~~Write: Set EAP control register index for subsequent EAP control register access~~ ~~Read: Confirm current EAP control register index~~	~~0~~

EAP_DATA (offset:0x161C, default : 0x0000_0000)

~~Bits~~	~~Type~~	~~Name~~	~~Description~~	~~Initial value~~
~~31:0~~	~~R/W~~	~~EAP_DATA~~	~~EAP control register data~~ ~~Write: Pass data to EAP control register of EAP_INDEX~~ ~~Read: Get data from EAP control register of EAP_INDEX~~	~~0~~

TX_TXBF_CFG_0 (offset: 0x1624, default: 0x4004_FC21)

Bits	Type	Name	Description	Initial value
31:16	R/W	ETXBF_FBK_RATE	Explicit TxBF feedback rate Default : HT_MM MCS4 If AUTO_FBK_PHYMODE_DIS is 0, the PHY Mode of VHT Sounding feedback frame is auto fixed in VHT PHY mode.	0x4004
15	R/W	ETXBF_FBK_EN	Explicit TxBF feedback enable 0: disable, 1: enable	0x1
14	R/W	ETXBF_FBK_SEQ_EN	Explicit TxBF feedback frame sequence number counting enable 0: disable, 1: enable	0x1
13:12	R/W	ETXBF_FBK_COEF	Explicit TxBF feedback coefficient for non-compressed form 0: 4bit 1: 2bit 2: 6bit 3: 8bit	0x3
11:10	R/W	ETXBF_FBK_CODE	Explicit TxBF feedback codebook for compressed form 0: 1 bit psi, 3 bit phi 1: 2 bit psi, 4 bit phi 2: 3 bit psi, 5 bit phi 3: 4 bit psi, 6 bit phi	0x3
9:8	R/W	ETXBF_FBK_NG	Explicit TxBF feedback number of group 0: 1 subcarrier in each group 1: 2 subcarrier in each group 2: 4 subcarrier in each group 3: reserved	0x0
7	R/W	VHT_NDPA_RATE_CHK	Validate VHT feedback only when VHT NDPA is sent in VHT mode 0: disable, 1: enable	0x0
6	R/W	TXWI_RTS_BWSIG_EN	0 : Any RTS frame for protecting non-VHT packet will be in legacy format regardless of the TXWI RTS_BWSIG of the packet. 1 : If the TXWI RTS_BWSIG of a non-VHT packet is set and an RTS protection is solicited. The RTS frame will be in signaling TA format.	0x0
5	R/W	TXBF_VALID_VHT_RATE	Enable VHT as omplicit TxBF profile update trigger frame rate	0x1
4 :3	R		Reserved	0x0
2	R/W	FORCE VHT20_9TO8_DIS	Disable auto restrict VHT 20M Max MCS to MCS 8 0: Auto restrict VHT 20M Max MCS to MCS 8 1: Don't auto switch VHT 20M MCS	0
1	R/W	AUTO_FBK_PHYMODE_DIS	Disable auto switch the PHY mode of VHT sounding feedback frame to VHT PY mode. 0: Auto switch PHY mode, 1: Don't auto switch PHY mode	0
0	R/W	AUTO_ACK_BLK_CCA_EN	Tx auto responsed ACK/BA without reference CCA. 0: disable, 1: enable	1

TX_TXBF_CFG_1 (offset: 0x1628, default: 0xFE23_727F)

Bits	Type	Name	Description	Initial value
31:27	R/W	ETXBF_FBK_TIMEOUT	Explicit TxBF feedback timeout value (unit: slot	0x1F

			time)	
26	R/W	ETXBF_FBK_TIMEOUT_EN	Explicit TxBF feedback timeout enable 0: disable, 1: enable	0x1
25	R/W	ETXBF_NDP_WAIT_EN	Explicit TxBF feedback wait for NDP 0: disable, 1: enable	0x1
24	R/W	ETXBF_BKOFF_EN	Explicit TxBF feedback backoff before transmission (Delayed Feedback) 0: disable, 1: enable	0x0
23:20	R/W	ETXBF_AIFSN	Explicit TxBF feedback backoff AIFS	0x2
19:16	R/W	ETXBF_CWMIN	Explicit TxBF feedback backoff CWMIN	0x3
15:12	R/W	ETXBF_RTY_LIMIT	Explicit TxBF feedback retry limit	0x7
11:8	R/W	ETXBF_ACK_TIMEOUT	Explicit TxBF feedback ACK timeout window (unit: slot time)	0x2
7	R/W	ETXBF_TSF_SEL	Enable select TSF value sel in feedback frame 0: Wse BSS0 TSF. 1: Auto select Rx BSS TSF	1
6:4	R/W	TXBF_VALID_TYPE	Implicit TxBF profile update trigger frame types Bit6: data frame Bit5: control frame Bit4: management frame	0x7
3:0	R/W	TXBF_VALID_RATE	Implicit TxBF profile update trigger frame rates Bit3: HT-Greenfield Bit2: HT-Mixmode Bit1: OFDM Bit0: CCK	0xF

TX_TXBF_CFG_2 (offset: 0x162C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_TSF_DELTA	The explicit TxBF feedback is applied only when the value of (local TSF timer) - (TSF timestamp of the feedback frame) is greater then or equal to ETXBF_TSF_DELTA.	0x0

TX_TXBF_CFG_3 (offset: 0x1630, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31	R/W	TX_NDP_DIS	Disable Transmit HT/VHT NDP	0x0
30:16	R		Reserved	0x0
15:0	R/W	ETXBF_TIMEOUT	Explicit TxBF profile timeout value (unit: usec)	0x0

TX_ETXBF_MAN_0 (offset: 0x1634, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_0	Explicit TxBF manual write data bit31:bit0	0x0

TX_ETXBF_MAN_1 (offset: 0x1638, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_1	Explicit TxBF manual write data bit63:bit32	0x0

TX_ETXBF_MAN_2 (offset: 0x163C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_2	Explicit TxBF manual write data bit95:bit64	0x0

TX_ETXBF_MAN_3 (offset: 0x1640, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:0	R/W	ETXBF_MAN_DATA_3	Explicit TxBF manual write data bit127:bit96	0x0

TX_ETXBF_MAN_4 (offset: 0x1644, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:27	R		Reserved	0x0
26	R/W	ETXBF_MAN_EN	Explicit TxBF manual write enable	0x0
25	R/W	ETXBF_MAN_KICK	Explicit TxBF manual write kick/busy Write- 1 to kick explicit TxBF manual write Read- 0: idle, 1: busy	0x0
24	R/W	ETXBF_MAN_TAG	Explicit TxBF manual write tag bit	0x0
23	R/W	ETXBF_MAN_COMP	Explicit TxBF manual write compress bit	0x0
22:16	R/W	ETXBF_MAN_SUBC	Explicit TxBF manual write sub-carrier bit6:bit0	0x0
15:0	R/W	ETXBF_MAN_DATA_4	Explicit TxBF manual write data bit143:bti128	0x0

PROT_AUTO_TX_CFG (offset: 0x1648, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:28	R/W		Reserved	0x0
27:24	R/W	AUTO_PWR_ADJ	Tx power adjustment of auto response frame. The format is the same with tx_pwr_adj in TXWI.	0x0
23:16	R/W	AUTO_STR_MODE	Stream mode of auto response frame The format is the same with Tx stream mode in TXWI.	0x0
15:12	R/W		Reserved	0x0
11:8	R/W	PROT_PWR_ADJ	Tx power adjustment of protection frame. The format is the same with tx_pwr_adj in TXWI.	0x0
7:0	R/W	PROT_STR_MODE	Stream mode of protection frame.The format is the same with Tx stream mode in TXWI.	0x0

5.9.8 MAC Statistic Counters (offset:0x1700)

RX_STA_CNT0 (offset:0x1700, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	PHY_ERRCNT	RX PHY error frame count	0
15:0	RC	CRC_ERRCNT	RX CRC error frame count	0

Note1: RX PHY error means PSDU length is shorter than indicated by PLCP.

Note2: RX PHY error is also treated as CRC error.

RX_STA_CNT1 (offset:0x1704, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	PLPC_ERRCNT	RX PLCP error count	0
15:0	RC	CCA_ERRCNT	CCA false alarm count	0

Note1: CCA false alarm means there is no PLCP after CCA indication.

Note2: RX PLCP error means there is no PSDU after PLCP indication.

RX_STA_CNT2 (offset:0x1708, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value

31:16	RC	RX_OVFL_CNT	RX FIFO overflow frame count	0
15:0	RC	RX_DUPL_CNT	RX duplicated filtered frame count	0

Note: MAC will NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow.

However, MAC will respond when frame is duplicated filtered.

TX_STA_CNT0 (offset:0x170C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_BCN_CNT	TX beacon count	0
15:0	RC	TX_FAIL_CNT	Failed TX count	0

TX_STA_CNT1 (offset:0x1710, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_RTY_CNT	TX retransmission count	0
15:0	RC	TX_SUCC_CNT	Successful TX count	0

TX_STA_CNT2 (offset:0x1714, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_UDFL_CNT	TX underflow count	0
15:0	RC	TX_ZERO_CNT	TX zero length frame count	0

TX_STAT_FIFO (offset:0x1718, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R	TXQ_RATE	TX success rate (The same as TXWI rate format). bit [28] means Implicit TxBF is applied. bit [27] means Explicit TxBF is applied.	*
15:8	R	TXQ_WCID	TX WCID	*
7	R	TXQ_ACKREQ	TX acknowledge required 0: not required 1: required	*
6	R	TXQ_AGG	TX aggregate 0: non-aggregated 1: aggregated	*
5	R	TXQ_OK	TX success 0: failed 1: success	*
4:1	R		Reserved	*
0	RC	TXQ_VLD	TX status queue valid 0: queue empty 1: valid	0

Note: TX status FIFO size = 16.

TX_NAG_AGG_CNT (offset:0x171C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_CNT	Aggregate TX count	0
15:0	RC	TX_NAG_CNT	Non-aggregate TX count	0

TX_AGG_CNT0 (offset:0x1720, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_2_CNT	Aggregate Size = 2 MPDU count	0
15:0	RC	TX_AGG_1_CNT	Aggregate Size = 1 MPDU count	0

TX_AGG_CNT1 (offset:0x1724, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_4_CNT	Aggregate Size = 4 MPDU count	0
15:0	RC	TX_AGG_3_CNT	Aggregate Size = 3 MPDU count	0

TX_AGG_CNT2 (offset:0x1728, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_6_CNT	Aggregate Size = 6 MPDU count	0
15:0	RC	TX_AGG_5_CNT	Aggregate Size = 5 MPDU count	0

TX_AGG_CNT3 (offset:0x172C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_8_CNT	Aggregate Size = 8 MPDU count	0
15:0	RC	TX_AGG_7_CNT	Aggregate Size = 7 MPDU count	0

TX_AGG_CNT4 (offset:0x1730, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_10_CNT	Aggregate Size = 10 MPDU count	0
15:0	RC	TX_AGG_9_CNT	Aggregate Size = 9 MPDU count	0

TX_AGG_CNT5 (offset:0x1734, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_12_CNT	Aggregate Size = 12 MPDU count	0
15:0	RC	TX_AGG_11_CNT	Aggregate Size = 11 MPDU count	0

TX_AGG_CNT6 (offset:0x1738, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_14_CNT	Aggregate Size = 14 MPDU count	0
15:0	RC	TX_AGG_13_CNT	Aggregate Size = 13 MPDU count	0

TX_AGG_CNT7 (offset:0x173C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_16_CNT	Aggregate Size > 16 MPDU count	0
15:0	RC	TX_AGG_15_CNT	Aggregate Size = 15 MPDU count	0

MPDU_DENSITY_CNT (offset:0x1740, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RX_ZERO_DEL_CNT	RX zero length delimiter count	0
15:0	RC	TX_ZERO_DEL_CNT	TX zero length delimiter count	0

RTS_TX_CNT (offset:0x1744, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	RTS_TX_FAIL_CNT	RTS TX fail count	0
15:0	RC	RTS_TX_OK_CNT	RTS TX OK count	0

CTS_TX_CNT (offset:0x1748, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	RC	CTSTS_TX_CNT	CTS-to-self TX count	0

TX_AGG_CNT8 (offset:0x174C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_18_CNT	Aggregate Size = 18 MPDU count	0
15:0	RC	TX_AGG_17_CNT	Aggregate Size = 17 MPDU count	0

TX_AGG_CNT9 (offset:0x1750, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_20_CNT	Aggregate Size = 20 MPDU count	0
15:0	RC	TX_AGG_19_CNT	Aggregate Size = 19 MPDU count	0

TX_AGG_CNT10 (offset:0x1754, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_22_CNT	Aggregate Size = 22 MPDU count	0
15:0	RC	TX_AGG_21_CNT	Aggregate Size = 21 MPDU count	0

TX_AGG_CNT11 (offset:0x1758, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_24_CNT	Aggregate Size = 24 MPDU count	0
15:0	RC	TX_AGG_23_CNT	Aggregate Size = 23 MPDU count	0

TX_AGG_CNT12 (offset:0x175C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_26_CNT	Aggregate Size = 26 MPDU count	0
15:0	RC	TX_AGG_25_CNT	Aggregate Size = 25 MPDU count	0

TX_AGG_CNT13 (offset:0x1760, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_28_CNT	Aggregate Size = 28 MPDU count	0
15:0	RC	TX_AGG_27_CNT	Aggregate Size = 27 MPDU count	0

TX_AGG_CNT14 (offset:0x1764, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_30_CNT	Aggregate Size = 30 MPDU count	0
15:0	RC	TX_AGG_29_CNT	Aggregate Size = 29 MPDU count	0

TX_AGG_CNT 15(offset:0x1768, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_32_CNT	Aggregate Size = 32 MPDU count	0
15:0	RC	TX_AGG_31_CNT	Aggregate Size = 31 MPDU count	0

WCID_A_TX_CNT (offset:0x176C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_A_TXRTY_CNT	WCDI_A TX retry count	0
15:0	RC	WCID_A_TXOK_CNT	WCDI_A TX OK count	0

WCID_B_TX_CNT (offset:0x1770, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_B_TXRTY_CNT	WCDI_B TX retry count	0
15:0	RC	WCID_B_TXOK_CNT	WCDI_B TX OK count	0

WCID_C_TX_CNT (offset:0x1774, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_C_TXRTY_CNT	WCDI_C TX retry count	0
15:0	RC	WCID_C_TXOK_CNT	WCDI_C TX OK count	0

WCID_D_TX_CNT (offset:0x1778, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_D_TXRTY_CNT	WCDI_D TX retry count	0
15:0	RC	WCID_D_TXOK_CNT	WCDI_D TX OK count	0

WCID_E_TX_CNT (offset:0x177C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_E_TXRTY_CNT	WCDI_E TX retry count	0
15:0	RC	WCID_E_TXOK_CNT	WCDI_E TX OK count	0

WCID_F_TX_CNT (offset:0x1780, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_F_TXRTY_CNT	WCDI_F TX retry count	0
15:0	RC	WCID_F_TXOK_CNT	WCDI_F TX OK count	0

WCID_G_TX_CNT (offset:0x1784, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_G_TXRTY_CNT	WCDI_G TX retry count	0
15:0	RC	WCID_G_TXOK_CNT	WCDI_G TX OK count	0

WCID_H_TX_CNT (offset:0x1788, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	WCID_H_TXRTY_CNT	WCDI_H TX retry count	0
15:0	RC	WCID_H_TXOK_CNT	WCDI_H TX OK count	0

WCID_X_SELECT (offset:0x178C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	WCID_D_SELECT	WCID selection for WCID_D TX counters	0
23:16	R/W	WCID_C_SELECT	WCID selection for WCID_C TX counters	0
15:8	R/W	WCID_B_SELECT	WCID selection for WCID_B TX counters	0
7:0	R/W	WCID_A_SELECT	WCID selection for WCID_A TX counters	0

WCID_X_SELECT (offset:0x1790, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:24	R/W	WCID_H_SELECT	WCID selection for WCID_H TX counters	0
23:16	R/W	WCID_G_SELECT	WCID selection for WCID_G TX counters	0
15:8	R/W	WCID_F_SELECT	WCID selection for WCID_F TX counters	0
7:0	R/W	WCID_E_SELECT	WCID selection for WCID_E TX counters	0

TX_REPORT_CNT (offset:0x1794, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:0	RC	TX_REPORT_CNT	Transmission complete of TX frame of which TXWI.TX_RPT is set to 1.	0

TX_STAT_FIFO_EXT (offset:0x1798, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	R		Reserved	0
15:8	R	TX_PKT_ID	TX Packet ID (copied from per packet TXWI)	*
7:0	R	TX_RTY_CNT	Tx retry count	*

TX_AGG_CNT 16(offset:0x179C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_34_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_33_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 17(offset:0x17A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_36_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_35_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 18(offset:0x17A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_38_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_37_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 19(offset:0x17A8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_40_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_39_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 20(offset:0x17AC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_42_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_41_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 21(offset:0x17B0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_44_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_43_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 22(offset:0x17B4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_46_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_45_CNT	Aggregate Size = 33 MPDU count	0

TX_AGG_CNT 23(offset:0x17B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial value
31:16	RC	TX_AGG_48_CNT	Aggregate Size = 34 MPDU count	0
15:0	RC	TX_AGG_47_CNT	Aggregate Size = 33 MPDU count	0

5.9.9 MAC search table (offset: 0x1800)

RX WCID search entry format (8 bytes)

Offset	Type	Name	Description	Initial value
0x00	R/W	WC_MAC_ADDR0	Client MAC address byte0	0x00
0x01	R/W	WC_MAC_ADDR1	Client MAC address byte1	0x00
0x02	R/W	WC_MAC_ADDR2	Client MAC address byte2	0x00
0x03	R/W	WC_MAC_ADDR3	Client MAC address byte3	0x00
0x04	R/W	WC_MAC_ADDR4	Client MAC address byte4	0x00
0x05	R/W	WC_MAC_ADDR5	Client MAC address byte5	0x00
0x06	R/W	BA_SESS_MASK0	BA session mask (lower) Bit0 for TID0 Bit7 for TID7	0x00
0x07	R/W	BA_SESS_MASK1	BA session mask (upper) Bit8 for TID8 Bit15 for TID15	0x00

RX WCID search table (offset:0x1800)

Offset	Type	Name	Description	Initial value
0x1800	R/W	WC_ENTRY_0	WC MAC address with WCID=0	0
0x1808	R/W	WC_ENTRY_1	WC MAC address with WCID=1	0
….	R/W	….	WC MAC address with WCID=2~126	0
0x1BF8	R/W	WC_ENTRY_127	WC MAC address with WCID=127	0
0x1C00	R/W	WCID0_TX_RATE	B15:B0: WCID0 TX Rate	0
0x1C08	R/W	WCID1_TX_RATE	B15:B0: WCID1TX Rate	0
….	R/W	….	B15:B0: WCID=2~126 TX Rate	0
0x1FF8	R/W	WCID127_TX_RATE	B15:B0: WCID127 TX Rate	0

Note1: WCID=Wireless Client ID

5.9.10 Security table/CIS/Beacon/NULL frame (offset: 0x4000)

Security Entry format

Security Key Format (8DW)

Offset	Type	Name	Description	Initial value

0x00	R/W	SECKEY_DW0	Security key byte3~0	*
0x04	R/W	SECKEY_DW1	Security key byte7~4	*
0x08	R/W	SECKEY_DW2	Security key byte11~8	*
0x0C	R/W	SECKEY_DW3	Security key byte15~12	*
0x10	R/W	TXMIC_DW0	TX MIC key byte3~0	*
0x14	R/W	TXMIC_DW1	TX MIC key byte7~4	*
0x18	R/W	RXMIC_DW0	RX MIC key byte3~0	*
0x1C	R/W	RXMIC_DW1	RX MIC key byte7~4	*

Note:

1. For WEP40, CKIP40, only byte4~0 of security key are valid.

2. For WEP104, CKIP104, only byte12~0 of security key are valid.

3. For TKIP, AES, all the bytes of security key are valid.

4. TX/RX MIC key is used only for TKIP MIC calculation.

5. 128 byte space of TX/RX MIC key are used together for WAPI MIC key.

IV/EIV/WAPI_PN format (4 DW)

When TXINFO.WIV=0, hardware will auto lookup IV/EIV/WAPI_PN from this table and update IV/EIV/WAPI_PN after encryption is finished.

Offset	Type	Name	Description	Initial value
0x00	R/W	IV_FIELED	IV field	*
0x04	R/W	EIV_FIELED	EIV field	*

Offset	Type	Name	Description	Initial value
0x00	R/W	WAPI_PN_MSB	WAPI PN byte11-byte8	*
0x04	R/W	WAPI_PN_MSB	WAPI PN byte15-byte12	*

Note1: The key index and extension IV bit shall be initialized by software. The MSB octet of IV will not be modified by hardware.

Note2: IV/EIV packet number (PN) counter modes:

a. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.

b. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f) is generated by hardware.

c. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.

d. For non-WAPI mode, PN = PN + 1 after each encryption.

e. For WAPI mode, PN={WAPI_PN_MSB_1[31:0], WAPI_PN_MSB_0[31:0], EIV[31:0], IV[31:0]}.

f. For WAPI mode, PN=PN+2 when WAPI_MC_BC=0 in WCID attribute.

g. For WAPI mode, PN=PN+1 when WAPI_MC_BC=1 in WCID attribute.

Note3: Software may initialize the PN counter to any value.

WCID attribute entry format (1DW)

Offset	Type	Name	Description	Initial value
31:24	R/W	WAPI_KEYID_BYTE	WAPI KeyID byte	*

			0-1: WAPI Key ID 2-255: reserved	
23:16	R/W	WAPI_RSV_BYTE	WAPI reserved byte (set to 0)	*
15	R/W	WAPI_MCBC	WAPI broadcast/multicast packet number (PN) increment 0: unicast, PN = PN + 2; 1: multicast/broadcast, PN = PN + 1;	*
14:12	R/W		Reserved	*
11	R/W	BSS_IDX_MBS	Use together with BSS_IDX(bit6:bit4), (BSS_IDX_MSB *8 + BSS_IDX) = BSS Index of the WCID	*
10	R/W	RX_PKEY_MODE_MSB	Use together with RX_PKEY_MODE(bit3:bit1), (RX_PKEY_MODE_MSB *8 + RX_PKEY_MODE) = 0~7: as listed in RX_PKEY_MODE 8: WAPI 9-15: Reserved	*
9:7	R/W	RXWI_UDF	RXWI user define field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	R/W	BSS_IDX	Multiple-BSS index for the WCID	*
3:1	R/W	RX_PKEY_MODE	Pair-wise key security mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128	*
0	R/W	RX_PKEY_EN	Key table selection 0: shared key table 1: pair-wise key table	*

Share key mode entry format (1DW)

Bits	Type	Name	Description	Initial value
31:28	R/W	SKEY_MODE_7+	Shared key7+(8x) mode, x=0~3	*
27:24	R/W	SKEY_MODE_6+	Shared key6+(8x) mode, x=0~3	*
23:20	R/W	SKEY_MODE_5+	Shared key5+(8x) mode, x=0~3	*
19:16	R/W	SKEY_MODE_4+	Shared key4+(8x) mode, x=0~3	*
15:12	R/W	SKEY_MODE_3+	Shared key3+(8x) mode, x=0~3	*
11:8	R/W	SKEY_MODE_2+	Shared key2+(8x) mode, x=0~3	*
7:4	R/W	SKEY_MODE_1+	Shared key1+(8x) mode, x=0~3	*
3:0	R/W	SKEY_MODE_0+	Shared key0+(8x) mode, x=0~3	*

Key mode definition:

0: No security 1: WEP40 2: WEP104 3: TKIP

4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128

8: WAPI 9~15: Reserved

Security Table

Pair-wise key table (offset:0x8000)

Offset	Type	Name	Description	Initial value
0x8000	R/W	PKEY_0	Pair-wise key for WCID0	*
0x8020	R/W	PKEY_1	Pair-wise key for WCID1	*
....	R/W	....	Pair-wise key for WCID2~253	*
0x9FC0	R/W	PKEY_254	Pair-wise key for WCID254	*
0x9FE0	R/W	PKEY_255	Pair-wise key for WCID255 (not used)	*

IV/EIV table (offset:0xa000)

Offset	Type	Name	Description	Initial value
0xA000	R/W	IVEIV_0	IV/EIV for WCID0	*
0xA008	R/W	IVEIV_1	IV/EIV for WCID1	*
….	R/W	….	IV/EIV for WCID2~253	*
0xA7F0	R/W	IVEIV_254	IV/EIV for WCID254	*
0xA7F8	R/W	IVEIV_255	IV/EIV for WCID255 (not used)	*

WCID attribute table (offset:0xa800)

Offset	Type	Name	Description	Initial value
0xA800	R/W	WCID_ATTR_0	WCID Attribute for WCID0	*
0xA804	R/W	WCID_ATTR_1	WCID Attribute for WCID1	*
….	R/W	….	WCID Attribute for WCID2~253	*
0xABF8	R/W	WCID_ATTR_254	WCID Attribute for WCID254	*
0xABFC	R/W	WCID_ATTR_255	WCID Attribute for WCID255	*

Shared Key Table (offset:0xaC00)

Offset	Type	Name	Description	Initial value
0xAC00	R/W	SKEY_0	Shared key for BSS_IDX=0, KEY_IDX=0	*
0xAC20	R/W	SKEY_1	Shared key for BSS_IDX=0, KEY_IDX=1	*
0xAC40	R/W	SKEY_2	Shared key for BSS_IDX=0, KEY_IDX=2	*
0xAC60	R/W	SKEY_3	Shared key for BSS_IDX=0, KEY_IDX=3	*
0xAC80	R/W	SKEY_4	Shared key for BSS_IDX=1, KEY_IDX=0	*
0xACA0	R/W	SKEY_5	Shared key for BSS_IDX=1, KEY_IDX=1	*
0xACC0	R/W	SKEY_6	Shared key for BSS_IDX=1, KEY_IDX=2	*
0xACE0	R/W	SKEY_7	Shared key for BSS_IDX=1, KEY_IDX=3	*
0xAD00	R/W	SKEY_8	Shared key for BSS_IDX=2, KEY_IDX=0	*
0xAD20	R/W	SKEY_9	Shared key for BSS_IDX=2, KEY_IDX=1	*
0xAD40	R/W	SKEY_10	Shared key for BSS_IDX=2, KEY_IDX=2	*
0xAD60	R/W	SKEY_11	Shared key for BSS_IDX=2, KEY_IDX=3	*
0xAD80	R/W	SKEY_12	Shared key for BSS_IDX=3, KEY_IDX=0	*
0xADA0	R/W	SKEY_13	Shared key for BSS_IDX=3, KEY_IDX=1	*
0xADC0	R/W	SKEY_14	Shared key for BSS_IDX=3, KEY_IDX=2	*
0xADE0	R/W	SKEY_15	Shared key for BSS_IDX=3, KEY_IDX=3	*
0xAE00	R/W	SKEY_16	Shared key for BSS_IDX=4, KEY_IDX=0	*
0xAE20	R/W	SKEY_17	Shared key for BSS_IDX=4, KEY_IDX=1	*
0xAE40	R/W	SKEY_18	Shared key for BSS_IDX=4, KEY_IDX=2	*
0xAE60	R/W	SKEY_19	Shared key for BSS_IDX=4, KEY_IDX=3	*
0xAE80	R/W	SKEY_20	Shared key for BSS_IDX=5, KEY_IDX=0	*
0xAEA0	R/W	SKEY_21	Shared key for BSS_IDX=5, KEY_IDX=1	*
0xAEC0	R/W	SKEY_22	Shared key for BSS_IDX=5, KEY_IDX=2	*
0xAEE0	R/W	SKEY_23	Shared key for BSS_IDX=5, KEY_IDX=3	*
0xAF00	R/W	SKEY_24	Shared key for BSS_IDX=6, KEY_IDX=0	*
0xAF20	R/W	SKEY_25	Shared key for BSS_IDX=6, KEY_IDX=1	*
0xAF40	R/W	SKEY_26	Shared key for BSS_IDX=6, KEY_IDX=2	*
0xAF60	R/W	SKEY_27	Shared key for BSS_IDX=6, KEY_IDX=3	*
0xAF80	R/W	SKEY_28	Shared key for BSS_IDX=7, KEY_IDX=0	*
0xAFA0	R/W	SKEY_29	Shared key for BSS_IDX=7, KEY_IDX=1	*
0xAFC0	R/W	SKEY_30	Shared key for BSS_IDX=7, KEY_IDX=2	*
0xAFE0	R/W	SKEY_31	Shared key for BSS_IDX=7, KEY_IDX=3	*

Shared Key Mode (offset:0xb000)

Offset	Type	Name	Description	Initial value
0xB000	R/W	SKEY_MODE_0_7	Shared mode for SKEY0-SKEY7	*
0xB004	R/W	SKEY_MODE_8_15	Shared mode for SKEY8-SKEY15	*
0xB008	R/W	SKEY_MODE_16_23	Shared mode forSKEY16-SKEY23	*
0xB00C	R/W	SKEY_MODE_24_31	Shared mode for SKEY24-SKEY31	*

Spared Memory Space Mode (offset:0x7010~0x73EC)

Shared Key Mode Extension (for BSS_IDX=8~15) (offset:0xb3F0)

Offset	Type	Name	Description	Initial value
0xB3F0	R/W	SKEY_MODE_32_39	Shared mode for SKEY32-SKEY39	*
0xB3F4	R/W	SKEY_MODE_40_47	Shared mode for SKEY40-SKEY47	*
0xB3F8	R/W	SKEY_MODE_48_55	Shared mode forSKEY48-SKEY55	*
0xB3FC	R/W	SKEY_MODE_56_63	Shared mode for SKEY56-SKEY63	*

Shared Key Table Extension (for BSS_IDX=8~15) (offset:0xb400)

Offset	Type	Name	Description	Initial value
0xB400	R/W	SKEY_32	Shared key for BSS_IDX=8, KEY_IDX=0	*
0xB420	R/W	SKEY_33	Shared key for BSS_IDX=8, KEY_IDX=1	*
0xB440	R/W	SKEY_34	Shared key for BSS_IDX=8, KEY_IDX=2	*
0xB460	R/W	SKEY_35	Shared key for BSS_IDX=8, KEY_IDX=3	*
0xB480	R/W	SKEY_36	Shared key for BSS_IDX=9, KEY_IDX=0	*
0xB4A0	R/W	SKEY_37	Shared key for BSS_IDX=9, KEY_IDX=1	*
0xB4C0	R/W	SKEY_38	Shared key for BSS_IDX=9, KEY_IDX=2	*
0xB4E0	R/W	SKEY_39	Shared key for BSS_IDX=9, KEY_IDX=3	*
0xB500	R/W	SKEY_40	Shared key for BSS_IDX=10, KEY_IDX=0	*
0xB520	R/W	SKEY_41	Shared key for BSS_IDX=10, KEY_IDX=1	*
0xB540	R/W	SKEY_42	Shared key for BSS_IDX=10, KEY_IDX=2	*
0xB560	R/W	SKEY_43	Shared key for BSS_IDX=10, KEY_IDX=3	*
0xB580	R/W	SKEY_44	Shared key for BSS_IDX=11, KEY_IDX=0	*
0xB5A0	R/W	SKEY_45	Shared key for BSS_IDX=11, KEY_IDX=1	*
0xB5C0	R/W	SKEY_46	Shared key for BSS_IDX=11, KEY_IDX=2	*
0xB5E0	R/W	SKEY_47	Shared key for BSS_IDX=11, KEY_IDX=3	*
0xB600	R/W	SKEY_48	Shared key for BSS_IDX=12, KEY_IDX=0	*
0xB620	R/W	SKEY_49	Shared key for BSS_IDX=12, KEY_IDX=1	*
0xB640	R/W	SKEY_50	Shared key for BSS_IDX=12, KEY_IDX=2	*
0xB660	R/W	SKEY_51	Shared key for BSS_IDX=12, KEY_IDX=3	*
0xB680	R/W	SKEY_52	Shared key for BSS_IDX=13, KEY_IDX=0	*
0xB6A0	R/W	SKEY_53	Shared key for BSS_IDX=13, KEY_IDX=1	*
0xB6C0	R/W	SKEY_54	Shared key for BSS_IDX=13, KEY_IDX=2	*
0xB6E0	R/W	SKEY_55	Shared key for BSS_IDX=13, KEY_IDX=3	*
0xB700	R/W	SKEY_56	Shared key for BSS_IDX=14, KEY_IDX=0	*
0xB720	R/W	SKEY_57	Shared key for BSS_IDX=14, KEY_IDX=1	*
0xB740	R/W	SKEY_58	Shared key for BSS_IDX=14, KEY_IDX=2	*
0xB760	R/W	SKEY_59	Shared key for BSS_IDX=14, KEY_IDX=3	*
0xB780	R/W	SKEY_60	Shared key for BSS_IDX=15, KEY_IDX=0	*
0xB7A0	R/W	SKEY_61	Shared key for BSS_IDX=15, KEY_IDX=1	*
0xB7C0	R/W	SKEY_62	Shared key for BSS_IDX=15, KEY_IDX=2	*
0xB7E0	R/W	SKEY_63	Shared key for BSS_IDX=15, KEY_IDX=3	*

WAPI PN table (extension of IV/EIV table) (offset:0xb800)

Offset	Type	Name	Description	Initial value
0xB800	R/W	WAPI_PN_MSB_0	Extension byte11-byte8 of WAPI PN for WCID0	*
0xB804	R/W	WAPI_PN_MSB_0	Extension byte15-byte12 of WAPI PN for WCID0	*
0xB808	R/W	WAPI_PN_MSB_1	Extension byte11-byte8 of WAPI PN for WCID1	*
0xB80C	R/W	WAPI_PN_MSB_1	Extension byte15-byte12 of WAPI PN for WCID1	*
....	R/W	....	Extension byte11-byte8 of WAPI PN for WCID2~254	*
....	R/W	....	Extension byte15-byte12 of WAPI PN for WCID2~254	*
0xBFF8	R/W	WAPI_PN_MSB_255	Extension byte11-byte8 of WAPI PN for WCID255	*
0xBFFC	R/W	WAPI_PN_MSB_255	Extension byte15-byte12 of WAPI PN for WCID255	*

Note: Do not set WIV bit to 1 when WAPI mode is turned on.

5.10 SPI command mode registers

Driver/Firmware/TESTIF	Base Address
PCIe WLAN driver	0xE004_0000
Reserve	0xF004_0000
Andes firmware/TESTIF	0x0050_0000

Note: read for FLASH data, write for SPI command.

SPI_WR_BYTE (offset: 0x0000, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	WO	SPI_WR_BYTE	Write 1 byte on SPI.	8'b0

SPI_WR_LAST_BYTE (offset: 0x0004, default: 0x0)

Bits	Type	Name	Description	Initial value
31:8	-	-	Reserved	-
7:0	WO	SPI_WR_LAST_BYTE	Write the last byte on SPI.	8'b0

SPI_WR_WORD_BE (offset: 0x0008, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	WO	SPI_WR_WORD_BE	Write 1 word with big endian on SPI.	32'b0

SPI_WR_LAST_WORD_BE (offset: 0x000C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	WO	SPI_WR_LAST_WORD_BE	Write the last word with big endian on SPI.	32'b0

SPI_WR_WORD_LE (offset: 0x0010, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	WO	SPI_WR_WORD_LE	Write 1 word with little endian on SPI.	32'b0

SPI_WR_LAST_WORD_LE (offset: 0x0014, default: 0x0)

Bits	Type	Name	Description	Initial value
31:0	WO	SPI_WR_LAST_WORD_LE	Write the last word with little endian on SPI.	32'b0

SPI_RD_BYTE (offset: 0x0018, default: 0x0)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	-
0	WO	SPI_RD_BYTE	Read 1 byte on SPI.	1'b0

SPI_RD_LAST_BYTE (offset: 0x001C, default: 0x0)

Bits	Type	Name	Description	Initial value
31:1	-	-	Reserved	-
0	WO	SPI_RD_LAST_BYTE	Read the last byte on SPI.	1'b0

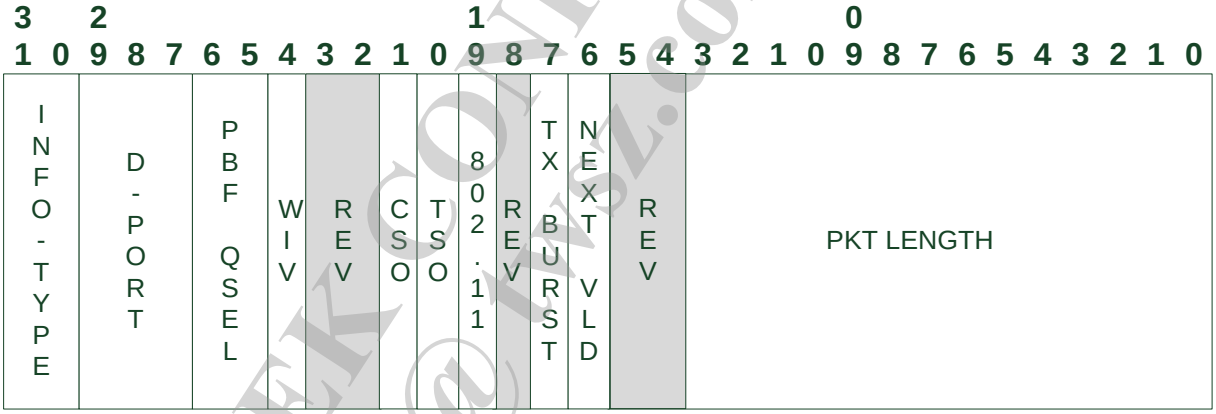
5.11 Descriptor and Wireless information

5.11.1 TXINFO for packet

For new MCU, there are 2 types of TXINFO. One is legacy mode for normal packet and the other is command packet for MCU to do more applications. Bits 31 to 30 of TXINFO are used to indicate the packet type.

- ***INFO_TYPE**: Type of this packet*
  - 00 : normal packet
  - 01 : command packet
  - Others: Reserved

5.11.2 Normal Packet(INFO_TYPE == 2'b00)



TXINFO is prepared by host driver and used for passing information to DMA. Its size is 1 DW and put at the head of each Tx frame. Following is the detail description of each field of TXINFO:

- ***INFO_TYPE**: Type of this packet*
  - 00 : normal packet
  - 01 : command packet
  - Others: Reserved
- ***D_PORT[2:0]**: This packet will be forwarded through which FCE port.*
  - ***3'b000** : WLAN port*
  - ***3'b001 : CPU RX port***
  - ***3'b010 : CPU TX port***
  - ***3'b011 : Host port (PCIe)***
  - ***3'b100 : Virtual CPU RX port***

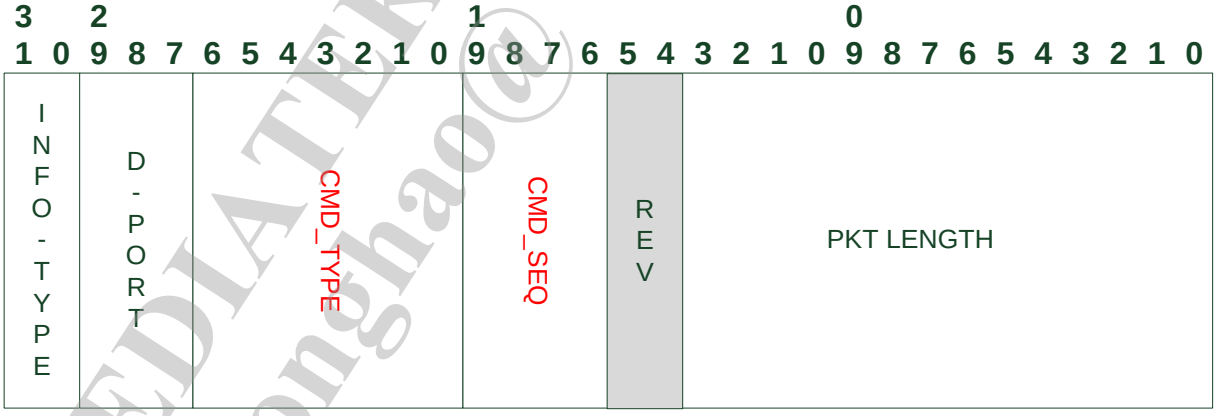
- ***3'b101 : Virtual CPU TX port***
- ***3'b110 : discard***

- ***PBF QSEL[1:0]:*** packet buffer Q selection.

QSEL	Dest. In PBF	Function	Tx Priority
2'b00	Tx0Q	Management	Highest
2'b01	Tx1Q	HCCA	Medium
2'b10	Tx2Q	EDCA	Lowest for Channel1
2'b11	Tx3Q	EDCA	Lowest for Channel2

- ***WIV:*** with IV.
- ***CSO****: checksum offload. When CSO is 1, this packet needs to do checksum.*
- ***TSO****: TCP segmentation offload enable. When TSO is 1, this packet needs to do TCP segmentation.*
- ***802.11****: This is a 802.11 packet or 802.3 packet. 1:802.11, 0:802.3*
- ***TxBurst:*** force DMA transmit frame from current selected endpoint.
- ***NextVLD:*** host driver info DMA current frame is not he last frame in current Tx queue.
- ***TxPacketLength[15:0]:*** *this field specify the frame length in unit of byte. It includes WI, 802.11 header, and payload, but TXINF is not included.*

5.11.3 Command Packet(INFO_TYPE == 2'b01)

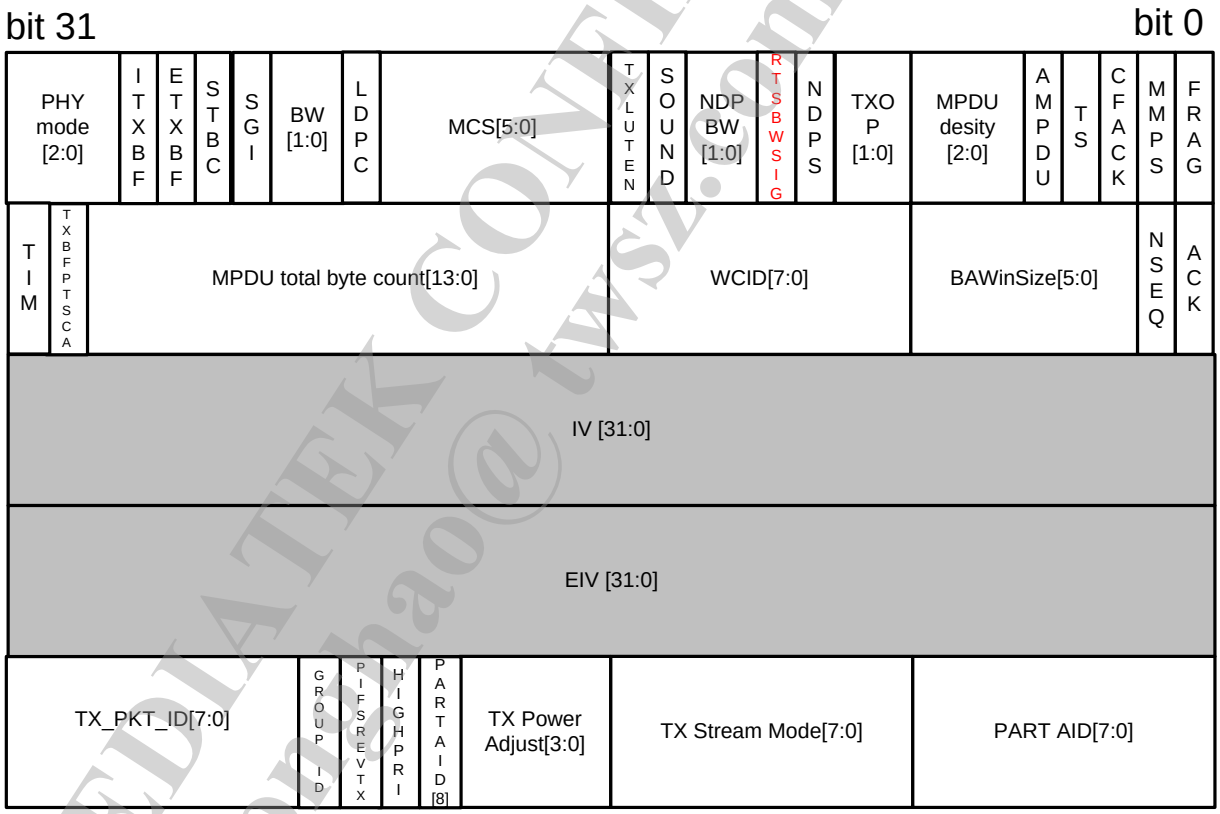


- ***INFO_TYPE****: Type of this packet*
  - 00 : normal packet
  - 01 : command packet
  - Others : Reserved
- ***PORT[2:0]****: This packet will be forwarded through which FCE port.*
  - ***3'b000*** *: WLAN port*

- ***3'b001 : CPU RX port***
- ***3'b010 : CPU TX port***
- ***3'b011 : Host port (PCIe)***
- ***3'b100 : Virtual CPU RX port***
- ***3'b101 : Virtual CPU TX port***
- ***3'b110 : discard***

- ***CMD_TYPE[6:0]****: packet command type*
- ***CMD_SEQ[3:0]****: packet command sequence*

5.11.4 TXWI format



- ***FRAG***: 1: to inform TKIP engine this is a fragment, so that TKIP MIC is appended by driver at the last fragment; hardware TKIP engine only need to insert IV/EIV and ICV.
- ***MMPS***: 1: the remote peer is in dynamic MIMO-PS mode
- ***CFACK***: 1: if an ACK is required to the same peer as this outgoing DATA frame, then MAC TX will send a single DATA+CFACK frame instead of separate ACK and DATA frames. 0: no piggyback ACK allowed for the RA of this frame.

- ***TS***: 1: This is a BEACON or ProbeResponse frame and MAC needs to auto insert 8-byte timestamp after 802.11 WLAN header.
- ***AMPDU***: this frame is eligible for AMPDU. MAC TX will aggregate subsequent outgoing frames having <same RA, same TID, AMPDU=1> whenever TXOP allows. Even there's only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC will still package it as AMPDU with implicit BAR. This adds only 4-byte AMPDU delimiter overhead into the outgoing frame and imply the response frame is a BA instead of ACK. NOTE: driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge in AMPDU case.
- ***MPDU density***: 1/4usec ~ 16usec per-peer parameter used in outgoing A-MPDU. (This field complies with the "minimum MDPU Starting Spacing" of the A-MPDU parameter field of draft 1.08).

000- no restriction
001- 1/4 µsec
010- 1/2 µsec
011- 1 µsec
100- 2 µsec
101- 4 µsec
110- 8 µsec
111- 16 µsec

- ***TXOP***: TX back off mode. 0: HT TXOP rule; 1: PIFS TX; 2: SIFS (only when previous frame exchange is successful); 3: Back off.
- ***NDPS***: Number of stream in NDP, 0: 1s, 1: 2s
- ***RTS BWSIG*** : The RTS for protecting the packet will be sent in signaling TA format. (only valid when MAC register TXWI_RTS_BWSIG_EN = 1 and the PHY mode of the packet is non-VHT
- ***NDPBW***: NDP bandwidth, 0: 20MHz, 1: 40MHz. 2: 80MHz
- ***TXLUTEN:*** TX RATE Looks up by MAC rate table(0x1C00~0x1FF8) instead of tx rate in txwi.
- ***TXBFK:*** Disable TX auto fallback for this frame, 1: disable, 0: follow the register setting
- ***TXRPT:*** TX report tag. Set to 1: TX_REPROT_CNT increase by one. Set to 0: do nothing.
- ***"MCS/BW/ShortGI/PHY mode /OFDM/MIMO"***: TX data rate & MIMO parameters for this outgoing frame to be filled into BBP
- ***LDPC:*** LDPC encode the Tx frame.
- ***ITXBF***: Implicit TxBF enable
- ***SOUND***: Sounding packet enable
- ***ETXBF***: Explicit TxBF enable
- ***ACK***: this bit informs MAC to wait for ACK or not after transmission of the frame. Event though QOD DATA frame has ACK policy in its QOS CONTROL field, MAC TX solely depends on this ACK bit to decide waiting of ACK or not.
- ***NSEQ***: 1: to use the special h/w SEQ number register in MAC block.
- ***BA window size***: tell MAC the maximum number of to-be-BAed frames is allowed of the RA (RA's BA re-

ordering buffer size)

- ***WCID (Wireless Client Index)*** : lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. TX rate, TX power, pair-wise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- ***MSDU total byte count or L2 header length:*** total length of this frame. If this is a TSO packet, this filed is exactly L2 header length
- ***TXBF_PT_SCA:*** Enable TxBeamForming Per-tone scaling
- ***TIM:*** Indicate Tx TIM broadcast.
- ***IV***: used by encryption engine.
- ***EIV***: used by encryption engine.
- ***Partial ID:*** VHT Partial AID[8:0]
- ***Group ID:*** VHT Group ID. 0: Group ID = 0, 1: Group ID =63.
- ***Tx stream mode:*** Transmit Stream Mode Control
- ***Tx pwr adjustment:*** Transmit Power Adjustment from -16dB to +7dB.

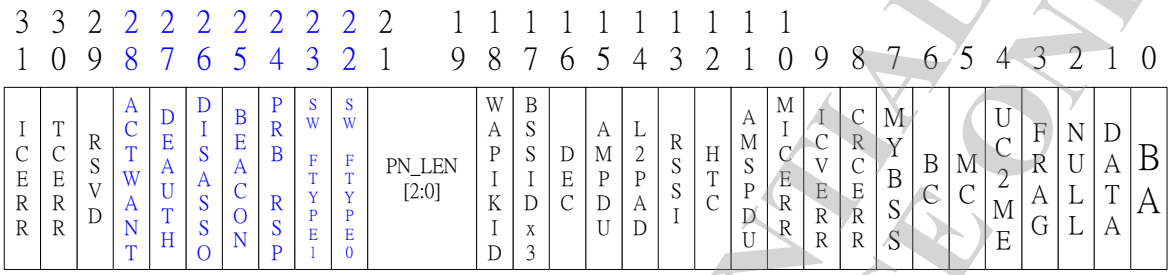
  When negative, each unit represents 2dB; when positive, each unit represents 1dB.

tx_pwr_adj[3:0]	0	1	2	3	4	5	6	7
Tx power (dB)	0	1	2	3	4	5	6	7
tx_pwr_adj[3:0]	8	9	10	11	12	13	14	15
Tx power (dB)	-16	-14	-12	-10	-8	-6	-4	-2

- ***HIGH_PRI:*** Reserve
- ***PIFS_REV_EN:*** Enable PIFS time reverse Tx after successfully transmit BA/ACK
- ***TX_PKT_ID:*** As a cookie specified by driver and will be latched into the TX result register stack.

  Driver use this field to identify special frame's TX result.

5.11.5 RXINFO format



Bit	Name	Description
31	ICERR	IP checksum error
30	TCPERR	TCP checksum error
29	Reserved	Reserved
28	ACTION WANTED	Acion frame from mybss with category and action field matches value set in RXINFO_FCTYPE_CFG CR (0x1428)
27	DEAUTH	Deauthentication Frame
26	DISASSO	Disassociation Frame
25	BEACON	Beacon Frame
24	PRB_RSP	Probe Response Frame
23	SW_FTYPE1	SW specified Frame type 1 in RXINFO_FCTYPE_CFG CR (0x1428)
22	SW_FTYPE0	SW specified Frame type 0 in RXINFO_FCTYPE_CFG CR (0x1428)
21:19	PN_LEN	IV/EIV/PN padding length (unit: DW)
18	WAPI_KID	WAPI Key ID
17	BSSIDX3	BSS index bit3, use together with BSS index bit2:bit0 in RXWI
16	DEC	Decrypted frame
15	AMPDU	AMPDU segregated frame
14	L2PAD	2 byte zero are padding after MAC header (+ HTC)
13	RSSI	RSSI / SNR / PHY rate are valid
12	HTC	4 byte HTC are padding after MAC header
11	AMSDU	AMSDU segregated frame
10	MICERR	TKIP MIC error
9	ICVERR	ICV/AES MIC error
8	CRCERR	CRC error
7	MYBSS	My BSSID frame
6	BC	Broadcast frame
5	MC	Multicast frame

4	UC2ME	Unicast to me frame
3	FRAG	Fragmented data frame TKIP MIC will be skipped on fragmented data frame
2	NULL	Null data frame
1	DATA	Data frame
0	BA	BA session 0: not under BA agreement 1: under BA agreement (need packet reordering)

5.11.6 RXWI format

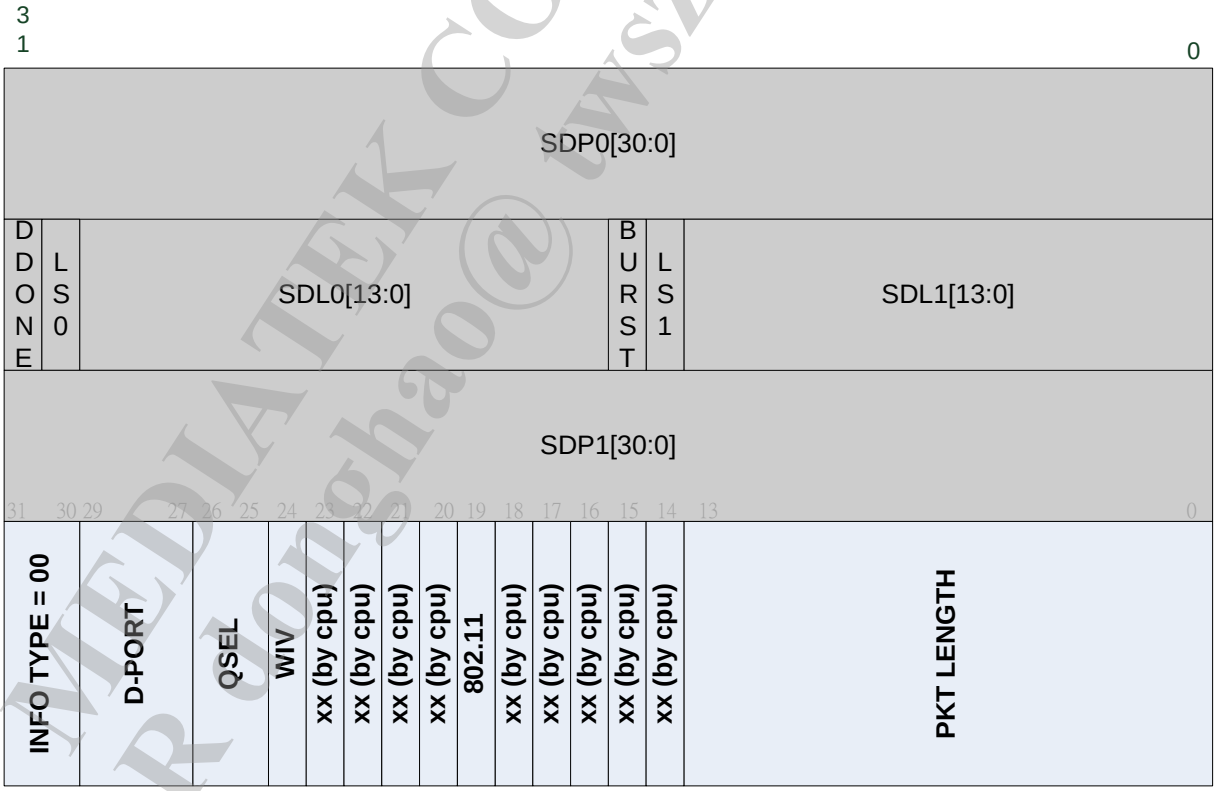
bit 31 bit 0

EOF	RSV	MPDU total byte count[13:0]								UDF [2:0]			BSS idx [2:0]	Key idx [1:0]	WCID[7:0]
PHY mode [2:0]			RSV	LDPCEXSYM	STBC	SGI	BW [1:0]	LDPC	MCS[5:0]				SN[11:0]		TID [3:0]
RSSI_3[7:0]				RSSI_2[7:0]						RSSI_1[7:0]			RSSI_0[7:0]		
BBP_RXINFO_3[7:0]				BBP_RXINFO_2[7:0]						BBP_RXINFO_1[7:0]			BBP_RXINFO_0[7:0]		
BBP_RXINFO_7[7:0]				BBP_RXINFO_6[7:0]						BBP_RXINFO_5[7:0]			BBP_RXINFO_4[7:0]		
BBP_RXINFO_11[7:0]				BBP_RXINFO_10[7:0]						BBP_RXINFO_9[7:0]			BBP_RXINFO_8[7:0]		
BBP_RXINFO_15[7:0]				BBP_RXINFO_14[7:0]						BBP_RXINFO_13[7:0]			BBP_RXINFO_12[7:0]		

- ***WCID***: index of ADDR2 in the pair wise KEY table. This value uniquely identifies the TA. WCID=255 means not found.
- ***KEY Index***: 0~3 extracted from IV field. For driver reference only, no particular usage so far.

- ***BSSID index***: 0~7 for BSSID0~7. Extract from 802.11 header (the last three bits of BSSID field).
- ***UDF***: User Defined Field.
- ***MPDU total byte count***: the entire MPDU length.
- ***EOF***: The VHT A-MPDU delimiter EOF bit value of the MPDU.
- ***TID***: extracted from 802.11 QOS control field.
- ***SN***: sequence number of the received MPDU. Used for BA re-ordering especially that AMSDU are auto segregated by hardware and lost the 802.11 header.
- ***"MCS/BW/SGI/PHYmode"***: RX data rate & related MIMO parameters of this frame got from PLCP header. See next section for the detail.
- ***LDPC :*** The Rx frame is LDPC encoded.
- ***LDPC_EX_SYM :*** The LDPC PPDU encoding process results in an extra OFDM symbol.
- ***RSSI0~3***: BBP reported RSSI information of the received frame.
- ***RXINFO0~15***: BBP reported Rx End Status 0~15

5.11.7 TX FCEINFO format to W port packet (support for embedded CPU)

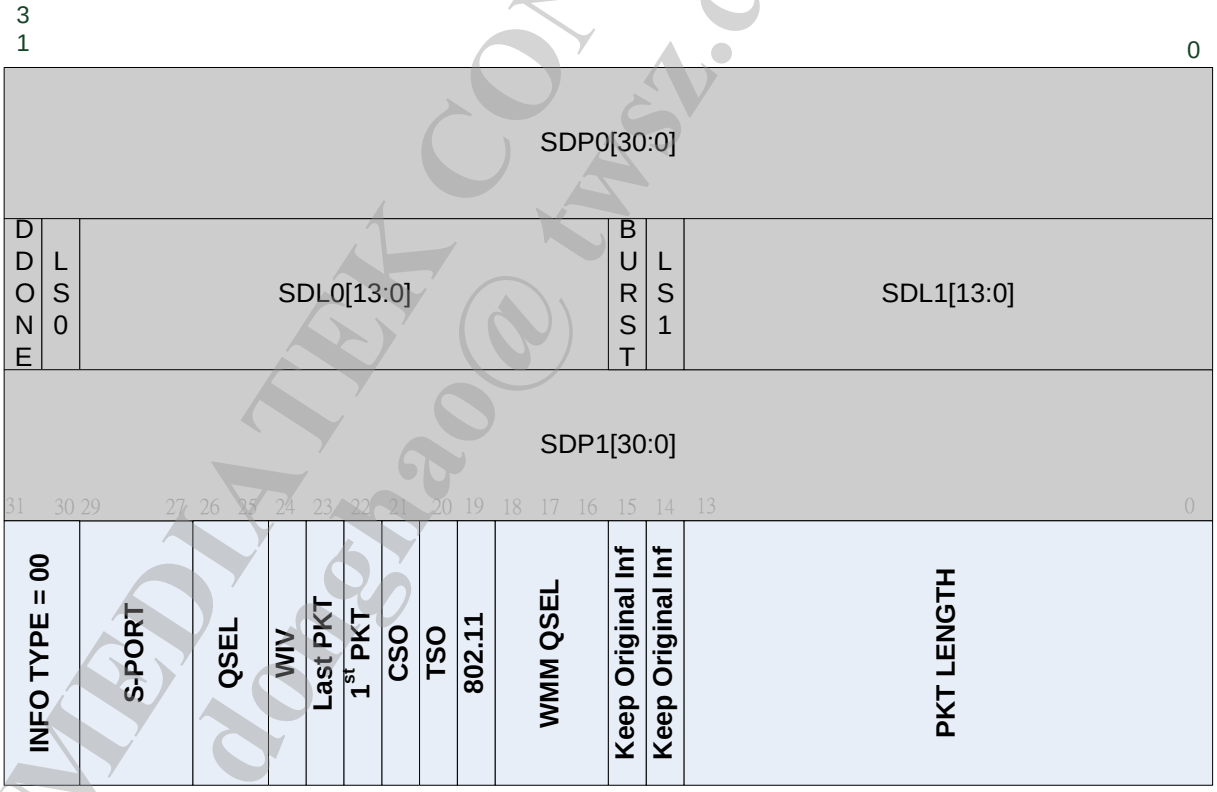


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **D-Port [2:0] : The frame is routing to D-Port**

- ***3'b000** : WLAN port*
- ***3'b001 : CPU RX port***
- ***3'b010 : CPU TX port***
- ***3'b011 : Host port (PCIe)***
- ***3'b100 : Virtual CPU RX port***
- ***3'b101 : Virtual CPU TX port***
- ***3'b110 : discard***

- **QSEL: This packet belongs to which QoS queue in PBF**
- **WIV : valid WLAN INFO**
- **802.11 : must be 1**
- **PKT_LEN: Total length of this packet including RXINFO (LENGTH from MAC+4) when RX. Including TXINFO when TX.**

5.11.8 TX FCEINFO format from H port packet (support for embedded CPU)

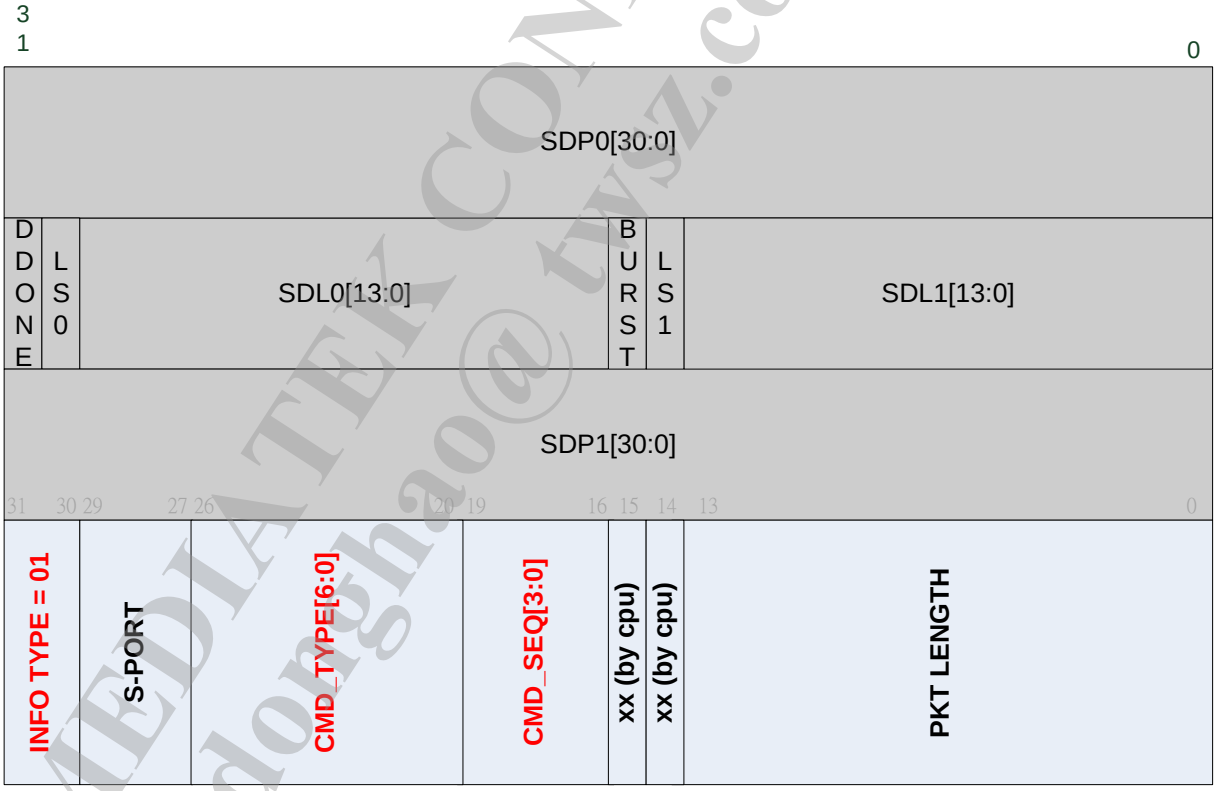


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **S-Port [2:0] : The frame is routing to S-Port**
  - ***3'b000** : WLAN port*
  - ***3'b001 : CPU RX port***

- *3'b010 : CPU TX port*
- *3'b011 : Host port (PCIe)*
- *3'b100 : Virtual CPU RX port*
- *3'b101 : Virtual CPU TX port*
- *3'b110 : discard*

- **QSEL: This packet belongs to which QoS queue in PBF**
- **WIV : valid WLAN INFO**
- **802.11 : must be 1**
- **PKT_LEN: Total length of this packet including RXINFO (LENGTH from MAC+4) when RX. Including TXINFO when TX.**

5.11.9 TX FCEINFO format for command (support for embedded CPU)

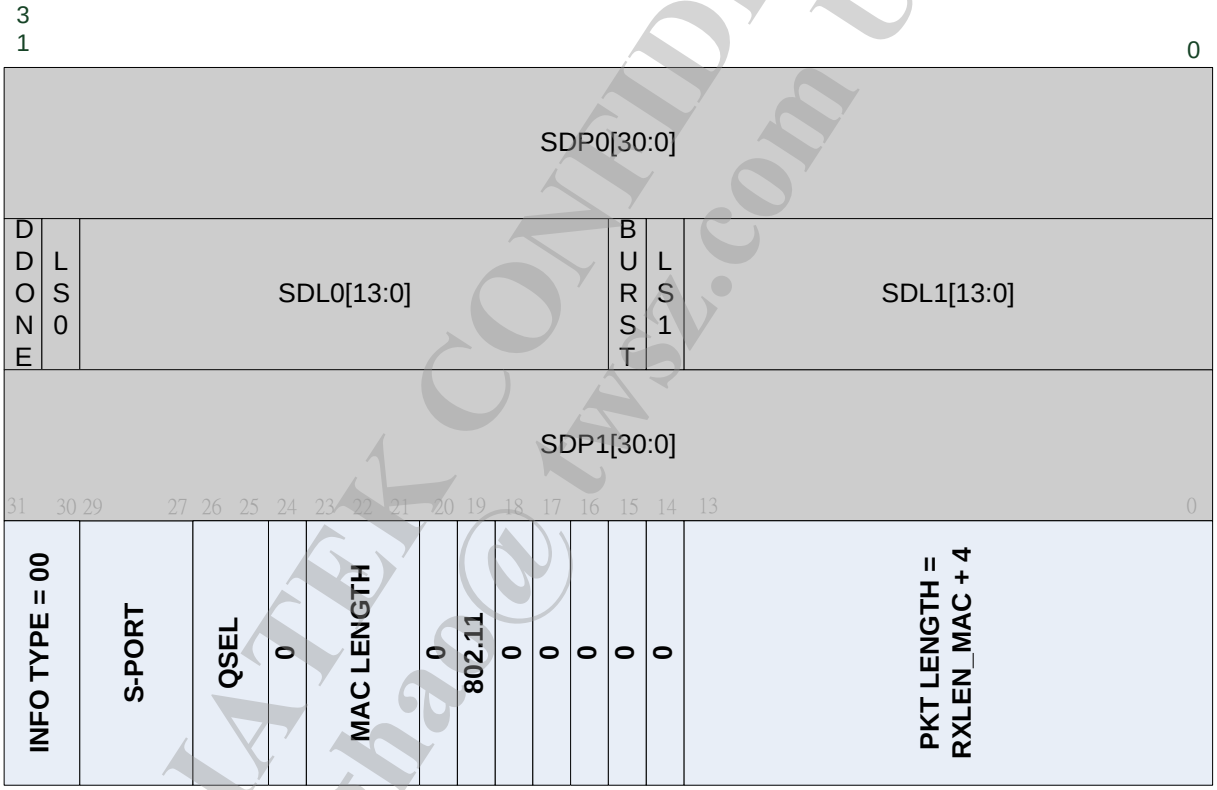


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **S-Port [2:0] : The frame is routing to D-Port**
  - ***3'b000** : WLAN port*
  - ***3'b001 : CPU RX port***
  - ***3'b010 : CPU TX port***

- *3'b011 : Host port (PCIe)*
- *3'b100 : Virtual CPU RX port*
- *3'b101 : Virtual CPU TX port*
- *3'b110 : discard*

- **CMD_TYPE[2:0]: packet command typw**
- **CMD_SEQ[3:0] : packet command sequence**

5.11.10 RX FCEINFO format from W port packet (support for embedded CPU)

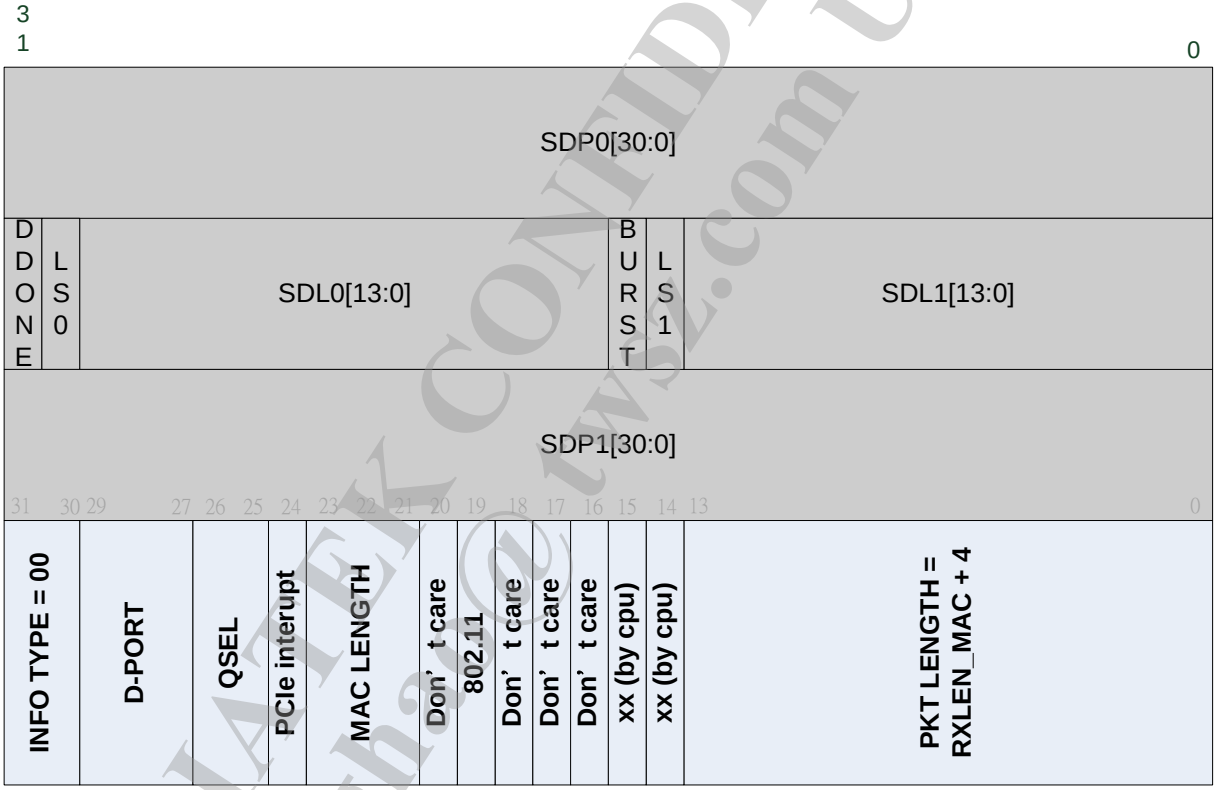


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **S-Port [2:0] : The frame is routing from S-Port**
  - *3'b000 : WLAN port*
  - *3'b001 : CPU RX port*
  - *3'b010 : CPU TX port*
  - *3'b011 : Host port (PCIe)*
  - *3'b100 : Virtual CPU RX port*
  - *3'b101 : Virtual CPU TX port*

- *3'b110 : discard*

- **QSEL : The frame is routing to D-Port Queue 0~3**
- **PCIE intreq : embedded embedded CPU parse L4 packet and generate PCI-E interrupt per packet base to do D0-offload**
- **MAC-LENOFS[2:0] : (MAC header length = 24byte+ MAC_LENOFS*2)**
- **802.11 : must be 1**
- **PKT_LEN: Total length of this packet including RXINFO (LENGTH from MAC+4) when RX. Including TXINFO when TX..**

5.11.11 RX FCEINFO format to H port packet (support for embedded CPU)

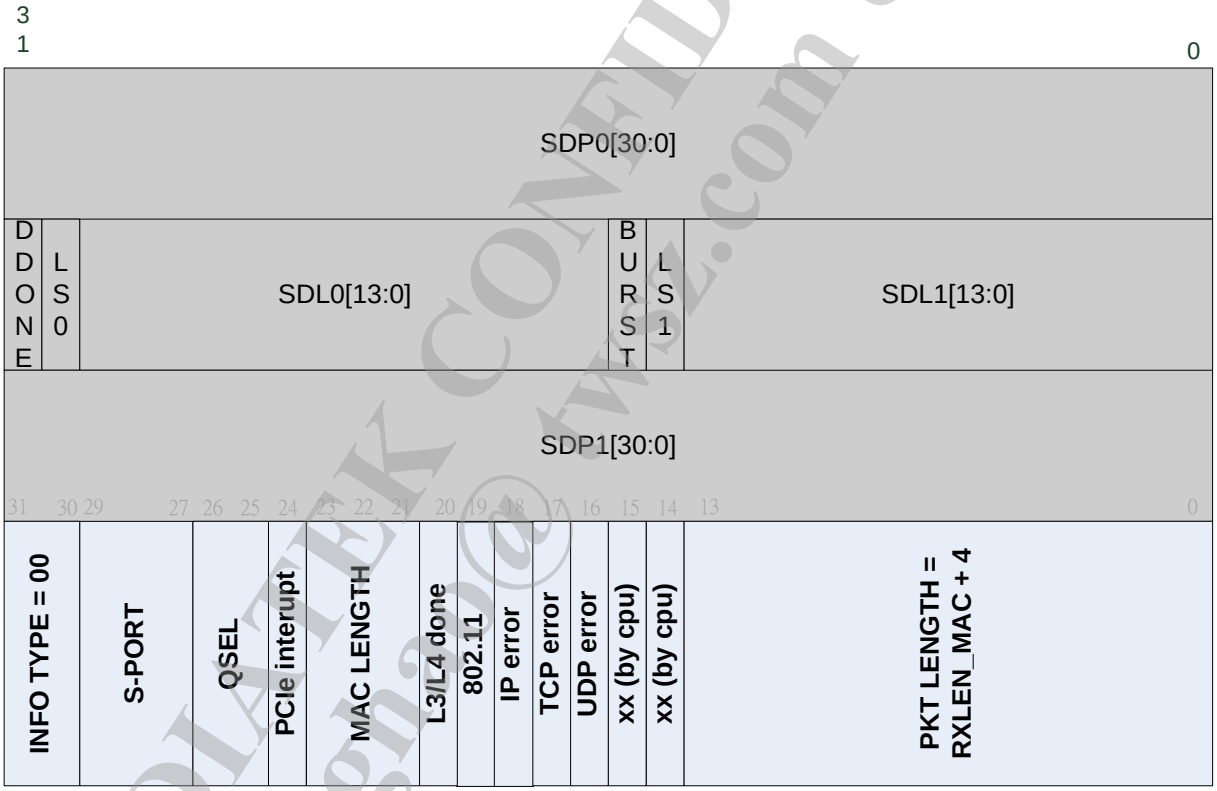


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **D-Port [2:0] : The frame is routing to D-Port**
  - *3'b000 : WLAN port*
  - *3'b001 : CPU RX port*
  - *3'b010 : CPU TX port*
  - *3'b011 : Host port (PCIe)*
  - *3'b100 : Virtual CPU RX port*
  - *3'b101 : Virtual CPU TX port*

- *3'b110 : discard*

- **QSEL : The frame is routing to D-Port Queue 0~3**
- **PCIE intreq : embedded embedded CPU parse L4 packet and generate PCI-E interrupt per packet base to do D0-offload**
- **MAC-LENOFS[2:0] : (MAC header length = 24byte+ MAC_LENOFS*2)**
- **802.11 : must be 1**
- **PKT_LEN: Total length of this packet including RXINFO (LENGTH from MAC+4) when RX. Including TXINFO when TX..**

5.11.12 RX FCEINFO format for packet (support for Host)

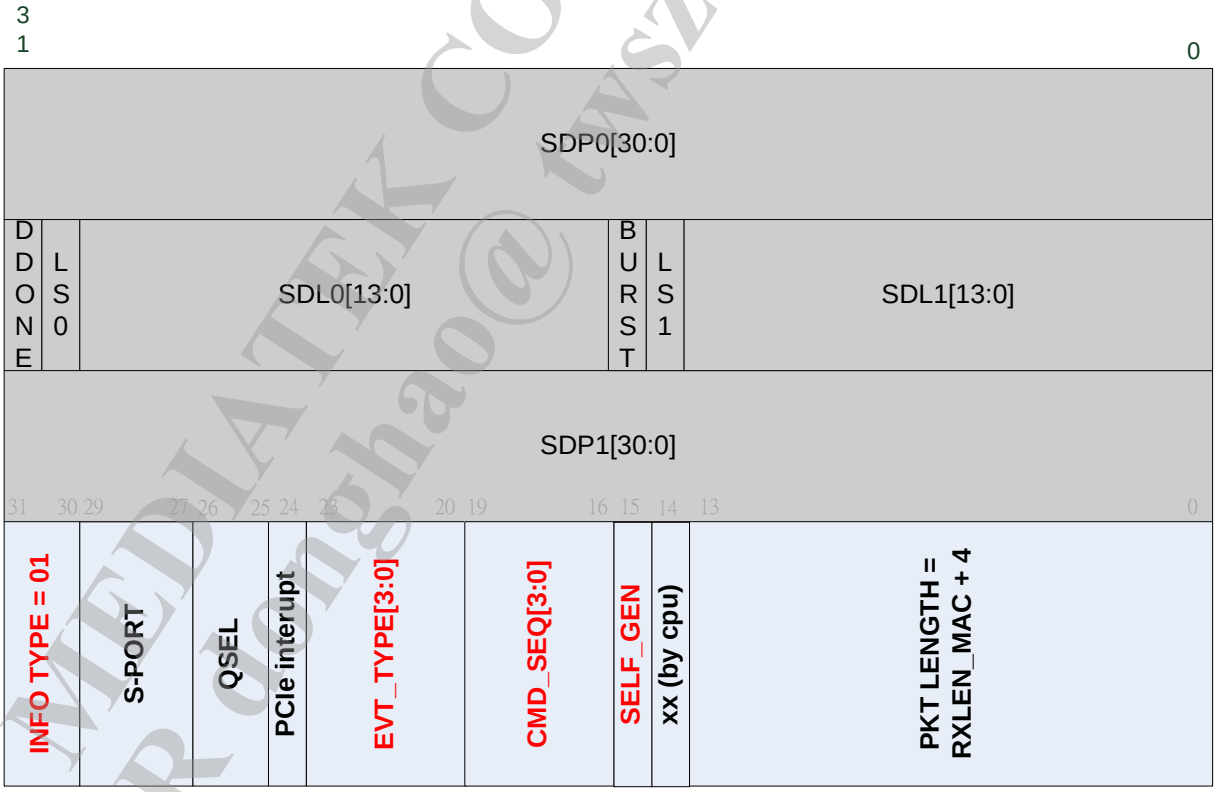


- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **S-Port [2:0] : The frame is routing to S-Port**
  - *3'b000 : WLAN port*
  - *3'b001 : CPU RX port*
  - *3'b010 : CPU TX port*
  - *3'b011 : Host port (PCIe)*
  - *3'b100 : Virtual CPU RX port*
  - *3'b101 : Virtual CPU TX port*

- *3'b110 : discard*

- **QSEL : The frame is routing to D-Port Queue 0~3**
- **PCIE intreq : embedded embedded CPU parse L4 packet and generate PCI-E interrupt per packet base to do D0-offload**
- **MAC-LENOFS[2:0] : (MAC header length = 24byte+ MAC_LENOFS*2)**
- **L3_L4 done : indicate the validity of IP/TCP/UDP error status bits**
- **IP error : status report . '1', IPv4 header checksum error**
- **802.11 : must be 1**
- **TCP error : status report . '1', checksum error**
- **UDP error : status report. '1', checksum error**
- **PKT_LEN: Total length of this packet including RXINFO (LENGTH from MAC+4) when RX. Including TXINFO when TX..**

5.11.13 RX FCEINFO format for command (support for Host)



- **INFO-TYPE : 2'b00 packet, 2'b01 command, 2'b10 reserve, 2'b11 reserve**
- **D-Port [2:0] : The frame is routing to D-Port**
  - ***3'b000** : WLAN port*

- *3'b001 : CPU RX port*
- *3'b010 : CPU TX port*
- *3'b011 : Host port (PCIe)*
- *3'b100 : Virtual CPU RX port*
- *3'b101 : Virtual CPU TX port*
- *3'b110 : discard*

- **QSEL : The frame is routing to D-Port Queue 0~3**
- **PCIE intreq : embedded embedded CPU parse L4 packet and generate PCI-E interrupt per packet base to do D0-offload**
- **EVENT_TYPE[3:0] : response event type**
- **CMD_SEQ[3:0] : packet command sequence**
- **SELF_GEN : A response event by self-generate**

5.11.14 Brief PHY rate format and definition

A 16-bit brief PHY rate is used in MAC hardware.
It is the same PHY rate field described in TXWI and RXWI.

Bit	Name	Description
15:13	MODE	PHY mode 0: Legacy CCK, 1: Legacy OFDM, 2: HT mix mode, 3: HT green field 4: VHT mode, 5-7: Reserved
12:11		Reserved
10	STBC	STBC, only support for HT mode 0: no STBC 1: STBC (Only support STBC in HT MCS=0~7,VHT mode MCS=0~9)
9	SGI	Short Guard Interval, only support for HT/VHT mode 0: 800ns, 1: 400ns
8:7	BW	Bandwidth Support both legacy and HT modes 40Mhz in legacy mode means duplicate legacy 0: 20Mhz, 1: 40Mhz, 2: 80Mhz, 3: Reserved
6	LDPC	LDPC 0: no LDPC, 1: LDPC encoding
5:0	MCS/NSS	Modulation Coding Scheme/Number of Spatial Stream **In HT mode:** MCS[2:0] stands for Modulation Coding Scheme (MCS). MCS[2:0]=0~7 are supported in this version. MCS[5:3] stands for Number of Spatial Stream (NSS). Only MCS[5:3]=0,1 are supported in this version. **In VHT mode:** MCS[3:0] stands for Modulation Coding Scheme (MCS). MCS[3:0]=0~8 are supported for BW = 20Mhz MCS[3:0]=0~9 are supported for BW = 40 or 80Mhz MCS[5:4] plus one stands for Number of Spatial Stream (NSS). Only MCS[5:4]=0, 1are supported in this version.

Table. Brief PHY rate format

MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1Mbps
MCS = 1	Long Preamble CCK 2Mbps
MCS = 2	Long Preamble CCK 5.5Mbps

MCS = 3	Long Preamble CCK 11Mbps
MCS = 8	Short Preamble CCK 1Mbps * illegal rate
MCS = 9	Short Preamble CCK 2Mbps
MCS = 10	Short Preamble 5.5Mbps
MCS = 11	Short Preamble 11Mbps
Other MCS codes are reserved in legacy CCK mode. BW, SGI and STBC are reserved in legacy CCK mode.	
MODE = Legacy OFDM	
MCS = 0	6Mbps
MCS = 1	9Mbps
MCS = 2	12Mbps
MCS = 3	18Mbps
MCS = 4	24Mbps
MCS = 5	36Mbps
MCS = 6	48Mbps
MCS = 7	54Mbps
Other MCS code in legacy CCK mode are reserved When BW = 1, duplicate legacy OFDM is sent. SGI, STBC are reserved in legacy OFDM mode.	
MODE = HT mix mode / HT green field	
MCS = 0 (1S)	(BW=0, SGI=0) 6.5Mbps
MCS = 1	(BW=0, SGI=0) 13Mbps
MCS = 2	(BW=0, SGI=0) 19.5Mbps
MCS = 3	(BW=0, SGI=0) 26Mbps
MCS = 4	(BW=0, SGI=0) 39Mbps
MCS = 5	(BW=0, SGI=0) 52Mbps
MCS = 6	(BW=0, SGI=0) 58.5Mbps
MCS = 7	(BW=0, SGI=0) 65Mbps
MCS = 8 (2S)	(BW=0, SGI=0) 13Mbps
MCS = 9	(BW=0, SGI=0) 26Mbps
MCS = 10	(BW=0, SGI=0) 39Mbps
MCS = 11	(BW=0, SGI=0) 52Mbps
MCS = 12	(BW=0, SGI=0) 78Mbps
MCS = 13	(BW=0, SGI=0) 104Mbps
MCS = 14	(BW=0, SGI=0) 117Mbps
MCS = 15	(BW=0, SGI=0) 130Mbps

MCS = 32	(BW=1, SGI=0) HT duplicate 6Mbps
MODE = VHT mode	
MCS = 0~7 (1S)	Data Rate is the same as HT MCS 0~7
MCS = 8 (1S)	(BW=0, SGI=0) 78Mbps (BW=1, SGI=0) 162Mbps (BW=2, SGI=0) 351Mbps
MCS = 9 (1S)	(BW=0, SGI=0) **Not Valid** (BW=1, SGI=0) 180Mbps (BW=2, SGI=0) 390Mbps
MCS = 0~7 (2S)	Data Rate is the same as HT MCS 8~15
MCS = 8 (2S)	(BW=0, SGI=0) 156Mbps (BW=1, SGI=0) 324Mbps (BW=2, SGI=0) 702Mbps
MCS = 9 (2S)	(BW=0, SGI=0) **Not Valid** (BW=1, SGI=0) 360Mbps (BW=2, SGI=0) 780Mbps

When BW=1, PHY_RATE = PHY_RATE * 2
When SGI=1, PHY_RATE = PHY_RATE * 10/9
The effects of BW and SGI are accumulative.

When 1S, STBC option is supported. SGI option is supported. BW option is supported.

When 2S, STBC option is NOT supported. SGI option is supported. BW option is supported.

When MCS=32, only SGI option is supported. BW and STBC option are not supported. (BW =1, STBC=0)

Other MCS code in HT mode are reserved

When STBC is supported. Only STBC = 1 is allowed. STBC will extend the transmission range but will not increase transmission rate.

ESD CAUTION

MT7612E is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7632U is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.