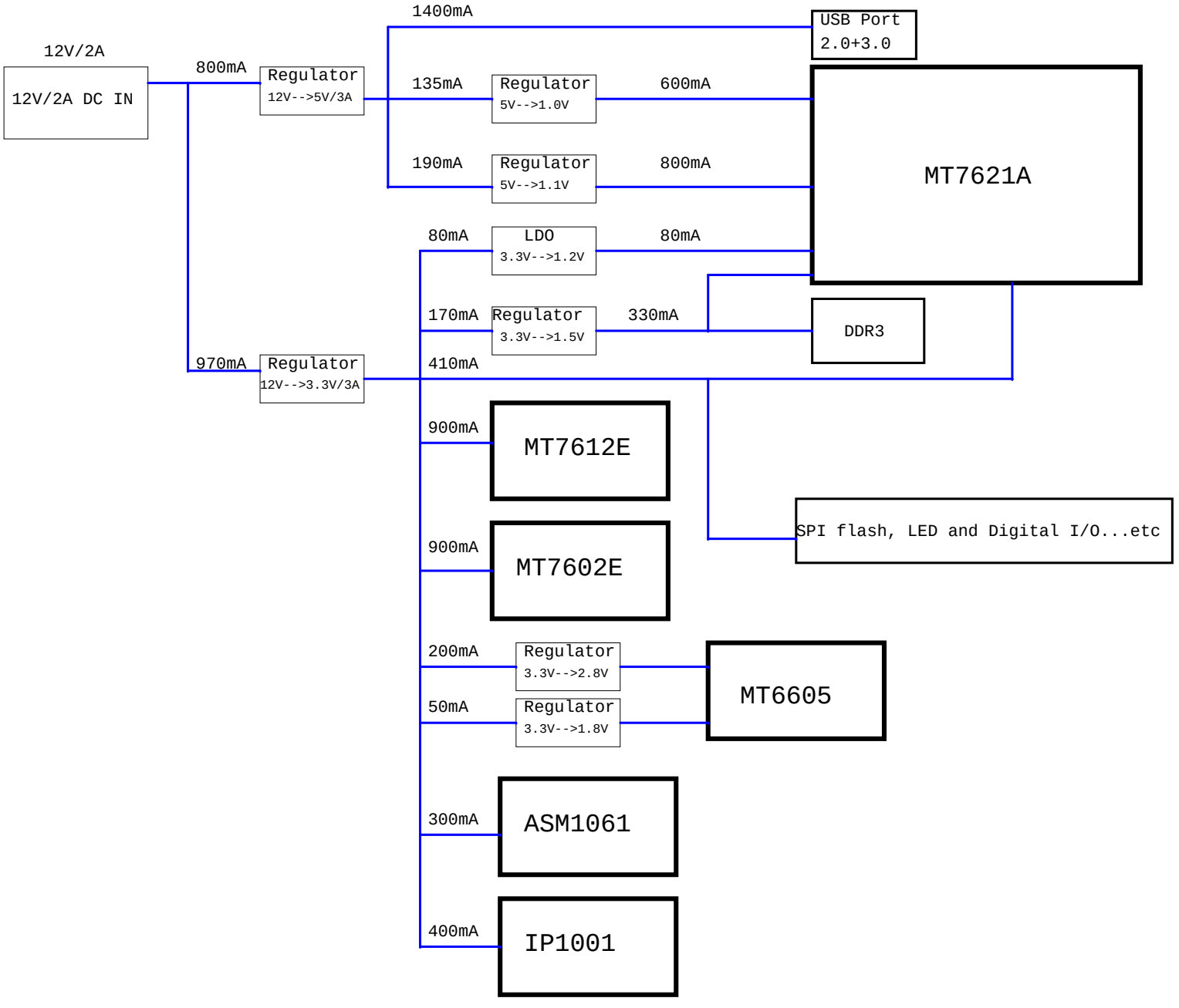
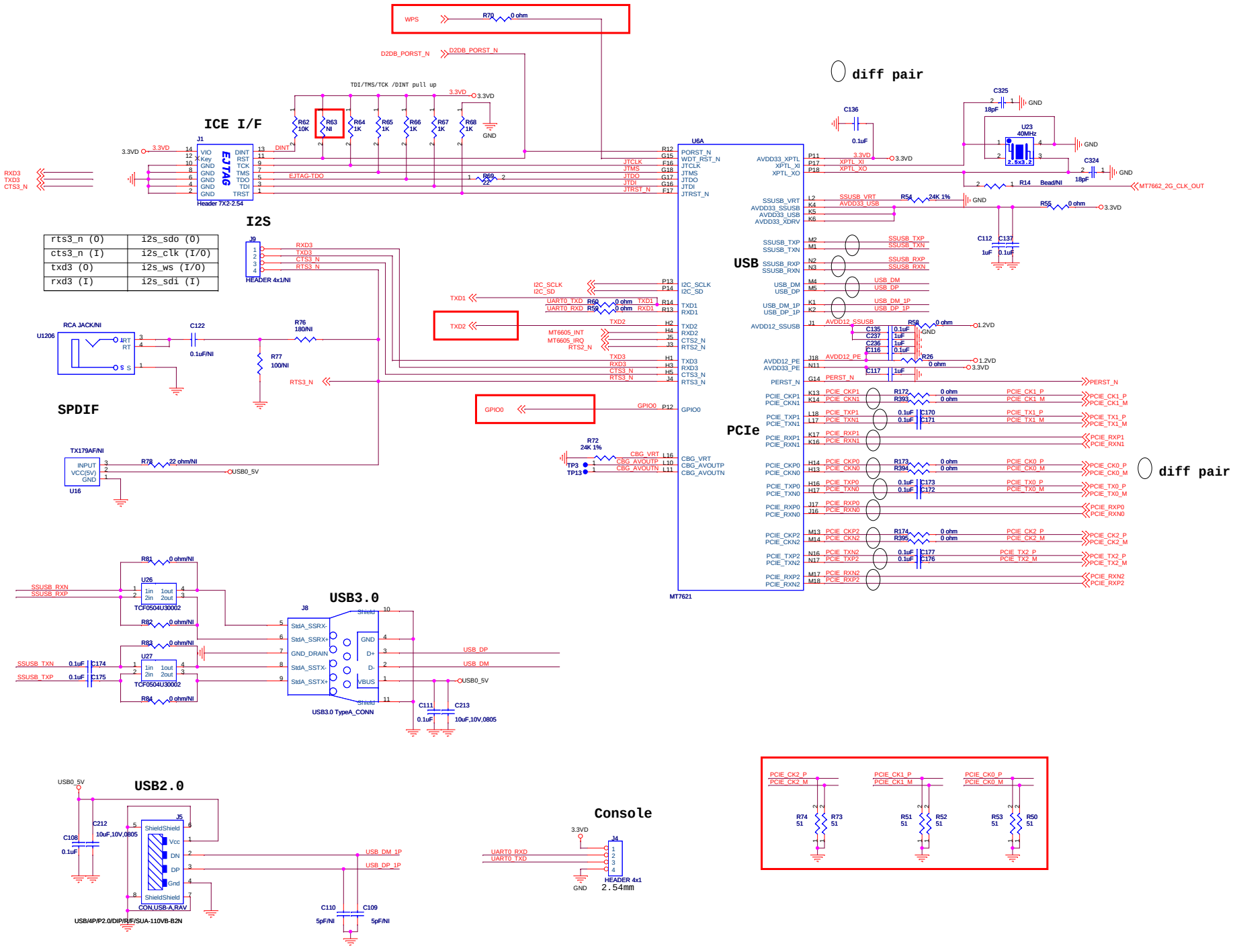

12V/2A
12V/2A DC IN
800mA
Regulator
12V-->5V/3A
1400mA
USB Port
2.0+3.0
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
MT7621A
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
DDR3
970mA
Regulator
12V-->3.3V/3A
410mA
900mA
MT7612E
SPI flash, LED and Digital I/O...etc
900mA
MT7602E
200mA
Regulator
3.3V-->2.8V
50mA
Regulator
3.3V-->1.8V
MT6605
300mA
ASM1061
400mA
IP1001


ICE I/F
I2S
SPDIF
USB
PCIe
USB3.0
USB2.0
Console
diff pair
diff pair
MT7621
WPS
R70 0 ohm
D2DB_PORST_N
TDI/TMS/TCK /DINT pull up
3.3VD
R62 10K
R63 NI
R64 1K
R65 1K
R66 1K
R67 1K
R68 1K
GND
J1
EJTAG
VIO
DINT
RST
TCK
TMS
TDO
TDI
TRST
Header 7X2-2.54
RXD3
TXD3
CTS3_N
EJTAG-TDO
R69 22
U6A
PORST_N
WDT_RST_N
JTCLK
JTMS
JTDO
JTDI
JTRST_N
rts3_n (O) | i2s_sdo (O)
cts3_n (I) | i2s_clk (I/O)
txd3 (O) | i2s_ws (I/O)
rxd3 (I) | i2s_sdi (I)
J9
HEADER 4x1/NI
I2C_SCLK
I2C_SD
TXD1
RXD1
UART0_TXD R60 0 ohm
UART0_RXD R59 0 ohm
TXD2
RXD2
CTS2_N
RTS2_N
MT6605_INT
MT6605_IRQ
RTS3_N
GPIO0
RCA JACK/NI
U1206
C122 0.1uF/NI
R76 180/NI
R77 100/NI
TX179AF/NI
U16
R78 22 ohm/NI
USB0_5V
R72 24K 1%
TP3
TP13
CBG_VRT
CBG_AVOUTP
CBG_AVOUTN
C136 0.1uF
C325 18pF
U23 40MHz
C324 18pF
R14 Bead/NI
MT7662_2G_CLK_OUT
AVDD33_XPTL
XPTL_XI
XPTL_XO
R54 24K 1%
R55 0 ohm
AVDD33_SSUSB
AVDD33_USB
AVDD33_XDRV
SSUSB_VRT
C112 1uF
C137 0.1uF
SSUSB_TXP
SSUSB_TXN
SSUSB_RXP
SSUSB_RXN
USB_DM
USB_DP
USB_DM_1P
USB_DP_1P
AVDD12_SSUSB
R58 0 ohm
C135 0.1uF
C237 1uF
C236 1uF
C116 0.1uF
1.2VD
AVDD12_PE
AVDD33_PE
R26 0 ohm
C117 1uF
3.3VD
PERST_N
PCIE_CKP1
PCIE_CKN1
PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1
PCIE_CKP0
PCIE_CKN0
PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0
PCIE_CKP2
PCIE_CKN2
PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2
R172
R393
R173
R394
R174
R395
C170
C171
C173
C172
C177
C176
R81 0 ohm/NI
U26
TCP0504U30002
R82 0 ohm/NI
R83 0 ohm/NI
U27
TCP0504U30002
R84 0 ohm/NI
SSUSB_RXN
SSUSB_RXP
SSUSB_TXN
SSUSB_TXP
C174 0.1uF
C175 0.1uF
J8
USB3.0 TypeA_CONN
StdA_SSRX-
StdA_SSRX+
GND_DRAIN
StdA_SSTX-
StdA_SSTX+
Shield
GND
D+
D-
VBUS
C111 0.1uF
C213 10uF,10V,0805
USB0_5V
USB_DP
USB_DM
C212 10uF,10V,0805
C108 0.1uF
J5
ShieldShield
Vcc
DN
DP
Gnd
CON,USB-A,RAV
USB4P/P2.0/DIP/R/F/SUA-110VB-B2N
USB_DM_1P
USB_DP_1P
C110 5pF/NI
C109 5pF/NI
UART0_RXD
UART0_TXD
J4
HEADER 4x1
2.54mm
R74 51
R73 51
R51 51
R52 51
R53 51
R50 51
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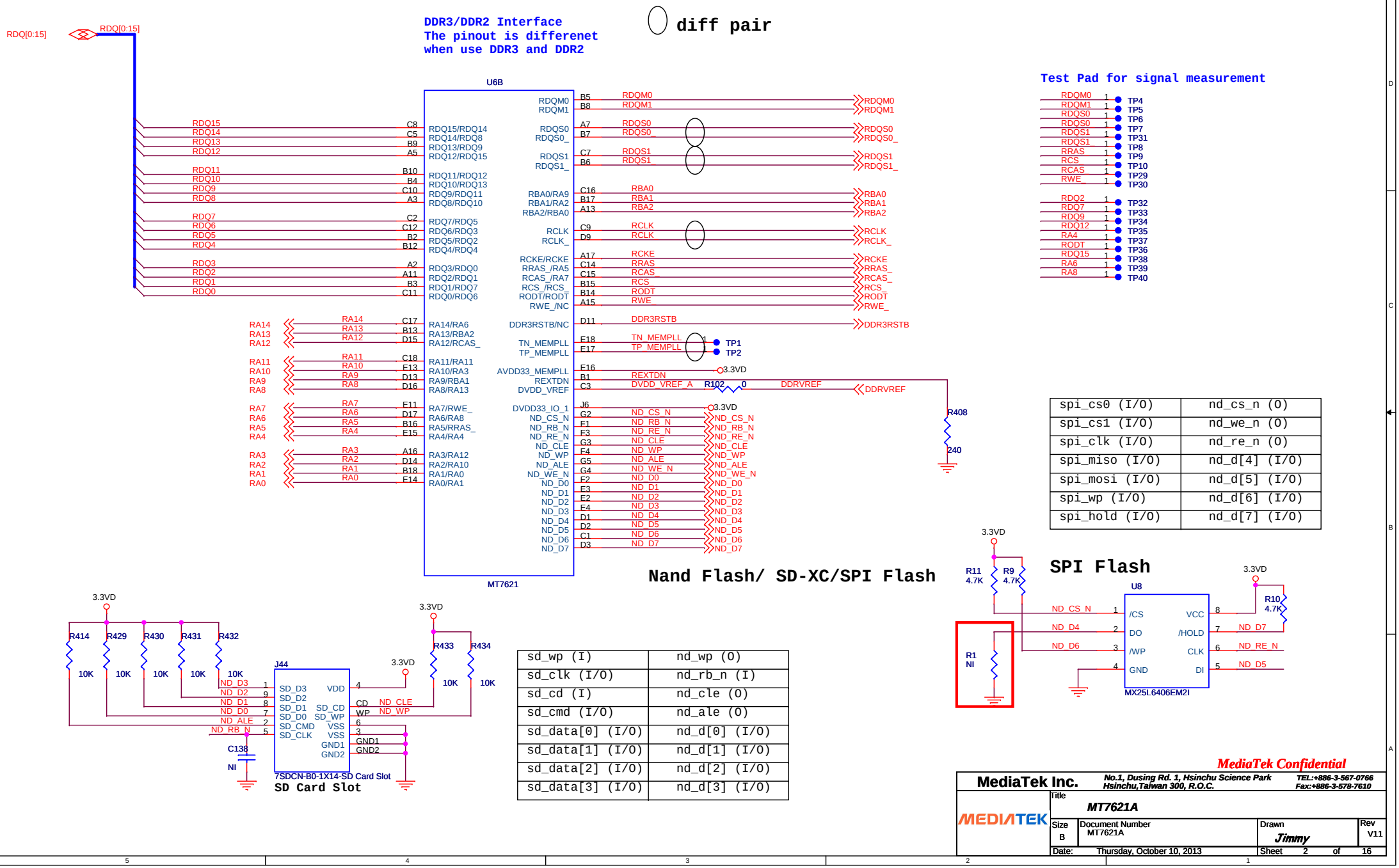
MT7621A
Size C
Document Number MT7621A
Drawn Jimmy
Rev V11
Date: Thursday, October 10, 2013
Sheet 1 of 16



spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

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Title: MT7621A			
Size: B	Document Number: MT7621A	Drawn: Jimmy	Rev: V11
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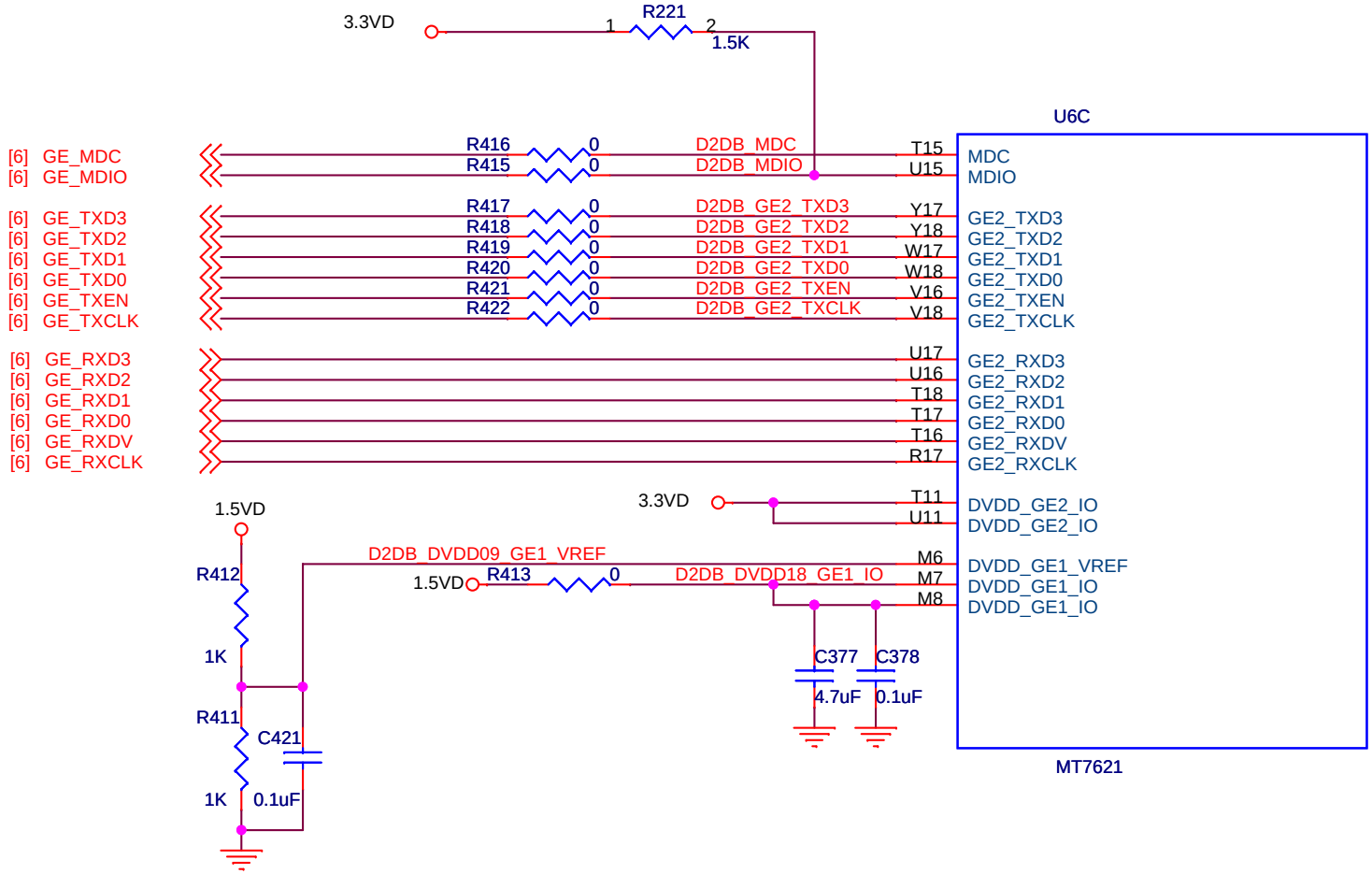
RGMII Interface



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Title: MT7621A			
Size: A	Document Number: MT7621A	Drawn: Jimmy	Rev: V11
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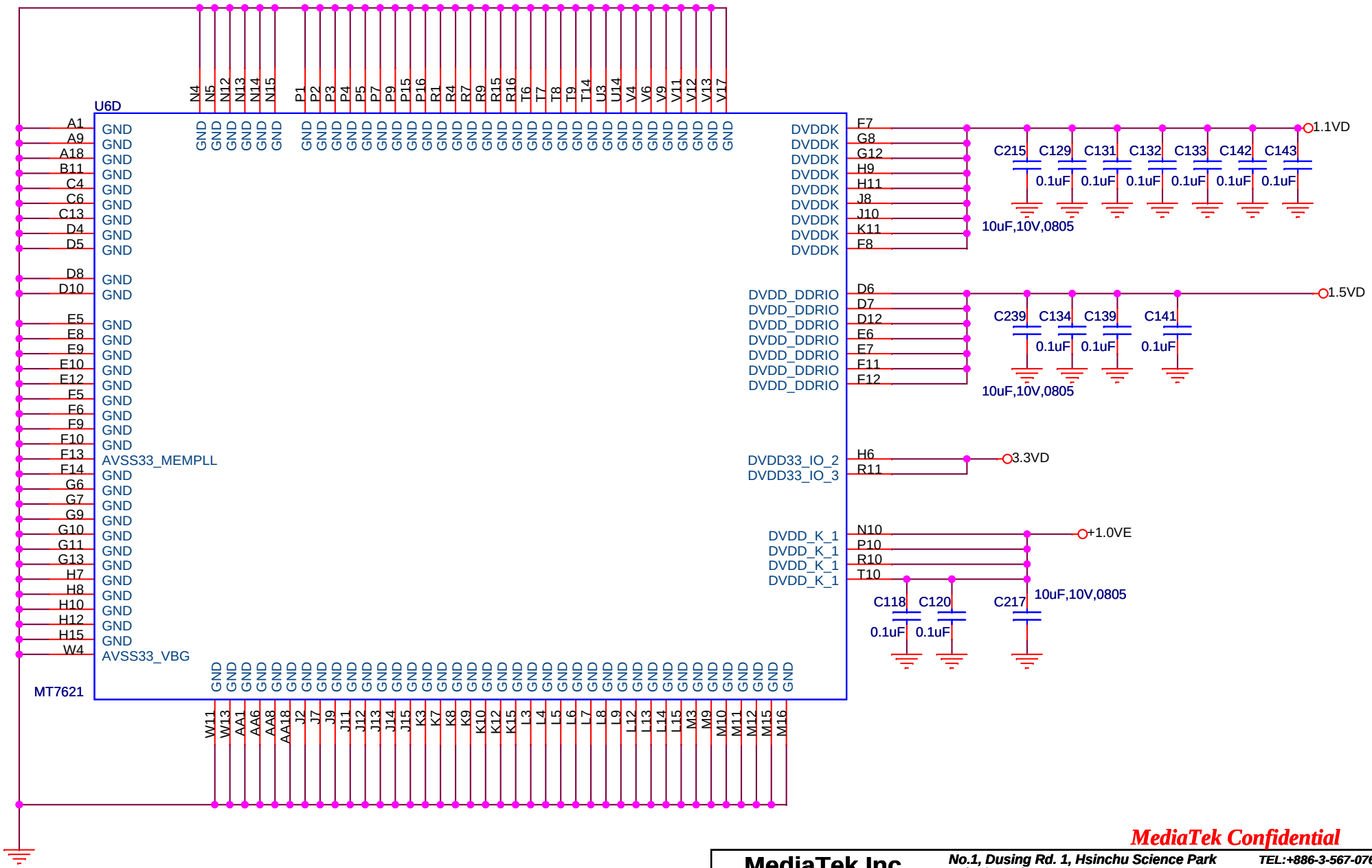
MT7621 Power



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Title: ***MT7621A***			
Size: A	Document Number: MT7621A	Drawn: *Jimmy*	Rev: V11
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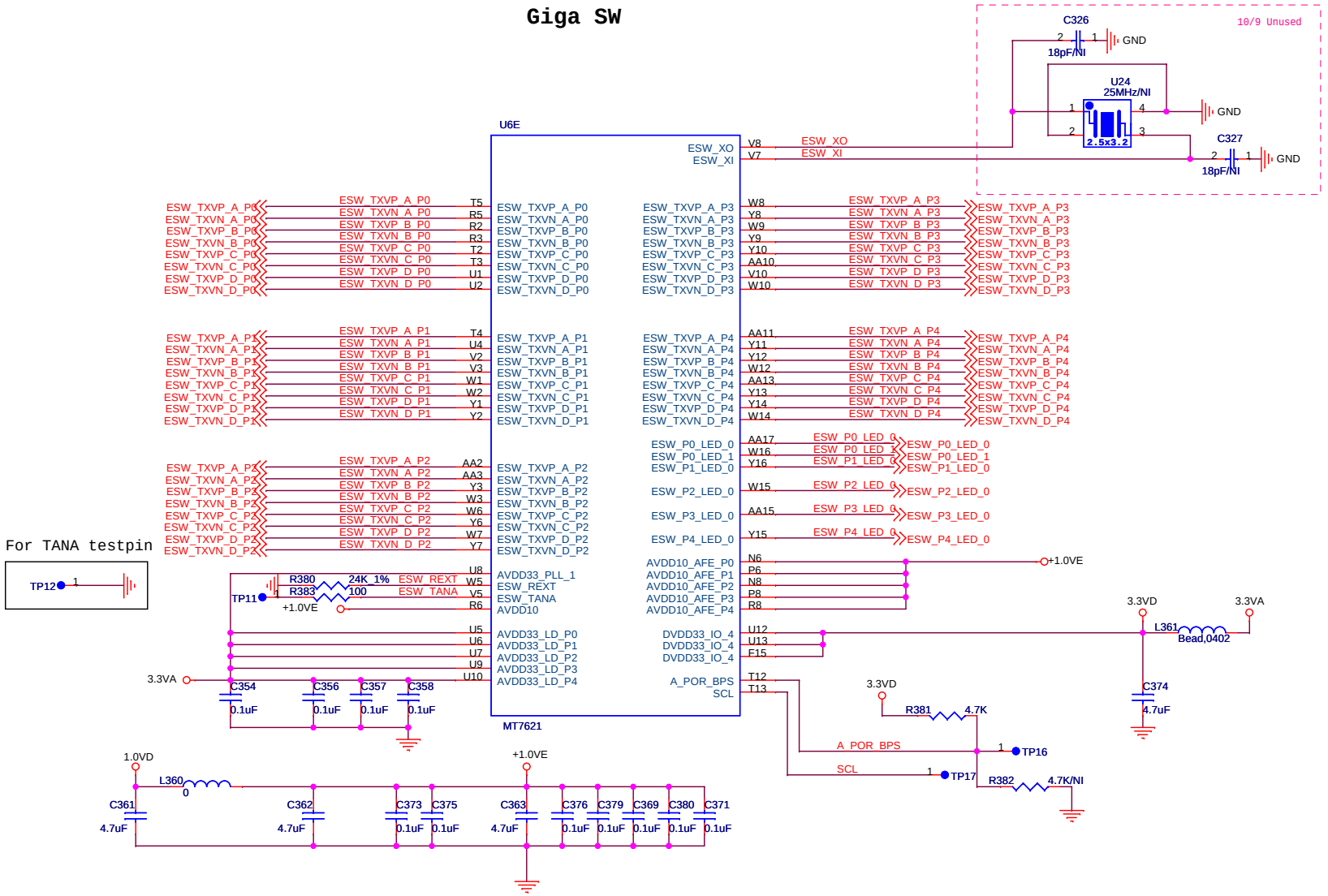
Giga SW



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MEDIATEK	Title: MT7621A		
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Giga Phy

Close to IP1001

C65810pF/NI GE_RC_IP1001 R709 22/NI

[6] GE_RXCLK
[6] GE_RXDV
[6] GE_RXD0
[6] GE_RXD1
[6] GE_RXD2
[6] GE_RXD3

R708 22 R702 22 R703 22 R697 22 R693 22 R692 22

P_RXCLK P_RXDV P_RXD0 P_RXD1 P_RXD2 P_RXD3

R716 10K/NI RC2 4.7uF/NI R733 22 ohm X2_IP1001-o R734 1M ohm X601 CXP 25MHz C801 22pF C802 22pF

3.3VD L608 0 P_VDDO_IP1001 C661 10uF C654 0.1uF

3.3V to 1.2V

Q600 2SB1386 C653 0.1uF

P_DVDD_IP1001 C633 0.1uF C631 10uF C632 1uF

U607 IP1001

TXDELAY_IP1001 PADDR4_IP1001 PADDR3_IP1001 3.3VD PADDR2_IP1001 P_DVDD_IP1001 PM_TXCLK 3.3VD

TP600

[6] GE_TXCLK
[6] GE_TXEN
[6] GE_TXD0
[6] GE_TXD1
[6] GE_TXD2
[6] GE_TXD3

GE_TXCLK GE_TXEN GE_TXD0 GE_TXD1 GE_TXD2 GE_TXD3 P_DVDD_IP1001 3.3VD GND

CRTL12V_IP1001 P_AVDD_IP1001 CHANNEL_D- CHANNEL_D+ P_AVDD_IP1001 CHANNEL_C- CHANNEL_C+ PCAP_IP1001 3.3VD P_AVDD_IP1001 CHANNEL_B- CHANNEL_B+ P_AVDD_IP1001 CHANNEL_A- CHANNEL_A+ PRSET_IP1001

C674 0.1uF C680 10uF

R723 6.19KR,1%

[6,9] GE_MDC R707 0 P_MDC_IP1001 C656 10pF/NI
[6,9] GE_MDIO R711 0 ohm P_MDIO_IP1001

3.3V to 2.1V

[6] P_LED0_IP1001 P_LED0_IP1001
P_VDDO_IP1001 R714 4.7K/NI P_LED1_IP1001
[6] P_LED2_IP1001 P_LED2_IP1001

P_AVDD_IP1001 C666 0.1uF Q601 2SB1386 C667 0.1uF C797 10uF C796 1uF

P_AVDDH_IP1001 L613 0 P_AVDDH_IP1001 C682 10uF C683 0.1uF

P_AVDD_IP1001 C673 0.1uF C669 0.1uF C670 0.1uF C668 0.1uF

C816 0.1uF/100V C817 0.1uF/100V C734 0.1uF/100V C733 0.1uF/100V CHGND_GE_A

2.5V or 2.1V (Use 2.1V)

P_AVDD_IP1001 L616 0 PTCT_GE

T600

CHANNEL_D- CHANNEL_D+ CHANNEL_C- CHANNEL_C+ CHANNEL_B- CHANNEL_B+ CHANNEL_A- CHANNEL_A+

C717 0.1uF C716 0.1uF C715 0.1uF C714 0.1uF

TCT1 TD1_P TD1_M TCT2 TD2_P TD2_M TCT3 TD3_P TD3_M TCT4 TD4_P TD4_M
MCT1 MX1_P MX1_M MCT2 MX2_P MX2_M MCT3 MX3_P MX3_M MCT4 MX4_P MX4_M

PMCT1_GE PMCT2_GE PMCT3_GE PMCT4_GE
GP8_GE GP7_GE GP6_GE GP5_GE GP4_GE GP3_GE GP2_GE GP1_GE

R798 75 R797 75 R796 75 R795 75

U614 RJ-45X1P

R790 49.9 R789 49.9 R788 49.9 R787 49.9 R786 49.9 R785 49.9 R784 49.9 R783 49.9

PTC1_GE PTC2_GE PTC3_GE PTC4_GE

C809 1nF C808 1nF C807 1nF C806 1nF

CHGND_GE PMCT_HV_GE C735 1000pF/2KV/NI

Transformer :
FUN-JIN->GT24-03S,GT24-03SM
Pulse->H5004, H5007, H5062, H5091NL
Bothhand->24HST1041A-2,GST5009

PHY address setting 00101b

P_VDDO_IP1001 R686 4.7K PADDR4_IP1001 R679 4.7K PADDR3_IP1001 R678 4.7K PADDR2_IP1001 PADDR1_IP1001 R691 4.7K P_VDDO_IP1001 R696 4.7K PADDR0_IP1001

P_DVDD_IP1001 C634 0.1uF C768 0.1uF C647 0.1uF C657 0.1uF C642 0.1uF

3.3VD C641 0.1uF C648 0.1uF C636 0.1uF C635 0.1uF C655 0.1uF C640 0.1uF

Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
RXCLK output delay 2ns in 1000Base-T
TXCLK input delay 0ns in 1000Base-T

P_VDDO_IP1001 R690 4.7K TXDELAY_IP1001 R680 4.7K RXDELAY_IP1001

Pull low for RGMII interface
Pull high for GMII/MII interface

RGMII_SEL_IP1001 R718 4.7K

LED Mode 0

PM_TXCLK R676 4.7K

Closed to X'FML

CHANNEL_D- C713 10pF
CHANNEL_D+ C712 10pF
CHANNEL_C- C711 10pF
CHANNEL_C+ C710 10pF
CHANNEL_B- C709 10pF
CHANNEL_B+ C708 10pF
CHANNEL_A- C707 10pF
CHANNEL_A+ C706 10pF

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MEDIATEK	Title: MT7621A		
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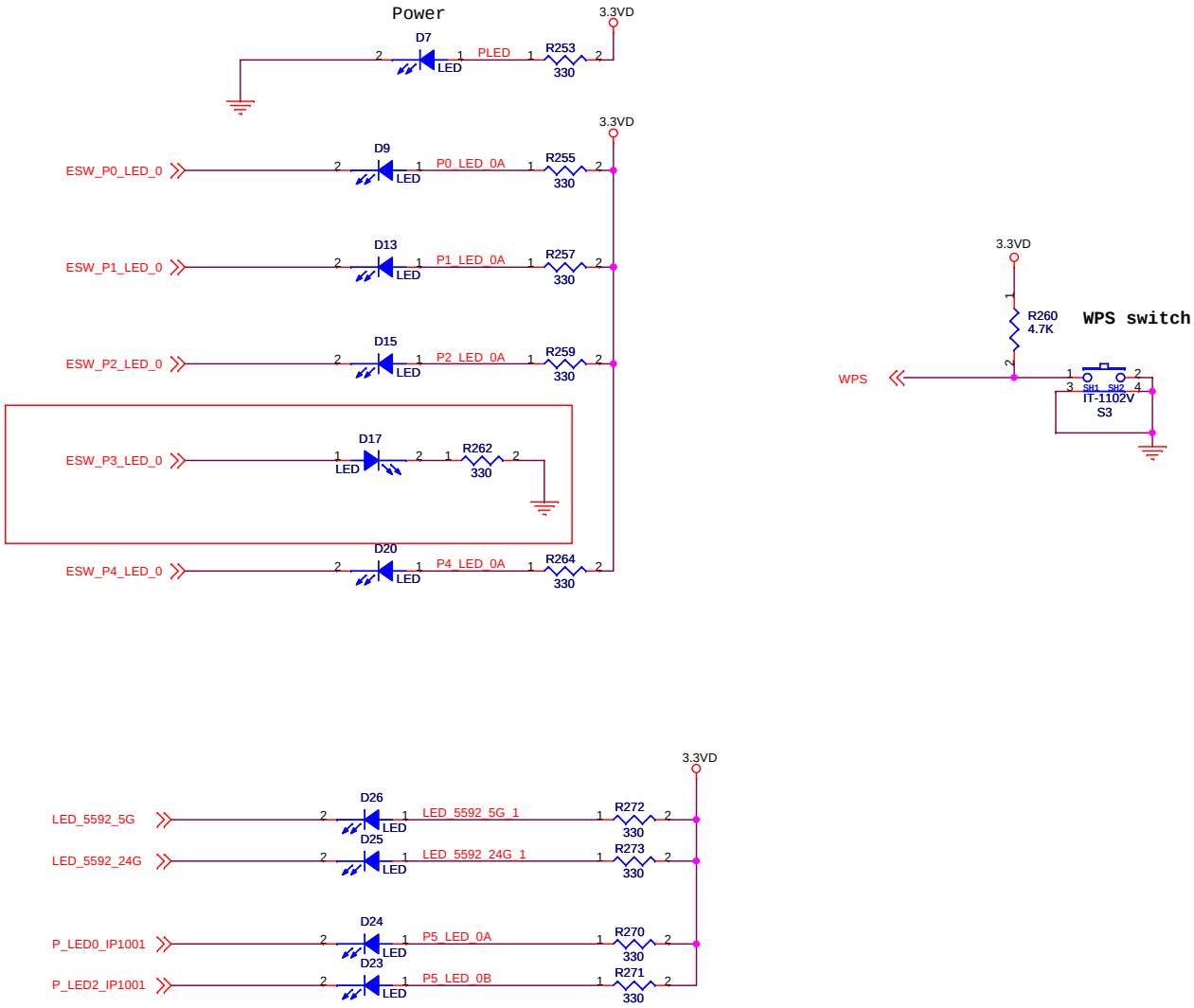
LED



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	Size: B	Document Number: MT7621A	Drawn: Jimmy / Rev: V11
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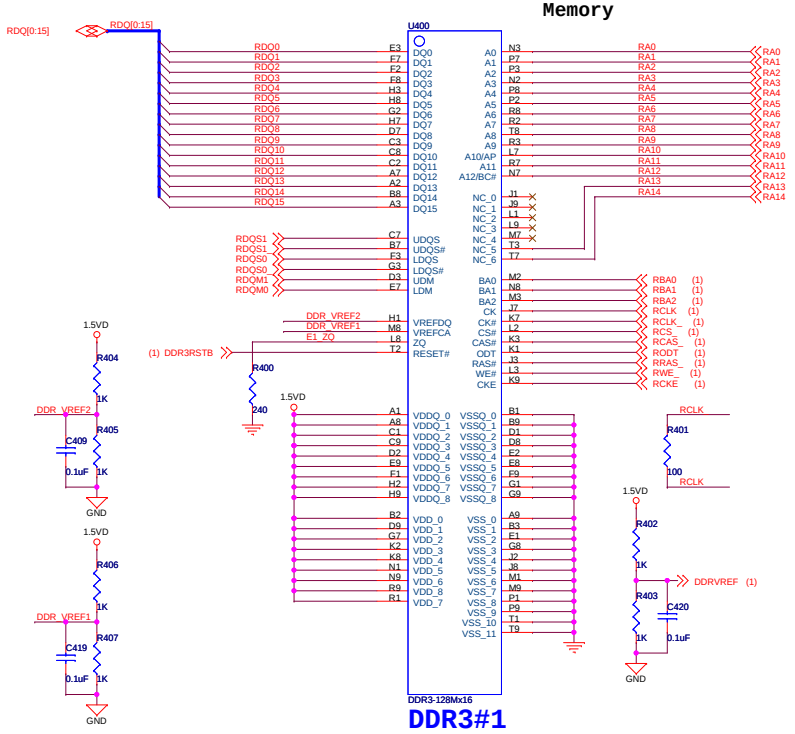
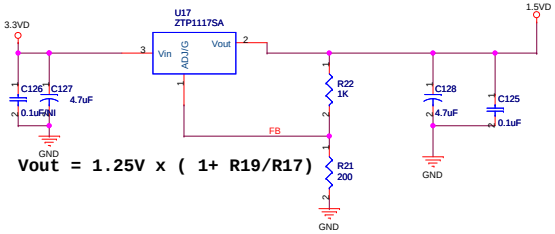
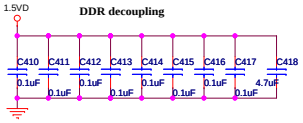
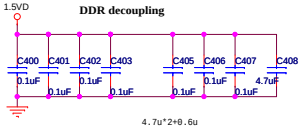
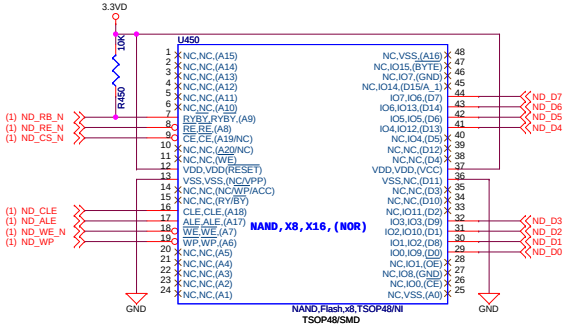
Memory

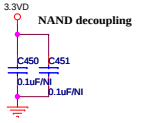












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	Size: C	Document Number: MT7621A	Drawn: Jimmy / Rev: V11
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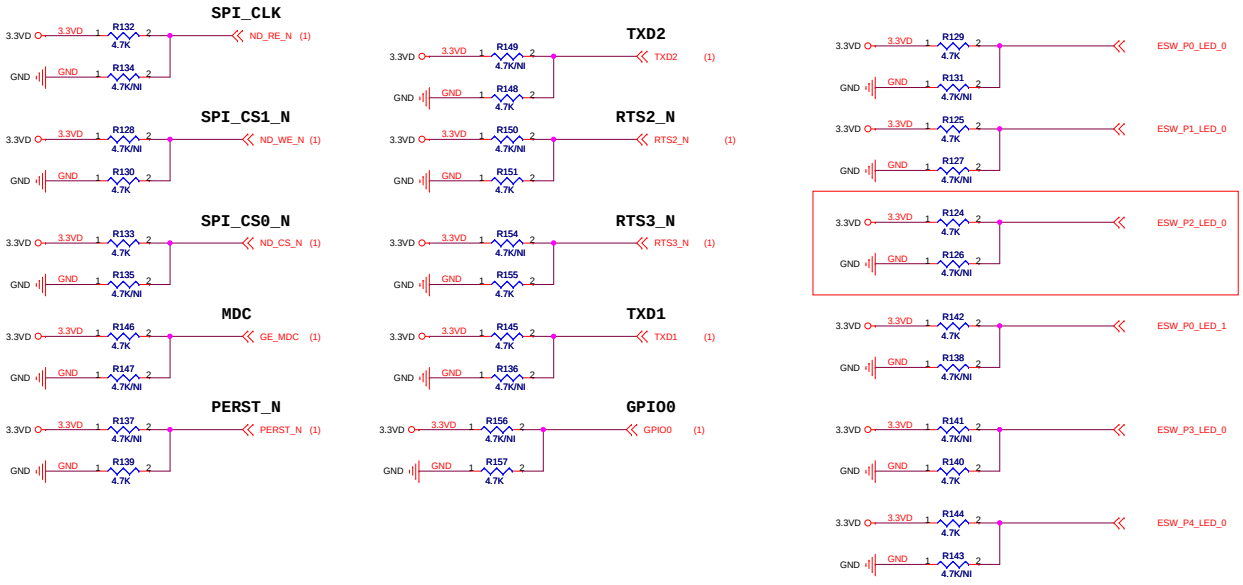
Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



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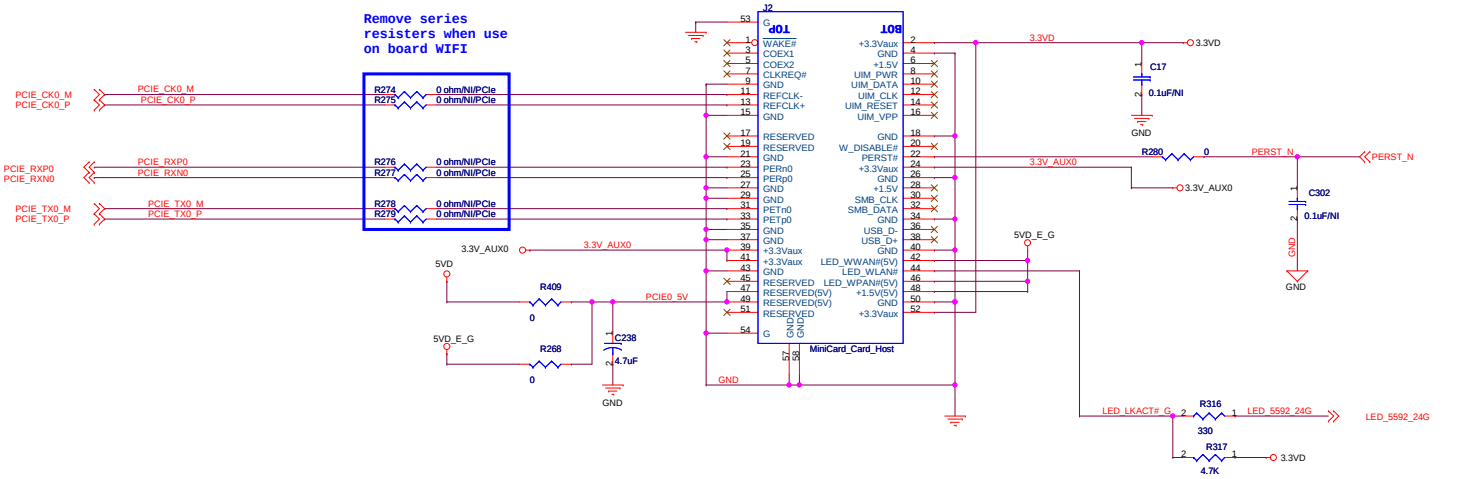
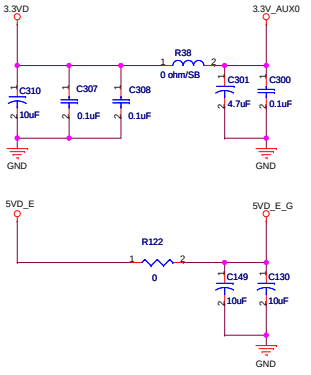
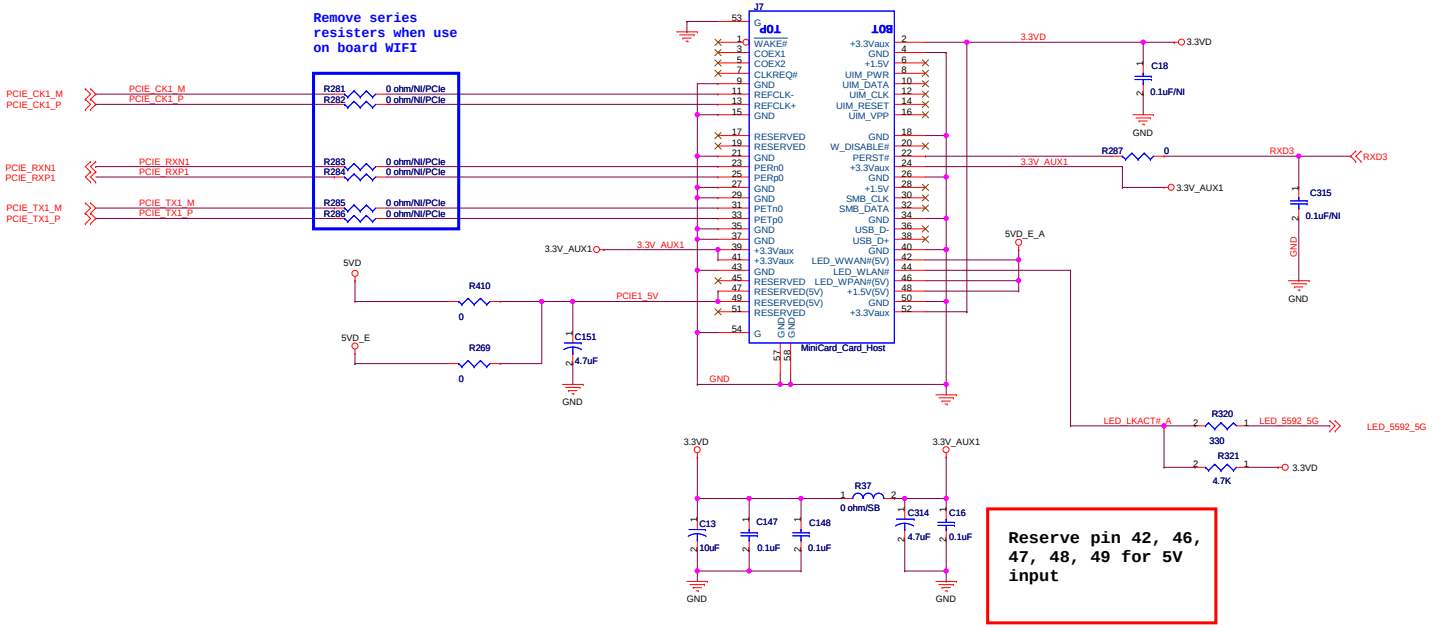
PCIe Slot

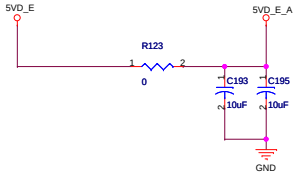




Reserve pin 42, 46, 47, 48, 49 for 5V input



Reserve pin 42, 46, 47, 48, 49 for 5V input



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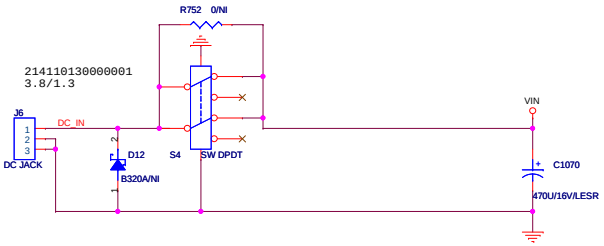
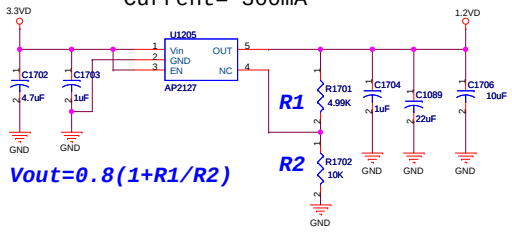
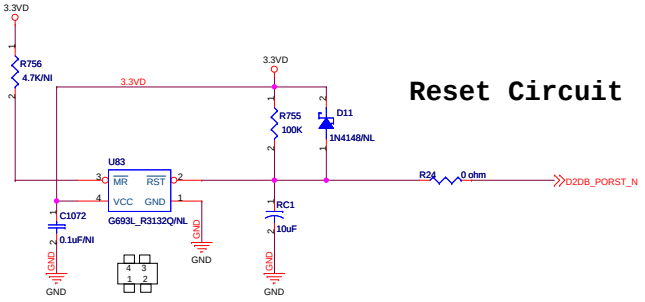
System Power



For USB/PCIe PHY Power (1.2V)
Current= 300mA

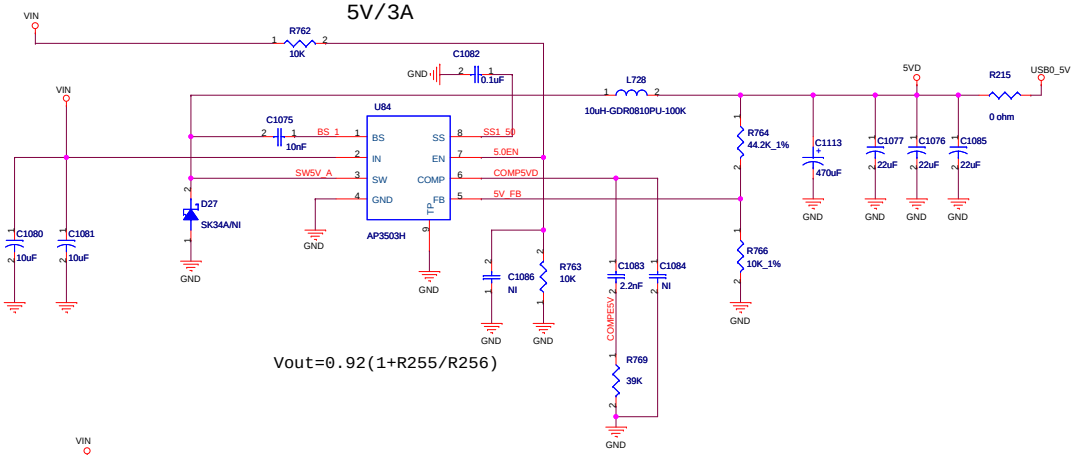


Vout=0.8(1+R1/R2)



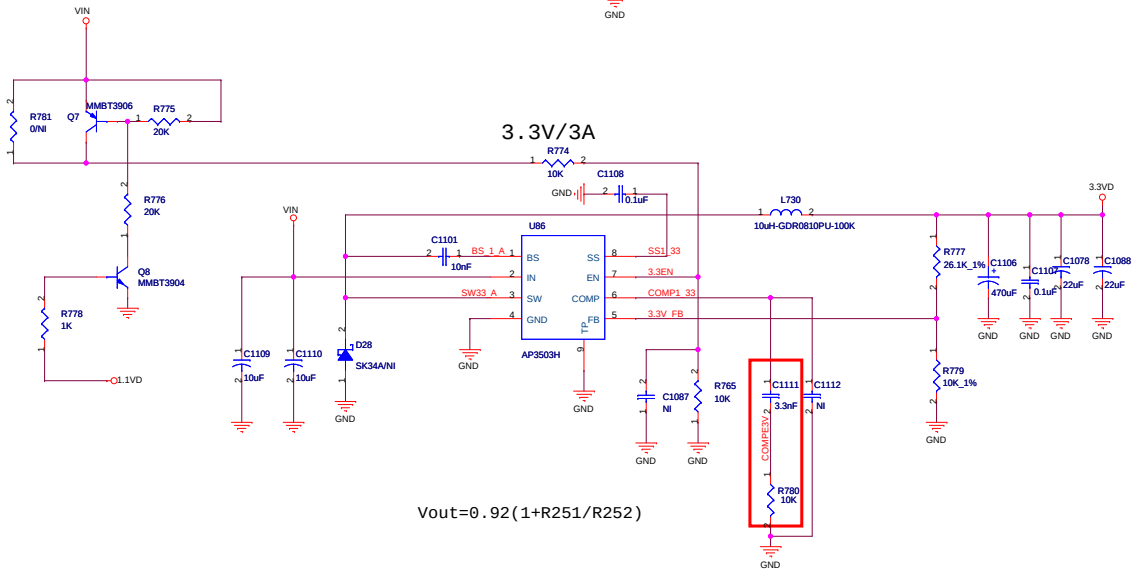
Reset Circuit

5V/3A



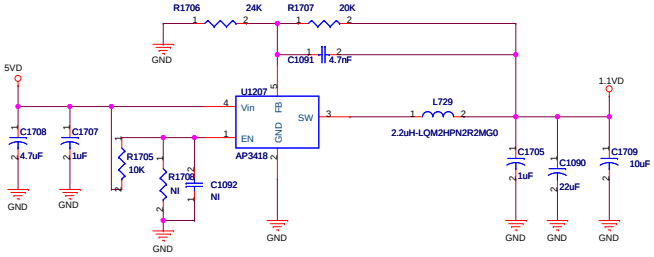
Vout=0.92(1+R255/R256)

3.3V/3A

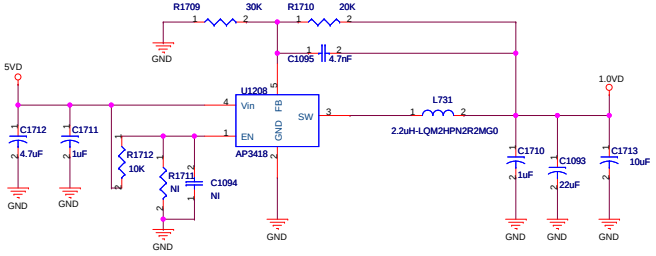


Vout=0.92(1+R251/R252)

1.1V/1.5A



1.0V/1.5A



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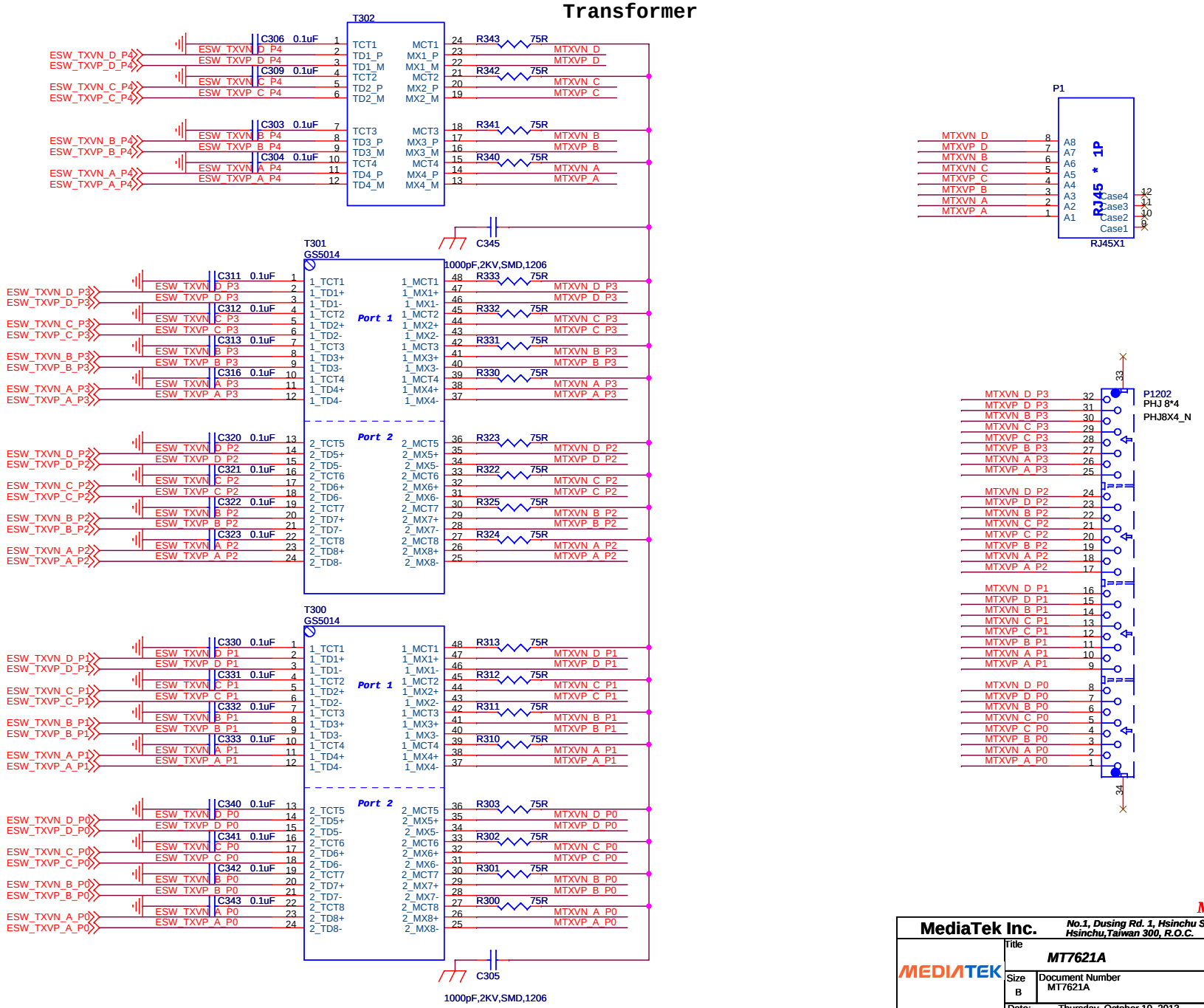
Transformer



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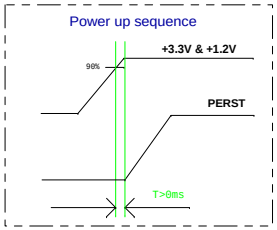
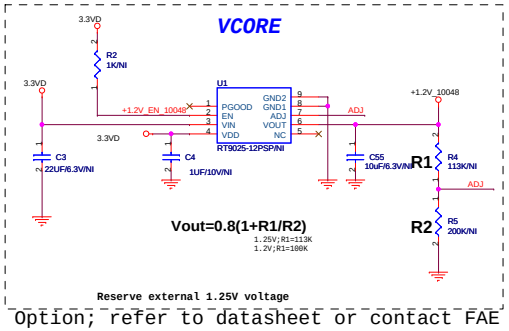
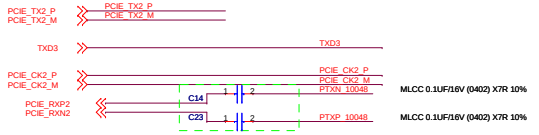
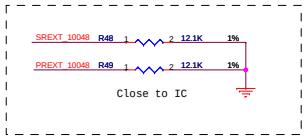
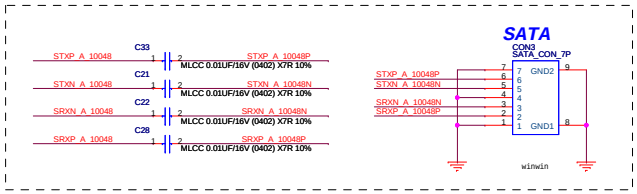
PCIe to SATA

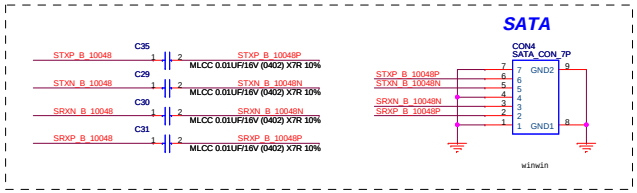


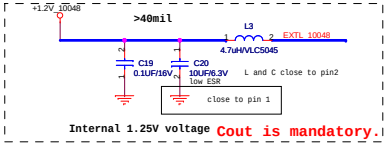


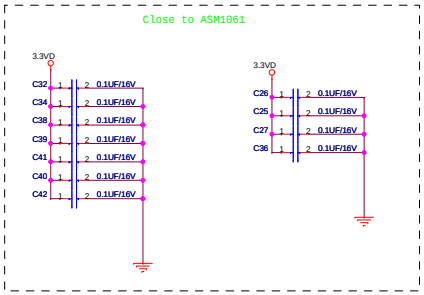


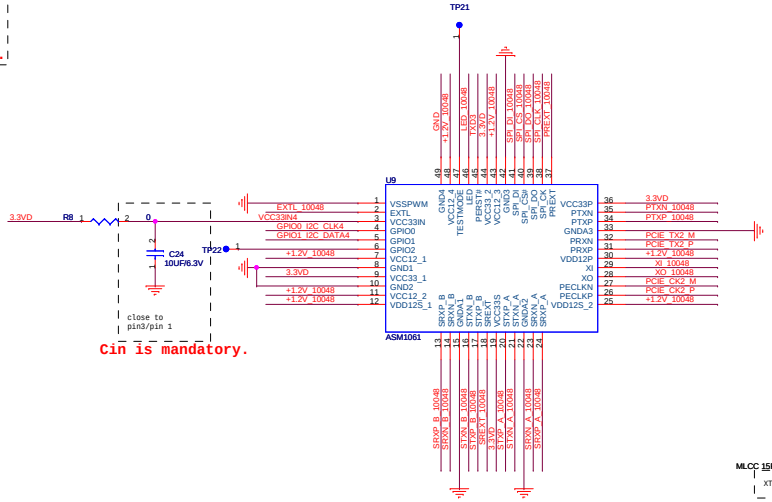


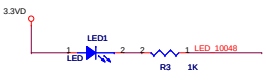


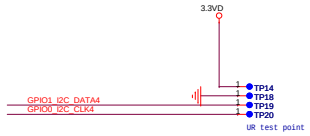


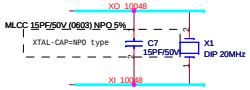




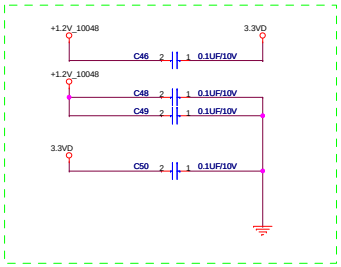








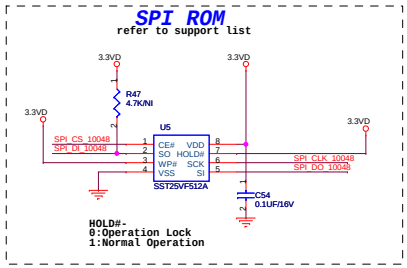
XI & XO follow differential layout rule for Min. jitter



H/W Strapping

refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W



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No.1, Dusing Rd. 1, Hsinchu Science Park
Hsinchu,Taiwan 300, R.O.C.
TEL:+886-3-567-0766
Fax:+886-3-578-7610

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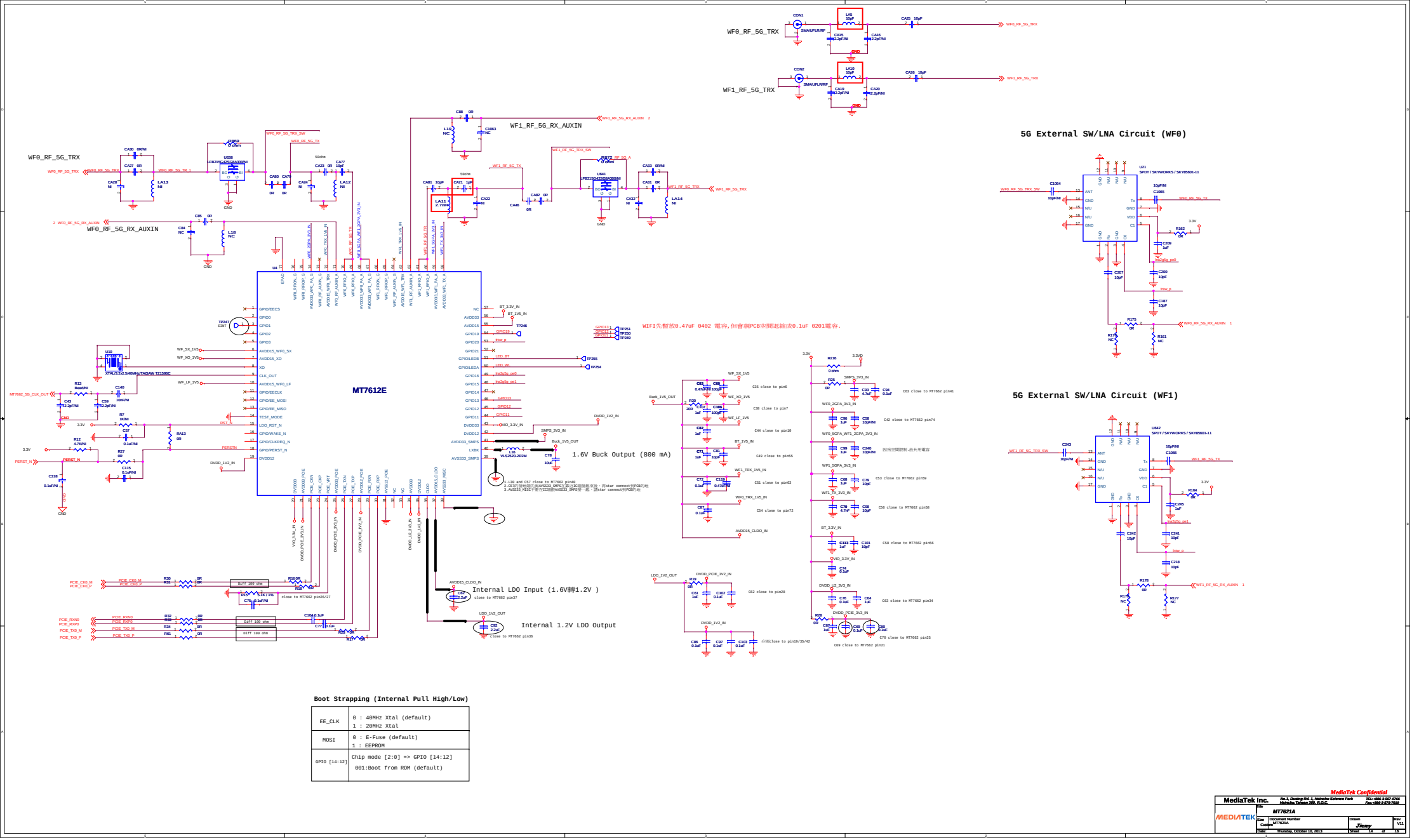

Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Fuse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001:Boot from ROM (default)

MediaTek Inc.
No. 1, Dusing Rd. 1, Hsinchu Science Park
Hsinchu, Taiwan 300, R.O.C.
TEL: +886-3-567-0766
Fax: +886-3-579-7690

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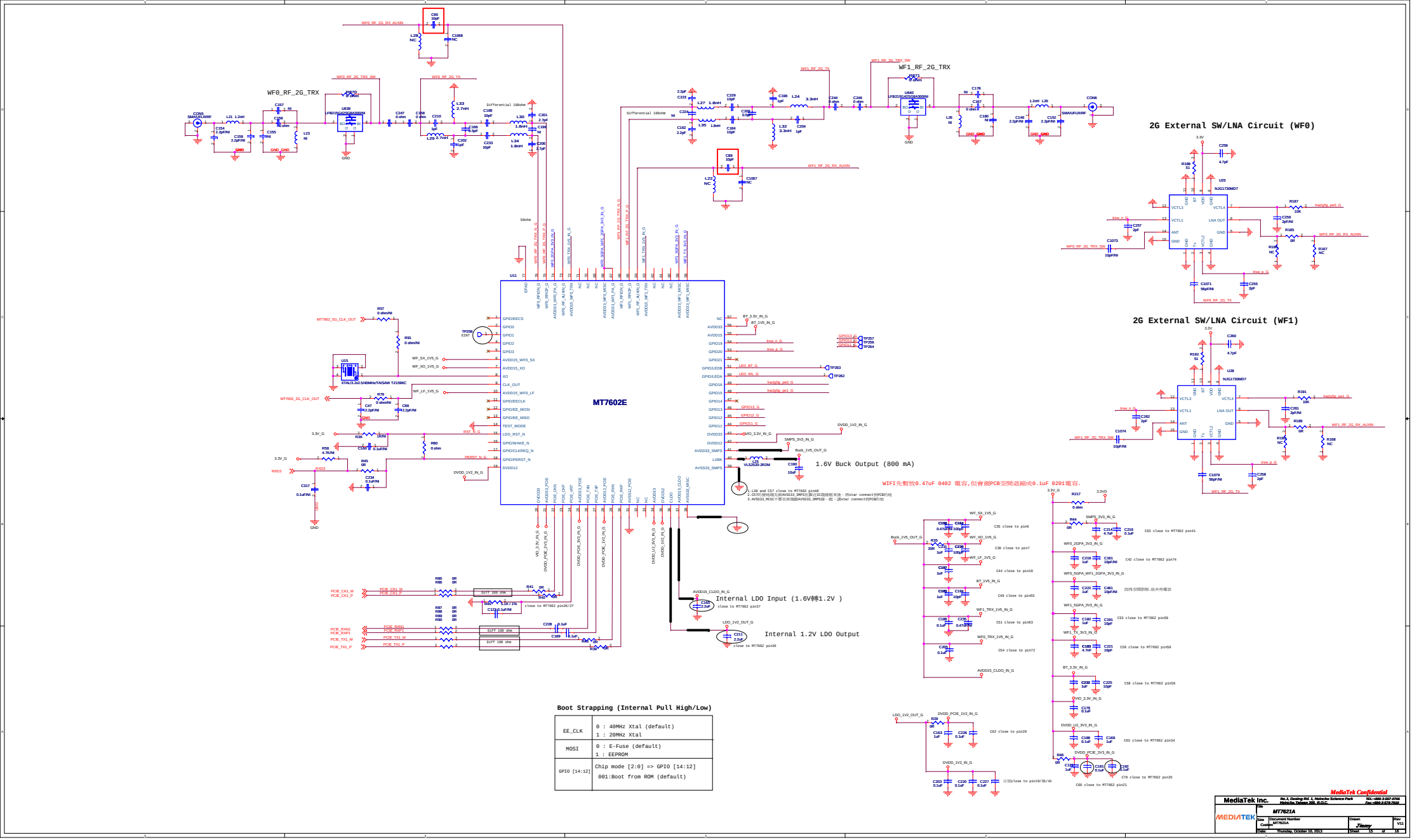
WF0_RF_2G_TRX
WF1_RF_2G_TRX
2G External SW/LNA Circuit (WF0)
2G External SW/LNA Circuit (WF1)
MT7602E
1.6V Buck Output (800 mA)
Internal LDO Input (1.6V轉1.2V)
Internal 1.2V LDO Output
WIFI先暫放0.47uF 0402 電容,但會砌PCB空間退縮成0.1uF 0201電容.
Boot Strapping (Internal Pull High/Low)
EE_CLK
0 : 40MHz Xtal (default)
1 : 20MHz Xtal
MOSI
0 : E-Fuse (default)
1 : EEPROM
GPIO [14:12]
Chip mode [2:0] => GPIO [14:12]
001:Boot from ROM (default)
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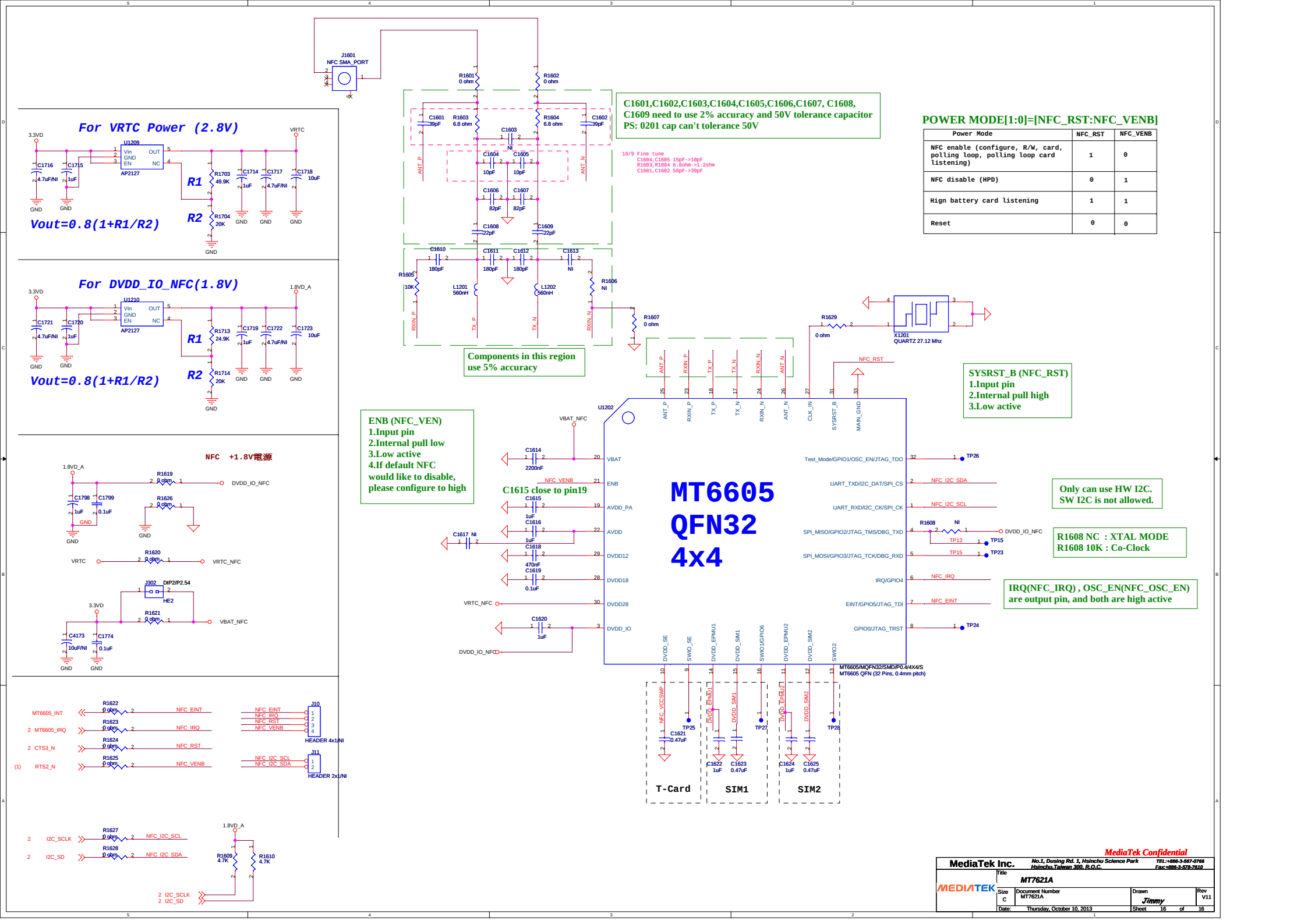
MT7621A
Thursday, October 10, 2013


For VRTC Power (2.8V)
Vout=0.8(1+R1/R2)
For DVDD_IO_NFC(1.8V)
Vout=0.8(1+R1/R2)
NFC +1.8V電源
C1601,C1602,C1603,C1604,C1605,C1606,C1607, C1608, C1609 need to use 2% accuracy and 50V tolerance capacitor
PS: 0201 cap can't tolerance 50V
10/9 Fine tune
C1604,C1605 15pF->10pF
R1603,R1604 6.8ohm->1.2ohm
C1601,C1602 56pF->39pF
Components in this region use 5% accuracy
POWER MODE[1:0]=[NFC_RST:NFC_VENB]
Power Mode | NFC_RST | NFC_VENB
NFC enable (configure, R/W, card, polling loop, polling loop card listening) | 1 | 0
NFC disable (HPD) | 0 | 1
Hign battery card listening | 1 | 1
Reset | 0 | 0
SYSRST_B (NFC_RST)
1.Input pin
2.Internal pull high
3.Low active
ENB (NFC_VEN)
1.Input pin
2.Internal pull low
3.Low active
4.If default NFC would like to disable, please configure to high
C1615 close to pin19
MT6605 QFN32 4x4
Only can use HW I2C.
SW I2C is not allowed.
R1608 NC : XTAL MODE
R1608 10K : Co-Clock
IRQ(NFC_IRQ) , OSC_EN(NFC_OSC_EN) are output pin, and both are high active
MT6605/MQFN32/SMD/P0.4/4X4/S
MT6605 QFN (32 Pins, 0.4mm pitch)
T-Card
SIM1
SIM2
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No.1, Dusing Rd. 1, Hsinchu Science Park
Hsinchu,Taiwan 300, R.O.C.
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Fax:+886-3-578-7610
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