MT7530B/MT7530W

Approval Datasheet

7-port Gigabit Ethernet Switch

Version: 0.91
Release date: 2013-02-22

Table of Contents

Lists of Tables and Figures

1 General Description

1.1 Overview

MT7530B/MT7530W is a highly integrated Ethernet switch with high performance and non-blocking transmission. It includes a 7-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for several applications, such as xDSL, xPON, WiFi AP, and cable modem. MT7530B/MT7530W enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. MT7530B/MT7530W is also designed for cost-sensitive applications in retail and Telecom market. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry.

1.1.1 Features

- 5-port 10/100/1000Mbps MDI transceivers, 1-port RGMII/GMII/TMII/MII MAC, and 1-port RGMII/TRGMII MAC
- One RGMII port supports PHY mode for router application
- Supports 2Gbps TRGMII mode
- Accessible MAC address table with 2048 entries and auto aging and learning capabilities
- Programmable aging timer for MAC address table
- Supports programmable 1518/1536/1552 and 9K Jumbo frame length
- Supports 20/25/40MHz clock source
- Supports SVL and IVL with 8 filtering database
- Supports RSTP and MSTP
- Supports 802.1X
- Supports 4K VLAN entries
- Supports VLAN ID tag and un-tag options for each port
- Supports double tagging VLAN
- Supports hardware port isolation
- Supports 8 priority queues per port
- Supports SP, WFQ, and SP+WFQ latency scheduler
- Supports Max-Min bandwidth scheduler
- Supports ingress and egress rate control
- Supports 64 sets of ACL rules
- Supports IGMPv1/v2/v3 and MLDv1/v2 snooping
- Supports IPv4 and IPv6 multicast frames hardware forwarding
- Supports 40 MIB counters per port
- Supports IEEE 1588v2
- Supports Loop detection indicator
- Supports Broadcast/Multicast/Unknown frames storm suppression
- 10Base-T, 10Base-Te, 100Base-TX, and 1000Base-T compliant Transceivers
- Compliant with IEEE 802.3 Auto-Negotiation

- Supports 3 LEDs per GEPHY port
- Supports short-cable power saving
- Integrated MDI resistors
- Supports IEEE 802.3az Energy Efficient Ethernet
- 128-pin E-PAD, QFP, 14mm x 14mm

2 Block Diagram

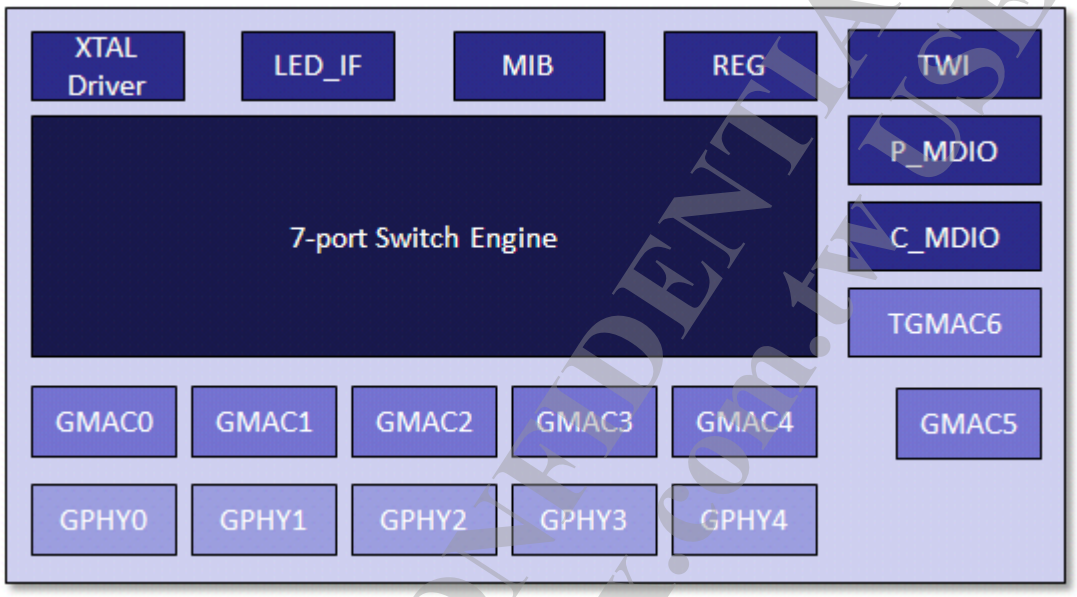


Figure 2-1. MT7530B/MT7530W Block Diagram

3 Pin Assignment

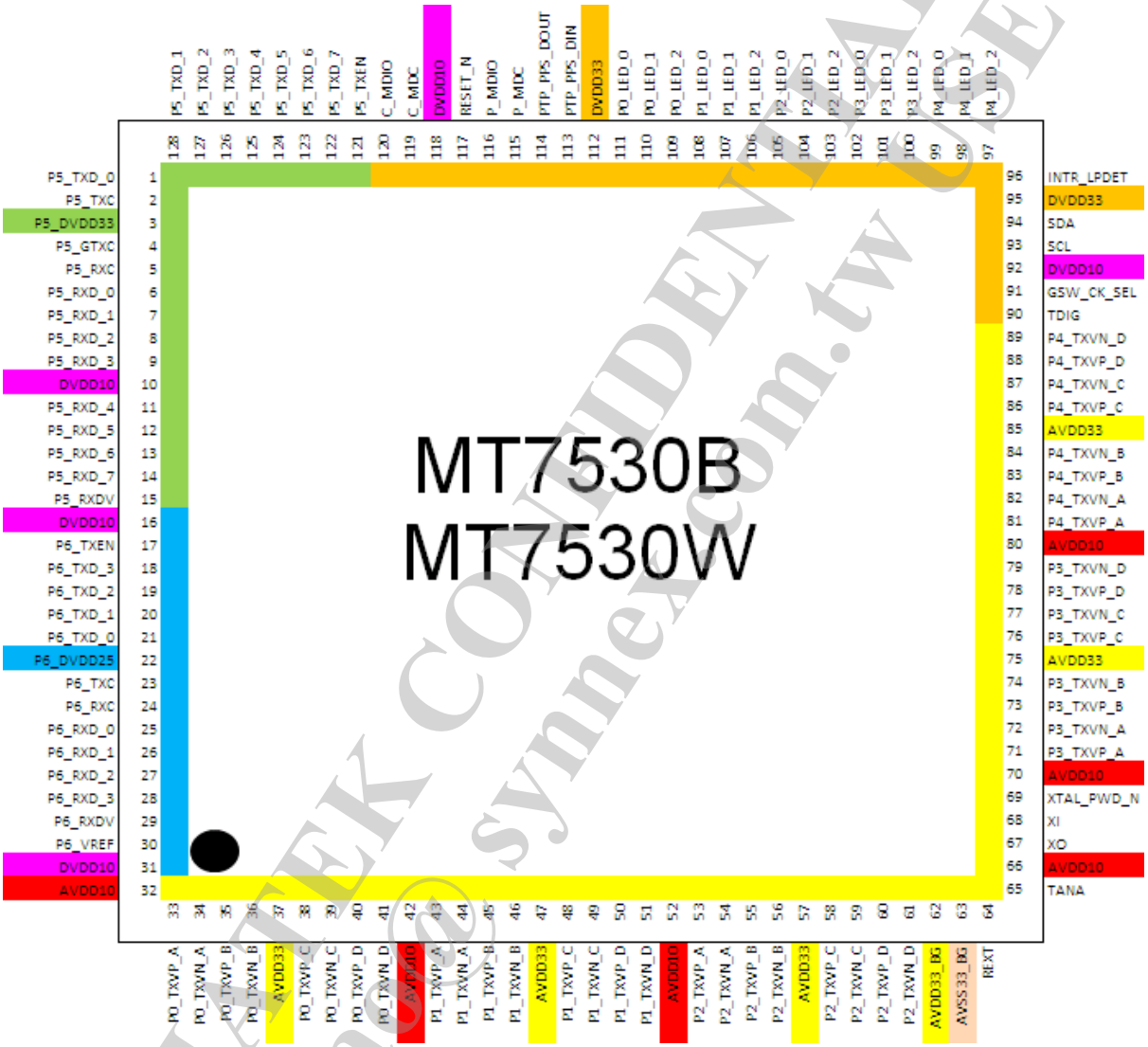


Figure 3-1. MT7530B/MT7530W Pin Diagram

Table 3-1. MT7530B/MT7530W Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	P5_TXD_0	33	P0_TXVP_A	65	TANA	97	P4_LED_2
2	P5_TXC	34	P0_TXVN_A	66	AVDD10	98	P4_LED_1
3	P5_DVDD33	35	P0_TXVP_B	67	XO	99	P4_LED_0
4	P5_GTXC	36	P0_TXVN_B	68	XI	100	P3_LED_2
5	P5_RXC	37	AVDD33	69	XTAL_PWD_N	101	P3_LED_1
6	P5_RXD_0	38	P0_TXVP_C	70	AVDD10	102	P3_LED_0
7	P5_RXD_1	39	P0_TXVN_C	71	P3_TXVP_A	103	P2_LED_2
8	P5_RXD_2	40	P0_TXVP_D	72	P3_TXVN_A	104	P2_LED_1
9	P5_RXD_3	41	P0_TXVN_D	73	P3_TXVP_B	105	P2_LED_0
10	DVDD10	42	AVDD10	74	P3_TXVN_B	106	P1_LED_2
11	P5_RXD_4	43	P1_TXVP_A	75	AVDD33	107	P1_LED_1
12	P5_RXD_5	44	P1_TXVN_A	76	P3_TXVP_C	108	P1_LED_0
13	P5_RXD_6	45	P1_TXVP_B	77	P3_TXVN_C	109	P0_LED_2
14	P5_RXD_7	46	P1_TXVN_B	78	P3_TXVP_D	110	P0_LED_1
15	P5_RXDV	47	AVDD33	79	P3_TXVN_D	111	P0_LED_0
16	DVDD10	48	P1_TXVP_C	80	AVDD10	112	DVDD33
17	P6_TXEN	49	P1_TXVN_C	81	P4_TXVP_A	113	PTP_PPS_DIN
18	P6_TXD_3	50	P1_TXVP_D	82	P4_TXVN_A	114	PTP_PPS_DOUT
19	P6_TXD_2	51	P1_TXVN_D	83	P4_TXVP_B	115	P_MDC
20	P6_TXD_1	52	AVDD10	84	P4_TXVN_B	116	P_MDIO
21	P6_TXD_0	53	P2_TXVP_A	85	AVDD33	117	RESET_N
22	P6_DVDD25	54	P2_TXVN_A	86	P4_TXVP_C	118	DVDD10
23	P6_TXC	55	P2_TXVP_B	87	P4_TXVN_C	119	C_MDC
24	P6_RXC	56	P2_TXVN_B	88	P4_TXVP_D	120	C_MDIO
25	P6_RXD_0	57	AVDD33	89	P4_TXVN_D	121	P5_TXEN
26	P6_RXD_1	58	P2_TXVP_C	90	TDIG	122	P5_TXD_7
27	P6_RXD_2	59	P2_TXVN_C	91	GSW_CK_SEL	123	P5_TXD_6
28	P6_RXD_3	60	P2_TXVP_D	92	DVDD10	124	P5_TXD_5
29	P6_RXDV	61	P2_TXVN_D	93	SCL	125	P5_TXD_4
30	P6_VREF	62	AVDD33_BG	94	SDA	126	P5_TXD_3
31	DVDD10	63	AVSS33_BG	95	DVDD33	127	P5_TXD_2
32	AVDD10	64	REXT	96	INTR_LPDET	128	P5_TXD_1

4 Pin Description

The following notations are used in Type column of Pin description tables:

I	Digital input pin
O	Digital output pin
I/O	Digital bidirectional pin
A	Analog pin
P	Power or ground pin

4.1 System Pins

Table 4-1. System Clock and Reset Pins

Pin Name	Type	Pin Number	Description
RESET_N	I	117	Active low hardware reset.
XO XI	A	68 67	Crystal clock inputs which can support 20MHz and 25MHz crystal driver and 20MHz, 25MHz, and 40MHz external clock.
XTAL_PWD_N	A	69	Crystal driver power down. Put a pull-down resister if external clock source, not crystal driver, is used in XO pin.

Table 4-2. System hardware trap pins

Pin Name	Type	Pin Number	Description
P4_LED_0 P3_LED_0	I/O	99 102	Crystal clock frequency selection {P4_LED_0, P3_LED_0} signals are used to control the crystal clock input frequency to XO and XI. 00: Reserved. 01: 20MHz 10: 40MHz 11: 25MHz (default)
P3_LED_2 P3_LED_1	I/O	100 101	SMI Address selection {P3_LED_2, P3_LED_1} signals are used to define decoded Serial Management Interface(SMI) addresses of C_MDC/C_MDIO for command registers access 00 : Use 7 to 12 SMI addresses 01 : Use 15 to 20 SMI addresses 10 : Use 23 to 28 SMI addresses 11 : Use 31 and 0 to 4 SMI addresses (default)
P1_LED_1	I/O	107	SMI Access control 0: PHY access mode 0 1: PHY access mode 1 (default)
P1_LED_2	I/O	106	P5 Interface Disable

Pin Name	Type	Pin Number	Description
			0: Enable P5 IO 1: Disable P5 IO (default)
P2_LED_1	I/O	104	P5 Interface Mode 0: GMII or MII mode 1: RGMII mode (default)
P4_LED_1	I/O	98	P5 Interface Selection 0: P5 IO is connected to GPHY4 1: P5 IO is connected to GMAC5 (default)
P2_LED_2	I/O	103	P6 Interface Disable 0: Enable P6 IO 1: Disable P6 IO (default)
P0_LED_2	I/O	109	EEPROM Auto Initialization 0: Disable EEPROM auto initialization 1: Enable EEPROM auto initialization (default)
P4_LED_2	I/O	97	Loop Detection Alarm 0: Enable loop detection 1: Disable loop detection (default)

4.2 Digital Signal Pins

Table 4-3. P5 RGMII/GMII pins

Pin Name	Type	Pin Number	Description
P5_TXC	I/O	2	P5 Transmit Clock in MII and GMII mode. P5_TXC provides the timing reference for the transfer of the P5_TXEN and P5_TXD_[3:0] during 10/100 mode.
P5_GTXC	O	4	P5 1000M mode clock in RGMII and GMII. P5_GTXC provides the timing reference for the transfer of the P5_TXEN and P5_TXD_[7:0] during 1000M mode
P5_TXEN	O	121	P5 Transmit Enable
P5_TXD_0 P5_TXD_1 P5_TXD_2 P5_TXD_3 P5_TXD_4 P5_TXD_5 P5_TXD_6 P5_TXD_7	O	1 128 127 126 125 124 123 122	P5 Transmit Data All 8 bits are used in GMII mode, and only the first 4 bits are used in MII and RGMII mode.
P5_RXC	I	5	P5 Receive clock in RGMII and GMII mode. P5_RXC provides the timing reference for the transfer of the P5_RXDV and P5_RXD_[7:0]
P5_RXDV	I	15	P5 Receive Data Valid
P5_RXD_0 P5_RXD_1	I	6 7	P5 Receive Data All 8 bits are used in GMII mode, and only the first 4 bits

Pin Name	Type	Pin Number	Description
P5_RXD_2		8	are used in MII and RGMII mode.
P5_RXD_3		9	
P5_RXD_4		11	
P5_RXD_5		12	
P5_RXD_6		13	
P5_RXD_7		14	

Table 4-4. P6 RGMII/TRGMII Pins

Pin Name	Type	Pin Number	Description
P6_TXC	O	23	P6 Transmit Clock
P6_TXEN	O	17	P6 Transmit Enable
P6_TXD_0	O	21	P6 Transmit Data
P6_TXD_1		20	
P6_TXD_2		19	
P6_TXD_3		18	
P6_RXC	I	24	P6 Receive Clock
P6_RXDV	I	29	P6 Receive Data Valid
P6_RXD_0	I	25	P6 Receive Data
P6_RXD_1		26	
P6_RXD_2		27	
P6_RXD_3		28	
P6_VREF	I	30	P6 IO reference voltage. The pin is connected to the voltage source which is equal to 0.5*P6_DVDD25

Table 4-5. P0 to P5 PHY LED pins

Pin Name	Type	Pin Number	Description
P0_LED_0	I/O	111	P0 PHY LED indicators
P0_LED_1		110	
P0_LED_2		109	
P1_LED_0	I/O	108	P1 PHY LED indicators
P1_LED_1		107	
P1_LED_2		106	
P2_LED_0	I/O	105	P2 PHY LED indicators
P2_LED_1		104	
P2_LED_2		103	
P3_LED_0	I/O	102	P3 PHY LED indicators
P3_LED_1		101	
P3_LED_2		100	
P4_LED_0	I/O	99	P4 PHY LED indicators
P4_LED_1		98	
P4_LED_2		97	

Table 4-6. Digital control pins

Pin Name	Type	Pin Number	Description
TDIG	I/O	90	Digital test pin
GSW_CK_SEL	I	91	Switch clock frequency selection
SCL	I	93	Serial Clock for EEPROM
SDA	I/O	94	Serial Data for EEPROM
INTR_LDDET	O	96	Interrupt and Loop detection
PTP_PPS_DIN	I	113	1588 1PPS input
PTP_PPS_DOUT	O	114	1588 1PPS output
P_MDC	O	115	Management data clock for external transceivers
P_MDIO	I/O	116	Management data input/output for external transceivers
C_MDC	I	119	Management data clock for CPU control
C_MDIO	I/O	120	Management data input/output for CPU control

4.3 Analog Signal Pins

Table 4-7. Analog signal pins

Pin Name	Type	Pin Number	Description
P0_TXVP_A	A	33	Port 0 MDI Transceivers
P0_TXVN_A		34	
P0_TXVP_B		35	
P0_TXVN_B		36	
P0_TXVP_C		38	
P0_TXVN_C		39	
P0_TXVP_D		40	
P0_TXVN_D		41	
P1_TXVP_A	A	43	Port 1 MDI Transceivers
P1_TXVN_A		44	
P1_TXVP_B		45	
P1_TXVN_B		46	
P1_TXVP_C		48	
P1_TXVN_C		49	
P1_TXVP_D		50	
P1_TXVN_D		51	
P2_TXVP_A	A	53	Port 2 MDI Transceivers
P2_TXVN_A		54	
P2_TXVP_B		55	
P2_TXVN_B		56	
P2_TXVP_C		58	
P2_TXVN_C		59	
P2_TXVP_D		60	
P2_TXVN_D		61	
P3_TXVP_A	A	71	Port 3 MDI Transceivers
P3_TXVN_A		72	

Pin Name	Type	Pin Number	Description
P3_TXVP_B		73	
P3_TXVN_B		74	
P3_TXVP_C		76	
P3_TXVN_C		77	
P3_TXVP_D		78	
P3_TXVN_D		79	
P4_TXVP_A	A	81	Port 4 MDI Transceivers
P4_TXVN_A		82	
P4_TXVP_B		83	
P4_TXVN_B		84	
P4_TXVP_C		86	
P4_TXVN_C		87	
P4_TXVP_D		88	
P4_TXVN_D		89	
REXT	A	64	Band gap resistor which is connected to AVSS33_BG through a 24kΩ (±1%) resistor
TANA	A	65	Analog test pin

4.4 Power Pins

Table 4-8. Analog and digital power pins

Pin Name	Type	Pin Number	Description
AVDD33	P	37,47,57,75,85	3.3V Analog IO power
AVDD10	P	32,42,52,66,70,80	1.0V Analog core power
AVDD33_BG	P	62	3.3V Analog power for Bandgap
AVSS_BG	P	63	Analog ground for Bandgap
DVDD33	P	95,112	3.3V digital IO power
P5_DVDD33	P	3	3.3V/2.5V port-5 IO power
P6_DVDD25	P	22	2.5V/1.8V/1.5V port-6 IO power
DVDD10	P	10,16,31,92,118	1.0V digital core power

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage of IO power				TBD	V
Supply voltage of Core power				TBD	V

5.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage of Analog IO power	AVDD33	3.14	3.3	3.46	V
Supply voltage of Analog Core power	AVDD10	0.95	1.0	1.10	V
Supply voltage of Digital IO power @3.3V mode	DVDD33	3.14	3.3	3.46	V
Supply voltage of Digital IO power @2.5V mode	DVDD25	2.38	2.5	2.75	V
Supply voltage of Digital IO power @1.8V mode	DVDD18	1.71	1.8	1.98	V
Supply voltage of Digital IO power @1.5V mode	DVDD15	1.43	1.5	1.65	V
Supply voltage of Digital Core power	DVDD10	0.95	1.0	1.10	V
Ambient temperature	Ta	0		70	°C

5.3 DC Characteristics

5.3.1 P5 IO (3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input logic low voltage	V_{IH}	1.7			V
Input logic high voltage	V_{IL}			0.9	V
DC Output logic low voltage	V_{OH}(DC)	2.1			V
DC Output logic high voltage	V_{OL}(DC)			0.5	V

5.3.2 P5 IO (2.5V), P6 IO (2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input logic low voltage	V_{IH}	1.7			V
Input logic high voltage	V_{IL}			0.7	V
DC Output logic low voltage	V_{OH}(DC)	2.0			V
DC Output logic high voltage	V_{OL}(DC)			0.4	V

5.3.3 P6 IO (1.8V)

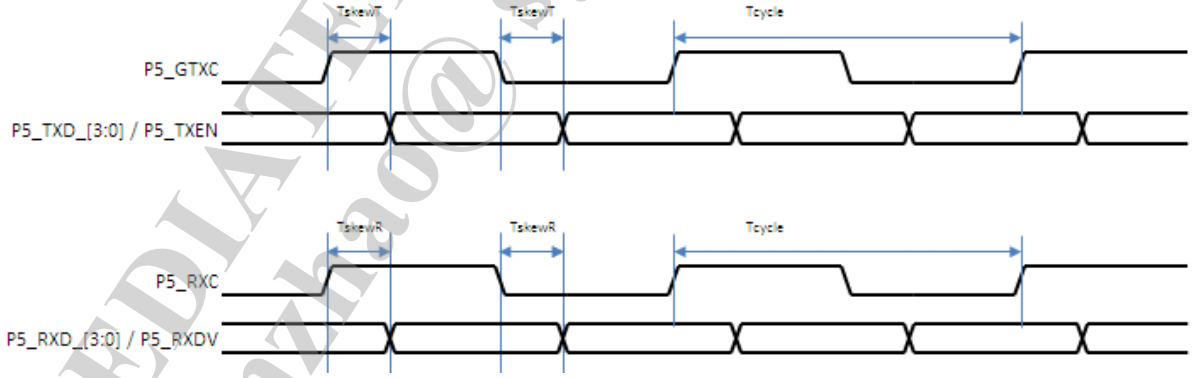
Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference Voltage			0.9		V
Input logic low voltage	V_{IH}	1.025			V
Input logic high voltage	V_{IL}			0.775	V
DC Output logic low voltage	V_{OH}(DC)	1.42			V
DC Output logic high voltage	V_{OL}(DC)			0.28	V

5.3.4 P6 IO (1.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference Voltage			0.75		V
Input logic low voltage	V_{IH}	0.85			V
Input logic high voltage	V_{IL}			0.65	V
DC Output logic low voltage	V_{OH}(DC)	1.2			V
DC Output logic high voltage	V_{OL}(DC)			0.28	V

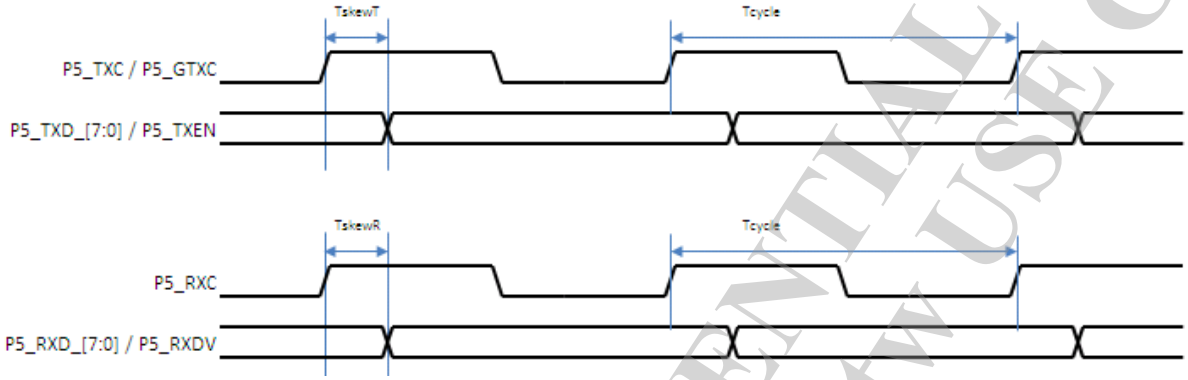
5.4 AC Characteristics

5.4.1 P5 RGMII Timing



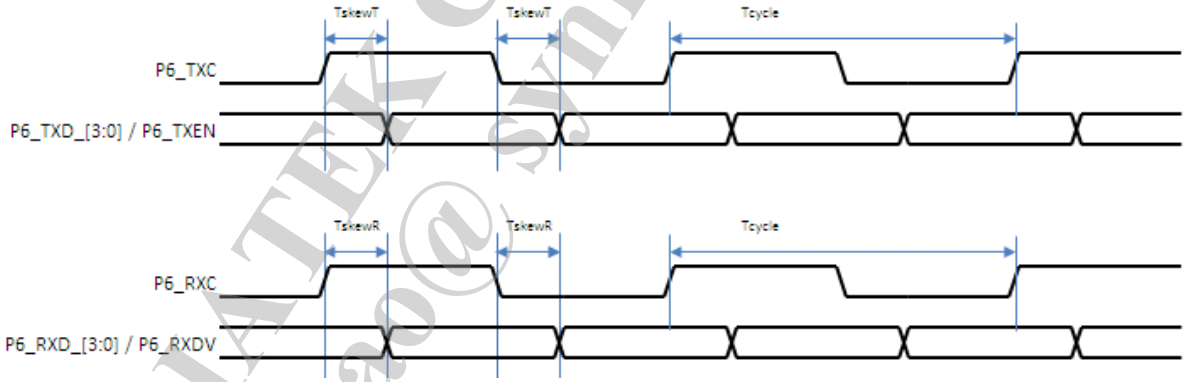
Parameter	Symbol	Min.	Typ.	Max.	Unit
Data to Clock output Skew (at Transmitter)	TskewT	1.2		2.8	ns
Data to Clock input Skew (at Receiver)	TskewR	1.0		3.0	ns
Clock cycle duration (1Gbps)	Tcycle		8		ns
Clock Duty Cycle		45		55	%

5.4.2 P5 GMII Timing



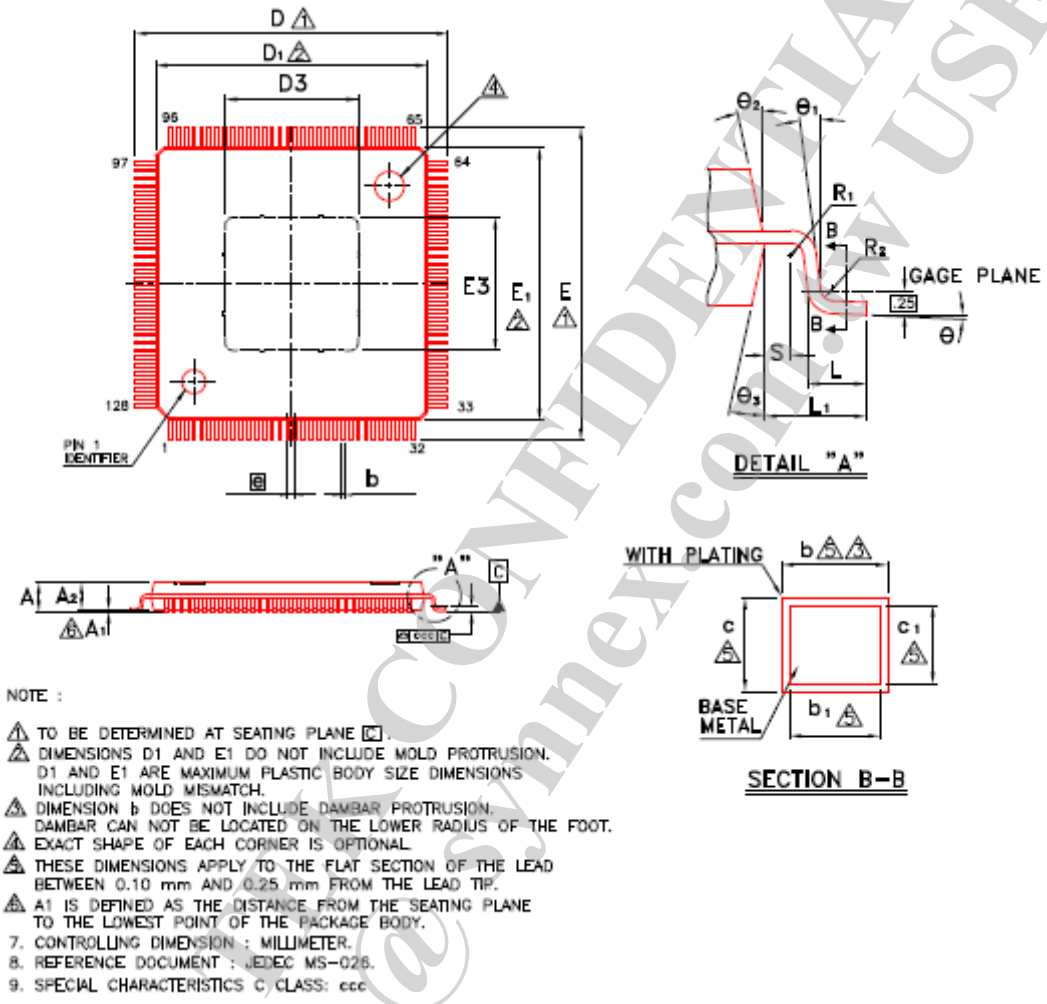
Parameter	Symbol	Min.	Typ.	Max.	Unit
Data to Clock output Skew (at Transmitter)	TskewT	0.5		5.5	ns
Data to Clock input Skew (at Receiver)	TskewR	0		6.0	ns
Clock cycle duration (1Gbps)	Tcycle		8		ns
Clock Duty Cycle		45		55	%

5.4.3 P6 TRGMII Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
Data to Clock output Skew (at Transmitter)	TskewT		0.2		ns
Data to Clock input Skew (at Receiver)	TskewR		0.2		ns
Clock cycle duration (2Gbps)	Tcycle		4		ns
Clock Duty Cycle		47		53	%

6 Package Dimension



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Figure 6-1. 128-pin LQFP package drawing

Table 6-1. 128-pin LQFP package dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.125	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		
ccc	0.08			0.003		

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	6.80 REF	0.268 REF

7 Top Marking

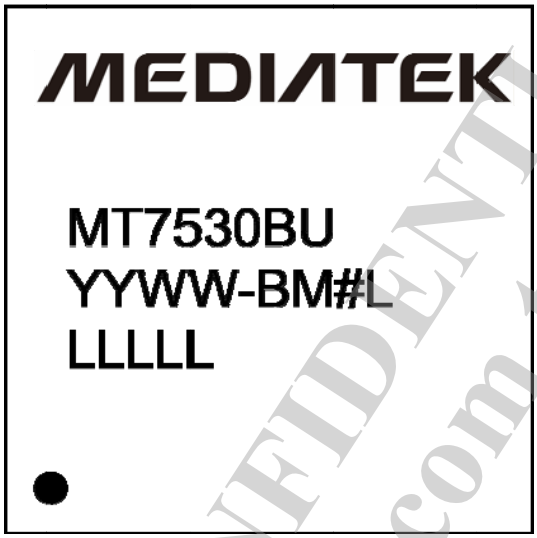


Figure 7-1. MT7530B Top marking

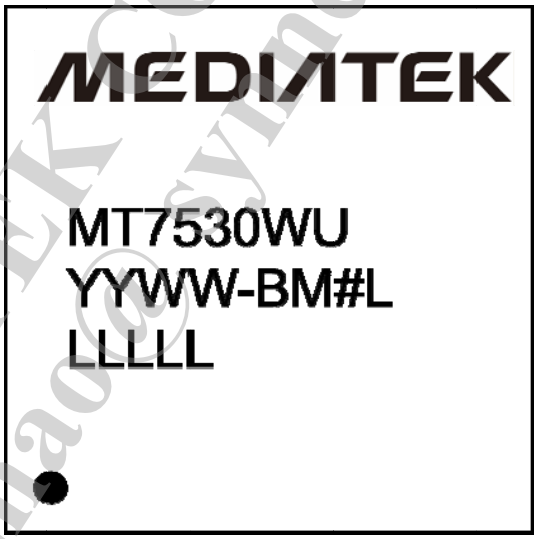


Figure 7-2. MT7530W Top marking