MT7602E
802.11b/g/n Wi-Fi 2T2R single chip
Preliminary datasheet

Version: 0.01

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Document Revision History

Revision	Date	Author	Description
0.01	2013/7/1	Ben Lin	Preliminary release

Table of Contents

1 System Overview

1.1 General Descriptions

The MT7602E is a highly integrated single chip which has built in a 2x2 single-band wireless LAN radio. It supports IEEE 802.11b/g/n standard and provides the highest PHY rate up to 300Mbps, offering feature-rich wireless connectivity and reliable throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. MT7602E integrates PA/LNA such that the number of the external components is reduced to minimum. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7602E supports the 802.11i security standard and implements hardware acceleration for TKIP, CCMP, GCMP, and WAPI. The device also supports 802.11e QoS for video, voice, and multimedia applications.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- 20/40MHz crystal clock support with low power operation in sleep mode
- Best-in-class active and idle power consumption performance
- Compact 9mm x 9mm QFN76L package
- Fully compliance with PCIe base specification v1.1 with OBFF, LTR ECN support
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- External serial flash support
- 14 programmable general purpose Input / Output
- 2 configurable LED pins
- Internal thermal sensor for temperature compensation and thermal protection.
- Self calibration

1.2.2 WLAN

- IEEE 802.11 b/g/n compliant
- Support 20MHz and 40MHz bandwidth in 2.4GHz band
- 2T2R mode with data rate up to 300Mbps
- Support STBC, LDPC, MRC, and transmit Beamforming
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- Integrated LNA, PA, and T/R switch.
- Optional external LNA and PA support.
- IEEE 802.11 d/e/h/i/k/r/w support

- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- TCP checksum offload
- 802.11 to 802.3 header translation offload
- Supports Wi-Fi Direct
- Per packet transmit power control

1.3   Applications

MT7602E is designed for PCI Express Full/Half Mini Card as well as Next Generation Form Factor (NGFF). It is suitable for the following applications.

- Desktop PC
- Laptop NB
- Tablet NB
- xDSL modem
- AP router

1.4   Block Diagram
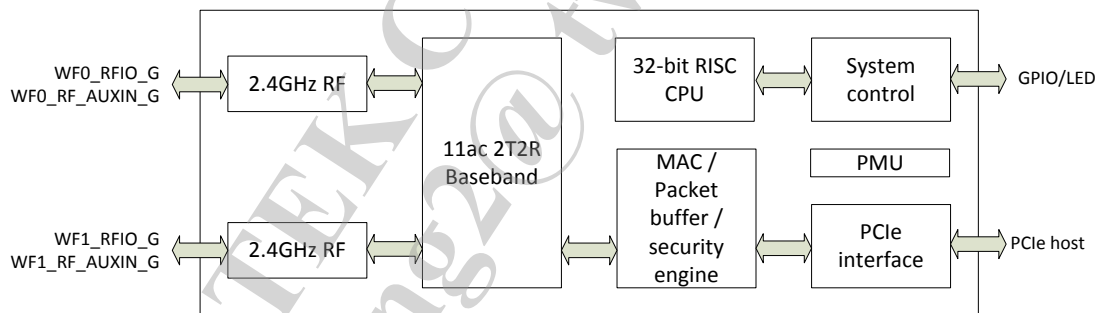
Figure 1 MT7602E block diagram

2 Product Descriptions

2.1 Pin Layout

Top pins (left to right, 76 to 58):

Pin	Name
76	WF0_RFION_G
75	WF0_RFIOP_G
74	AVDD33_WF0_PA_G
73	WF0_RF_AUXIN_G
72	AVDD15_WF0_TRX
71	NC
70	NC
69	NC
68	AVDD33_WF0_MISC
67	AVDD33_WF1_PA_G
66	WF1_RFION_G
65	WF1_RFIOP_G
64	WF1_RF_AUXIN_G
63	AVDD15_WF1_TRX
62	NC
61	NC
60	NC
59	AVDD33_WF1_MISC
58	AVDD33_WF1_MISC

Left pins (top to bottom):

Pin	Name
1	EE_CS
2	GPIO00
3	GPIO01
4	GPIO02
5	GPIO03
6	AVDD15_WF0_SX
7	AVDD15_XO
8	XO
9	CLK_OUT
10	AVDD15_WF0_LF
11	EE_CLK
12	EE_MOSI
13	EE_MISO
14	TEST_MODE
15	LDO_RST_N
16	WAKE_N
17	CLKREQ_N
18	PERST_N
19	DVDD12

MT7602E

Right pins (top to bottom):

Pin	Name
57	NC
56	AVDD33
55	AVDD15
54	GPIO19
53	GPIO20
52	GPIO21
51	LED_B
50	LED_A
49	GPIO16
48	GPIO15
47	GPIO14
46	GPIO13
45	GPIO12
44	GPIO11
42	DVDD33
42	DVDD12
41	AVDD33_SMPS
40	LXBK
39	AVSS33_SMPS

Bottom pins (left to right, 20 to 38):

Pin	Name
20	DVDD33
21	AVDD33_PCIE
22	PCIE_CKN
23	PCIE_CKP
24	PCIE_VRT
25	AVDD33_PCIE
26	PCIE_TXN
27	PCIE_TXP
28	AVDD12_PCIE
29	PCIE_RXN
30	PCIE_RXP
31	AVSS12_PCIE
32	NC
33	NC
34	AVDD33
35	DVDD12
36	CLDO
37	AVDD15_CLDO
38	AVSS33_MISC

Figure 2 Top view of MT7602E QFN pin-out.

2.2   PIN Description

QFN76	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
15	LDO_RST_N	External system reset active low	N/A	Input	DVDD33
8	XO	Crystal input or external clock input	N/A	Input	AVDD15_XO
PCIe interface					
16	WAKE_N	Request system to wake from the sleep/suspend state	PU	Output	DVDD33
17	CLKREQ_N	Reference clock request signal	PU	Output	DVDD33
18	PERST_N	PCIe functional reset	PU	Input	DVDD33
22	PCIE_CKN	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
23	PCIE_CKP	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
26	PCIE_TXN	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
27	PCIE_TXP	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
29	PCIE_RXN	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
30	PCIE_RXP	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
24	PCIE_VRT	PCIe resister reference	N/A	Analog	
EEPROM/flash interface					
13	EE_MISO	External memory data input / Antenna select	PD	Input	DVDD33
12	EE_MOSI	External memory data output / Antenna select	PD	Output	DVDD33
11	EE_CLK	External clock	PD	Output	DVDD33
1	EE_CS	External chip select	PU	Output	DVDD33
Programmable I/O					
2	GPIO0	Programmable input/output	PD	In/out	DVDD33
3	GPIO1	Programmable input/output	PD	In/out	DVDD33
4	GPIO2	Programmable input/output	PD	In/out	DVDD33
5	GPIO3	Programmable input/output	PD	In/out	DVDD33
44	GPIO11	Programmable input/output	PD	In/out	DVDD33
45	GPIO12	Programmable input/output	PD	In/out	DVDD33
46	GPIO13	Programmable input/output	PD	In/out	DVDD33
47	GPIO14	Programmable input/output	PD	In/out	DVDD33
48	GPIO15	Programmable input/output	PD	In/out	DVDD33
49	GPIO16	Programmable input/output	PU	In/out	DVDD33

45	GPIO19	Programmable input/output	PD	In/out	DVDD33
53	GPIO20	Programmable input/output	PD	In/out	DVDD33
52	GPIO21	Programmable input/output	PD	In/out	DVDD33
LED					
50	LED_A	Programmable open-drain LED controller	PU	Output	DVDD33
51	LED_B	Programmable open-drain LED controller	PU	Output	DVDD33
WIFI radio interface					
64	WF1_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Output	
65	WF1_RFIOP_G	RF g-band RF port	N/A	Input	
66	WF1_RFION_G	RF g-band RF port	N/A	Input	
73	WF0_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Output	
75	WF0_RFIOP_G	RF g-band RF port	N/A	Input	
76	WF0_RFION_G	RF g-band RF port	N/A	Input	
9	CLK_OUT	XTAL buffered clock output	N/A	Output	
PMU/SMPS					
36	CLDO	LDO 1.2V output	N/A	Output	
37	AVDD15_CLDO	Digital LDO 1.5V input	N/A	Input	
41	AVDD33_SMPS	SMPS 3.3V power supply	N/A	Input	
40	LXBK	SMPS 1.5V output	N/A	Output	
Miscellaneous					
14	TEST_MODE	Test mode enable	N/A	Input	DVDD33
Power supplies					
20, 43	DVDD33	Digital 3.3v I/O power supply	N/A	Power	
19, 35, 42	DVDD12	Digital 1.2v core power supply	N/A	Power	
21, 25	AVDD33_PCIE	PCIe 3.3V power supply	N/A	Power	
28	AVDD12_PCIE	PCIe 1.2V power supply	N/A	Power	
58, 59	AVDD33_WF1_MISC	RF 3.3v power supply	N/A	Power	
67	AVDD33_WF1_PA_G	RF 3.3v power supply	N/A	Power	
68	AVDD33_WF0_MISC	RF 3.3v power supply	N/A	Power	
74	AVDD33_WF0_PA_G	RF 3.3v power supply	N/A	Power	
34, 56	AVDD33	Analog power supply	N/A	Power	
6	AVDD15_WF0_SX	RF 1.5v power supply	N/A	Power	
7	AVDD15_XO	RF 1.5v power supply	N/A	Power	
10	AVDD15_WF0_LF	RF 1.5v power supply	N/A	Power	
63	AVDD15_WF1_TRX	RF 1.5v power supply	N/A	Power	

72	AVDD15_WF0_TRX	RF 1.5v power supply	N/A	Power	
55	AVDD15	Analog 1.5v power supply	N/A	Power	
31	AVSS12_PCIE	PCIe ground	N/A	Ground	
38	AVSS33_MISC	PMU ground	N/A	Ground	
39	AVSS33_SMPS	PMU ground	N/A	Ground	
32, 33, 57, 60, 61, 62, 69, 70, 71	NC	Reserved	N/A	N/A	
E-PAD	VSS	Ground	N/A	Ground	

Table 1 Pin descriptions

2.3   Strapping option

| QFN76	Pin Name	Pin description	Default PU/PD
12	EE_MOSI	EXT_EE_SEL: Pull down	PD
11	EE_CLK	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
47	GPIO14	CHIP_MODE[2]: Pull down	PD
46	GPIO13	CHIP_MODE[1]: Pull down	PD
45	GPIO12	CHIP_MODE[0]: Pull up	PD

Table 2 Strapping option

2.4   IO control option

MT7602E provides 14 configurable I/O functions to support diversified applications. It supports external front-end module for high power requirement. Open drained I/Os are available for LED.

QFN76	Pin Name	GPIO mode	Default mode	External FEM mode 7	External FEM mode 4	External FEM mode 3
2	GPIO0	GPIO0	Reserved	Reserved	Reserved	Reserved
3	GPIO1	GPIO1	GPIO1	Reserved	GPIO1	Reserved
4	GPIO2	GPIO2	WL_DISABLE	Reserved	WL_DISABLE	WL_DISABLE
5	GPIO3	GPIO3	GPIO3	Reserved	GPIO3	Reserved
44	GPIO11	GPIO11	GPIO11	PA2G_PE1	Reserved	GPIO11
45	GPIO12	GPIO12	GPIO12	PA2G_PE0	Reserved	LED_WL
46	GPIO13	GPIO13	GPIO13	Reserved	LNA2G_PE1	PA2G_PE1
47	GPIO14	GPIO14	GPIO14	Reserved	LNA2G_PE0	PA2G_PE0
48	GPIO15	GPIO15	Reserved	LNA2G_PE1	Reserved	Reserved
49	GPIO16	GPIO16	Reserved	LNA2G_PE0	Reserved	Reserved
50	LED_A	GPIO17	LED_WL	GPIO17	LED_WL	LNA2G_PE1
51	LED_B	GPIO18	LED_B	LED_B	LED_B	LNA2G_PE0
54	GPIO19	GPIO19	GPIO19	TRSW_N	TRSW_N	TRSW_N
53	GPIO20	GPIO20	Reserved	TRSW_P	TRSW_P	TRSW_P

Table 3 IO control option

2.5   Package information
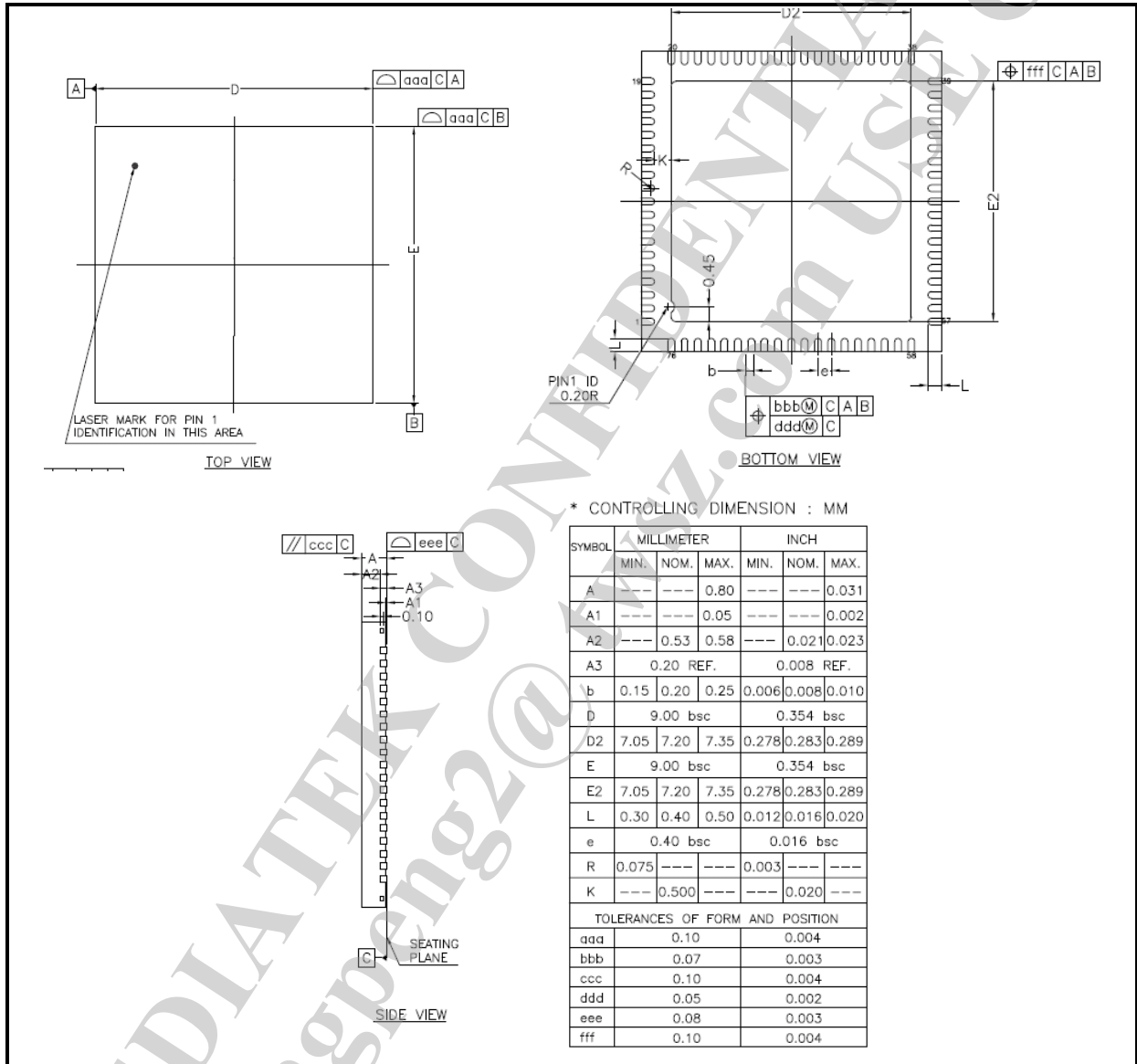
Figure 3 Package outline drawing

2.6   Ordering Information

Part number	Package	Operational temperature range
MT7602EN/A-L	9x9x0.8 mm 76-QFN	-10~70°C

Table 4 Ordering information

2.7   TOP Marking Information

```
MEDIATEK
MT7602EN
DDDD-####
BBBBBBB
```

```
MT7602EN : Part number
DDDD     : Date code
####     : Internal control code
BBBBBBB  : Lot number
```

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.5V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 5 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 6 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$|I_{OL}|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$|I_{OH}|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 7 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
T_J	Maximum Junction Temperature (Plastic Package)	TBD	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	TBD	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	TBD	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	TBD	°C/W

Note:

[1] Half mini-card, 4-layer PCB
[2] 9mm x 9mm QFN76L package

Table 8 Thermal information

3.5 Current consumption

3.5.1 WLAN current consumption

Description	Performance	
	TYP	Unit
Sleep mode	TBD	mA
RX Active, HT40, MCS7	TBD	mA
RX Power saving, DTIM=1	TBD	mA
RX Listen	TBD	mA
TX HT40, MCS7 @15dBm	TBD	mA
TX CCK, 11Mbps @19dBm	TBD	mA

Note: All result is measured with internal switching regulator enabled.

Table 9 WLAN 2.4GHz Current Consumption

ESD CAUTION

MT7602E is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7602E is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.