CORDIC: Cartesian to Polar Coordinate Transformation

COordinate Rotation DIgital Computer (CORDIC) is a simple and efficient algorithm to calculate trigonometric functions, hyperbolic functions, square roots, multiplications, divisions, and exponentials and logarithms with arbitrary base, typically converging with one digit (or bit) per iteration. It is required to design a digital circuit for implementing the transformation from cartesian coordinates into polar coordinates using the CORDIC algorithm in Vectoring mode. It is implemented with these recursive equations:

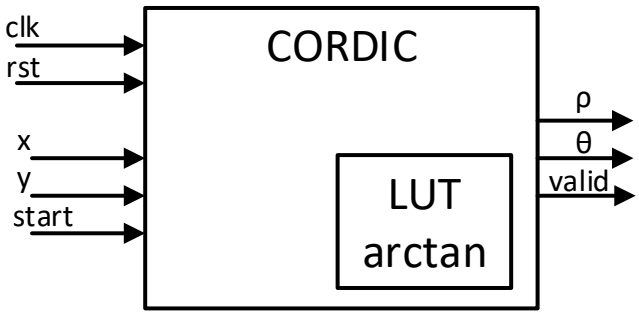
$$x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i}$$
$$y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i}$$
$$z_{i+1} = z_i - d_i \cdot \arctan\left(2^{-i}\right)$$

where $d_i = -1$, if $y_i < 0$, +1 otherwise. After *n* iterations, the equations converge to:

$$x_n = A_n \cdot \sqrt{{x_0}^2 + {y_0}^2}$$
$$y_n = 0$$
$$z_n = z_0 + \arctan\left(\frac{y_0}{x_0}\right)$$

$$A_n = \prod_{i=0}^{n} \sqrt{1 + 2^{2^{-i}}}$$

The interface of the circuit to be designed is as follows:



Once defined the number of iterations to perform into the CORDIC circuit, a LUT of proper size can be used to store the *arctan* values. The number of bits (and the fixed-point representation) of both inputs and output must be defined, evaluating the error committed.

You are requested to deal with the various possible error situations, documenting the choices made. In particular, it is necessary to take into consideration:

- Zero point (0, 0)
- Start asserted when processing is ongoing

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.).
- Description of the architecture designed (block diagram, inputs/outputs, etc.).
- VHDL code (with detailed comments) to be attached to the report.

- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning.
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions.