

UNIVERSITÀ DI PISA

CORDIC: Cartesian to Polar Coordinate Transformation

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1 Introduction

1.1 Specification

It is required to design a digital circuit for implementing the transformation from cartesian coordinates into polar coordinates using the CORDIC algorithm in Vectoring mode. It is implemented with these recursive equations:

$$\begin{aligned}x_{i+1} &= x_i - y_i \cdot d_i \cdot 2^{-i} \\y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\z_{i+1} &= z_i - d_i \cdot \arctan(2^{-i})\end{aligned}$$

where $d_i = -1$ if $y_i > 0$, $+1$ otherwise. After n iterations, the equations converge to:

$$\begin{aligned}x_n &= A_n \cdot \sqrt{x_0^2 + y_0^2} \\y_n &= 0 \\z_n &= z_0 + \arctan\left(\frac{y_0}{x_0}\right) \\A_n &= \prod_{i=0}^n \sqrt{1 + 2^{-2i}}\end{aligned}$$

1.2 Circuit Applications

The CORDIC (COordinate Rotation DIgital Computer) algorithm is an iterative method for performing vector rotations and solving mathematical functions such as trigonometric, hyperbolic, exponential, logarithmic, and square root operations. It was introduced by Jack E. Volder in 1959 to simplify the computation of these functions in hardware with limited resources.

CORDIC is widely used because it eliminates the need for multiplication and division, relying instead on shift and addition operations. This makes it highly efficient for

hardware implementations, particularly in devices with limited computational power, such as embedded systems, calculators, and digital signal processors (DSPs).

For example the Intel 8087, a floating-point coprocessor introduced in the early 1980s, utilized the CORDIC algorithm to perform efficient trigonometric and hyperbolic computations, such as sine, cosine, and arctangent, without relying on hardware multipliers. Similarly, during the Apollo Lunar Module missions, a precursor concept to CORDIC was employed in the Apollo Guidance Computer (AGC) to perform real-time navigation calculations. The AGC used iterative methods to determine angles and distances for lunar landings, efficiently converting Cartesian spacecraft coordinates to polar forms to ensure precise trajectory adjustments during descent.

The CORDIC algorithm can operate in two different modes: **rotation mode** and **vectoring mode**

- **Rotation mode:** rotates a vector by a specified angle, used for calculating trigonometric functions or vector transformations
- **Vectoring mode:** determines the magnitude and angle of a vector, useful for converting Cartesian to polar coordinates

In this context, this project will focus on developing the vectoring mode of the CORDIC algorithm to convert Cartesian coordinates into polar form.

2 Architecture

By default, the CORDIC algorithm converges only for input angles within the range $(-99.7^\circ, 99.7^\circ)$. To address this limitation and enable the algorithm to handle arbitrary input angles, we introduced an **initial correction step**. This step adjusts the input angle to bring it into the principal range of the algorithm. The adjustment ensures that the CORDIC algorithm works seamlessly for all input angles, not just those within the default convergence range.

$$x_0 = -y_{\text{input}} \cdot d_{\text{input}}$$

$$y_0 = x_{\text{input}} \cdot d_{\text{input}}$$

$$z_0 = -\frac{\pi}{2} \cdot d_{\text{input}}$$

Additionally, since the iterative process of the CORDIC algorithm introduces a scaling factor A_n , we normalize the final result by dividing ρ (the magnitude) by A_n .

2.1 Data Representation

To implement the CORDIC algorithm, we used fixed-point arithmetic for the input and intermediate values. Specifically:

- For x, y, ρ we used 16-bit fixed-point representation with 8 bits allocated for the fractional part.
- For z and θ we used a 16-bit fixed-point representation with 13 bits allocated for the fractional part. This decision was made because they always lie within the range $[-\pi, \pi]$, and the additional fractional bits ensure high angular precision.
- For the intermediate calculations a 24-bit representation was used to minimize truncation errors during the iterative process.
- All the inputs and the outputs are limited to 16 bits due to the I/O pin constraints of the Zybo board, which restricts the width of the data buses and necessitate uniform bit-width for inputs and outputs.

The number of iterations for the CORDIC algorithm was set to 16, as this provides a high level of precision while balancing computational efficiency. Beyond 16 iterations,

the precision gained decreases significantly.

2.2 Phase Precision and Error Analysis

Focusing on the phase, the intermediate values are represented in Q3.21 fixed-point format, offering a maximum absolute error ϵ_a of 2^{-21} . Over the course of 16 iterations, the maximum accumulated absolute sum of these values ϵ_M is

$$\epsilon_M = \epsilon_a * 16 = 2^{-21} * 2^4 = 2^{-17}$$

Since the final result is truncated to Q3.13, which involves discarding the least significant bits (LSBs), the accumulated error from the iterative sums becomes negligible. This ensures that the phase computation maintains high precision.

3 VHDL code

3.1 Cordic

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3 USE ieee.numeric_std.ALL;
4 ENTITY CORDIC IS
5
6     GENERIC (
7         N : POSITIVE := 20;
8         ITERATIONS : POSITIVE := 16;
9         ITER_BITS : POSITIVE := 4
10    );
11    PORT (
12        clk : IN STD_LOGIC;
13        rst : IN STD_LOGIC;
14        x : IN STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
15        y : IN STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
16        start : IN STD_LOGIC;
17        rho : OUT STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
18        theta : OUT STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
19        valid : OUT STD_LOGIC
20    );
21
22 END ENTITY;
23
24 ARCHITECTURE behavioral OF CORDIC IS
25
26     -- CONSTANT k : SIGNED(N - 1 DOWNTO 0) :=
27     --     to_signed(1304065748, N); -- 1/(Gain factor) multiplied by
28     --     2^N-1
29     CONSTANT k : SIGNED(N - 1 DOWNTO 0) :=
30         to_signed(INTEGER(0.6072529351031394 * (2 ** (N - 2))), N);
31         -- todo documentare meglio il N-2 (vivado si lamenta)
32         -- ((probabilmente per la dimensione massima degli integer))
33     CONSTANT HALF_PI : SIGNED(N - 1 DOWNTO 0) :=
34         to_signed(INTEGER(1.570796327 * (2 ** (N - 3))), N); --
35         -- todo documentare meglio il N-3
```

```

30  -- internal registers
31  SIGNAL x_t : SIGNED(N - 1 DOWNTO 0);
32  SIGNAL y_t : SIGNED(N - 1 DOWNTO 0);
33  SIGNAL z_t : SIGNED(N - 1 DOWNTO 0);
34
35  SIGNAL x_out : STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
36  SIGNAL z_out : STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
37
38  SIGNAL address : STD_LOGIC_VECTOR(ITER_BITS - 1 DOWNTO 0);
39  SIGNAL atan_out : STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
40
41  SIGNAL sign : STD_LOGIC;
42
43  -- atan table
44  COMPONENT ATAN_LUT IS
45    PORT (
46      address : IN STD_LOGIC_VECTOR(ITER_BITS - 1 DOWNTO 0);
47      lut_out : OUT STD_LOGIC_VECTOR(N - 1 DOWNTO 0)
48    );
49  END COMPONENT;
50
51  -- state type and registers
52  TYPE state_t IS (WAITING, FIX_STEP, COMPUTING, FINISHED);
53  SIGNAL current_state : state_t;
54
55  SIGNAL counter : UNSIGNED(ITER_BITS - 1 DOWNTO 0);
56
57 BEGIN
58  -----
59  -- INSTANTIATE ALL COMPONENTS
60  -----
61
62  -- output assignment
63  rho <= x_out;
64  theta <= z_out;
65
66  -- sign bit
67  sign <= '0' WHEN y_t > 0 ELSE
68    '1';
69
70  -- atan table
71  -- todo probably needs fix (next clock)
72  atan_lut_inst : ATAN_LUT
73  PORT MAP(
74    address => address,
75    lut_out => atan_out
76  );
77
78  -- atan table address
79  address <= STD_LOGIC_VECTOR(counter);
80

```

```

81  -- todo decidere se tenere o togliere gli assegnamenti
82  --      stupidi
83  -- todo forse z dovrebbe avere solo 2 bit interi e il resto
84  --      frazionari
85  -- aggiustare meglio spiegazione e codice per i 29 bit di
86  --      atan
87
88  -- control part
89  controllo : PROCESS (clk, rst)
90  BEGIN
91      IF (rising_edge(clk)) THEN
92
93          IF rst = '1' THEN
94              current_state <= WAITING;
95          ELSE
96
97              CASE current_state IS
98
99                  WHEN WAITING =>
100                      IF start = '1' THEN
101                          current_state <= FIX_STEP;
102                      ELSE
103                          current_state <= WAITING;
104                      END IF;
105
106                  WHEN FIX_STEP =>
107                      current_state <= COMPUTING;
108
109                  WHEN COMPUTING =>
110                      IF counter = ITERATIONS - 1 THEN
111                          current_state <= FINISHED;
112                      ELSE
113                          current_state <= COMPUTING;
114                      END IF;
115
116                  WHEN FINISHED =>
117                      current_state <= WAITING;
118                  WHEN OTHERS =>
119                      current_state <= WAITING;
120
121              END CASE;
122          END IF;
123      END IF;
124  END PROCESS;
125
126  -- operation part
127  operativa : PROCESS (clk, rst)
128  BEGIN
129      IF (rising_edge(clk)) THEN
130
131          IF rst = '1' THEN

```

```

129      valid <= '0';
130      -- Non utili
131      x_out <= (OTHERS => '0');
132      z_out <= (OTHERS => '0');
133      counter <= (OTHERS => '0');
134      x_t <= (OTHERS => '0');
135      y_t <= (OTHERS => '0');
136      z_t <= (OTHERS => '0');
137  ELSE
138
139      -- Default assignment
140      -- todo vedere se tenere o togliere
141      x_t <= (OTHERS => '-');
142      y_t <= (OTHERS => '-');
143      z_t <= (OTHERS => '-');
144      x_out <= (OTHERS => '-');
145      z_out <= (OTHERS => '-');
146      counter <= (OTHERS => '-');
147
148  CASE current_state IS
149      WHEN WAITING =>
150
151          x_t <= signed(x);
152          y_t <= signed(y);
153          z_t <= to_signed(0, N);
154          valid <= '1';
155          x_out <= x_out;
156          z_out <= z_out;
157
158      WHEN FIX_STEP =>
159          IF sign = '0' THEN
160              x_t <= y_t;
161              y_t <= - x_t;
162              z_t <= z_t + HALF_PI;
163          ELSE
164              x_t <= - y_t;
165              y_t <= x_t;
166              z_t <= z_t - HALF_PI;
167          END IF;
168
169          valid <= '0';
170          counter <= (OTHERS => '0');
171
172      WHEN COMPUTING =>
173          IF sign = '1' THEN
174              -- x_t <= x_t - y_t/(2 **
175              --      to_integer(counter));
176              x_t <= x_t - shift_right(y_t,
177              --      to_integer(counter));
178              -- y_t <= y_t + x_t/(2 **
179              --      to_integer(counter));

```

```

177          y_t <= y_t + shift_right(x_t,
178              ↳ to_integer(counter));
179          z_t <= z_t - signed(atan_out);
180      ELSE
181          -- x_t <= x_t + y_t/(2 **
182              ↳ to_integer(counter));
183          x_t <= x_t + shift_right(y_t,
184              ↳ to_integer(counter));
185          -- y_t <= y_t - x_t/(2 **
186              ↳ to_integer(counter));
187          y_t <= y_t - shift_right(x_t,
188              ↳ to_integer(counter));
189          z_t <= z_t + signed(atan_out);
190      END IF;
191
192      counter <= counter + 1;
193      valid <= '0';
194
195      WHEN FINISHED =>
196          -- x_out <=
197              STD_LOGIC_VECTOR(resize(shift_right(x_t
198                  ↳ * k , N-2),N));
199          x_out <= STD_LOGIC_VECTOR(resize(x_t * k/(2
200              ↳ ** (N - 2)), N));
201          -- x_out <= STD_LOGIC_VECTOR(x_t);
202          z_out <= STD_LOGIC_VECTOR(z_t);
203          valid <= '1';
204      END CASE;
205  END IF;
206
207  END IF;
208
209  END PROCESS;
210 END ARCHITECTURE;

```

Listing 3.1: CORDIC.vhd

```

1 library IEEE;
2 use IEEE.std_logic_1164.all;
3 use IEEE.numeric_std.all;
4
5 ENTITY ATAN_LUT IS
6     port (
7         address : in std_logic_vector(3 downto 0);
8         lut_out : out std_logic_vector(19 downto 0)
9     );
10    end entity;
11
12 architecture rtl of ATAN_LUT is
13
14     type LUT_t is array (natural range 0 to 15) of integer;
15

```

```
16  constant LUT: LUT_t := (
17    0 => 102943,
18    1 => 60771,
19    2 => 32109,
20    3 => 16299,
21    4 => 8181,
22    5 => 4094,
23    6 => 2047,
24    7 => 1023,
25    8 => 511,
26    9 => 255,
27    10 => 127,
28    11 => 63,
29    12 => 31,
30    13 => 15,
31    14 => 7,
32    15 => 3
33  );
34
35 begin
36
37 PROCESS (address)
38 BEGIN
39   lut_out <=
40     STD_LOGIC_VECTOR(to_signed(LUT(to_integer(unsigned(address))), 
41     20));
42 END PROCESS;
43
44 end architecture;
```

Listing 3.2: ATAN_LUT.vhd

4 Verification and testing

4.1 Testbench

```
1 LIBRARY IEEE;
2 USE IEEE.STD_LOGIC_1164.ALL;
3 USE IEEE.NUMERIC_STD.ALL;
4 USE ieee.math_real.ALL;
5
6 ENTITY CORDIC_TB IS
7     GENERIC (
8         N : POSITIVE := 20;
9         floating : INTEGER := 10
10    );
11 END CORDIC_TB;
12
13 ARCHITECTURE Behavioral OF CORDIC_TB IS
14     -- Component declaration for CORDIC
15
16     COMPONENT CORDIC
17         PORT (
18             clk : IN STD_LOGIC;
19             rst : IN STD_LOGIC;
20             x : IN STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
21             y : IN STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
22             start : IN STD_LOGIC;
23             rho : OUT STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
24             theta : OUT STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
25             valid : OUT STD_LOGIC
26        );
27     END COMPONENT;
28
29     -- Signals for CORDIC inputs and outputs
30
31     SIGNAL clk : STD_LOGIC := '0';
32     SIGNAL reset : STD_LOGIC := '0';
33     SIGNAL x : STD_LOGIC_VECTOR(N - 1 DOWNTO 0) := (OTHERS => '0');
34     SIGNAL y : STD_LOGIC_VECTOR(N - 1 DOWNTO 0) := (OTHERS => '0');
35     SIGNAL start : STD_LOGIC := '0';
36     SIGNAL rho : STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
```

```

37   SIGNAL theta : STD_LOGIC_VECTOR(N - 1 DOWNTO 0);
38   SIGNAL valid : STD_LOGIC := '0';
39
40   SIGNAL run_simulation : STD_LOGIC := '1';
41
42   -- Clock period definition
43   CONSTANT T_clk : TIME := 10 ns;
44
45   -- Coordinate type
46   TYPE Coordinate IS RECORD
47     x : real;
48     y : real;
49   END RECORD;
50   CONSTANT n_coordinates : NATURAL := 6;
51
52   TYPE CoordinateArray IS ARRAY (0 TO n_coordinates - 1) OF
53     Coordinate;
54
55   -- Array of coordinates to test
56   CONSTANT Coordinates : CoordinateArray := (
57     (1.0, 0.0),
58     (10.0, 10.0),
59     (0.1, 3.0),
60     (-0.1, -4.0),
61     (-1.0, 1.0),
62     (-1.0, 0.0)
63   );
64
65 BEGIN
66   -- Instantiate the CORDIC component
67   cordic_inst : CORDIC
68   PORT MAP(
69     clk => clk,
70     rst => reset,
71     x => x,
72     y => y,
73     start => start,
74     rho => rho,
75     theta => theta,
76     valid => valid
77   );
78
79   -- todo fix behavior if cordic is not ready / does not work
80
81   clk <= (NOT(clk) AND run_simulation) AFTER T_clk / 2;
82   -- Stimulus process
83   STIMULI : PROCESS
84     VARIABLE i : INTEGER := 0;
85   BEGIN
86     reset <= '1';

```

```

87      start <= '0';
88      WAIT FOR 2 * T_clk;
89
90      reset <= '0';
91
92      FOR i IN 0 TO n_coordinates - 1 LOOP
93
94          IF valid = '0' THEN
95              WAIT UNTIL valid = '1';
96          END IF;
97
98          x <=
99              STD_LOGIC_VECTOR(to_signed(INTEGER(Coordinates(i).x
100             * 2.0 ** floating), N));
101         y <=
102             STD_LOGIC_VECTOR(to_signed(INTEGER(Coordinates(i).y
103             * 2.0 ** floating), N));
104         start <= '1';
105
106         WAIT FOR 5 * T_clk;
107
108         start <= '0';
109
110         IF valid = '0' THEN
111             WAIT UNTIL valid = '1';
112         END IF;
113
114         wait for 10 * T_clk;
115
116     END LOOP;
117
118     run_simulation <= '0';
119
120     WAIT;
121 END PROCESS;
122 END ARCHITECTURE;

```

Listing 4.1: CORDIC_tb.vhd

4.2 Verification

4.3 Error verification

The implementation of the CORDIC algorithm in vectoring mode for Cartesian-to-polar conversion demonstrates exceptional accuracy in both the module (ρ) and phase (θ) outputs. Using a fixed-point representation of $Q8.8$ for ρ and $Q3.13$ for θ , the errors were summarized as follows:

Module Error: Max = 0.003938 units, Mean = 0.001889 units

Phase Error: Max = 0.000153 rad, Mean = 0.000061 rad

The test was performed on 512×512 input points uniformly distributed within a circle of radius $\frac{127}{A_n} \approx 77.1211$. This range ensures a comprehensive evaluation of the algorithm over a high range of valid inputs while maintaining consistency with the precision of the fixed-point formats used. The fixed-point representation employed provides a precision of 2^{-8} for $Q8.8$ (module) and 2^{-13} for $Q3.13$ (phase).

Module Error: $\log_2(\text{Max error}) \approx -7.988$

Phase Error: $\log_2(\text{Max error}) \approx -12.674$

The observed errors are well within these precision limits, with all measured deltas smaller than the respective numerical precision of the formats. Any discrepancies between the input and output values are solely due to the conversion of these fixed-point representations into real numbers for plotting and analysis.

The 3D plots of module and phase errors visually confirm the bounded and negligible nature of the errors across all tested input combinations. Assuming no error on the input, this analysis validates that the algorithm introduces no error in the output, demonstrating the precision and robustness of CORDIC algorithm thanks to the 24 bits internal logic.

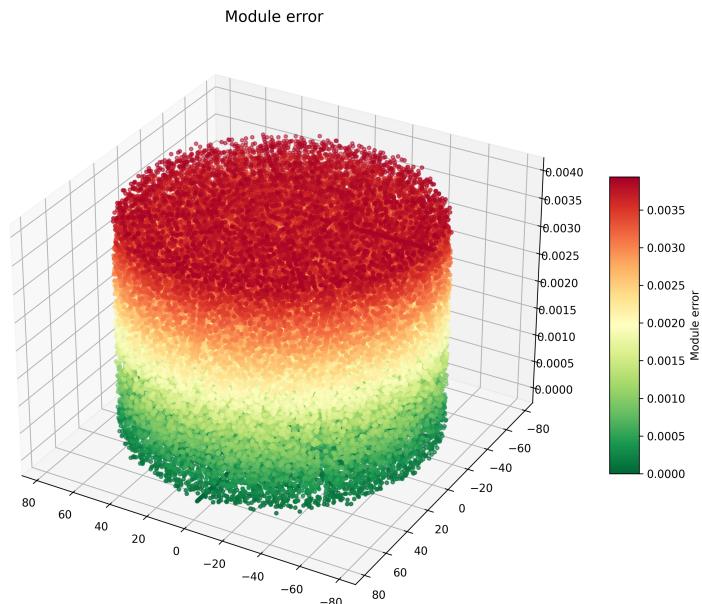


Figure 4.1: 3D plot of module error (ρ).

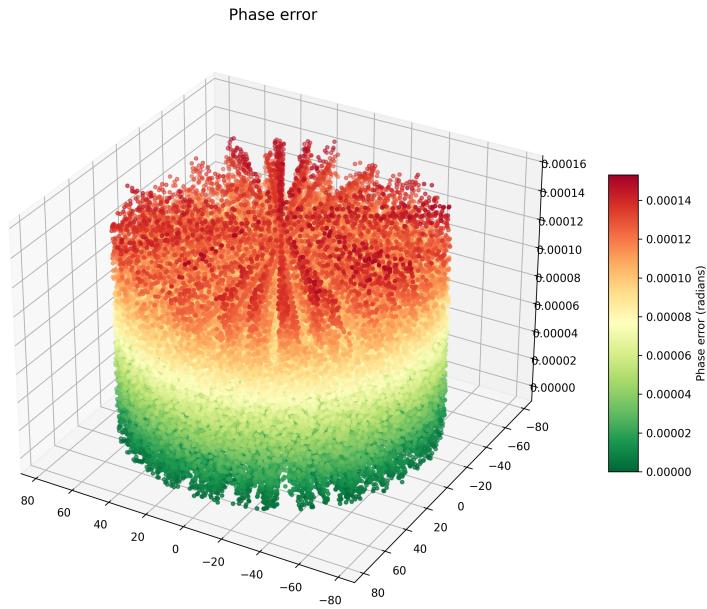


Figure 4.2: 3D plot of phase error (θ).

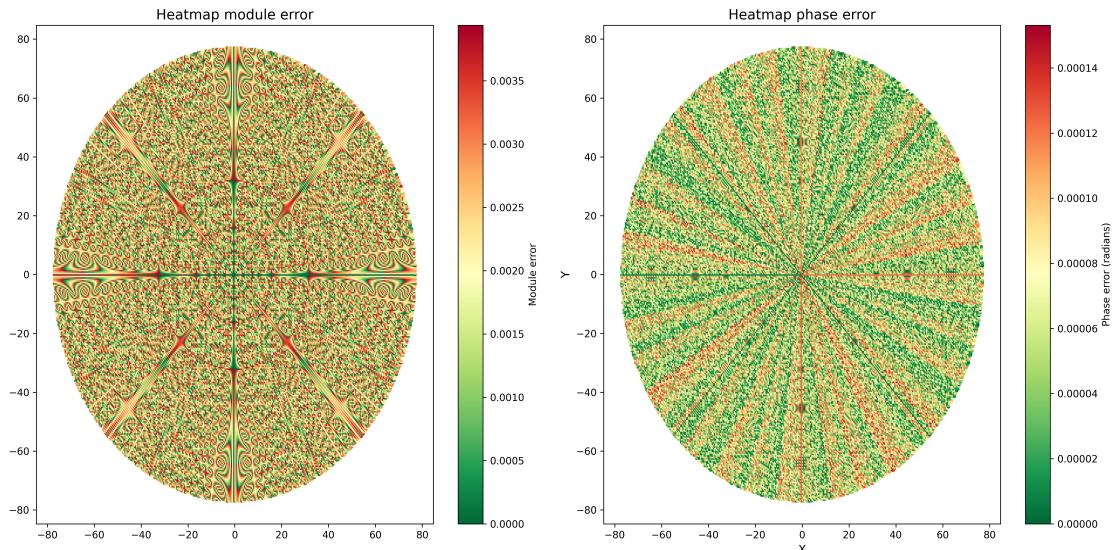


Figure 4.3: Heatmap for phase and module errors.

5 Synthesis and Implementation

After completing the verification phase, the circuit design was synthesized and implemented using the Vivado Tool, specifically targeting the Zybo Zynq-7010 development board.

5.1 Vivado Design flow

For the implementation of the CORDIC algorithm in vectoring mode for Cartesian-to-Polar conversion, the Vivado design flow was employed using Xilinx/AMD Vivado software. This process involved RTL Elaboration, Synthesis, and Implementation on the target FPGA, along with the application of design constraints and the extraction of power and timing reports. To ensure accurate and reliable timing analysis, all combinational logic paths were structured to follow a Register-Logic-Register configuration.

5.2 RTL

Vivado produced a logic network made of:

1. 155 cells (e.g. multiplexers, DFFs, adders)
2. 68 I/O ports ($16_x + 16_y + 16_\rho + 16_\theta + 1_{clk} + 1_{rst} + 1_{start} + 1_{valid}$)
3. 982 nets (for connecting all the components)

5.3 RTL Elaboration

[[Trenitalia: Or maybe just say that it's all loops even though it looks linear](#)] The RTL Analysis generated the following Elaborated Design consistent with the expected structure of the system and the block diagram:

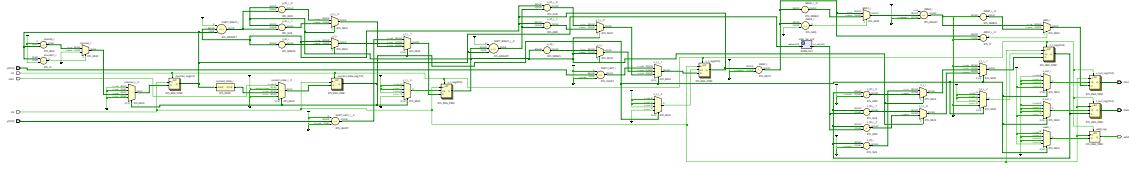


Figure 5.1: Elaborated RTL design.

5.4 Synthesis and Implementation

The Synthesis runs successfully without any errors, but a warning is reported regarding I/O constraints. The Timing Constraints are verified against a 20 ns clock period (50 MHz frequency), meeting the desired specifications. The Implementation also completes successfully; however, a warning (UCIO #1) is raised, indicating that all 68 logical ports lack user-assigned specific location constraints (LOC). This warning highlights potential risks such as I/O contention, board power or connectivity issues, performance degradation, signal integrity problems, or, in extreme cases, damage to the device or connected components. However, the assignment of specific pin locations was outside the scope of this project and was therefore not addressed.

6 Vivado results

6.1 Critical Path

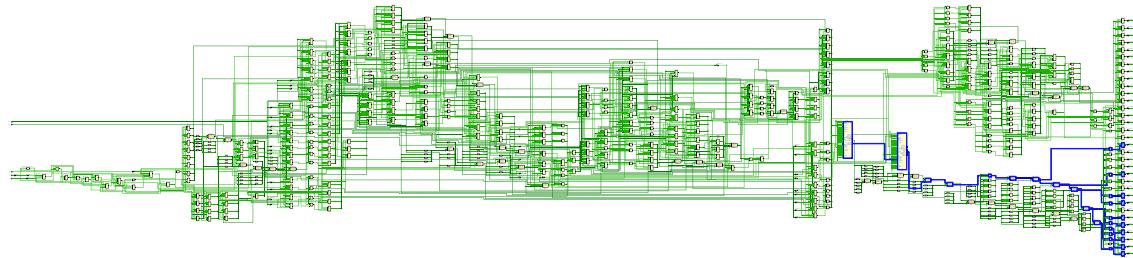


Figure 6.1: Figure showing the elaborated RTL design with the main critical paths for set-up-time-violation found in synthesis step highlighted in blue.

Name	Slack	Levels	Routes	From	To	Total Delay
Path 1	9.30	12	6	ARG2/CLK	x_out_reg[15]/D	10.55
Path 2	9.33	11	6	ARG2/CLK	x_out_reg[12]/D	10.52
Path 3	9.45	10	6	ARG2/CLK	x_out_reg[8]/D	10.40
Path 4	9.51	12	6	ARG2/CLK	x_out_reg[14]/D	10.33
Path 5	9.56	9	6	ARG2/CLK	x_out_reg[4]/D	10.28
Path 6	9.57	11	6	ARG2/CLK	x_out_reg[11]/D	10.28
Path 7	9.62	12	6	ARG2/CLK	x_out_reg[13]/D	10.23
Path 8	9.62	11	6	ARG2/CLK	x_out_reg[10]/D	10.23
Path 9	9.67	8	6	ARG2/CLK	x_out_reg[0]/D	10.18
Path 10	9.69	10	6	ARG2/CLK	x_out_reg[7]/D	10.16

Table 6.1: Table showing data of the main critical paths found in synthesis step

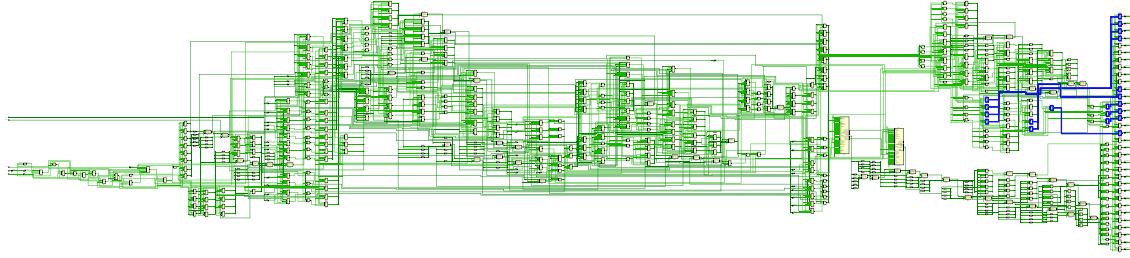


Figure 6.2: Figure showing the elaborated RTL design with the main critical paths for hold-time-violation found in synthesis step highlighted in blue.

Name	Slack	Levels	Routes	From	To	Total Delay
Path 11	0.16	0	1	z_t_reg[23]/C	z_out_reg[15]/D	0.29
Path 12	0.16	0	1	z_t_reg[8]/C	z_out_reg[0]/D	0.29
Path 13	0.16	0	1	z_t_reg[18]/C	z_out_reg[10]/D	0.29
Path 14	0.16	0	1	z_t_reg[19]/C	z_out_reg[11]/D	0.29
Path 15	0.16	0	1	z_t_reg[20]/C	z_out_reg[12]/D	0.29
Path 16	0.16	0	1	z_t_reg[21]/C	z_out_reg[13]/D	0.29
Path 17	0.16	0	1	z_t_reg[22]/C	z_out_reg[14]/D	0.29
Path 18	0.16	0	1	z_t_reg[9]/C	z_out_reg[1]/D	0.29
Path 19	0.16	0	1	z_t_reg[10]/C	z_out_reg[2]/D	0.29
Path 20	0.16	0	1	z_t_reg[11]/C	z_out_reg[3]/D	0.29

Table 6.2: Table showing the characteristics regarding critical paths for hold-time-violation found in synthesis step.

Name	Slack	Levels	Routes	From	To	Total Delay
Path 1	8.90	10	3	ARG2/CLK	x_out_reg[9]/D	10.99
Path 2	8.93	10	3	ARG2/CLK	x_out_reg[12]/D	10.96
Path 3	8.99	11	3	ARG2/CLK	x_out_reg[13]/D	10.86
Path 4	9.08	11	3	ARG2/CLK	x_out_reg[15]/D	10.82
Path 5	9.10	9	3	ARG2/CLK	x_out_reg[8]/D	10.84
Path 6	9.10	9	3	ARG2/CLK	x_out_reg[6]/D	10.84
Path 7	9.14	10	3	ARG2/CLK	x_out_reg[10]/D	10.71
Path 8	9.15	9	3	ARG2/CLK	x_out_reg[7]/D	10.74
Path 9	9.18	11	3	ARG2/CLK	x_out_reg[14]/D	10.72
Path 10	9.22	10	3	ARG2/CLK	x_out_reg[11]/D	10.63

Table 6.3: Table showing the main critical paths for the setup-time-violation during the implementation step.

[Trenitalia: need to comment a bit these results, for example the paths for setup-time-violation correspond exactly between synthesis and implementation, whereas

Name	Slack	Levels	Routes	From	To	Total Delay
Path 11	0.17	1	1	counter_reg[0]/C	counter_reg[2]/D	0.31
Path 12	0.17	1	1	counter_reg[0]/C	counter_reg[1]/D	0.31
Path 13	0.18	1	1	counter_reg[0]/C	counter_reg[3]/D	0.31
Path 14	0.22	0	1	z_t_reg[19]/C	z_out_reg[11]/D	0.25
Path 15	0.22	0	1	z_t_reg[23]/C	z_out_reg[15]/D	0.27
Path 16	0.23	0	1	z_t_reg[8]/C	z_out_reg[0]/D	0.26
Path 17	0.25	0	1	z_t_reg[12]/C	z_out_reg[4]/D	0.35
Path 18	0.25	0	1	z_t_reg[22]/C	z_out_reg[14]/D	0.33
Path 19	0.26	1	1	FSM_reg[0]/C	FSM_reg[0]/D	0.35
Path 20	0.27	0	1	z_t_reg[18]/C	z_out_reg[10]/D	0.37

Table 6.4: Table showing the main critical paths for hold-time-violation found in the implementation step.

hold-time-violation are different, these means that place and route had a significant impact in determining these values]

[**Trenitalia:** The DRC actually gives us 6 warnings, it tells us to pipeline the multiplier block in order to enhance performances and power consumption. But we adopted a CORDIC approach with loopbacks, that converges in 16 steps, 17 in the worst case when we have the fix step, inserting a register in between would cause higher delays in order to get the result.]

6.2 Utilization Report

Resource	Utilization (%)	Description
Slice LUTs	2.05%	Look-Up Tables used as logic
Slice Registers	0.32%	Registers used in the design
Slice	2.30%	Total slices utilized
LUT as Logic	2.05%	LUTs specifically used as logic
DSPs	2.50%	Digital Signal Processing blocks
Bonded IOB	68.00%	Bonded Input/Output Blocks
BUFGCTRL	3.13%	Global Clock Buffers

Table 6.5: Resource utilization for the CORDIC design (only non-zero values shown)

6.3 Power Report

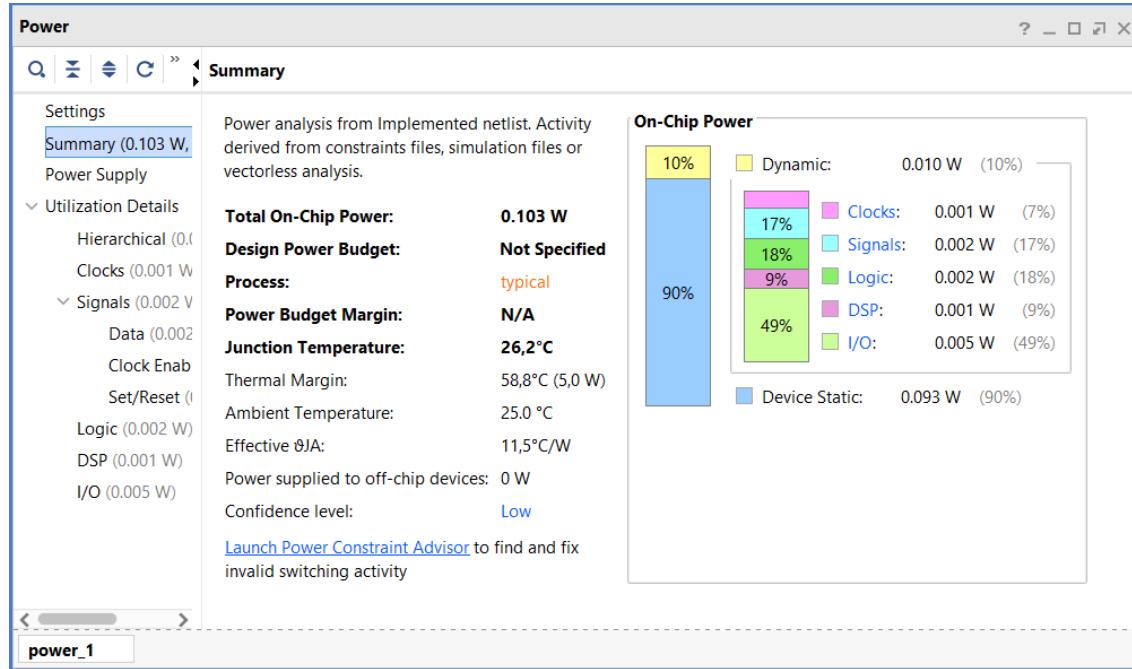


Figure 6.3: Vivado Power Report after implementation.

7 Final considerations