Final Project – Progress Report 1

CS 385 – Computer Architecture

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**Tasks:**

Daniel Kostecki:

* Gate level conversions in the regfile (4x1 mux)
* Report and diagrams

Thi Nguyen:

* 16-bit implementation of multiplexors using 4x1 mux

Sonia Leonato Soiras:

* ALU conversions to 16-bit
* Gate level conversions in the ALU (4x1 mux)
* Gate level conversions in the ALU (2x1 mux)
* Logic diagram, truth table

**Descriptions:**

The instruction set architecture currently in place for our 16-bit machine allows for R-type instructions as well as the addi instruction. The list of R-type instructions that are currently supported and their respective opcode are and(0000), sub(0001), and(0010), or(0011), and slt(0111). The only I-format instruction that we have currently implemented is addi(0100).

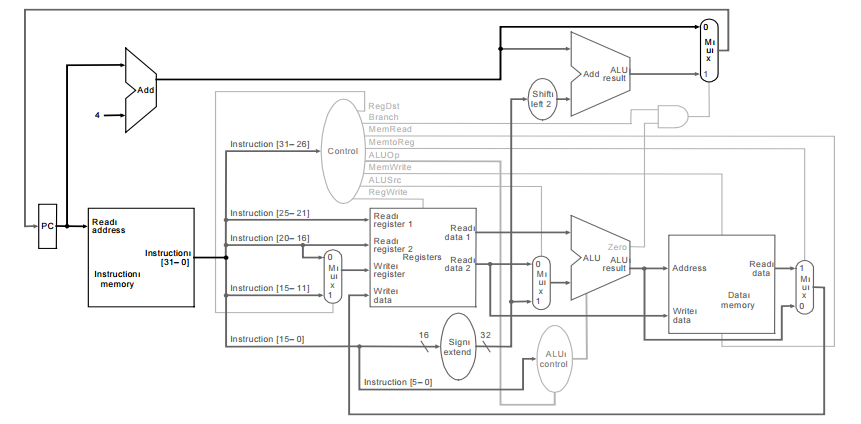
R-type format: I-type format:

|  |  |  |  |
| --- | --- | --- | --- |
| Op | Rs | Rt | Address/value |
| 4 | 2 | 2 | 8 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Op | Rs | Rt | Rd | Unused |
| 4 | 2 | 2 | 2 | 6 |

**Logic Diagrams/Truth Tables:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instr** | **RegDst** | **ALUSrc** | **MemReg** | **RegWrite** | **MemRead** | **MemWrite** | **Branch** | **ALUOp1** | **ALUOp2** |
| **Rtype** | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| **addi** | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

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**Verilog Source Code:**

**Test Results:**