深圳维盛半导体科技有限公司

VS11K16A IC手册参考

VS 32-Bit Cortex-M0 Micro-Controller

1 PRODUCT OVERVIEW

1.1 FEATURES

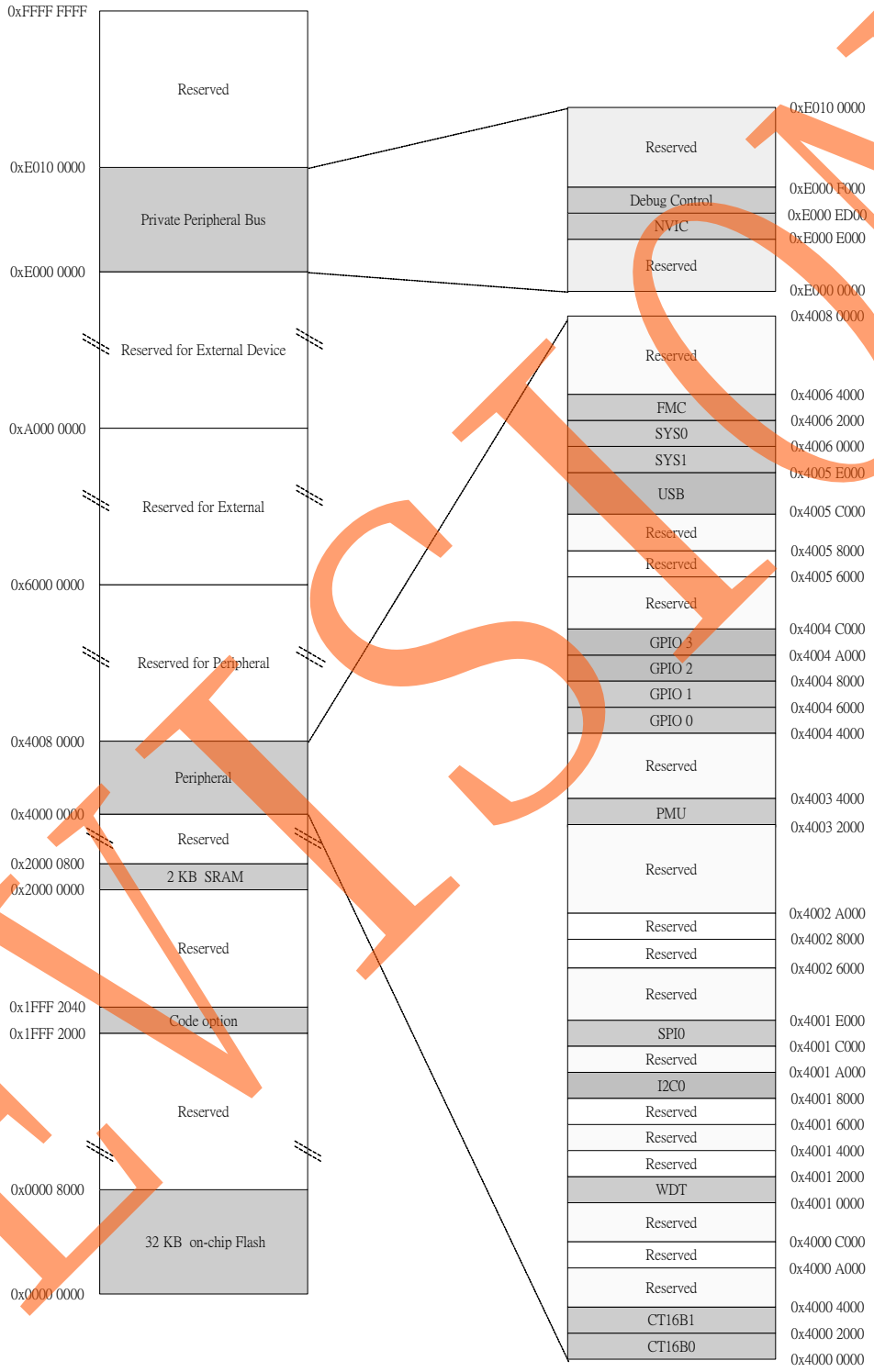
- **Memory configuration**
  Flash ROM size: 32KB.
  User RAM: 2KB.
  USB FIFO RAM: 256 bytes.
- **Operation Frequency up to 48MHz**
- **Interrupt sources**
  ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
- **I/O pin configuration**
  Bi-directional: P0, P1, P2, P3.
  Wakeup: P0, P1, P2, P3 level change.
  Pull-up resisters: P0, P1, P2, P3.
  20mA Sink/8mA Drive: P0, P1, P2, P3.
- **Programmable WatchDog Timer (WDT)**
  Programmable watchdog frequency with watchdog clock source and divider.
- **System tick timer**
  24-bit timer.
  The system tick timer clock is fixed to the frequency of the system clock.
  The SysTick timer is intended to generate a fixed 10-ms interrupt.
- **LVD with separate thresholds**
  Reset: 2.4V/3.3V for VDD.
- **Full Speed USB 2.0**
  3.3v regulator output for D+ internal 1.5k pull-up resistor.
  Supports one Full speed USB device address.
  Supports PS/2 mode.
  One control EP and 4 configurable INT/BULK Endpoints.
  EP0 supports 64-byte FIFO depth.
  Programmable EP1~EP4 FIFO depth.
  Total 5 endpoints share 256-byte USB RAM.
- **Working voltage 2.5V ~ 5.5V**
- **Timer**
  One 16-bit general purpose timer CT16B0 with CAP0.
  One 16-bit general purpose timer CT16B1 with 23-ch PWM.
- **Interfaces: I2C & SPI**
  - One I2C controller supporting I2C-bus specification.
  - One SPI controller supporting SPI protocol.
- **System clocks**
  Internal high clock: RC type 48MHz.
  Internal low clock: RC type 32KHz.
- Serial Wire Debug (SWD)
- **Operating modes**
  Normal, Sleep, and Deep-sleep.
- **Fcpu (Instruction cycle)**
  $F_{CPU} = F_{HCLK} = F_{SYSCLK}/1, F_{SYSCLK}/2, F_{SYSCLK}/4, \ldots, F_{SYSCLK}/128$.
- **In-System-Progamming (ISP) supported**
- **3.3V Regulator output**
  Driving current 60mA
  Power for USB D+ internal pull-up resistor.
  Can be IO power for P1.0~P1.5. (3.3V IOs)
  Can be power source for peripheral 3.3V devices.
- **Package (Chip form support)**
  LQFP48 pin

1.2 PIN ASSIGNMENT

(LQFP 48 pins)

2 CENTRAL PROCESSOR UNIT (CPU)

2.1 MEMORY MAP



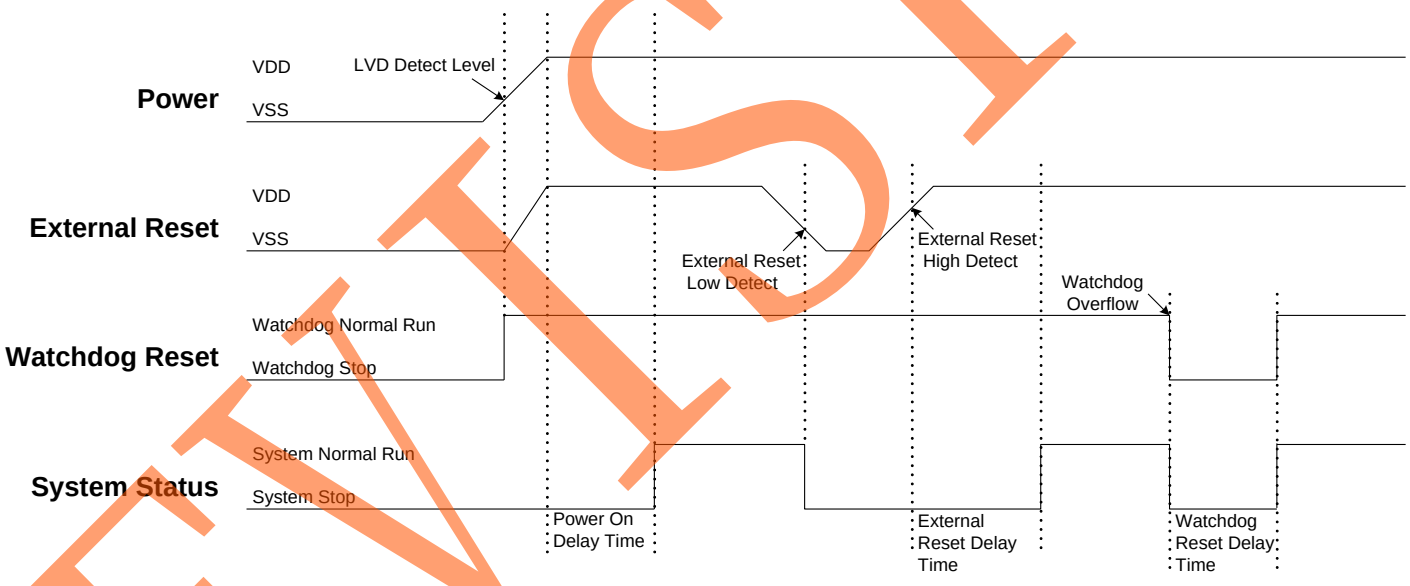
3 SYSTEM CONTROL

3.1 RESET

A system reset is generated when one of the following events occurs:
1. A low level on the RST pin (external reset).
2. Power-on reset (POR reset)
3. LVD reset
4. Watchdog Timer reset (WDT reset)
5. Software reset (SW reset)

The reset source can be identified by checking the reset flags in System Reset Status register (SYS0_RSTST). These sources act on the RST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x00000004 in the memory map. For more details, refer to Interrupt and Exception Vectors.

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care of the power on reset time for the master terminal requirement. The reset timing diagram is as following.



3.1.1 POWER-ON RESET (POR)

The power on reset depends on LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following:

- **Power-up:** System detects the power voltage up and waits for power stable.
- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from Boot loader.

4 SPI

4.1 OVERVIEW

The SPI controller can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

4.2 FEATURES

- Compatible with Motorola SPI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 25 Mbps (master) or 6 Mbps. (slave)
- Data transfer format is from MSB or LSB controlled by register.
- The start phase of data sampling location selection is 1st-phase or 2nd-phase controlled register.

4.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
SCKn	O	SPI Serial clock (Master)	
	I	SPI Serial clock (Slave)	Depends on GPIOn_CFG
SELn	O	SPI Slave Select/SSI Frame Sync (Master)	
	I	SPI Slave Select (Slave)	Depends on GPIOn_CFG
MISOn	I	Master In Slave Out (Master)	Depends on GPIOn_CFG
	O	Master In Slave Out (Slave)	
MOSIn	O	Master Out Slave In (Master)	
	I	Master Out Slave In (Slave)	Depends on GPIOn_CFG

5 I2C

5.1 OVERVIEW

The I2C bus is bidirectional for inter-IC control using only two wires: Serial Clock Line (SCL) and Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I2C is a multi-master bus and can be controlled by more than one bus master connected to it. It is also SMBus 2.0 compatible.

Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I2C bus:

- Data transfer from a master transmitter to a slave receiver.
  The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver.
  The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since a Repeated START condition is also the beginning of the next serial transfer, the I2C bus will not be released.

The I2C interface is byte oriented and has four operating modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode

5.2 FEATURES

The I2C interface complies with the entire I2C specification, supporting the ability to turn power off to the ARM Cortex-M0 without interfering with other devices on the same I2C-bus.

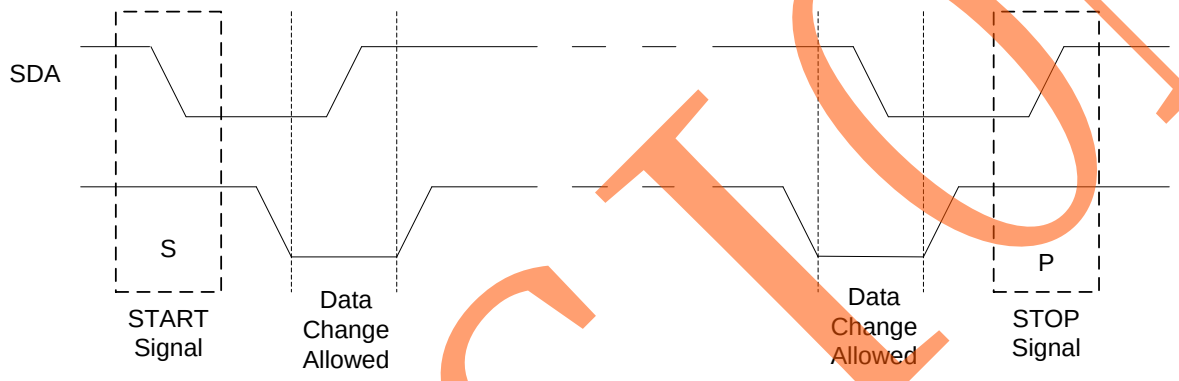
- Standard I2C-compliant bus interfaces may be configured as Master or Slave.
- I2C Master features:
  - Clock generation
  - Start and Stop generation
- I2C Slave features:
  - Programmable I2C Address detection
  - Optional recognition of up to four distinct slave addresses
  - Stop bit detection
- Supports different communication speeds:
  - Standard Speed (up to 100KHz)
  - Fast Speed (up to 400 KHz)
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I2C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.

- Monitor mode allows observing all I2C-bus traffic, regardless of slave address.
- I2C-bus can be used for test and diagnostic purposes.
- Generation and detection of 7-bit/10-bit addressing and General Call.

5.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
SCLn	I/O	I2C Serial clock	Output with Open-drain Input depends on GPIOn_CFG
SDAn	I/O	I2C Serial data	Output with Open-drain Input depends on GPIOn_CFG

9.4 WAVE CHARACTERISTICS



6 USB FS DEVICE INTERFACE

6.1 OVERVIEW

The USB is the answer to connectivity for the PC architecture. A fast, bi-directional interrupt pipe, low-cost, dynamically attachable serial interface is consistent with the requirements of the PC platform of today and tomorrow. The SONIX USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, keyboard, joystick, and game pad.

USB Specification Compliance

— Conforms to USB specifications, Version 2.0.

— Supports 1 Full-speed USB device address.

— Supports 1 control endpoint and 4 configurable endpoints for isochronous/interrupt/bulk transfer.

— Integrated USB transceiver.

— 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.

6.2 FEATURES

- Conforms to USB specifications, Version 2.0.
- Supports 1 Full-speed USB device address.
- Supports 1 control endpoint with maximum packet size 8 bytes, 16 bytes, 32 bytes, or 64 bytes.
- Supports 4 endpoints configurable for isochronous/interrupt/bulk transfer.
- Supports USB SRAM size 256 bytes shared by all 5 endpoints.
- Flexible data FIFO offset setting for endpoints except endpoint 0.
- 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.
- Integrated USB transceiver.

6.3 PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
DP	I/O	USB differential signal D+	N/A
DN	I/O	USB differential signal D-	N/A

7 FLASH

7.1 OVERVIEW

SONiX 32-bit MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the SONiX 32-bit MCU programming interface or by application code for maximum flexibility. SONiX 32-bit MCU provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory.

- The MCU is stalled during Flash program and erase operations, although peripherals (Timers, WDT, I/O, PWM, etc.) remain active.
- Watchdog timer should be cleared if enabled before the Flash write or erase operation.
- The erase operation sets all the bits in the Flash page to logic 1.
- HW will hold system clock and automatically move out data from RAM and do programming, after programming finished, HW will release system clock and let MCU execute the next instruction.

7.2 EMBEDDED FLASH MEMORY

The Flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants, and is located at a specific base address in the memory map of chip.

The high-performance Flash memory module in chip has the following key features:

- Memory organization: the Flash memory is organized as a User ROM.

User ROM	Up to 30K × 8 bits divided into 256 pages of 64 Bytes

The Flash interface implements instruction access and data access based on the AHB protocol. It implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range.

7.3 FEATURES

- Read interface (32-bit)
- Flash Program / Erase operation
- Code Option includes Code Security (CS)

Write operations to the main memory block and the code options are managed by an embedded Flash Memory Controller (FMC). The high voltage needed for Program/Erase operations is internally generated. The main Flash memory can be read/write protected against different levels of Code Security (CS).

During a write operation to the Flash memory, any attempt to read the Flash memory will stall the bus. The read operation will proceed correctly once the write operation has completed. This means that code or data fetches cannot be made while a write/erase operation is ongoing.

For write and erase operations on the Flash memory, the IHRC will be turn ON by FMC. The Flash memory can be programmed and erased using ICP and ISP.

7.4 ORGANIZATION

Block	Name	Base Address	Size (Byte)
User ROM	Page 0	0x00000000 ~ 0x0000003F	64

30KB	Page 1	0x00000040 ~ 0x0000007F	64
	. . .	. . .	
	Page 478	0x00007780 ~ 0x000077BF	64
	Page 479	0x000077C0 ~ 0x000077FF	64

7.5 READ

The embedded Flash module can be addressed directly, as a common memory space. Any data read operation accesses the content of the Flash module through dedicated read senses and provides the requested data.

The read interface consists of a read controller on one side to access the Flash memory, and an AHB interface on the other side to interface with the CPU. The main task of the read interface is to generate the control signals to read from the Flash memory as required by the CPU.

7.6 PROGRAM/ERASE

The Flash memory erase operation can be performed at page level.

To ensure that there is no over-programming, the Flash programming and erase controller blocks are clocked by IHRC.

7.7 EMBEDDED BOOT LOADER

The embedded boot loader is used to reprogram the Flash memory using the USB interface.

8 ELECTRICAL CHARACTERISTIC

8.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... -40°C ~ + 85°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

8.2 ELECTRICAL CHARACTERISTIC

All of voltages refer to Vss, Typical Vdd = 5.0V, Fosc = 12MHz, ambient temperature is 25℃ unless otherwise note.							
PARAMETER	**SYM.**	**DESCRIPTION**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Operating Voltage	Vdd1	Supply voltage for core and external rail		2.5	5.0	5.5	V
	Vdd2	USB mode		3.1	5.0	5.25	V
VDD rise rate	V_{POR}	VDD rise rate to ensure internal power-on reset		0.05	-	-	V/ms
Power Consumption							
Supply Current	Idd1	Normal mode	System clock = 48MHz [1][2][3]	-	12	-	mA
	Idd2	Sleep Mode	System clock = 32KHz [1][3][4]	-	160	230	uA
	Idd3	Deep-sleep Mode	Vdd=5V [1][5]	-	5	16	uA
Port Pins, RESET pin							
High-level input voltage	V_{IH}			0.7Vdd	-	Vdd	V
Low-level input voltage	V_{IL}			Vss	-	0.3Vdd	V
Input voltage	V_i			0	-	Vdd	V
Output voltage	V_o			0	-	Vdd	V
I/O port pull-up resistor	R_{PU}	Vin = Vss , Vdd = 5.0V		30	50	70	KΩ
I/O port pull-down resistor	R_{PD}	Vin = 5.0V		30	50	70	KΩ
I/O High-level output source current	I_{OH}	V_{OP} = Vdd – 0.5V;		6	10	-	mA
I/O Low-level output sink current	I_{OL}	V_{OP} = Vss + 0.5V		12	20	-	mA
FLASH							
Endurance time	T_{EN}	Erase + Program		20K	100K	-	Cycle
Page erase time	T_{ME}	All User ROM memory.		-	5	-	ms
Page Programming time	T_{PG}	1 -Page (64 bytes).		-	5	-	ms
MISC							
Low Voltage Detector	LVD	Interrupt/Reset	LVD24	2.2	2.4	2.6	V
			LVD33	3.1	3.3	3.5	V
3.3V Regulator Output voltage	Vreg33	Vcc ≧ 3.60V, I_{VREG33} >= 60 mA		3.03	-	3.27	V
IHRC Freq.	F_{IHRC}	*T=25℃*, Vdd=5V		11.97	12	12.03	MHz
		T=-40℃~85℃, Vdd=5V		11.64	12	12.36	MHz
	F_{IHRC2}	*T=-40℃~85℃*, Vdd=5V, USB function ON		11.97	12	12.03	MHz

*** These parameters are for design reference, not tested.**

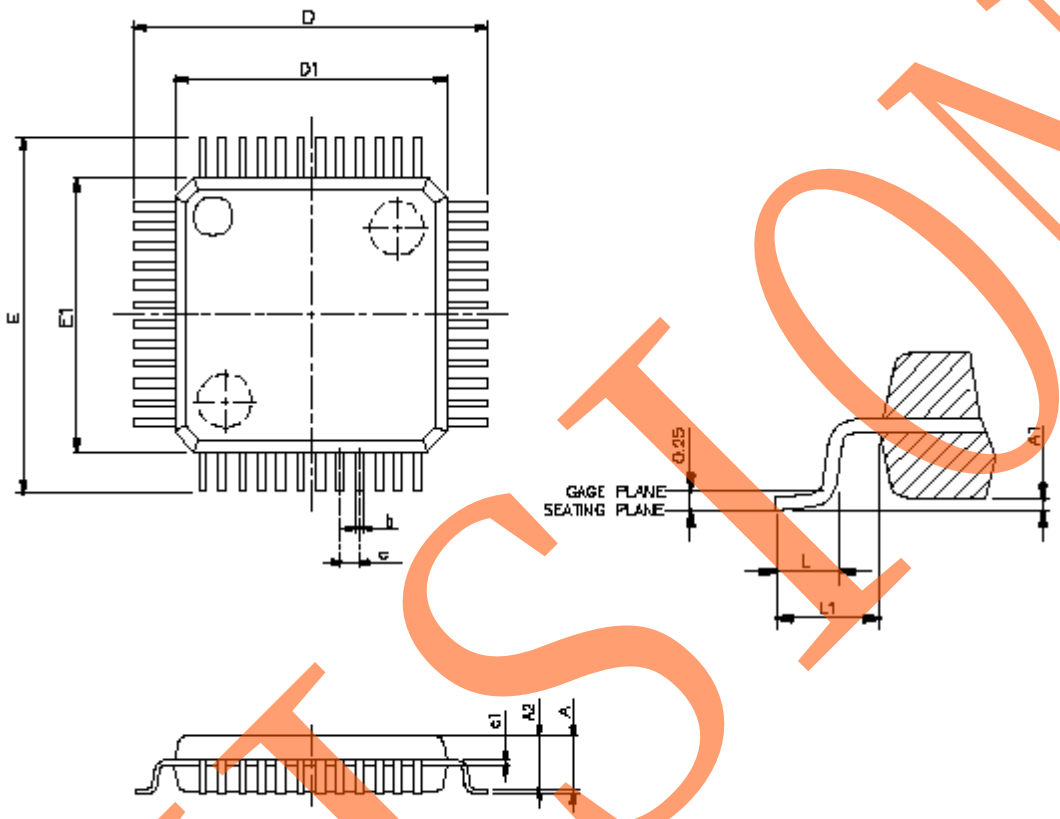
[1] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled and VDD=5V.
[2] IHRC and ILRC are enabled.
[3] LVD and GPIO peripherals are Enabled.
[4] IHRC is disabled, ILRC is enabled. [5] All oscillators and analog blocks are turned off.

9 FLASH ROM PROGRAMMING PIN

Programming Information of VS11K16A Series													
Chip Name		VS11K16A											
MP PRO Writer Connector		Flash IC / JP3 Pin Assignment											
Number	Name	Number	Pin	Number	Pin	Number	Pin	Number	Pin	Number	Pin	Number	Pin
1	VDD	*44*	VDD										
2	GND	*48*	VSS										
3	CLK	*5*	P0.1										
4	CE												
5	PGM	*26*	P3.6										
6	OE	*27*	P3.7										
7	D1												
8	D0												
9	D3												
10	D2												
11	D5												
12	D4												
13	D7												
14	D6												
15	VDD												
16	-												
17	HLS												
18	RST												
19	-												
20	ALSB/PDB	*6*	P0.2										

10 PACKAGE INFORMATION

10.1 LQFP 48 PIN



SYMBOLS	MIN	NOR	MAX
	(mm)		
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	-	1.45
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.5 BSC		
B	0.17	-	0.27
L	0.45	-	0.75
L1	1 REF		