PRODUCT OVERVIEW

FEATURES

- **Memory configuration**
  Up to 64KB on-chip Flash programming memory.
  Up to 8KB SRAM.
  4KB Boot ROM

- **Operation Frequency up to 50MHz**

- **Interrupt sources**
  ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).

- **I/O pin configuration**
  Up to 64 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  GPIO pins can be used as edge and level sensitive interrupt sources.
  High-current source driver (20 mA)

- **Programmable WatchDog Timer (WDT)**
  Programmable watchdog frequency with watchdog clock source and divider.

- **System tick timer**
  24-bit timer.
  The system tick timer clock is fixed to the frequency of the system clock.
  The SysTick timer is intended to generate a fixed 10-ms interrupt.

- **Hardware divider**

- **Real-Time Clock (RTC)**

- **LVD with separate thresholds**
  Reset: 1.65V for V_{CORE}
  Reset: 1.8V/2.0V/2.4V/2.7V/3.0V/3.6V for VDD
  Interrupt: 1.8V/2.0V/2.4V/2.7V/3.0V/3.6V for VDD

- **Fcpu (Instruction cycle)**
  $F_{CPU} = F_{HCLK} = F_{SYSCLK}/1$, $F_{SYSCLK}/2$, $F_{SYSCLK}/4$, …, $F_{SYSCLK}/512$.

- **Operating modes**
  Normal, Sleep, Deep-sleep, and Deep power-down

- **Serial Wire Debug (SWD)**

- **Timers**
  Three 16-bit and three 32-bit general purpose timers with a total of 6 capture inputs and 21 PWMs.

- **Working voltage 1.8V ~ 5.5V**

- **ADC**
  14-channel 12-bit SAR ADC
  Temperature sensor inside

- **Interface**
  -Two I2C controllers supporting I2C-bus specification with multiple address recognition and monitor mode.
  - USART controller with fractional baud rate generation, and EIA-485 support.
  - UART controller with fractional baud rate generation.
  -Two SPI controllers with SSP features and multi-protocol capabilities.
  -I2S Function with mono and stereo audio data supported, MSB justified data format supported, and can operate as either master or slave.

- **System clocks**
  -External high clock: Crystal type 10MHz~25MHz
  -External low clock: Crystal type 32.768 KHz
  -Internal high clock: RC type 12 MHz
  -Internal low clock: RC type 32 KHz
  -PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  -Clock output function which can reflect the internal high/low RC oscillator, HCLK, PLL output, and external high/low clock.

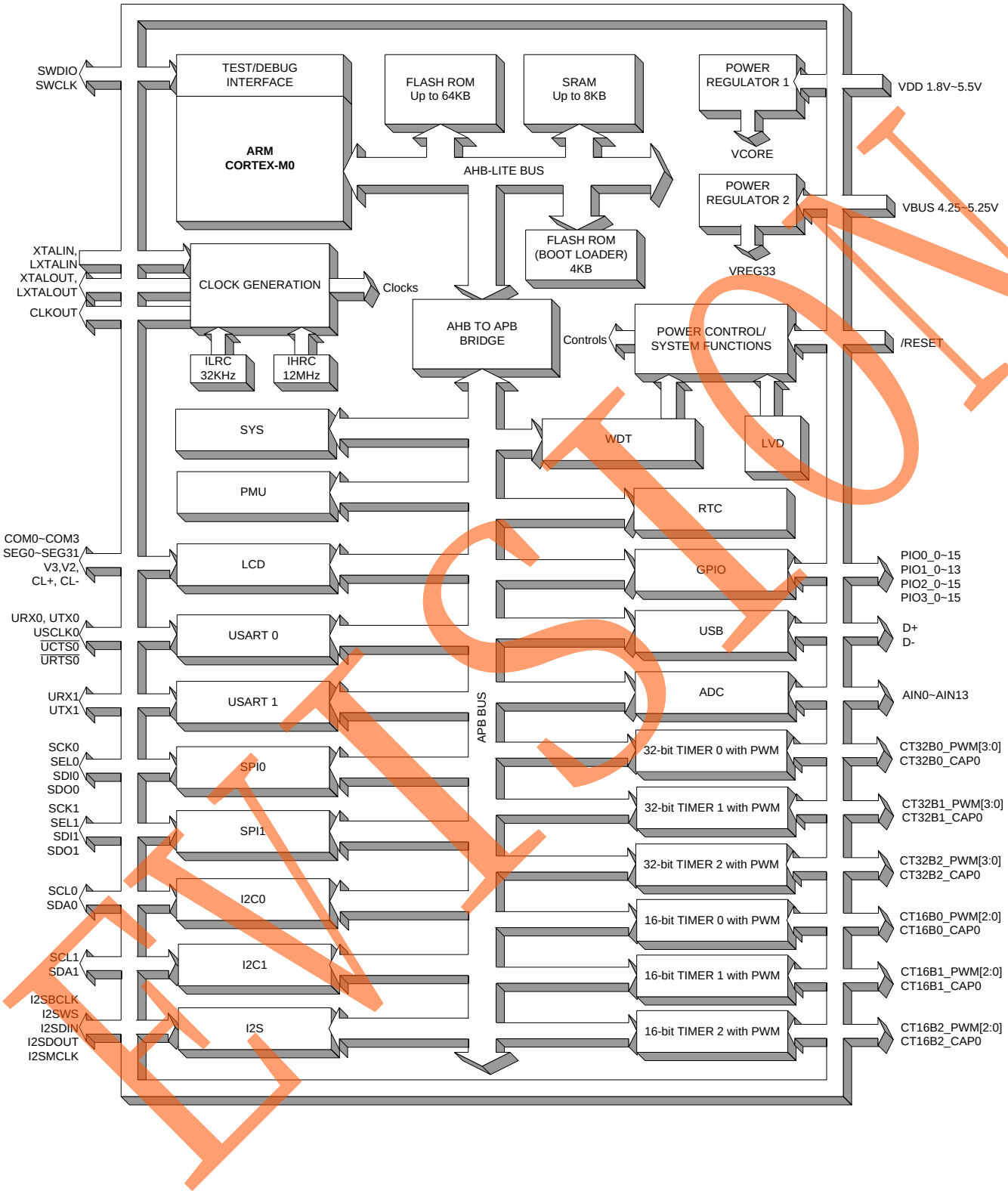
- **Full Speed USB 2.0**
  Conforms to USB specification version 2.0.
  3.3v regulator output for USB D+ pin internal 1.5k pull-up resistor.
  Supports one Full speed USB device address.
  One control endpoint and 6 configurable Isochronous/interrupt/bulk endpoints
  Total 7 endpoints share 512B USB SRAM.

- **LCD driver**
  Support both R-type and C-type
  4 common x 32 segment
  1/3 or 1/2 bias voltage
  Multiple C-type LCD Voltage: 2.7 ~5.0V
  R-type optional-bias resistor: 400K, 200K, 100K, 35K
  Support 1/2 duty, 1/3 duty, 1/4 duty

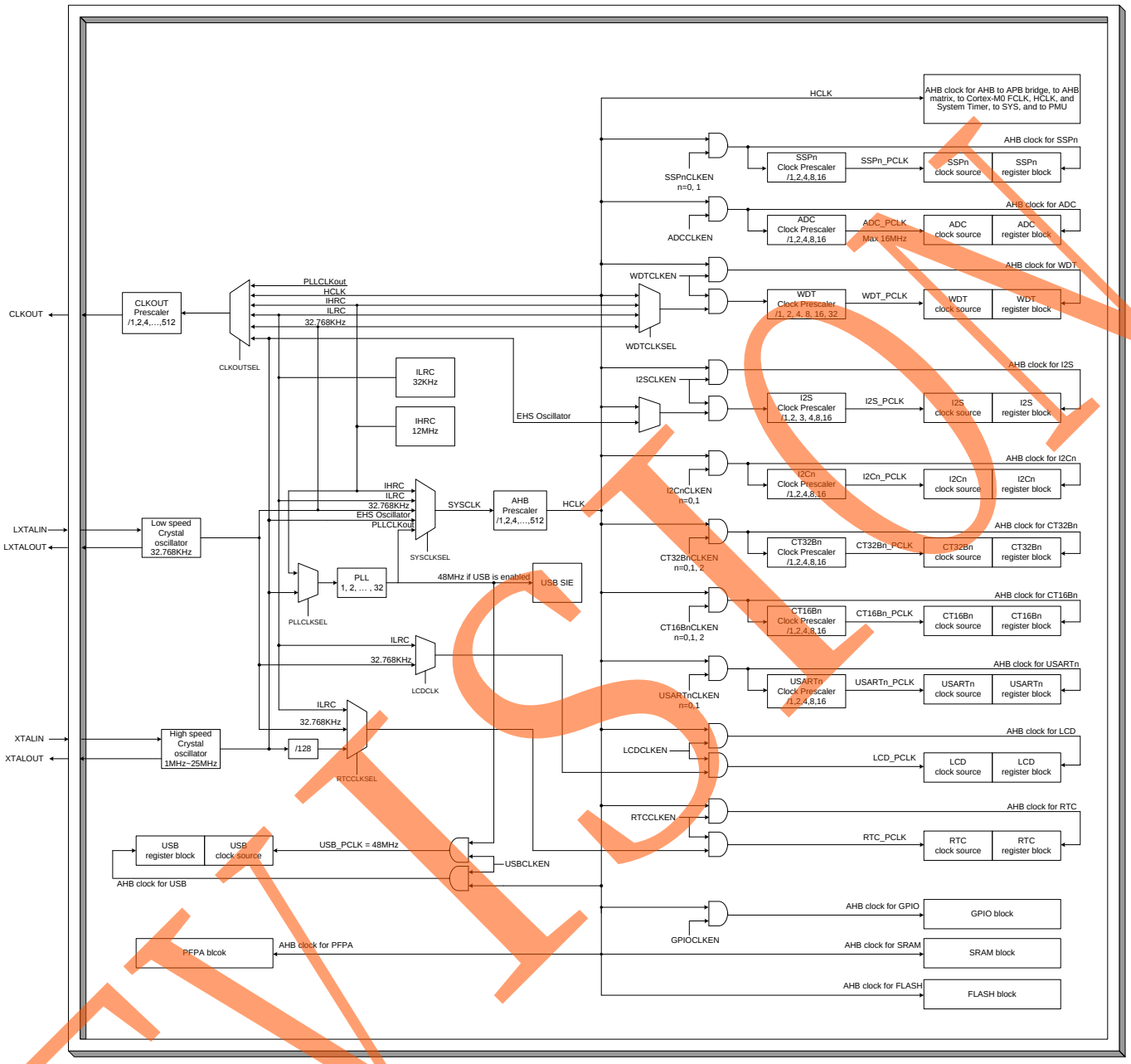
- **In-System Programming (ISP) supported**

- **Package (Chip form support)**
  LQFP 80/64/48 pin

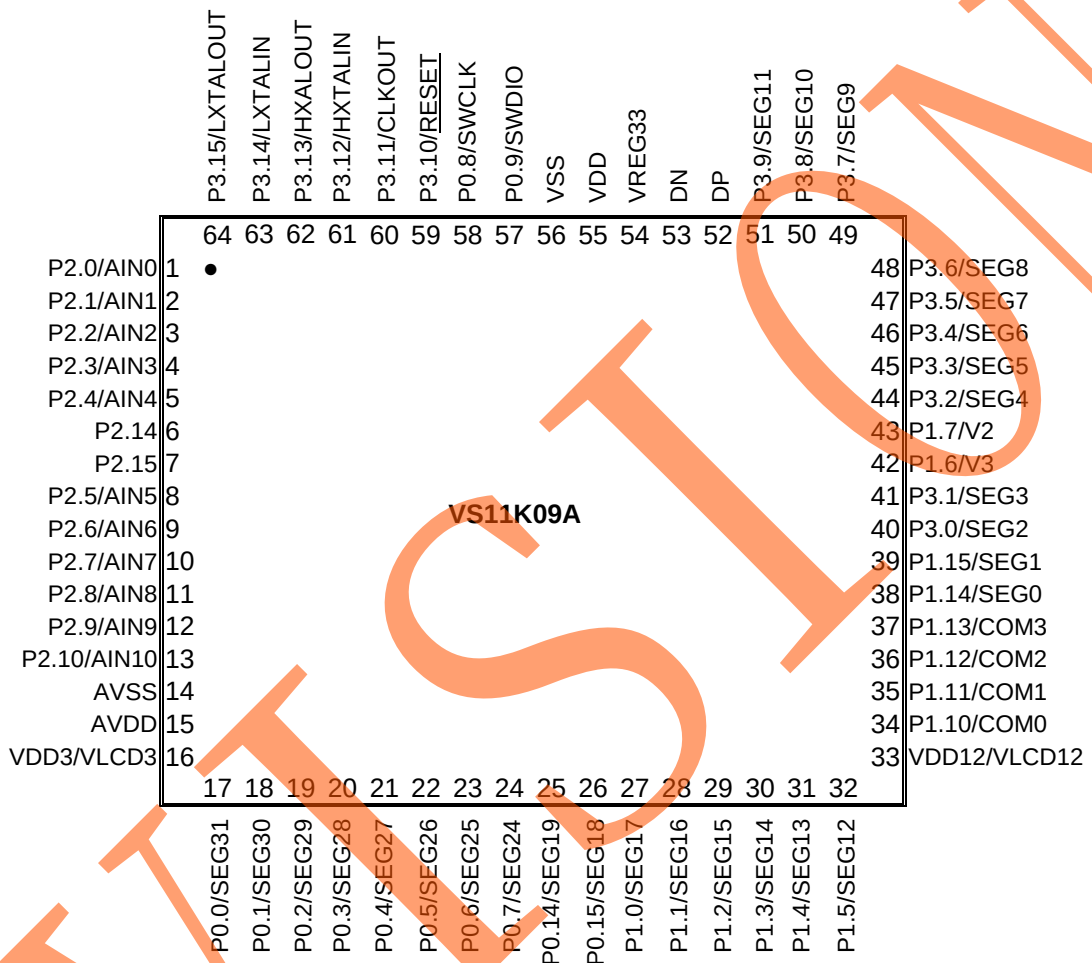
SYSTEM BLOCK DIAGRAM



CLOCK GENERATION BLOCK DIAGRAM



(LQFP 64 pins)



PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital circuit.
AVDD, AVSS	P	Power supply input pins for analog circuit.
VREG33	O	3.3v voltage output from USB 3.3v regulator.
DP, DN	I/O	USB differential data line.
VDD1/VLCD1	P	I/O and LCD driver power input pins for P1.6~P1.15 and P3.0~P3.9. This power input used for I/O power must be equal to VDD.
VDD2/VLCD2	P	I/O and LCD driver power input pins for P0.10~P0.15 and P1.0~P1.5.
VDD12/VLCD12	P	Double bonding pins with VDD1 and VDD2. This power input used for I/O power must be equal to VDD.
VDD3/VLCD3	P	I/O and LCD driver power input pins for P0.0~P0.7. If VDD3 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state in case of internal power collision.
P1.8/CL-, P1.9/CL+	I/O, P	**P1.8, P1.9 —** Port 1.8, P1.9 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **CL+, CL- —** C-Type LCD charge pump capacitor
P1.6/V3, P1.7/V2	I/O, P	**P1.6, P1.7 —** Port 1.6, P1.7 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **V3 —** 2/3 VLCD bias voltage. **V2 —** 1/3 VLCD bias voltage.
P0.0~P0.7	I/O	**P0.0~P0.7 —** Port 0 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode.
P0.8/SWCLK	I/O	**P0.8 —** Port 0.8 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **SWCLK —** Serial Wire Clock pin.
P0.9/SWDIO	I/O	**P0.9 —** Port 0.9 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **SWDIO —** Serial Wire Data input/output pin.
P0.10~P0.15	I/O	**P0.0~P0.15 —** Port 0 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function.
P1.0~P1.5, P1.10~P1.15	I/O	**P1.0~P1.5, P1.10~P1.15 —** Port 1 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function.
P2.0~P2.13/AIN0~13	I/O	**P2.0~P2.13 —** Port 2 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **AIN0~AIN13 —** ADC channel input 0~13 pins.
P2.14	I/O	**P2.14 —** Port 2.14 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function.
P2.15	I/O	**P2.15 —** Port 2.15 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function.
P3.0~P3.9	I/O	**P3.0~P3.9 —** Port 3 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function.

P3.10/RESET	I/O	**P3.10 —** Port 3.10 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **RESET —** External Reset input. Schmitt trigger structure, active “Low”, normally stay “High”.
P3.11/CLKOUT	I/O	**P3.11 —** Port 3.11 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **CLKOUT —** Clockout pin.
P3.12/HXTALIN	I/O	**P3.12 —** Port 3.12 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **HXTALIN —** External high-speed X’tal input pin.
P3.13/HXTALOUT	I/O	**P3.13 —** Port 3.13 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **HXTALOUT —** External high-speed X’tal output pin.
P3.14/LXTALIN	I/O	**P3.14 —** Port 3.14 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **LXTALIN —** External low-speed X’tal input pin.
P3.15/LXTALOUT	I/O	**P3.15 —** Port 3.15 bi-direction pin. Schmitt trigger structure and built-in pull-up/pull-down resistors as input mode. Built-in wakeup function. **LXTALOUT —** External low-speed X’tal output pin.

Please refer to Peripheral Function Pin Assignment (PFPA) chapters for setting of each GPIOs.

Pin Name	Shared pins
P0.0	SEG31 / URXD0 / CT32B0_CAP0 / SCL1 / MISO0
	CT16B0_PWM0 / CT16B2_PWM1 / CT32B2_PWM2
P0.1	SEG30 / UTXD0 / SDA1 / MOSI0
	CT16B0_PWM1 / CT16B2_PWM2 / CT32B1_PWM0
P0.2	SEG29 / SCL0 / MISO0 / SEL1
	CT16B0_CAP0 / CT32B1_CAP0 / CT16B2_PWM0/CT32B2_PWM1
P0.3	SEG28 / SDA0 / MOSI0 /
	CT16B2_CAP0 / CT32B2_PWM2 / CT32B0_PWM3 / CT32B2_PWM0
P0.4	SEG27 / URXD0 / SCK0 / MISO1
	CT16B0_PWM1 / CT32B0_PWM0 / CT32B1_PWM1
P0.5	SEG26 / UTXD0 / SEL0 / MOSI1
	CT16B1_PWM0 / CT32B0_PWM2 / CT32B1_PWM2
P0.6	SEG25 / UTXD1 / SCL1 / MISO0
	CT16B1_PWM2 / CT32B1_PWM3 / C32B2_PWM3
P0.7	SEG24 / URXD1 / SDA1 / MOSI0 / SCK1
	CT16B1_CAP0 / CT32B0_PWM3 / CT32B1_PWM3
P0.8	SWCLK / CT16B0_CAP0 / CT32B1_CAP0
	CT16B1_PWM1 / CT32B0_PWM1 / CT32B1_PWM2 / CT32B2_PWM0

P0.9	SWDIO / CT32B0_CAP0 / CT32B2_CAP0
	CT16B0_PWM2 / CT16B2_PWM1 / CT32B0_PWM2 / CT32B1_PWM0 / CT32B2_PWM2
P0.10	SEG23 / I2SDIN / SDA0 / SEL0 / MISO1
	CT16B0_PWM1 / CT16B1_PWM0 / CT32B2_CAP0
P0.11	SEG22 / I2SDOUT / SCK0
	CT16B0_PWM2 / CT32B0_PWM0 / CT16B1_PWM1 /CT32B1_PWM2
P0.12	SEG21 / URXD1 / SEL0 / MOSI1 / I2SMCLK
	CT16B1_PWM1 / CT16B1_CAP0
P0.13	SEG20 / UTXD1 / SCK0 / SEL1 / I2SBCLK
	CT16B2_CAP0 / CT32B2_PWM0
P0.14	SEG19 / MOSI0 / SCK1 / I2SWS
	CT32B2_PWM1 / CT16B2_PWM0 / CT32B0_PWM1
P0.15	SEG18 / SCL0 / MISO0
	CT32B1_PWM1 / CT16B1_PWM2 / CT32B0_PWM3 / CT32B2_PWM1 / CT32B1_CAP0
P1.0	SEG17 / URXD1 / SDA1 / MISO0 / SEL1
	CT16B0_CAP0 / CT16B2_PWM2 / CT32B2_PWM3
P1.1	SEG16 / UTXD1 / SCL1 / MOSI0 / SCK1
	CT16B0_PWM0 / CT32B2_PWM0 / CT32B0_CAP0
P1.2	SEG15 / UTXD0 / SDA0 / MOSI1
	CT16B1_PWM2 / CT32B1_PWM1 / CT32B0_PWM3 / CT32B1_PWM3
P1.3	SEG14 / URXD0 / SCL0 / MISO1
	CT32B1_CAP0 / CT16B1_PWM1 / CT32B1_PWM0
P1.4	SEG13 / UTXD1 / SDA0 / SCK0 / SEL1
	CT16B2_PWM1 / CT16B2_PWM0 / CT32B2_CAP0
P1.5	SEG12 / URXD1 / SCL0 / SEL0
	CT16B2_CAP0 / CT32B0_PWM1 / CT32B2_PWM1
P1.6	V3 / UCTS0 / I2SDIN / MOSI1
	CT16B0_PWM2 / CT32B1_PWM2 / CT32B2_PWM2 / CT32B1_CAP0
P1.7	V2 / USCLK0 / I2SDOUT / SEL1
	CT16B1_CAP0 / CT32B1_PWM3 / CT32B2_PWM0 / CT32B2_PWM3
P1.8	CL- / URTS0 / SDA1 / I2SMCLK
	CT16B0_PWM0 / CT16B2_CAP0 / CT32B0_PWM0
P1.9	CL+ / SCL1 / I2SBCLK
	CT16B1_PWM2 / CT16B1_PWM0 / CT32B0_PWM2
P1.10	COM0 / MISO1 / I2SWS
	CT16B1_PWM3 / CT16B1_PWM1 / CT32B1_PWM1
P1.11	COM1 / SEL0 / SCK1
	CT16B1_CAP0 / CT16B2_PWM1 / CT32B0_PWM1
P1.12	COM2 / SCK0
	CT16B0_PWM0 / CT16B0_PWM2 / CT16B2_PWM2 / CT32B0_PWM3
P1.13	COM3 / URXD1 / SDA0 / MOSI1
	CT16B0_PWM1 / CT32B1_PWM0 / CT32B2_CAP0

P1.14	SEG0 / UTXD1 / SCL0 / MISO0 / SEL1
	CT16B1_PWM2 / CT32B0_PWM0 / CT32B0_PWM2
P1.15	SEG1 / URXD1 / MOSI0 / SCK1
	CT16B1_PWM0 / CT32B0_PWM0 / CT32B2_PWM0
P2.0	AIN0 / I2SDIN / SEL0 / MOSI1
	CT16B0_CAP0 / CT16B1_PWM0 / CT32B0_PWM2
P2.1	AIN1 / MISO0 / MISO1 / SEL1 / I2SWS
	CT16B1_CAP0/ CT16B2_PWM1 / CT32B1_PWM1
P2.2	AIN2 / MOSI0 / SCK1 / I2SMCLK
	CT16B2_CAP0 / CT16B0_PWM1 / CT32B0_PWM3
P2.3	AIN3 / SCK0
	CT16B0_PWM0 / CT16B1_PWM2 / CT32B0_PWM0 / CT32B2_PWM3 / CT32B0_CAP0
P2.4	AIN4 / CT32B1_CAP0
	CT16B0_PWM2 / CT16B1_PWM1 / CT16B2_PWM2 / CT32B0_PWM1 / CT32B1_PWM3
P2.5	AIN5 / I2SDIN
	CT16B2_PWM0 / CT32B1_PWM2 / CT32B2_CAP0
P2.6	AIN6 / I2SMCLK
	CT16B2_PWM1 / CT32B1_PWM0
P2.7	AIN7 / I2SWS
	CT16B1_PWM2 / CT32B2_PWM1
P2.8	AIN8 / I2SDOUT
	CT16B1_PWM1 / CT32B1_PWM1 / CT32B2_PWM3
P2.9	AIN9 / I2SWS
	CT16B1_CAP0 / CT16B2_PWM0 / CT32B2_PWM3
P2.10	AIN10 / I2SBCLK
	CT16B0_PWM2 / CT16B2_PWM2 / CT32B1_CAP0
P2.11	AIN11 / I2SBCLK
	CT16B0_PWM1 / CT32B0_PWM2 / CT32B2_PWM0
P2.12	AIN12 / MISO0 / MISO1 / I2SDOUT
	CT16B1_PWM0 / CT32B0_PWM3 / CT32B1_PWM2 / CT32B2_CAP0
P2.13	AIN13 / MOSI0 / SCK1
	CT16B0_CAP0 / CT32B0_PWM1 / CT32B1_PWM3 / CT32B2_PWM1
P2.14	SCK0 / SEL1
	CT16B2_CAP0 / CT32B0_PWM0 / CT32B1_PWM2 / CT32B2_PWM2
P2.15	SEL0 / MOSI1
	CT16B0_PWM0 / CT32B1_PWM0 / CT32B2_PWM0 / CT32B2_PWM3 / CT32B0_CAP0
P3.0	SEG2 / URXD0 / I2SDIN / SCL1 / MISO1
	CT16B0_CAP0 / CT16B2_PWM2 / CT32B2_PWM1
P3.1	SEG3 / I2SDOUT / UTXD0 / SEL0
	CT16B2_PWM2 / CT16B2_PWM0 / CT32B2_PWM2 / CT32B0_CAP0
P3.2	SEG4 / UTXD0 / SDA1 / I2SMCLK / SCK0 / MOSI1
	CT16B0_CAP0 / CT32B1_PWM0
P3.3	SEG5 / URXD0 / SCL1 / MISO0 / SCK1 / I2SBCLK
	CT16B0_PWM0 / CT32B0_CAP0
P3.4	SEG6 / UTXD0 / SDA1 / MOSI0 / MISO1 / I2SWS
	CT16B0_PWM1 / CT32B0_PWM3
P3.5	SEG7 / URXD0 / SDA1 / SEL0
	CT16B1_CAP0 / CT16B2_PWM0 / CT16B2_PWM1 / CT32B1_PWM1

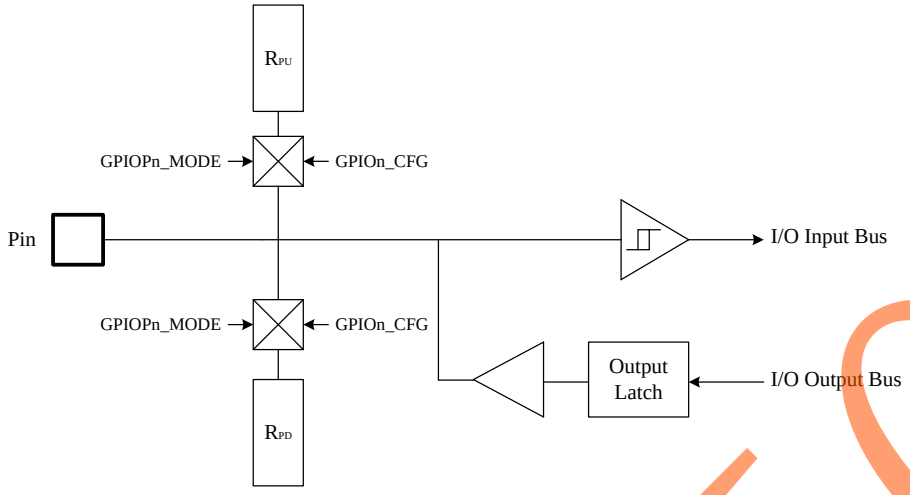
P3.6	SEG8 / URXD1 / SCL1 / SEL1 / SCK0 / I2SBCLK
	CT16B2_CAP0 / CT16B0_PWM2
P3.7	SEG9 / SDA0 / SCK1 / I2SMCLK
	CT16B1_PWM0 / CT32B0_PWM2 / CT32B2_PWM1 / CT32B2_CAP0
P3.8	SEG10 / UTXD1 / I2SDOUT / MOSI1
	CT16B1_PWM2 / CT32B0_PWM1 / CT32B1_CAP0
P3.9	SEG11 / I2SDIN / MISO1 / SCL0
	CT16B1_PWM1 / CT32B0_PWM0 / CT32B1_PWM3 / CT32B0_CAP0
P3.10	RESET / UTXD0 / UTXD1 / SEL0
	CT16B0_CAP0 / CT16B2_PWM0 / CT32B1_PWM1 / CT32B2_PWM3
P3.11	CLKOUT / URXD0 / SCL0 / SCK0 / SEL1
	CT16B0_PWM0 / CT16B2_PWM2 / CT32B1_PWM3
P3.12	HXTALIN / URXD1 / SDA1 / MISO1
	CT16B0_PWM1 / CT16B2_CAP0 / CT32B1_PWM2
P3.13	HXALOUT / UTXD1 / SCL1 / SDA0 / MOSI1
	CT16B1_CAP0 / CT32B0_PWM2 / CT32B2_PWM2
P3.14	LXTALIN / URXD0 / SCL0 / MOSI0 / SCK1
	CT16B1_PWM0 / CT32B0_PWM1 / CT32B2_CAP0
P3.15	LXTALOUT / UTXD0 / SDA0 / MISO0
	CT16B0_PWM2 / CT16B2_PWM1 / CT32B1_PWM0 / CT32B2_PWM2

✸ ***Note:***

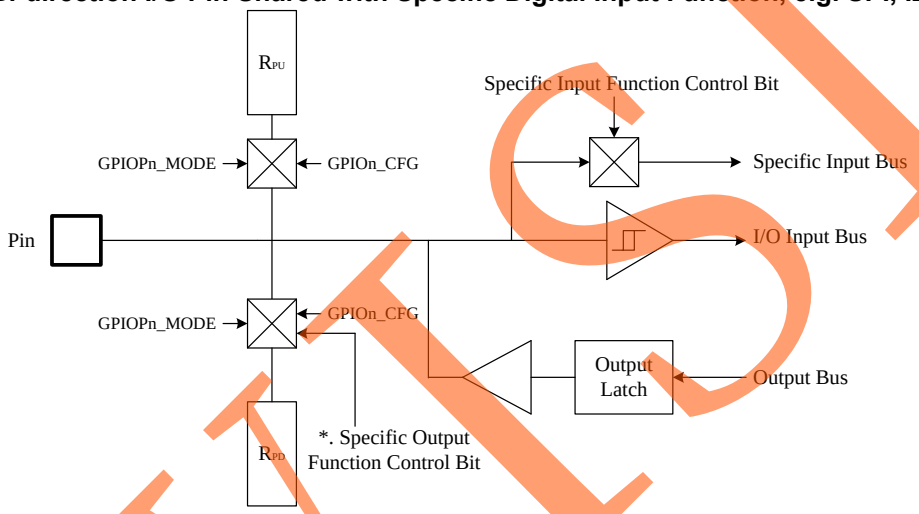
1. ***VDD1/VLCD1 is the*** **I/O and LCD driver power input pin for P1.6~P1.15 and P3.0~P3.9. This power input used for I/O power must be equal to VDD.**
2. **VDD12/VLCD12 is the double bonding pin with VDD1 and VDD2. This power input used for I/O power must be equal to VDD.**
3. ***VDD3/VLCD3 is the*** **I/O and LCD driver power input pin for P0.0~P0.7. If VDD3 voltage is lower than VDD, user should manually force to set the I/O port P1.6 and P1.7 as input pull-down state in case of internal power collision.**

PIN CIRCUIT DIAGRAMS

- **Normal Bi-direction I/O Pin.**

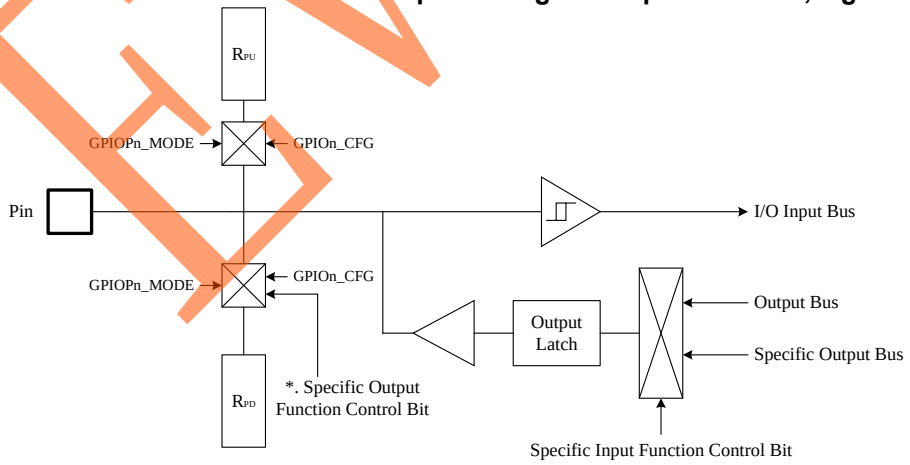


- **Bi-direction I/O Pin Shared with Specific Digital Input Function, e.g. SPI, I2C…**



***. Some specific functions switch I/O direction directly, not through GPIOn_MODE register.**

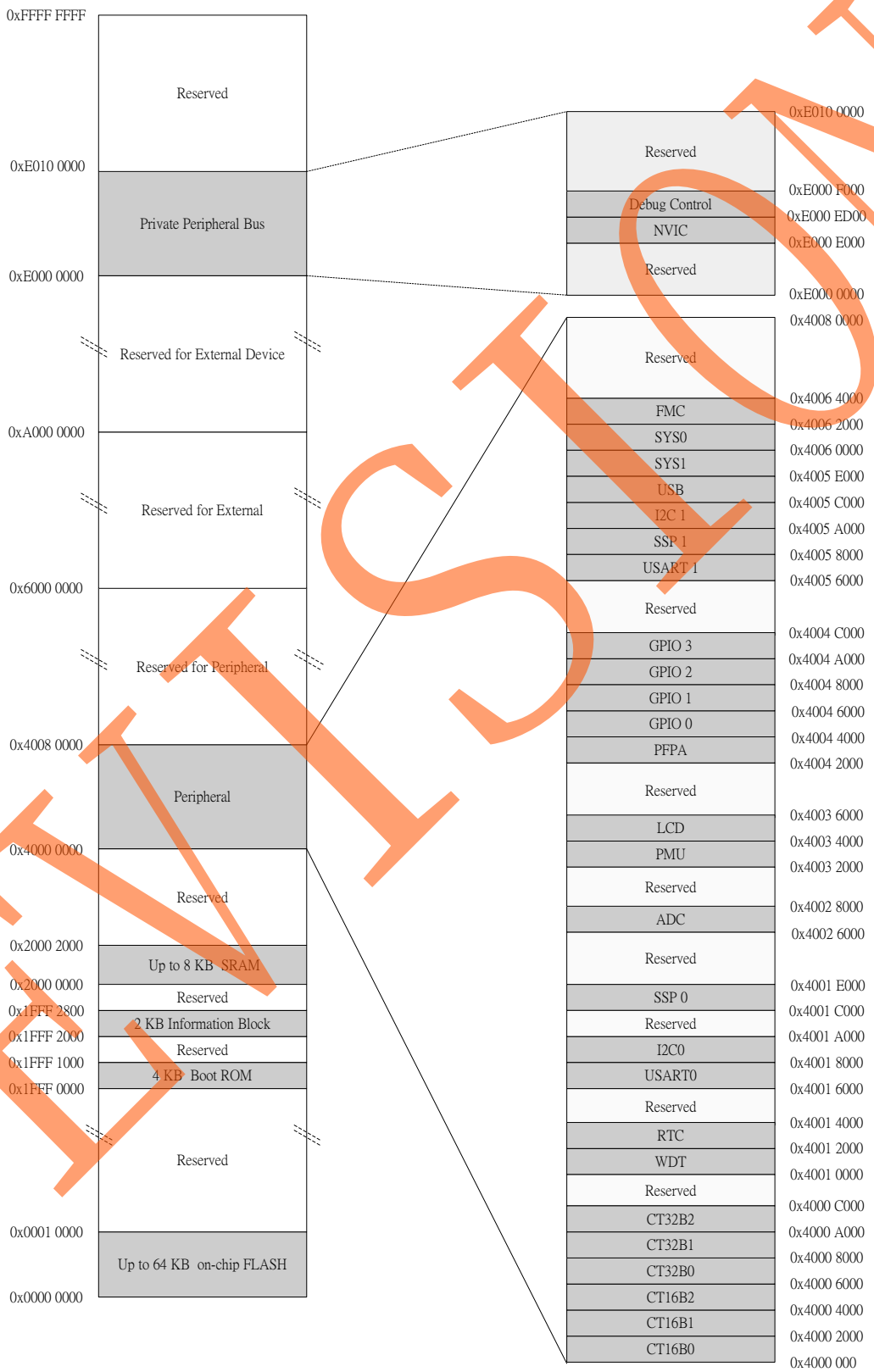
- **Bi-direction I/O Pin Shared with Specific Digital Output Function, e.g. SPI, I2C…**



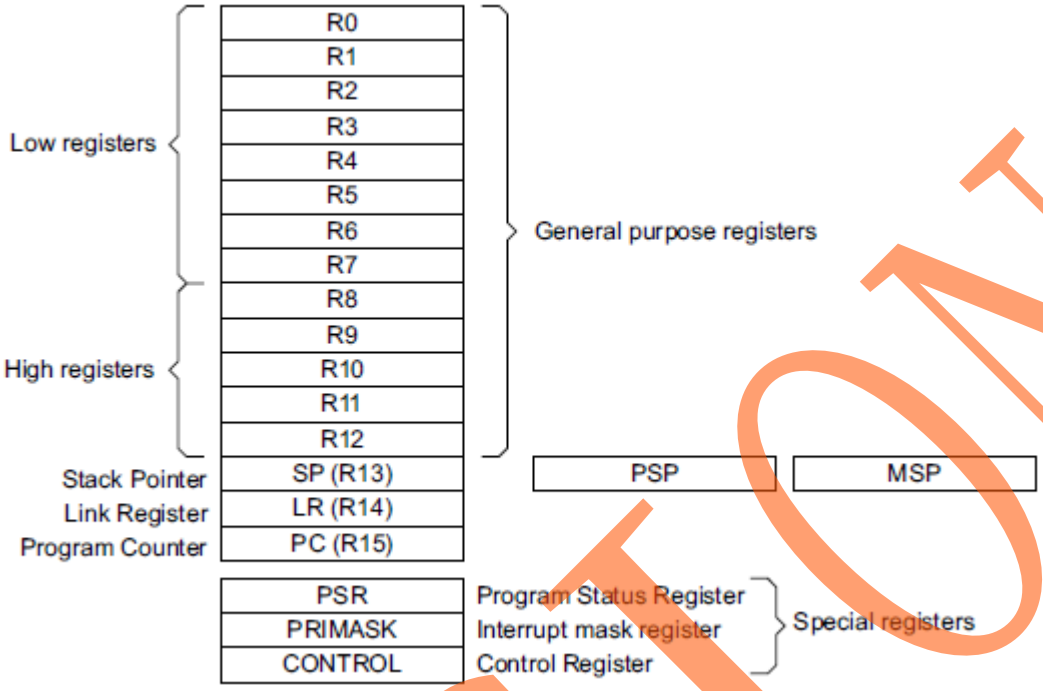
***. Some specific functions switch I/O direction directly, not through GPIOn_MODE register.**

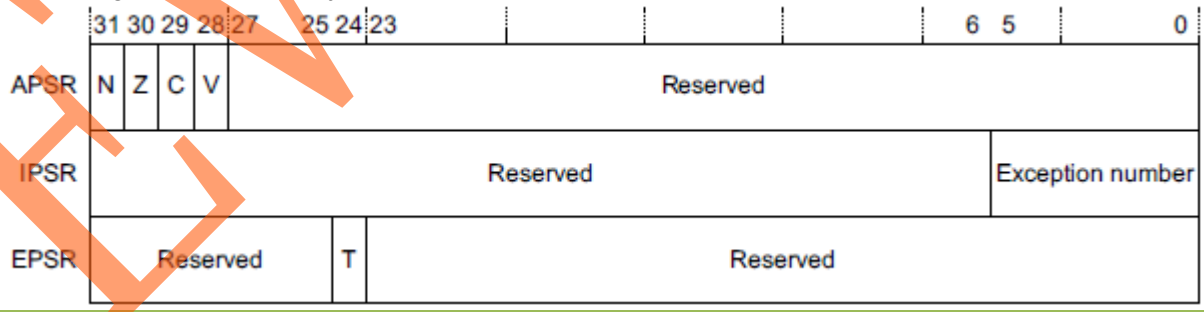
CENTRAL PROCESSOR UNIT (CPU)

MEMORY MAP



CORE REGISTER OVERVIEW



Register	Description (Refer to Cortex-M0 Spec)
R0~R12	General-purpose registers for data operations.
SP (R13)	The Stack Pointer (SP). In Thread mode, the CONTROL register indicates the stack pointer to use, Main Stack Pointer (MSP) or Process Stack Pointer (PSP) On reset, the processor loads the MSP with the value from address 0x00000000.
LR (R14)	The Link Register (LR). It stores the return information for subroutines, function calls, and exceptions.
PC (R15)	The Program Counter (PC). It contains the current program address. On reset, the processor loads the PC with the value of the reset vector, at address 0x00000004.
PSR	The Program Status Register (PSR) combines: • Application Program Status Register (APSR) • Interrupt Program Status Register (IPSR) • Execution Program Status Register (EPSR). These registers are mutually exclusive bit fields in the 32-bit PSR. 
PRIMASK	The PRIMASK register prevents activation of all exceptions with configurable priority.
CONTROL	The CONTROL register controls the stack used when the processor is in Thread mode.

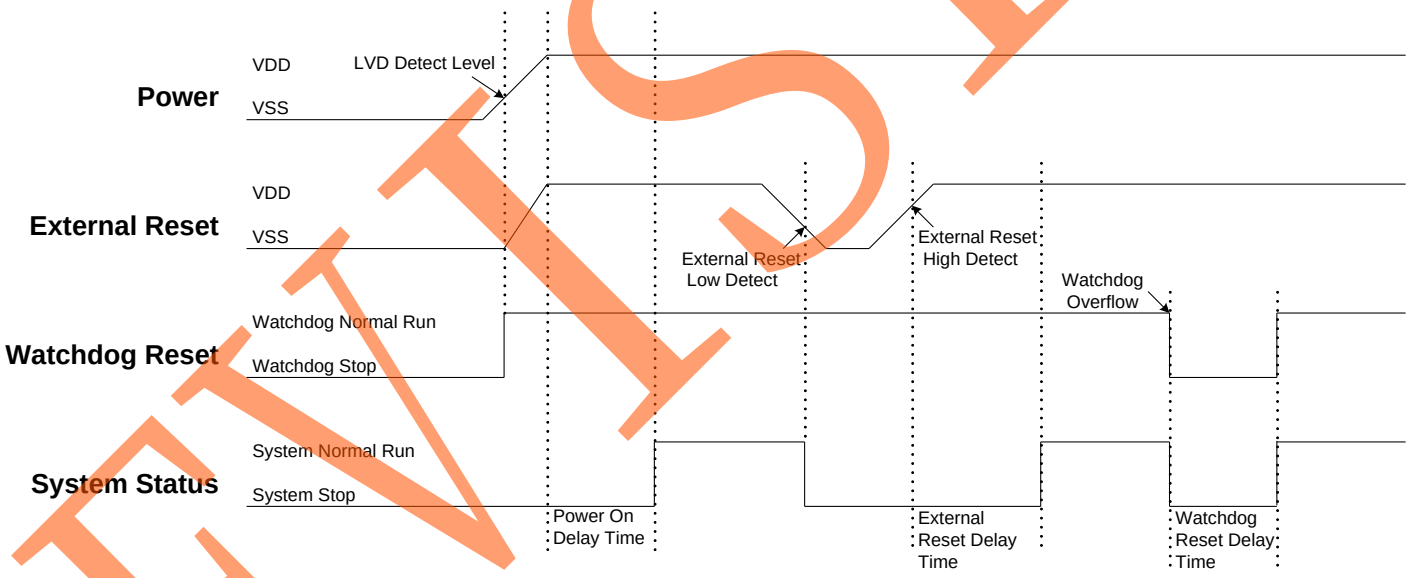
SYSTEM CONTROL

RESET

A system reset is generated when one of the following events occurs:
1. A low level on the RST pin (external reset).
2. Power-on reset (POR reset)
3. LVD reset
4. Watchdog Timer reset (WDT reset)
5. Software reset (SW reset)
6. DPDWAKEUP reset when exiting Deep power-down mode by DPDWAKEUP pin

The reset source can be identified by checking the reset flags in System Reset Status register (SYS0_RSTST). These sources act on the RST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x00000004 in the memory map. For more details, refer to Interrupt and Exception Vectors.

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care of the power on reset time for the master terminal requirement. The reset timing diagram is as following.



POWER-ON RESET (POR)

The power on reset depends on LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following:

- **Power-up:** System detects the power voltage up and waits for power stable.
- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.

➢ **Program executing:** Power on sequence is finished and program executes from Boot loader.

WATCHDOG RESET (WDT RESET)

Watchdog reset is a system protection. In normal condition, system works well and clears watchdog timer by program. Under error condition, system is in unknown situation and watchdog can't be clear by program before watchdog timer overflow. Watchdog timer overflow occurs and the system is reset. After watchdog reset, the system restarts and returns normal mode. Watchdog reset sequence is as following.

- **Watchdog timer status:** System checks watchdog timer overflow status. If watchdog timer overflow occurs, the system is reset.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from 0x0.

Watchdog timer application note is as following.

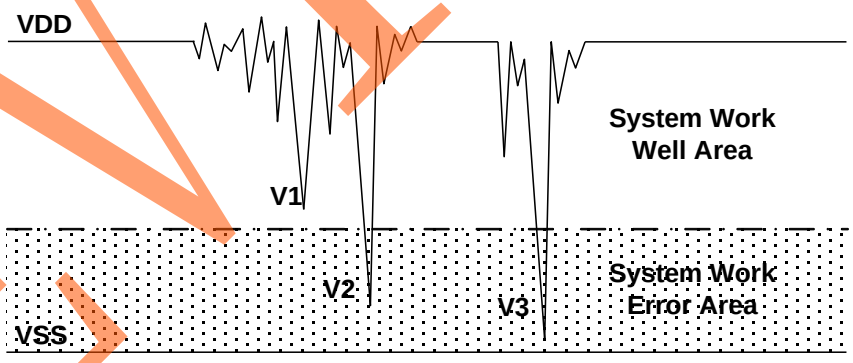
- Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

✷ ***Note: Please refer to the "WATCHDOG TIMER" about watchdog timer detail information.***

BROWN-OUT RESET

BROWN OUT DESCRIPTION

The brown-out reset is a power dropping condition. The power drops from normal voltage to low voltage by external factors (e.g. EFT interference or external loading changed). The brown out reset would make the system not work well or executing program error.



Brown-Out Reset Diagram

The power dropping might through the voltage range that's the system dead-band. The dead-band means the power range can't offer the system minimum operation power requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not affect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

USB FS DEVICE INTERFACE

OVERVIEW

The USB is the answer to connectivity for the PC architecture. A fast, bi-directional interrupt pipe, low-cost, dynamically attachable serial interface is consistent with the requirements of the PC platform of today and tomorrow. The SONIX USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, keyboard, joystick, and game pad.

USB Specification Compliance

— Conforms to USB specifications, Version 2.0.

— Supports 1 Full-speed USB device address.

— Supports 1 control endpoint and 6 configurable endpoints for isochronous/interrupt/bulk transfer.

— Integrated USB transceiver.

— 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.

✸ ***Note: HCLK must be at least ≧3MHz under USB active mode (except USB Suspend).***

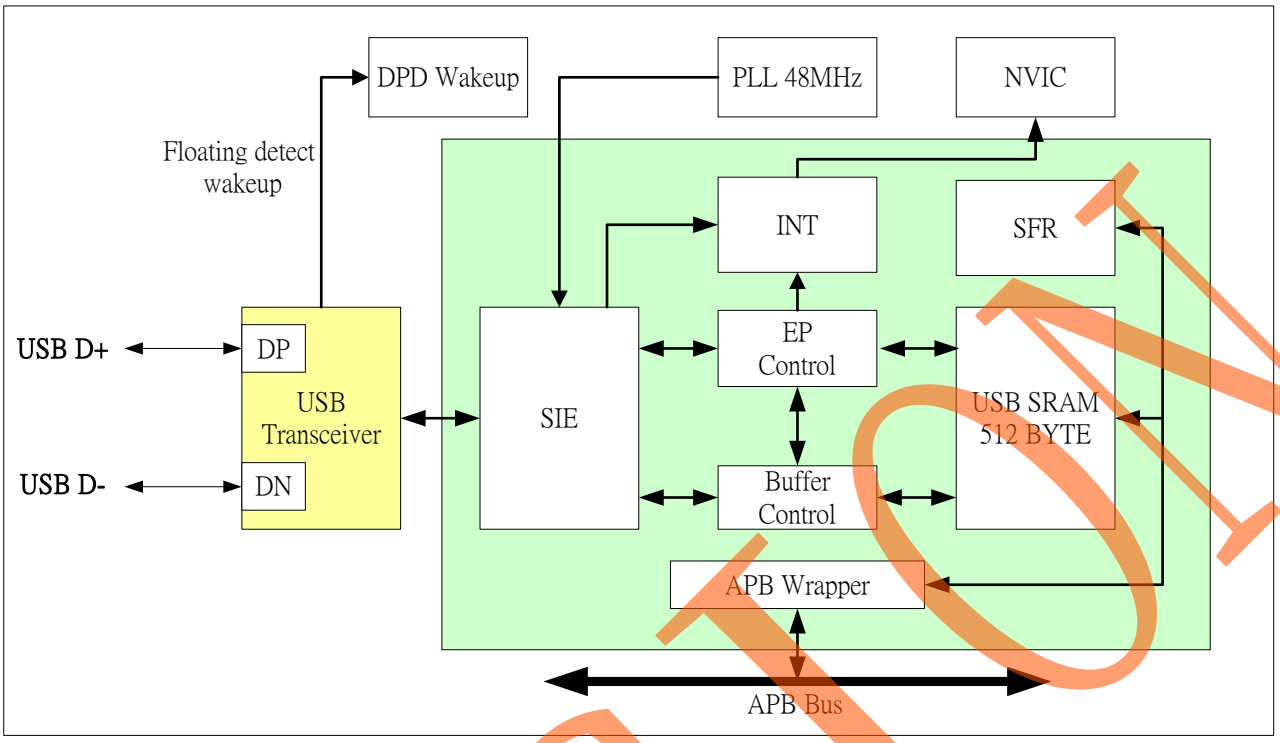
FEATURES

- Conforms to USB specifications, Version 2.0.
- Supports 1 Full-speed USB device address.
- Supports 1 control endpoint with maximum packet size 8 bytes, 16 bytes, 32 bytes, or 64 bytes.
- Supports 6 endpoints configurable for isochronous/interrupt/bulk transfer.
- Supports USB SRAM size 512 bytes shared by all 7 endpoints.
- Flexible data FIFO offset setting for endpoints except endpoint 0.
- 5V to 3.3V regulator output for D+ 1.5K ohm internal resistor pull up.
- Integrated USB transceiver.
- Floating detect wakeup from deep-power down mode.

PIN DESCRIPTION

Pin Name	Type	Description	GPIO Configuration
DP	I/O	USB differential signal D+	N/A
DN	I/O	USB differential signal D-	N/A

BLOCK DIAGRAM



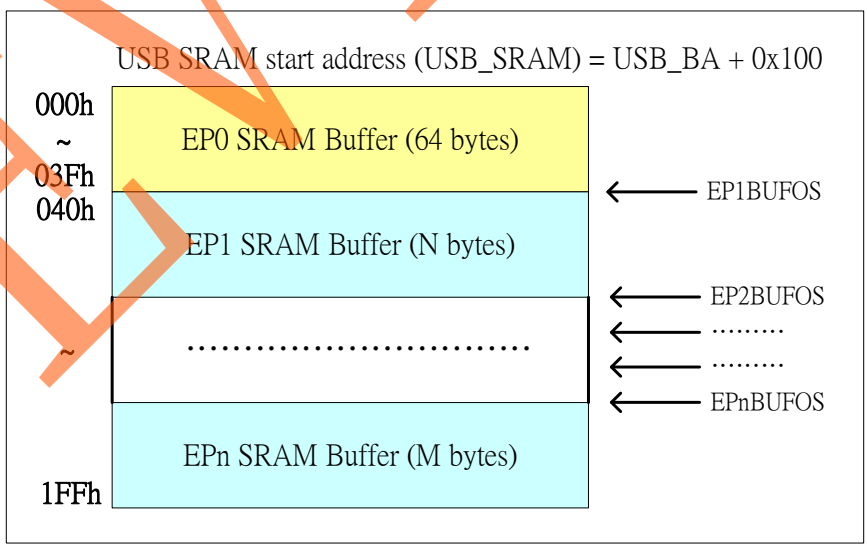
USB SRAM ACCESS

USB SRAM 512 bytes is shared by EP0~EP6, total 7 endpoints. The USB SRAM start address (USB_SRAM) is at (USB_BA + 0x100). EP0 SRAM buffer start address is fixed to range from offset 000h to 03Fh, and EP1~EP6 SRAM buffer start address are configurable by EPnBUFOS register.

The principles to access USB SRAM are as below.

– Each EPnBUFOS setting must be word-aligned, with 2 LSB bits equal to '0'.

– The maximum length of EPn SRAM buffer is defined by user. However, each endpoint should have its own EPn SRAM buffer without overlapping each other.



USB MACHINE

The USB machine allows the microcontroller to communicate with the USB host. The hardware handles the following USB bus activity independently of the microcontroller.

The USB machine will do:

– Translate the encoded received data and format the data to be transmitted on the bus.
– CRC checking and generation by hardware. If CRC is not correct, hardware will not send any response to USB host.
– Send and update the data toggle bit (Data1/0) automatically by hardware.
– Send appropriate ACK/NAK/STALL handshakes.
– SETUP, IN, or OUT Token type identification. Set the appropriate bit once a valid token is received.
– Place valid received data in the appropriate endpoint FIFOs.
– Bit stuffing/unstuffing.
– Address checking. Ignore the transactions not addressed to the device.
– Endpoint checking. Check the endpoint's request from USB host, and set the appropriate bit of registers.

Firmware is required to handle the rest of the following tasks:

– Coordinate enumeration by decoding USB device requests.
– Fill and empty the FIFOs.
– Reset/Suspend/Resume coordination.
– Remote wake up function.
– Determine the right interrupt request of USB communication

USB INTERRUPT

The USB function will accept the USB host command and generate the relative interrupts, and enter USB_IRQ_Handler. Firmware is required to check the USB status bit to realize what request comes from the USB host.

The USB function interrupt is generated when:

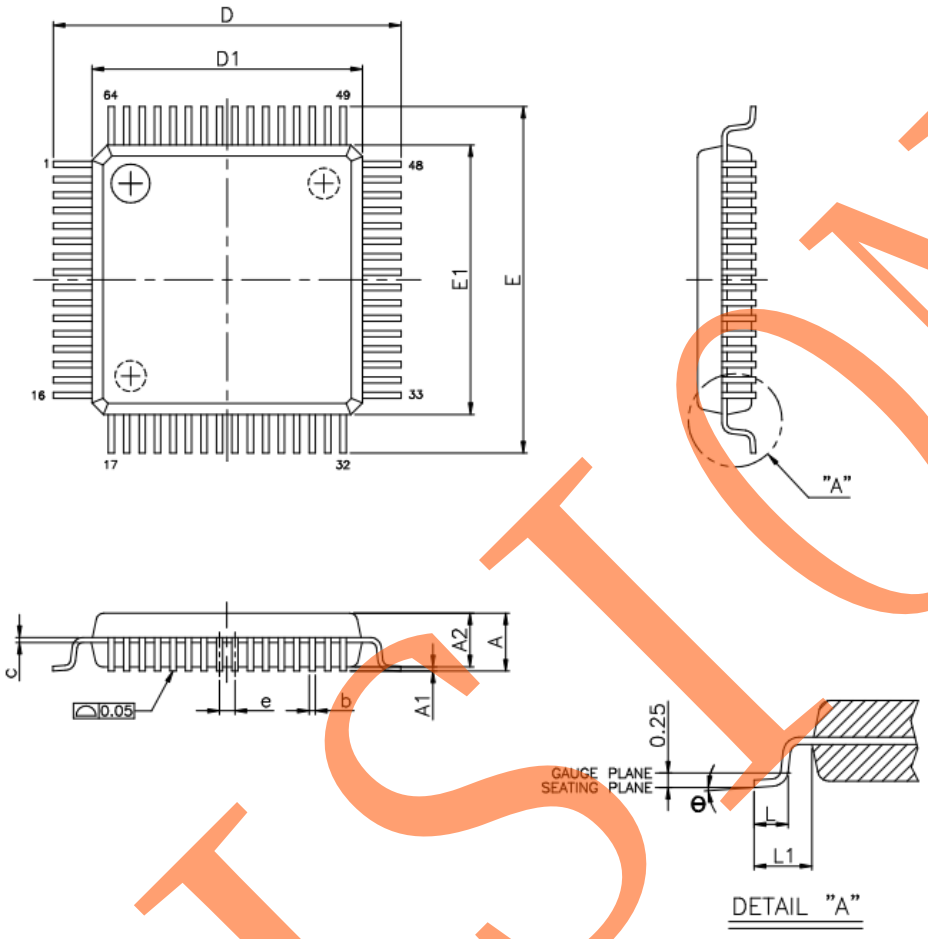
– The endpoint 0 is set to accept a SETUP token.
– The device receives an ACK handshake after a successful read transaction (IN) from the host.
– If the endpoint is in ACK OUT modes, an interrupt is generated when data is received.
– The USB host sends USB suspend request to the device.
– USB bus reset/resume event occurs.
– The USB endpoints interrupt after a USB transaction complete is on the bus.
– The NAK handshaking when the NAK interrupt enables.

USB ENUMERATION

A typical USB enumeration sequence is shown below.

1. The host computer sends a SETUP packet followed by a DATA packet to USB address 0 requesting the Device descriptor.
2. Firmware decodes the request and retrieves its Device descriptor from the program memory tables.
3. The host computer performs a control read sequence and firmware responds by sending the Device descriptor over the USB bus, via the on-chip USB SRAM.
4. After receiving the descriptor, the host sends a SETUP packet followed by a DATA packet to address 0 assigning a new USB address to the device.
5. Firmware stores the new address in its USB Device Address Register after the no-data control sequence completes.
6. The host sends a request for the Device descriptor using the new USB address.
7. Firmware decodes the request and retrieves the Device descriptor from program memory tables.
8. The host performs a control read sequence and firmware responds by sending its Device descriptor over the USB bus.
9. The host generates control reads from the device to request the Configuration and Report descriptors.
10. Once the device receives a Set Configuration request, its functions may now be used.
11. Firmware should take appropriate action for Endpoint 0~N transactions, which may occur from this point.

LQFP 64 PIN



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°