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VS11K18A IC手册参考

VS 8-Bit Micro Controler

1 PRODUCT OVERVIEW

1.1 FEATURES

Memory configuration.
FLASH ROM size: 4K x 16 bits.
RAM size: 160 x 8 bits.

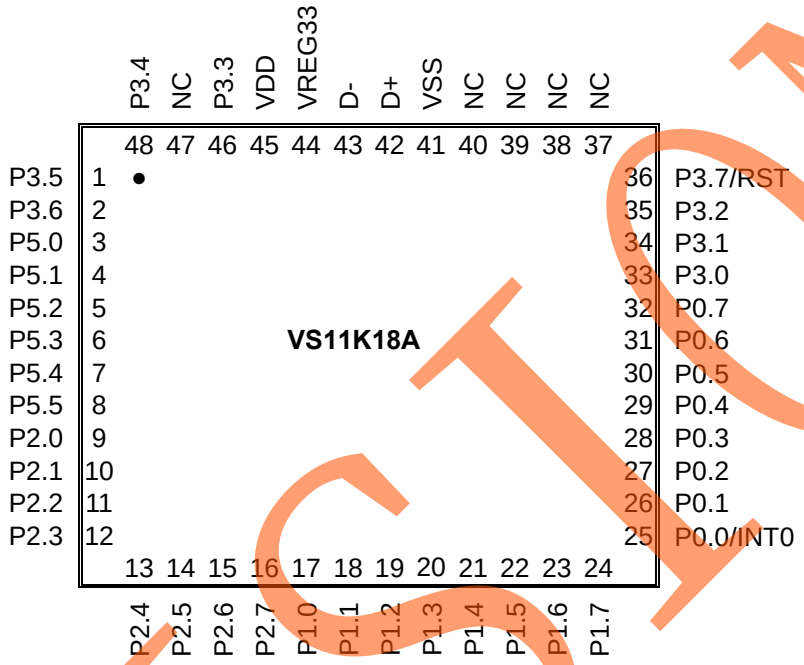
- **8 levels stack buffer.**
- **I/O pin configuration.**
  Bi-directional: P0, P1, P2, P3, P5
  Wake-up: P0/P1/P2/P3/P5 level change.
  Pull-up resistors: P0, P1, P2, P3, P5
  External interrupt: P0.0 controlled by PEDGE.
- **Low Speed USB 2.0**
  Conforms to USB Specification, Version 2.0
  3.3V regulator output for USB D- pin internal 1.5k ohm pull-up resistor.
  Integrated USB transceiver.
  Supports 1 Low speed USB device address and 1 control endpoint has 8 bytes FIFO
  2 interrupt endpoints, each has 8 bytes FIFO
- **Powerful instructions.**
  Instruction cycle controlled by code option.
  Instruction's length is one word.
  Most of instructions are one cycle only.
  Maximum instruction cycle is two.
  All ROM area JMP instruction.
  All ROM area lookup table function (MOVC)
- **USB mode only support.**
- **6 interrupt sources.**
  5 internal interrupts: TC0, USB, NDT, Wakeup, AKA
  1 external interrupts: INT0
- **8 bits timer counter (TC0)**
- **On chip watchdog timer.**
- **Two system clocks.**
  Internal high clock: Fcpu(max) = 6MHz
  Internal low clock: RC type 32KHz (5V).
- **Four operating modes.**
  Normal mode: Both high and low clock active
  Slow mode: Low clock only
  Sleep mode: Both high and low clock stop
  Green mode: Periodical wakeup by timer
- **Package (Chip form support).**
  LQFP 48 pin
  QFN 46 pin
- **In-system re-programmability**
  Allows easy firmware update

Features Selection Table

CHIP	ROM	RAM	STACK	TC0 TIMER	USB	I/O	WAKE-UP PIN NO.	PACKAGE
VS11K18A	4K*16	160*8	8	v	v	38	37	LQFP48

1.2 PIN ASSIGNMENT

(LQFP 48 pins)



1.3 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital circuit.
P0.0/INT0	I/O	P0.0: Port 0.0 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function. INT0: External interrupt 0 input pin.
P0[7:1]	I/O	P0: Port 0 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
P1[7:0]	I/O	P1: Port 1 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
P2[7:0]	I/O	P2: Port 2 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
P3.7/RST	I/O	RST is system external reset input pin under Ext_RST mode. Schmitt trigger structure, active “low”, normal stay to “high”. P3.7 is a bi-direction pin under P3.7 mode. Schmitt trigger structure and built-in pull-up resisters as input mode.
P3[6:0]	I/O	P3: Port 3 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
P5[5:0]	I/O	P5: Port 5 bi-direction pin. Schmitt trigger structure and built-in pull-up resisters as input mode. Built wakeup function.
VREG33	O	3.3V voltage output from USB 3.3V regulator.
D+, D-	I/O	USB differential data line.

2 UNIVERSAL SERIAL BUS (USB)

2.1 OVERVIEW

The USB is the answer to connectivity for the PC architecture. A fast, bi-directional interrupt pipe, low-cost, dynamically attachable serial interface is consistent with the requirements of the PC platform of today and tomorrow. The SONIX USB microcontrollers are optimized for human-interface computer peripherals such as a mouse, joystick, game pad.

USB Specification Compliance

— Conforms to USB specifications, Version 2.0.

— Supports 1 Low-speed USB device address.

— Supports 1 control endpoint, 3 interrupt endpoints.

— Integrated USB transceiver.

— 5V to 3.3V regulator output for D- 1.5K ohm internal resistor pull up.

2.2 USB MACHINE

The USB machine allows the microcontroller to communicate with the USB host. The hardware handles the following USB bus activity independently of the microcontroller.

The USB machine will do:

- Translate the encoded received data and format the data to be transmitted on the bus.
- CRC checking and generation by hardware. If CRC is not correct, hardware will not send any response to USB host.
- Send and update the data toggle bit (Data1/0) automatically by hardware.
- Send appropriate ACK/NAK/STALL handshakes.
- SETUP, IN, or OUT Token type identification. Set the appropriate bit once a valid token is received.
- Place valid received data in the appropriate endpoint FIFOs.
- Bit stuffing/unstuffing.
- Address checking. Ignore the transactions not addressed to the device.
- Endpoint checking. Check the endpoint's request from USB host, and set the appropriate bit of registers.

Firmware is required to handle the rest of the following tasks:

- Coordinate enumeration by decoding USB device requests.
- Fill and empty the FIFOs.
- Suspend/Resume coordination.
- Remote wake up function.
- Determine the right interrupt request of USB communication.

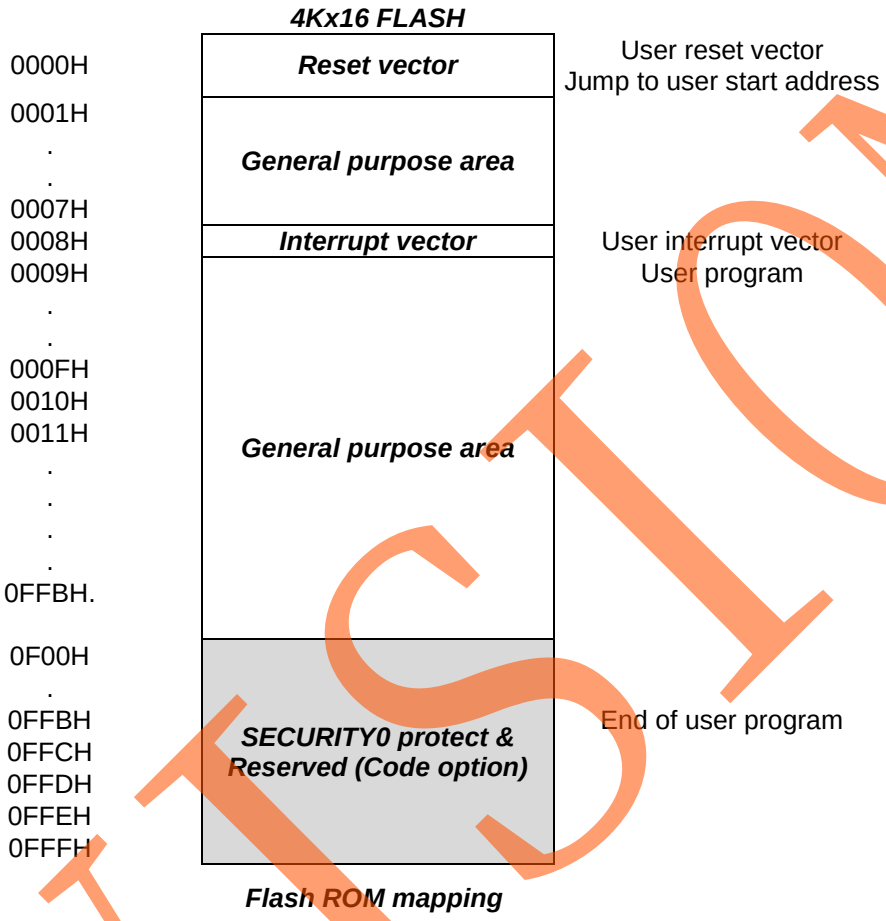
3 FLASH

3.1 OVERVIEW

The VS11K18A series USB MCU integrated device feature in-system programmable (ISP) FLASH memory for convenient, upgradeable code storage. The FLASH memory may be programmed via the SONiX 8 bit MCU programming interface or by application code and USB interface for maximum flexibility. The VS11K18A provides security options at the disposal of the designer to prevent unauthorized access to information stored in FLASH memory.

- The MCU is stalled during Flash write (program) and erase operations, although peripherals (USB, Timers, WDT, I/O, PWM, etc.) remain active.
- Interrupts will disable by firmware during a Flash write or erase operation.
- The Flash page containing the boot loader and code option (ROM address 0xF80 ~ 0xFFF) cannot be erased from application code when the code option's security1 enable.
- Watch dog timer should be clear before the Flash write or erase operation.
- The erase operation sets all the bits in the Flash page to logic 1.
- Hardware will hold system clock and automatically move out data from RAM and do programming, after programming finished, hardware will release system clock and let MCU execute the next instruction.(Recommend add two NOP instructions after this active).

The valid **PAGE PROGRAM** starting addresses are **0x0, 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0, 0xE0 … 0xFE0.** The page program function is used to program a page of 32 contiguous words in Flash ROM.



4 ELECTRICAL CHARACTERISTIC

4.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 6.0V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr) ..... 0°C ~ + 70°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

4.2 ELECTRICAL CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, fosc = 6MHz, ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd1	Normal mode except USB transmitter specifications, Vpp = Vdd		4.1	5	5.5	V
RAM Data Retention voltage	Vdr			-	1.5*	-	V
Vdd rise rate	Vpor	Vdd rise rate to ensure power-on reset		0.05	-	-	V/ms
Input Low Voltage	ViL1	All input ports		Vss	-	0.3Vdd	V
	ViL2	Reset pin		Vss	-	0.3Vdd	V
Input High Voltage	ViH1	All input ports		0.7Vdd	-	Vdd	V
	ViH2	Reset pin		0.7Vdd	-	Vdd	V
Reset pin leakage current	Ilekg	Vin = Vdd		-	-	2	uA
I/O port pull-up resistor	Rup	Vin = Vss , Vdd = 5V		40	80	120	KΩ
I/O port input leakage current	Ilekg	Pull-up resistor disable, Vin = Vdd		-	-	2	uA
I/O P0/P1/P2/P5/P3.0~P3.3/P3.7 output source current	IoH1	Vop = Vdd – 0.5V		2	4	6	mA
I/O P0/P1/P2/P5/P3.0~P3.3/P3.7 output source current (connect LED)	IoH2	Vop = 2V		10	12	14	
I/O P3.4~P3.6 output source current	IoH3	Vop = Vdd – 0.5V		8	11	14	
I/O P0/P1/P2/P5/P3.0~P3.3/P3.7 output sink current	IoL1	Vop = Vss + 0.5V		2	4	6	
I/O P0/P1/P2/P5/P3.0~P3.3/P3.7 output sink current. (connect LED)	IoL2	Vop = 2.9V		10	12	14	
I/O P3.4~P3.6 output sink current	IoL3	Vop = Vss + 0.5V		8	11	14	
INTn trigger pulse width	Tint0	INT0 interrupt request pulse width		2/fcpu	-	-	cycle
Regulator output voltage	Vreg	Regulator output voltage, Vin = Vdd		3.0		3.6	V
Regulator GND current	$I_{VREGn}1$	No loading. Vreg pin output 3.3V ((Regulator enable)			110	200	uA
Supply Current	Idd1	normal Mode (No loading, Fcpu = Fosc/1)	Vdd= 5V, 6Mhz	6	-	10	mA
	Idd2	Slow Mode (Internal low RC)	Vdd= 5V, 32Khz	-	160	200	uA
	Idd3	Sleep Mode	Vdd= 5V	-	110	200	uA
	Idd4	Green Mode (No loading, Fcpu = Fosc/4 Watchdog Disable)	Vdd= 5V,6Mhz	-	0.6	1.2	mA
			Vdd=5V, ILRC 32Khz	-	120	200	uA
LVD Voltage	Vdet0	Low voltage reset level.		2.8	3.1	3.8	V

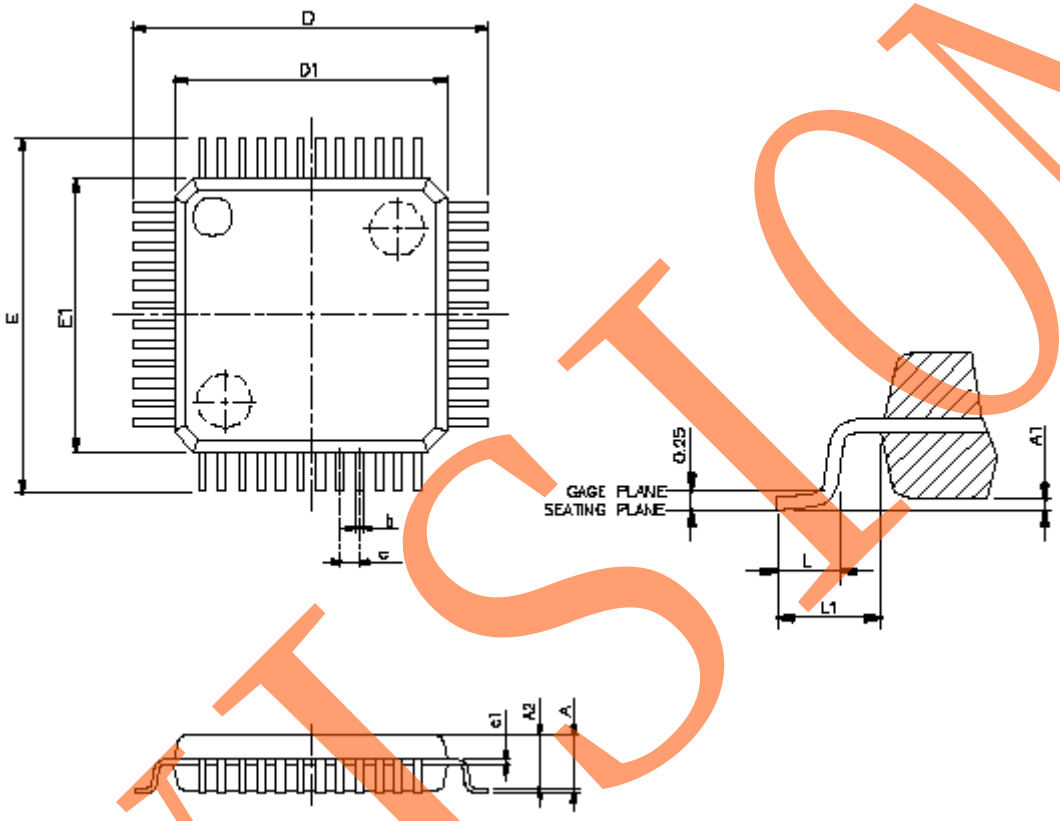
*** These parameters are for design reference, not tested.**

5 FLASH ROM PROGRAMMING PIN

Programming Information											
Chip Name		VS11K18A									
EZ Writer / MP Writer Connector		OTP IC / JP3 Pin Assigment									
Number	Name	Number	Pin	Number	Pin	Number	Pin	Number	Pin	Number	Pin
1	VDD	45	VDD								
2	GND	41	VSS								
		25	P0.0								
3	CLK	48	P3.4								
4	CE										
5	PGM	2	P3.6								
6	OE	46	P3.3								
7	D1										
8	D0										
9	D3										
10	D2										
11	D5										
12	D4										
13	D7										
14	D6										
15	VDD										
16	VPP										
17	HLS										
18	RST										
19	-										
20	ALSB/PDB	1	P3.5								

6 PACKAGE INFORMATION

15.1 LQFP 48 PIN



SYMBOLS	MIN	NOR	MAX
	(mm)		
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	-	1.45
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.5 BSC		
B	0.17	-	0.27
L	0.45	-	0.75
L1	1 REF		