

SLED1735 Series

USER'S MANUAL

SLED1732S

SLED17321S

SLED1733S

SLED17331S

SLED1734X/J

SLED17341X/J

SLED1735J

SONiX Matrix LED Driver IC

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AMENDENT HISTORY

Version	Date	Description
VER 0.1	2016/03/18	First version released.
VER 0.2	2016/03/22	<ol style="list-style-type: none">1. Fix the maximum RGB LEDs numbers supported by Matrix Type-1.2. Fix the application circuit of Matrix Type-4 with SPI interface.3. Fix the breath control 2 register's description.4. Add the page header and the page number.5. Fix the typing error of Vaf RAM mapping.
VER 0.3	2016/04/01	<ol style="list-style-type: none">1. Fix the Type-4 matrix diagrams.
VER 0.4	2016/04/06	<ol style="list-style-type: none">1. Fix the Type-4 matrix diagrams.
VER 0.6	2016/04/22	<ol style="list-style-type: none">1. Update QFN28 package information.2. Fix Vaf3(000) of VAF Register 2(15h) is Vdd.3. Update COMMON ANODE RGB LED IN MATRIX TYPE-3(Page30).
VER 0.7	2016/05/10	<ol style="list-style-type: none">1. Update Type-3 maximum to 70 anode RGB LEDs are supported.2. Add ADCEN(Bit_4) function in Configuration Register(00h).3. Update electrical characteristics.
VER 0.8	2016/06/13	<ol style="list-style-type: none">1. Update electrical characteristic.2. Update 00h, 05h, 14h, 15h, 18h, 19h, 1Ah, and 1Bh function register.3. Add wakeup time form power down mode.
VER 0.9	2016/09/05	<ol style="list-style-type: none">1. Fix typing error in COMMON CATHODE RGB LED IN MATRIX TYPE-1(Page25).2. Fix phase timing of matrix type-4(Page57).3. Update LVD voltage is 2.75V.4. Add SLED1732SG, SLED 7321SG, SLED1733SG and SLED17331SG.
VER 1.0	2016/09/26	<ol style="list-style-type: none">1. Fix SLED17341 SPI INTERFACE WITH LED MATRIX TYPE-3.
VER 1.1	2017/03/28	<ol style="list-style-type: none">1. Modify LVD Voltage.
VER 1.2	2017/05/12	<ol style="list-style-type: none">1. Modify Operating Voltage(Vdd) & Vds Voltage in ELECTRICAL CHARACTERISTIC.
VER 1.3	2017/06/30	<ol style="list-style-type: none">1. Modify COMMON CATHODE RGB LED IN MATRIX TYPE-3.
VER 1.4	2017/07/04	<ol style="list-style-type: none">1. Modify Operating Voltage.
VER 1.5	2017/08/15	<ol style="list-style-type: none">1. Modify COMMON CATHODE RGB LED IN MATRIX TYPE-1.2. Modify ID register is 0x73.
VER 1.6	2018/01/19	<ol style="list-style-type: none">1. Modify RGB LED MATRIX.

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1 PRODUCT OVERVIEW

1.1 FEATURES

- ◆ **Support I2C/SPI slave communication**
- ◆ **LED Controls**
 - Each LED has the on/off control.
 - Each LED has the blink enable/disable control.
 - Each LED has the 8-bit programmable PWM duty.
 - Each LED has the open/short detection status.
 - Each LED has the anti-forward control (Vaf) to prevent the ghost LED effects.
 - Each LED has the +/-6% current fine tune control.
 - Support global 8mA~40mA constant current source control.
- ◆ **MPWM IO (CA1~CA9, CB1~CB9, and CC1~CC6)**
 - Each MPWM IO has sink current of 320mA.
 - Each MPWM IO supports staggered delay.
 - Each MPWM IO supports slew rate control.
 - Each MPWM IO except CC1~CC6 has the precise current skew under +/-2%.
 - Current skew between chips is under +/-3%.
- ◆ **System Clock Synchronization for cascaded LED drivers**
 - Support SYNC output in master mode.
 - Support SYNC input in slave mode.
- ◆ **I2C Slave**
 - Maximum to 400KHz Support four auto-selective slave addresses by which AD pin is connected to (VDD/VSS/SCL/SDA).
- ◆ **SPI Slave**
 - Maximum to 2.4MHz.
- ◆ **Matrix Control Engine**
 - Support Type 1~4 matrixes by register setting.
 - The frame time depending on Matrix Type has different phase number.
 - Type-1 has the frame time 1098us including 9 phases.
 - Type-2 and Type-4 have the frame time 1464us including 12 phases.
 - Type-3 has the frame time 1952us including 16 phases.
 - Each phase includes the PWM duty time 107us and the blanking time 15us.
 - Support auto-breath control.
 - Support auto-blink control.
 - Support Audio-IN synchronous to auto-brightness control.
- ◆ **Audio In Gain Control**
 - Support register configurable gain for Audio-IN: 0dB, 3dB, 6dB, 9dB, 12dB, 15dB, 18dB, and 21dB.
 - Support auto-gain control.
- ◆ **Thermal Detection**
 - Support thermal shutdown at 150°C.
 - Support thermal flag at 70°C.
- ◆ **Power Modes**
 - Normal Mode.
 - Software power down mode.
 - Hardware power down mode.
- ◆ **Package**
 - SOP20/SOP24/QFN28/SSOP28/QFN46.

◆ **SLED1732/17321 built-in three LED Matrix Types.**

◆ **LED Matrix Type-1**

Achieve 9x8 LED matrix by CA1~CA9

Maximum to 72 LEDs are supported.

Maximum to 18 common anode RGB LEDs are supported.

Maximum to 18 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-2**

Achieve 9x9 LED matrix by CA1~CA9 and CB1.

Maximum to 81 LEDs are supported.

Maximum to 21 common anode RGB LEDs are supported.

Maximum to 22 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-3**

Achieve 9x9 LED matrix by CA1~CA9 and CB1.

Maximum to 81 LEDs are supported.

Maximum to 21 common anode RGB LEDs are supported.

Maximum to 22 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-4**

Not supported in SLED1732/SLED17321.

◆ **SLED1734/17341 built-in four LED Matrix Types.**

◆ **LED Matrix Type-1**

Achieve 9x8 + 9x8 LED matrix by CA1~CA9 and CB1~CB9.

Maximum to 72+72 LEDs are supported.

Maximum to 18+18 common anode RGB LEDs are supported.

Maximum to 18+18 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-2**

Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.

Maximum to 144 LEDs are supported.

Maximum to 40 common anode RGB LEDs are supported.

Maximum to 41 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-3**

Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8.

Maximum to 256 LEDs are supported.

Maximum to 70 common anode RGB LEDs are supported.

Maximum to 75 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-4**

Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9 and CB1~CB9.

Maximum to 72 LEDs are supported.

Maximum to 24 common anode RGB LEDs are supported.

Maximum to 24 common cathode RGB LEDs are supported.

◆ **SLED1733/17331 built-in four LED Matrix Types.**

◆ **LED Matrix Type-1**

Achieve 9x8+5x4 LED matrix by CA1~CA9 and CB1~CB5.

Maximum to 72+20 LEDs are supported.

Maximum to 18+5 common anode RGB LEDs are supported.

Maximum to 18+5 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-2**

Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.

Maximum to 144 LEDs are supported.

Maximum to 40 common anode RGB LEDs are supported.

Maximum to 41 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-3**

Achieve 13x13 LED matrix by CA1~CA9 and CB1~CB5.

Maximum to 169 LEDs are supported.

Maximum to 44 common anode RGB LEDs are supported.

Maximum to 48 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-4**

Achieve conventional COM x SEG (12x2) LED matrix by CA1~CA9 and CB1~CB5.

Maximum to 24 LEDs are supported.

Common anode RGB LED is not supported.

Maximum to 8 common cathode RGB LEDs are supported

◆ **SLED1735 built-in four LED Matrix Types.**

◆ **LED Matrix Type-1**

Achieve 9x8 + 9x8 LED matrix by CA1~CA9 and CB1~CB9.

Maximum to 72+72 LEDs are supported.

Maximum to 18+18 common anode RGB LEDs are supported.

Maximum to 18+18 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-2**

Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.

Maximum to 144 LEDs are supported.

Maximum to 40 common anode RGB LEDs are supported.

Maximum to 41 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-3**

Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8.

Maximum to 256 LEDs are supported.

Maximum to 70 common anode RGB LEDs are supported.

Maximum to 75 common cathode RGB LEDs are supported.

◆ **LED Matrix Type-4**

Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9, CB1~CB9 and CC1~CC6..

Maximum to 144 LEDs are supported.

Maximum to 48 common anode RGB LEDs are supported.

Maximum to 48 common cathode RGB LEDs are supported.

● **Features Selection Table**

CHIP	RAM	I2C Slave	SPI Slave	MPWM IO	Maximum LED Support				Audio-IN SYNC	Operating Voltage	Package
					Type1	Type2	Type3	Type4			
SLED1732	576*8	V	-	10-ch	72	81	81	-	V	2.7V~5.5V	SOP20
SLED17321	576*8	-	V	10-ch	72	81	81	-	V	2.7V~5.5V	SOP20
SLED1733	576*8	V	-	14-ch	92	144	169	24	V	2.7V~5.5V	SOP24
SLED17331	576*8	-	V	14-ch	92	144	169	24	V	2.7V~5.5V	SOP24
SLED1734	576*8	V	-	18-ch	144	144	256	72	V	2.7V~5.5V	SSOP28/QFN28
SLED17341	576*8	-	V	18-ch	144	144	256	72	V	2.7V~5.5V	SSOP28/QFN28
SLED1735	576*8	V	V	18+6-ch	144	144	256	144	V	2.7V~5.5V	QFN46

1.2 PIN ASSIGNMENT

SLED1732S (SOP 20 pins): I2C Interface

SDB	1	U	20	VDD
SYNC	2		19	CA9
VSS	3		18	CA8
R_EXT	4		17	CA7
CB1	5		16	CA6
AD	6		15	CA5
C_FILT	7		14	CA4
AGCIN	8		13	CA3
SDA	9		12	CA2
SCL	10		11	CA1

SLED1732S

SLED17321S (SOP 20 pins): SPI Interface

SDB	1	U	20	VDD
SYNC	2		19	CA9
VSS	3		18	CA8
CS	4		17	CA7
CB1	5		16	CA6
MISO	6		15	CA5
C_FILT	7		14	CA4
AGCIN	8		13	CA3
MOSI	9		12	CA2
SCK	10		11	CA1

SLED17321S

SLED1733S (SOP 24 pins): I2C Interface

SYNC	1	U	24	SDB
VSS	2		23	VDD
R_EXT	3		22	CA9
CB1	4		21	CA8
CB2	5		20	CA7
CB3	6		19	CA6
CB4	7		18	CA5
CB5	8		17	CA4
C_FILT	9		16	CA3
AGCIN	10		15	CA2
AD	11		14	CA1
SDA	12		13	SCL

SLED1733S

SLED17331S (SOP 24 pins): SPI Interface

SYNC	1	U	24	SDB
VSS	2		23	VDD
CS	3		22	CA9
CB1	4		21	CA8
CB2	5		20	CA7
CB3	6		19	CA6
CB4	7		18	CA5
CB5	8		17	CA4
C_FILT	9		16	CA3
AGCIN	10		15	CA2
MISO	11		14	CA1
MOSI	12		13	SCK

SLED17331S

SLED1734J (QFN 28pins): I2C Interface

CA9	1	•	28	27	25	25	24	23	22	21	CA1
VDD	2									20	SCL
SDB	3									19	SDA
SYNC	4									18	AD
VSS	5									17	AGCIN
R_EXT	6									16	C_FILT
CB1	7									15	CB9
	8	CB2	9	CB3	10	CB4	11	CB5	12	CB6	CB8

SLED1734J

SLED17341J (QFN 28pins): SPI Interface

CA9	1	•	28	27	25	25	24	23	22	21	CA1
VDD	2									20	SCK
SDB	3									19	MOSI
SYNC	4									18	MISO
VSS	5									17	AGCIN
CS	6									16	C_FILT
CB1	7									15	CB9
	8	CB2	9	CB3	10	CB4	11	CB5	12	CB6	CB8

SLED17341J

SLED1734X (SSOP 28pins): I2C Interface

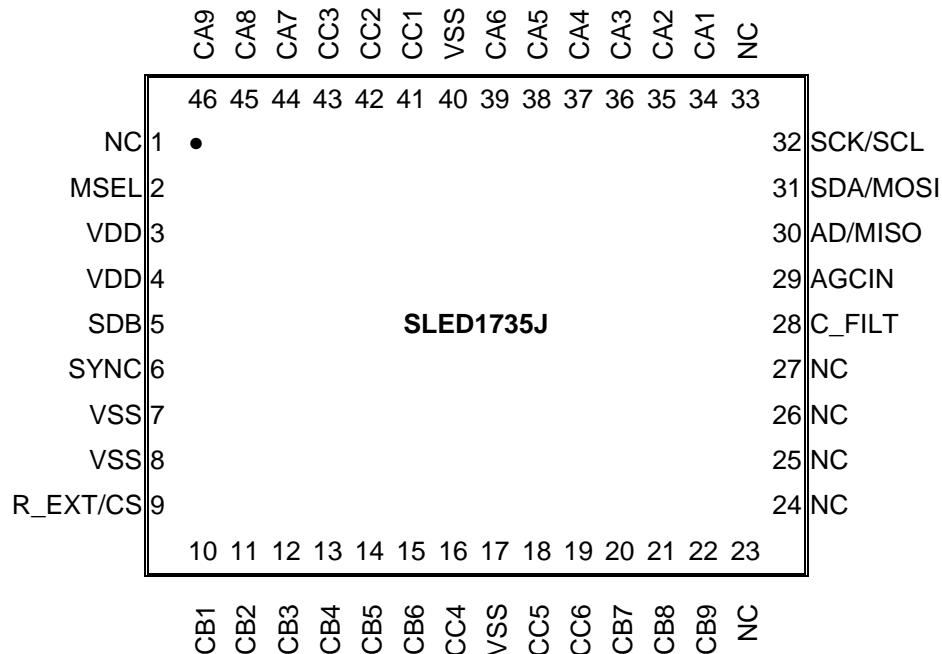
CA9	1	U	28	CA8
VDD	2		27	CA7
SDB	3		26	CA6
SYNC	4		25	CA5
VSS	5		24	CA4
R_EXT	6		23	CA3
CB1	7		22	CA2
CB2	8		21	CA1
CB3	9		20	SCL
CB4	10		19	SDA
CB5	11		18	AD
CB6	12		17	AGCIN
CB7	13		16	C_FILT
CB8	14		15	CB9

SLED1734X

SLED17341X (SSOP 28pins): SPI Interface

CA9	1	U	28	CA8
VDD	2		27	CA7
SDB	3		26	CA6
SYNC	4		25	CA5
VSS	5		24	CA4
CS	6		23	CA3
CB1	7		22	CA2
CB2	8		21	CA1
CB3	9		20	SCK
CB4	10		19	MOSI
CB5	11		18	MISO
CB6	12		17	AGCIN
CB7	13		16	C_FILT
CB8	14		15	CB9

SLED17341X

SLED1735J (QFN 46pins): I2C & SPI Interface


1.3 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	SLED1734X/J : Power supply input pin for digital and analog circuit. SLED17341X/J: Power supply input pin for digital and analog circuit. SLED1735J: Power supply input pins for digital and analog circuit.
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. MSEL = 0 : I2C, pMSEL = 1 : SPI.
SDB	I	Schmitt trigger structure as input mode with internal pull-down resistor. Shutdown the chip when pull to low.
SYNC	I/O	Clock synchronous input or output pin. Schmitt trigger structure as input mode.
R_EXT/CS	I	R_EXT: Input only with internal pull down resistor in I2C mode. No external pull-down resistor is required. CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.
C_FILT	O	Used for filter audio-in noise.
AGCIN	I	Audio-IN Input.
AD/MISO	I/O	AD: I2C slave address selection pin. Schmitt trigger structure as input mode. MISO: SPI Master-Input-Slave-Output pin.
SDA/MOSI	I/O	SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode. MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.
SCL/SCK	I/O	SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode. SCK: SPI Clock input pin. Schmitt trigger structure as input mode.
CA1~CA9	O	PWM IO with sink 320mA and constant current source.
CB1~CB9	O	PWM IO with sink 320mA and constant current source.
CC1~CC6	O	PWM IO with sink 320mA.

2 ARCHITECTURE DESCRIPTOR

2.1 RAM MAPPING FOR MATRIX TYPE 1 & 2 & 4

Frame No.	User Address	<i>Register Segment</i>	Comment
Frame 1	↑ 000H	<i>LED Control Register</i>	18-byte
	... 011H		
	012H		
	...	<i>Blink Control Register</i>	18-byte
	023H		
	024H	<i>PWM Register</i>	144-byte
	...		
	↓ 0B3H		
Frame C	↑ 000H	<i>LED Open Register</i>	18-byte
	... 011H		
	012H		
	...	<i>LED Short Register</i>	18-byte
	023H		
	024H	<i>Current Fine Tune Register</i>	72-byte
	...		
	↓ 06BH		
Frame D	↑ 000H	<i>LED Vaf Register</i>	36-byte
	... 023H		

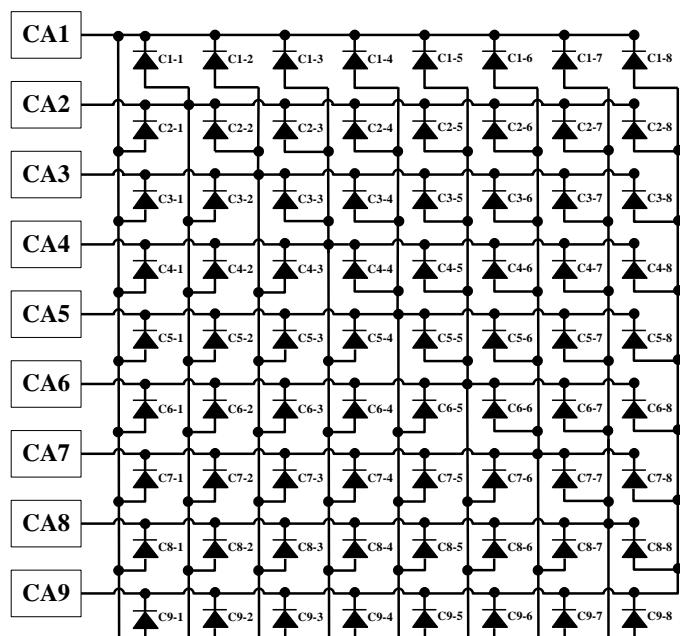
2.2 RAM MAPPING FOR MATRIX TYPE 3

Frame No.	User Address	Register Segment	Comment
Frame 1	↑ 000H	LED Control Register L	16-byte
	... 00FH		
	010H		
	... 01FH	Blink Control Register L	16-byte
	020H		
	... 09FH		
Frame 2	↑ 000H	LED Control Register H	16-byte
	... 00FH		
	010H		
	... 01FH	Blink Control Register H	16-byte
	020H		
	... 09FH		
Frame C	↑ 000H	LED Open Register	32-byte
	... 01FH		
	020H		
	... 03FH	LED Short Register	32-byte
	040H		
	... 0BFH		
Frame D	↑ 000H	Current Fine Tune Register	128-byte
	... 03FH		

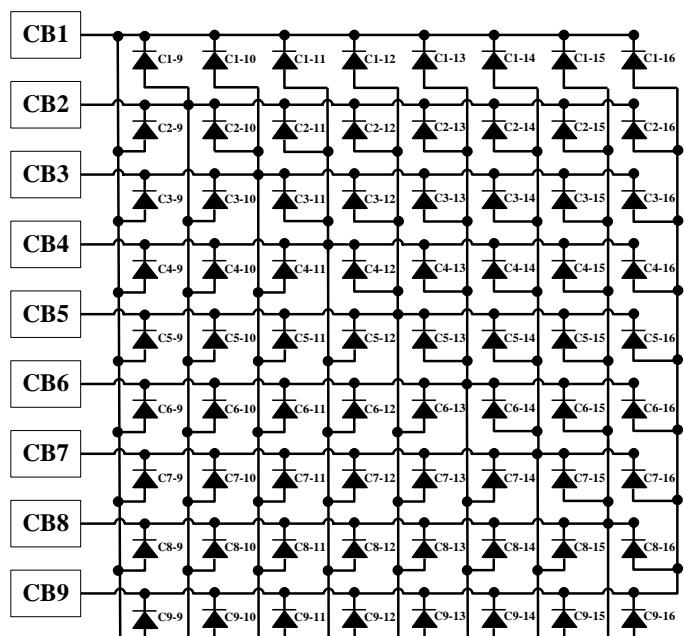
2.3 MATRIX TYPE-1 RAM MAP

Type-1 (9*8 + 9*8)

LED Location	Matrix A	CA1 (C1-1~C1-8)	CA2 (C2-1~C2-8)	CA3 (C3-1~C3-8)	CA4 (C4-1~C4-8)	CA5 (C5-1~C5-8)	CA6 (C6-1~C6-8)	CA7 (C7-1~C7-8)	CA8 (C8-1~C8-8)	CA9 (C9-1~C9-8)
	Matrix B	CB1 (C1-9~C1-16)	CB2 (C2-9~C2-16)	CB3 (C3-9~C3-16)	CB4 (C4-9~C4-16)	CB5 (C5-9~C5-16)	CB6 (C6-9~C6-16)	CB7 (C7-9~C7-16)	CB8 (C8-9~C8-16)	CB9 (C9-9~C9-16)
Frame 1										
LED Control Register	Matrix A	00h	02h	04h	06h	08h	0Ah	0Ch	0Eh	10h
	Matrix B	01h	03h	05h	07h	09h	0Bh	0Dh	0Fh	11h
Blink Control Register	Matrix A	12h	14h	16h	18h	1Ah	1Ch	1Eh	20h	22h
	Matrix B	13h	15h	17h	19h	1Bh	1Dh	1Fh	21h	23h
PWM Register	Matrix A	24h~2Bh	34h~3Bh	44h~4Bh	54h~5Bh	64h~6Bh	74h~7Bh	84h~8Bh	94h~9Bh	A4h~ABh
	Matrix B	2Ch~33h	3Ch~43h	4Ch~53h	5Ch~63h	6Ch~73h	7Ch~84h	8Ch~93h	9Ch~A3h	ACh~B3h
Frame C										
LED Open Register	Matrix A	00h	02h	04h	06h	08h	0Ah	0Ch	0Eh	10h
	Matrix B	01h	03h	05h	07h	09h	0Bh	0Dh	0Fh	11h
LED Short Register	Matrix A	12h	14h	16h	18h	1Ah	1Ch	1Eh	20h	22h
	Matrix B	13h	15h	17h	19h	1Bh	1Dh	1Fh	21h	23h
Current Fine Tune Register	Matrix A	24h~27h	2Ch~2Fh	34h~37h	3Ch~3Fh	44h~47h	4Ch~4Fh	54h~57h	5Ch~5Fh	64h~67h
	Matrix B	28h~2Bh	30h~33h	38h~3Bh	40h~43h	48h~4Bh	50h~53h	58h~5Bh	60h~63h	68h~6Bh
Frame D										
LED Vaf Register	Matrix A	00h~01h	04h~05h	08h~09h	0Ch~0Dh	10h~11h	14h~15h	18h~19h	1Ch~1Dh	20h~21h
	Matrix B	02h~03h	06h~07h	0Ah~0Bh	0Eh~0Fh	12h~13h	16h~17h	1Ah~1Bh	1Eh~1Fh	22h~23h



Type-1: Matrix A (9*8)

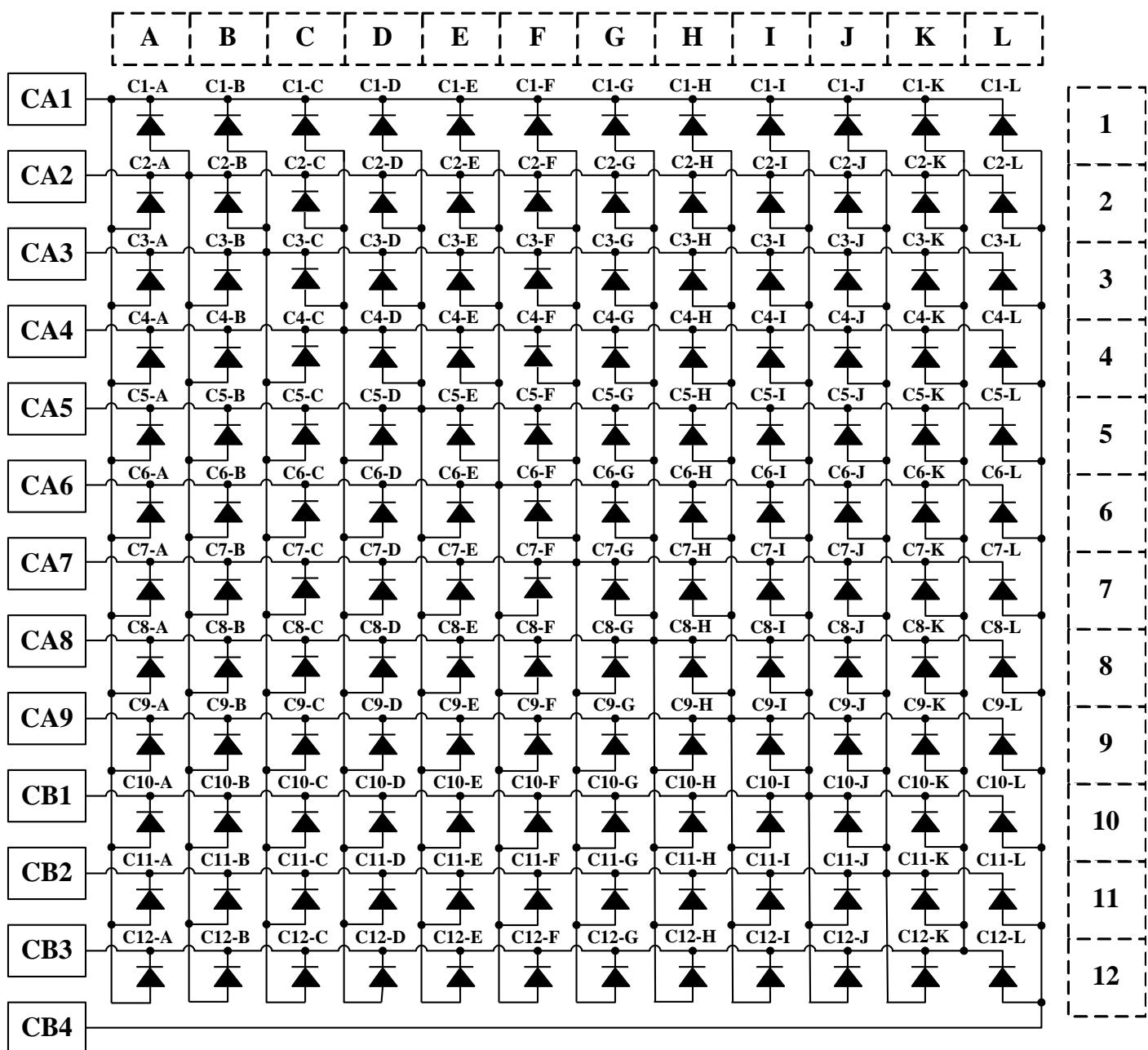


Type-1: Matrix B (9*8)

2.4 MATRIX TYPE-2 RAM MAP

Type-2 (12*12)

LED Location	Frame 1			Frame C		
	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA1(C1-A~C1-L)	00h + 01h[3:0]	12h + 13h[3:0]	24h~2Fh	00h + 01h[3:0]	12h + 13h[3:0]	24h~29h
CA2(C2-A~C2-L)	01h[7:4] + 02h	13h[7:4] + 14h	30h~3Bh	01h[7:4] + 02h	13h[7:4] + 14h	2Ah~2Fh
CA3(C3-A~C3-L)	03h + 04h[3:0]	15h + 16h[3:0]	3Ch~47h	03h + 04h[3:0]	15h + 16h[3:0]	30h~35h
CA4(C4-A~C4-L)	04h[7:4] + 05h	16h[7:4] + 17h	48h~53h	04h[7:4] + 05h	16h[7:4] + 17h	36h~3Bh
CA5(C5-A~C5-L)	06h + 07h[3:0]	18h + 19h[3:0]	54h~5Fh	06h + 07h[3:0]	18h + 19h[3:0]	3Ch~41h
CA6(C6-A~C6-L)	07h[7:4] + 08h	19h[7:4] + 1Ah	60h~6Bh	07h[7:4] + 08h	19h[7:4] + 1Ah	42h~47h
CA7(C7-A~C7-L)	09h + 0Ah[3:0]	1Bh + 1Ch[3:0]	6Ch~77h	09h + 0Ah[3:0]	1Bh + 1Ch[3:0]	48h~4Dh
CA8(C8-A~C8-L)	0Ah[7:4] + 0Bh	1Ch[7:4] + 1Dh	78h~83h	0Ah[7:4] + 0Bh	1Ch[7:4] + 1Dh	4Eh~53h
CA9(C9-A~C9-L)	0Ch + 0Dh[3:0]	1Eh + 1Fh[3:0]	84h~8Fh	0Ch + 0Dh[3:0]	1Eh + 1Fh[3:0]	54h~59h
CB1(C10-A~C10-L)	0Dh[7:4] + 0Eh	1Fh[7:4] + 20h	90h~9Bh	0Dh[7:4] + 0Eh	1Fh[7:4] + 20h	5Ah~5Fh
CB2(C11-A~C11-L)	0Fh + 10h[3:0]	21h + 22h[3:0]	9Ch~A7h	0Fh + 10h[3:0]	21h + 22h[3:0]	60h~65h
CB3(C12-A~C12-L)	10h[7:4] + 11h	22h[7:4] + 23h	A8h~B3h	10h[7:4] + 11h	22h[7:4] + 23h	66h~6Bh
Frame D						
LED Location	LED Vaf Register					
CA1(C1-A~C1-L)	00h~02h					
CA2(C2-A~C2-L)	03h~05h					
CA3(C3-A~C3-L)	06h~08h					
CA4(C4-A~C4-L)	09h~0Bh					
CA5(C5-A~C5-L)	0Ch~0Eh					
CA6(C6-A~C6-L)	0Fh~11h					
CA7(C7-A~C7-L)	12h~14h					
CA8(C8-A~C8-L)	15h~17h					
CA9(C9-A~C9-L)	18h~1Ah					
CB1(C10-A~C10-L)	1Bh~1Dh					
CB2(C11-A~C11-L)	1Eh~20h					
CB3(C12-A~C12-L)	21h~23h					

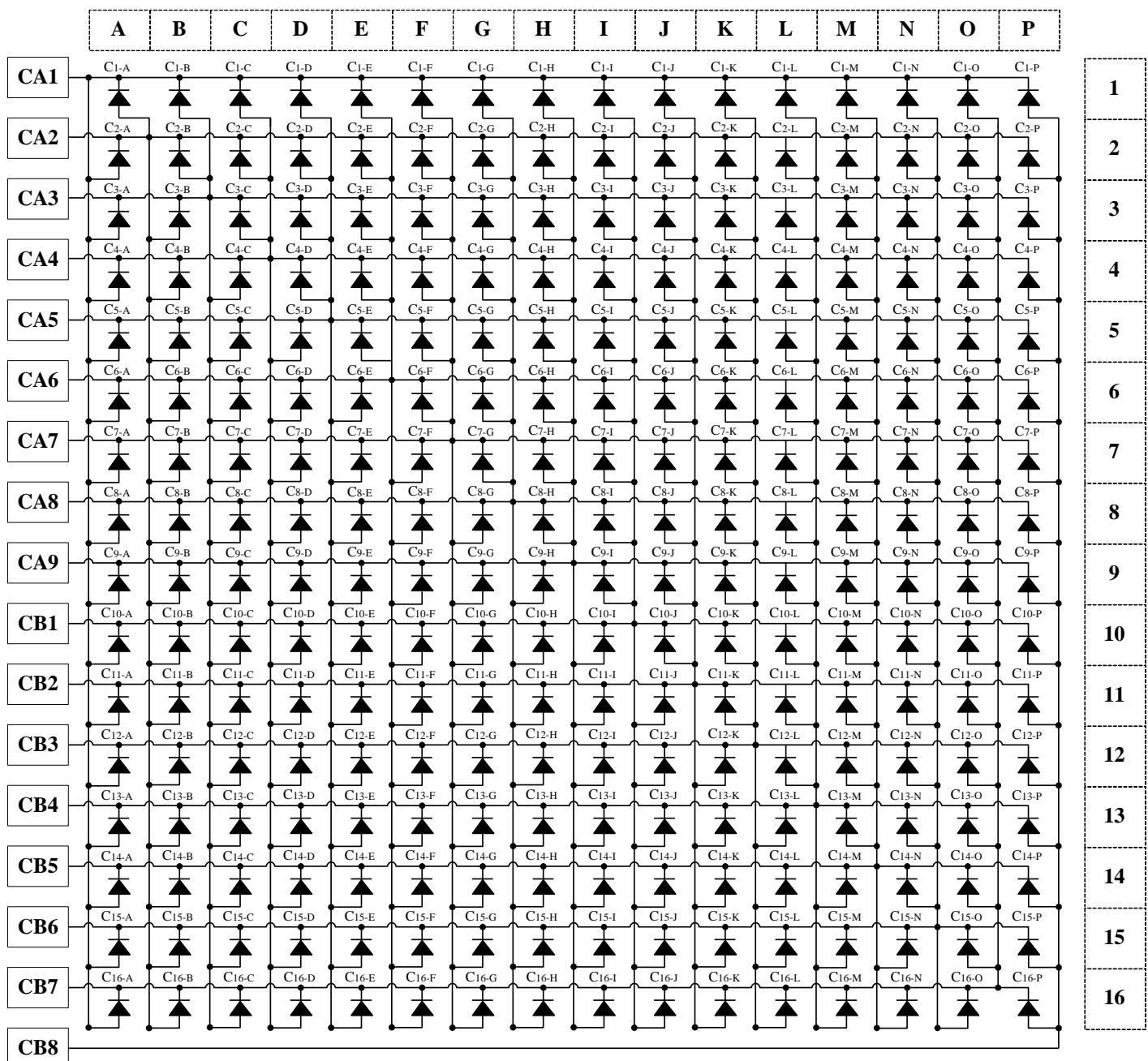


Type-2: 12*12

2.5 MATRIX TYPE-3 RAM MAP

Type-3 (16*16)

	Frame 1			Frame C		
LED Location	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA1(C1-A~C1-P)	00h~01h	10h~11h	20h~2Fh	00h~01h	20h~21h	40h~47h
CA2(C2-A~C2-P)	02h~03h	12h~13h	30h~3Fh	02h~03h	22h~23h	48h~4Fh
CA3(C3-A~C3-P)	04h~05h	14h~15h	40h~4Fh	04h~05h	24h~25h	50h~57h
CA4(C4-A~C4-P)	06h~07h	16h~17h	50h~5Fh	06h~07h	26h~27h	58h~5Fh
CA5(C5-A~C5-P)	08h~09h	18h~19h	60h~6Fh	08h~09h	28h~29h	60h~67h
CA6(C6-A~C6-P)	0Ah~0Bh	1Ah~1Bh	70h~7Fh	0Ah~0Bh	2Ah~2Bh	68h~6Fh
CA7(C7-A~C7-P)	0Ch~0Dh	1Ch~1Dh	80h~8Fh	0Ch~0Dh	2Ch~2Dh	70h~77h
CA8(C8-A~C8-P)	0Eh~0Fh	1Eh~1Fh	90h~9Fh	0Eh~0Fh	2Eh~2Fh	78h~7Fh
	Frame 2			Frame C		
LED Location	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA9(C9-A~C9-P)	00h~01h	10h~11h	20h~2Fh	10h~11h	30h~31h	80h~87h
CB1(C10-A~C10-P)	02h~03h	12h~13h	30h~3Fh	12h~13h	32h~33h	88h~8Fh
CB2(C11-A~C11-P)	04h~05h	14h~15h	40h~4Fh	14h~15h	34h~35h	90h~97h
CB3(C12-A~C12-P)	06h~07h	16h~17h	50h~5Fh	16h~17h	36h~37h	98h~9Fh
CB4(C13-A~C13-P)	08h~09h	18h~19h	60h~6Fh	18h~19h	38h~39h	A0h~A7h
CB5(C14-A~C14-P)	0Ah~0Bh	1Ah~1Bh	70h~7Fh	1Ah~1Bh	3Ah~3Bh	A8h~AFh
CB6(C15-A~C15-P)	0Ch~0Dh	1Ch~1Dh	80h~8Fh	1Ch~1Dh	3Ch~3Dh	B0h~B7h
CB7(C16-A~C16-P)	0Eh~0Fh	1Eh~1Fh	90h~9Fh	1Eh~1Fh	3Eh~3Fh	B8h~BFh
	Frame D					
LED Location	LED Vaf Register					
CA1(C1-A~C1-P)	00h~03h					
CA2(C2-A~C2-P)	04h~07h					
CA3(C3-A~C3-P)	08h~0Bh					
CA4(C4-A~C4-P)	0Ch~0Fh					
CA5(C5-A~C5-P)	10h~13h					
CA6(C6-A~C6-P)	14h~17h					
CA7(C7-A~C7-P)	18h~1Bh					
CA8(C8-A~C8-P)	1Ch~1Fh					
CA9(C9-A~C9-P)	20h~23h					
CB1(C10-A~C10-P)	24h~27h					
CB2(C11-A~C11-P)	28h~2Bh					
CB3(C12-A~C12-P)	2Ch~2Fh					
CB4(C13-A~C13-P)	30h~33h					
CB5(C14-A~C14-P)	34h~37h					
CB6(C15-A~C15-P)	38h~3Bh					
CB7(C16-A~C16-P)	3Ch~3Fh					

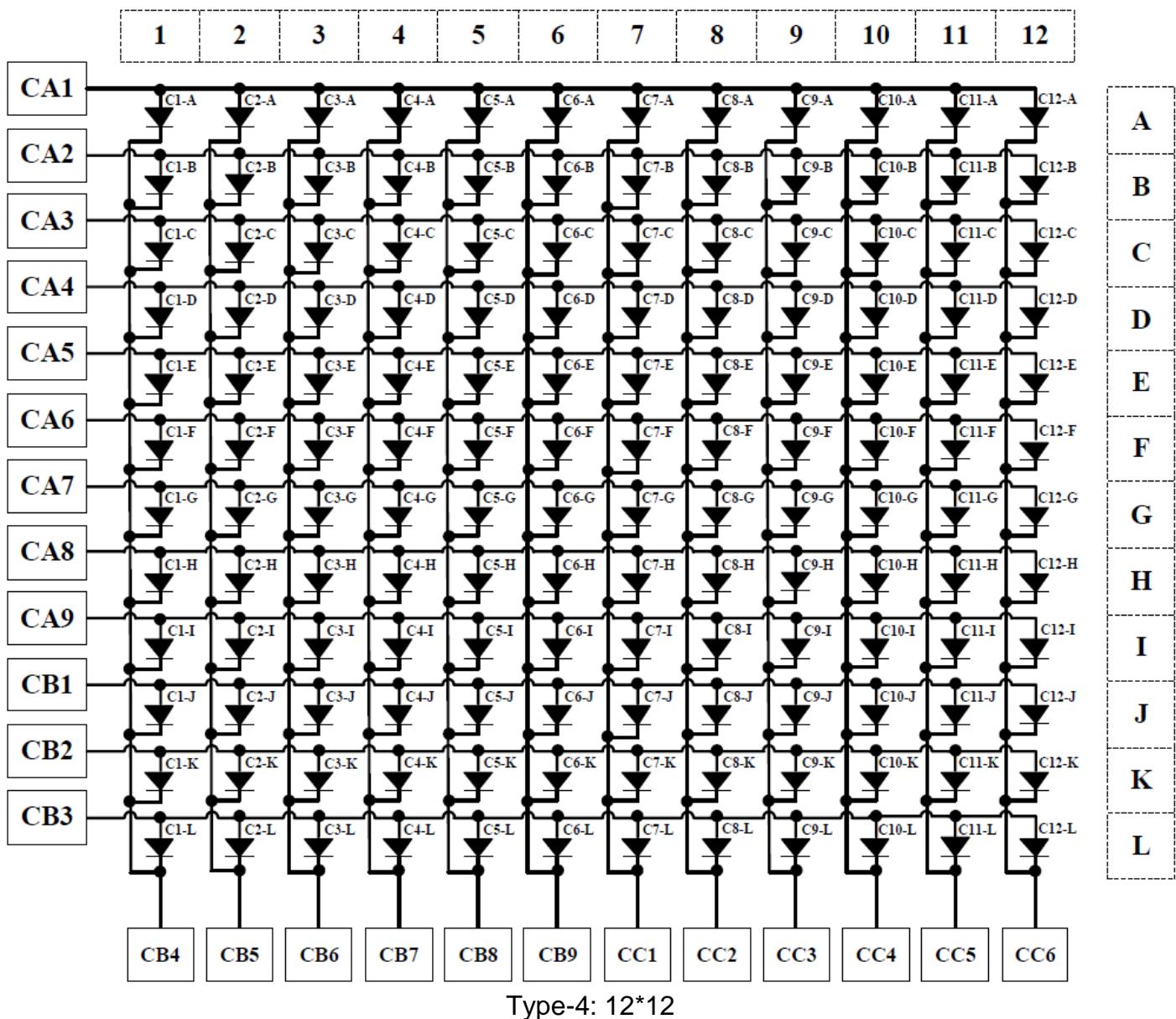


Type-3: 16*16

2.6 MATRIX TYPE-4 RAM MAP

Type-4 (12*12)

LED Location	Frame 1			Frame C		
	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA1(C1-A~C1-L)	00h + 01h[3:0]	12h + 13h[3:0]	24h~2Fh	00h + 01h[3:0]	12h + 13h[3:0]	24h~29h
CA2(C2-A~C2-L)	01h[7:4] + 02h	13h[7:4] + 14h	30h~3Bh	01h[7:4] + 02h	13h[7:4] + 14h	2Ah~2Fh
CA3(C3-A~C3-L)	03h + 04h[3:0]	15h + 16h[3:0]	3Ch~47h	03h + 04h[3:0]	15h + 16h[3:0]	30h~35h
CA4(C4-A~C4-L)	04h[7:4] + 05h	16h[7:4] + 17h	48h~53h	04h[7:4] + 05h	16h[7:4] + 17h	36h~3Bh
CA5(C5-A~C5-L)	06h + 07h[3:0]	18h + 19h[3:0]	54h~5Fh	06h + 07h[3:0]	18h + 19h[3:0]	3Ch~41h
CA6(C6-A~C6-L)	07h[7:4] + 08h	19h[7:4] + 1Ah	60h~6Bh	07h[7:4] + 08h	19h[7:4] + 1Ah	42h~47h
CA7(C7-A~C7-L)	09h + 0Ah[3:0]	1Bh + 1Ch[3:0]	6Ch~77h	09h + 0Ah[3:0]	1Bh + 1Ch[3:0]	48h~4Dh
CA8(C8-A~C8-L)	0Ah[7:4] + 0Bh	1Ch[7:4] + 1Dh	78h~83h	0Ah[7:4] + 0Bh	1Ch[7:4] + 1Dh	4Eh~53h
CA9(C9-A~C9-L)	0Ch + 0Dh[3:0]	1Eh + 1Fh[3:0]	84h~8Fh	0Ch + 0Dh[3:0]	1Eh + 1Fh[3:0]	54h~59h
CB1(C10-A~C10-L)	0Dh[7:4] + 0Eh	1Fh[7:4] + 20h	90h~9Bh	0Dh[7:4] + 0Eh	1Fh[7:4] + 20h	5Ah~5Fh
CB2(C11-A~C11-L)	0Fh + 10h[3:0]	21h + 22h[3:0]	9Ch~A7h	0Fh + 10h[3:0]	21h + 22h[3:0]	60h~65h
CB3(C12-A~C12-L)	10h[7:4] + 11h	22h[7:4] + 23h	A8h~B3h	10h[7:4] + 11h	22h[7:4] + 23h	66h~6Bh
Frame D						
LED Location	LED Vaf Register					
CA1(C1-A~C1-L)	00h~02h					
CA2(C2-A~C2-L)	03h~05h					
CA3(C3-A~C3-L)	06h~08h					
CA4(C4-A~C4-L)	09h~0Bh					
CA5(C5-A~C5-L)	0Ch~0Eh					
CA6(C6-A~C6-L)	0Fh~11h					
CA7(C7-A~C7-L)	12h~14h					
CA8(C8-A~C8-L)	15h~17h					
CA9(C9-A~C9-L)	18h~1Ah					
CB1(C10-A~C10-L)	1Bh~1Dh					
CB2(C11-A~C11-L)	1Eh~20h					
CB3(C12-A~C12-L)	21h~23h					

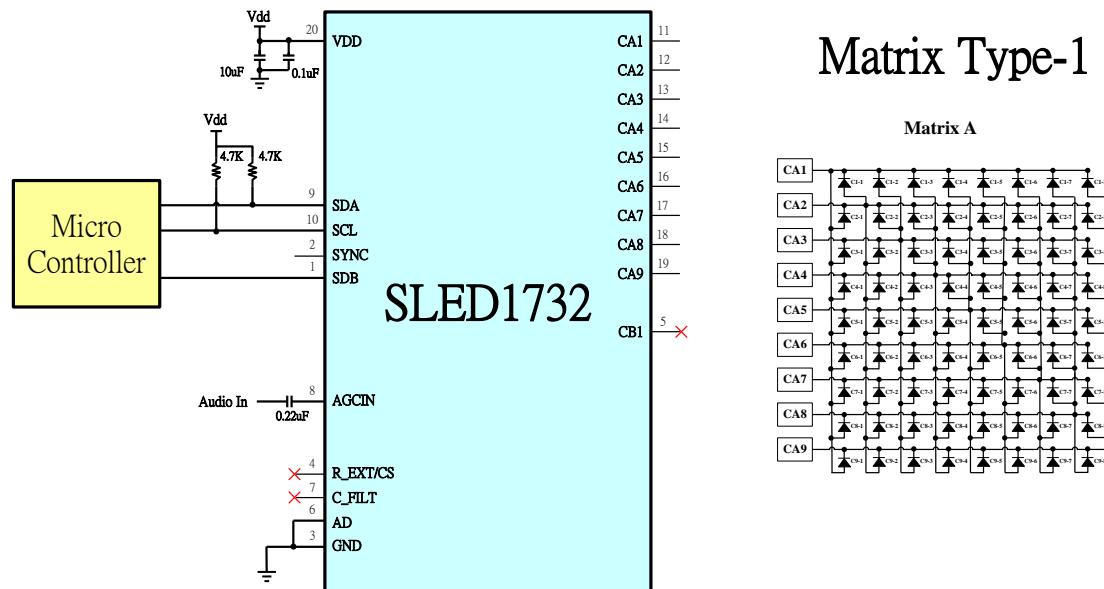


Type-4: 12*12

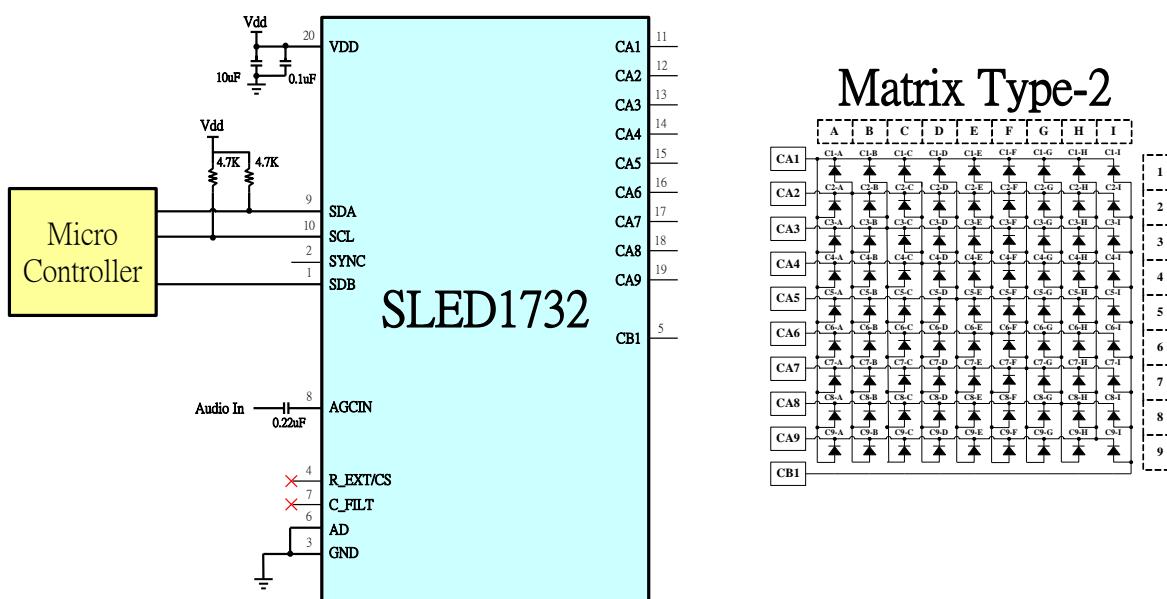
3 APPLICATION CIRCUIT

3.1 SLED1732/17321 INTERFACE WITH LED MATRIX

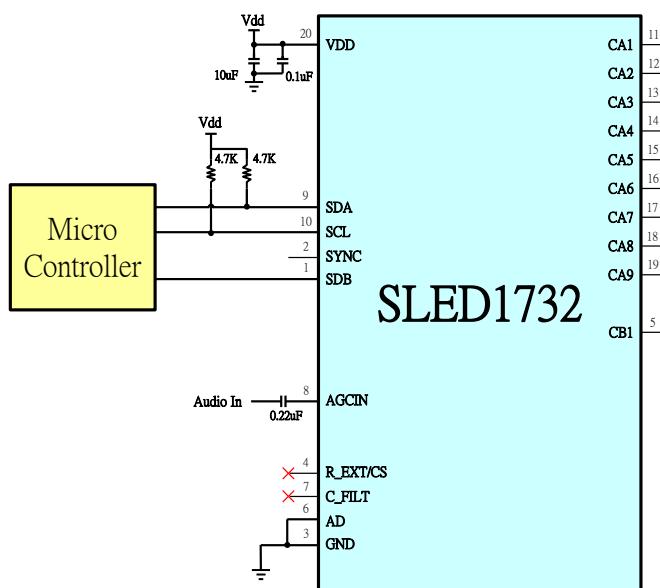
3.1.1 SLED1732 I2C INTERFACE WITH LED MATRIX TYPE-1



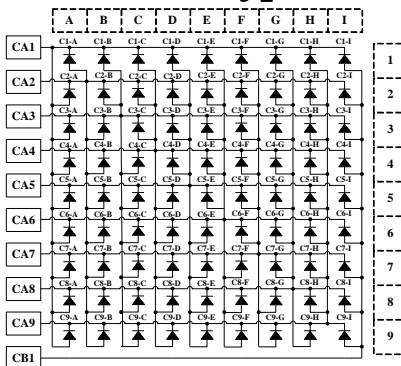
3.1.2 SLED1732 I2C INTERFACE WITH LED MATRIX TYPE-2



3.1.3 SLED1732 I2C INTERFACE WITH LED MATRIX TYPE-3



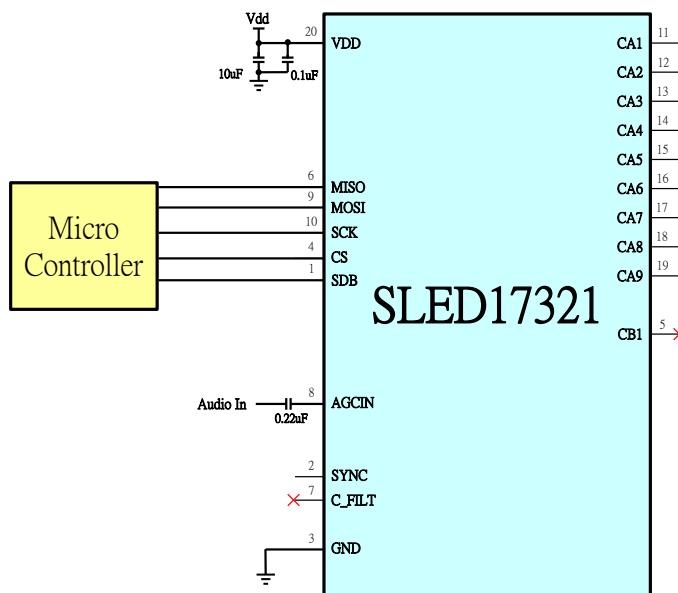
Matrix Type-3



3.1.4 SLED1732 I2C INTERFACE WITH LED MATRIX TYPE-4

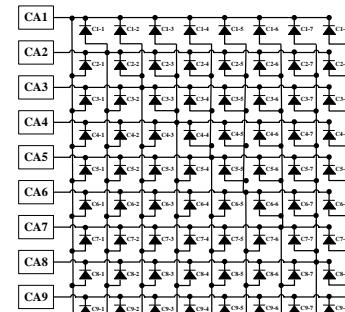
Matrix Type-4 is not supported.

3.1.5 SLED17321 SPI INTERFACE WITH LED MATRIX TYPE-1

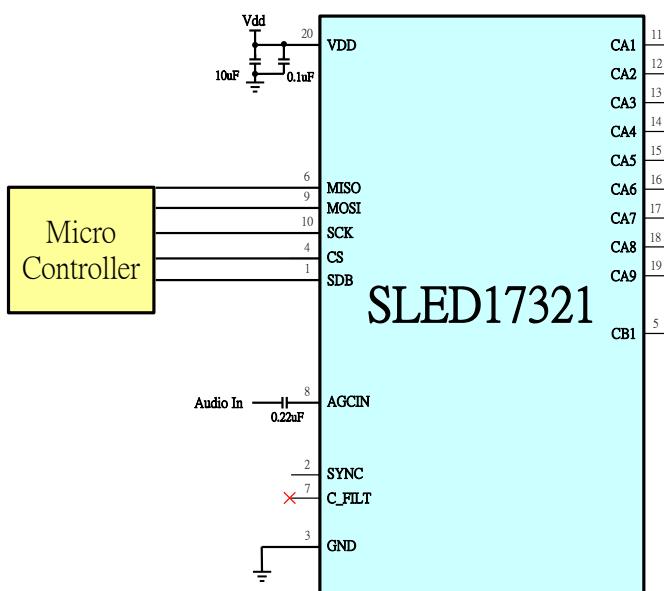


Matrix Type-1

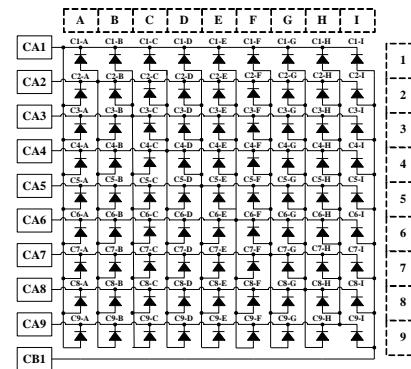
Matrix A



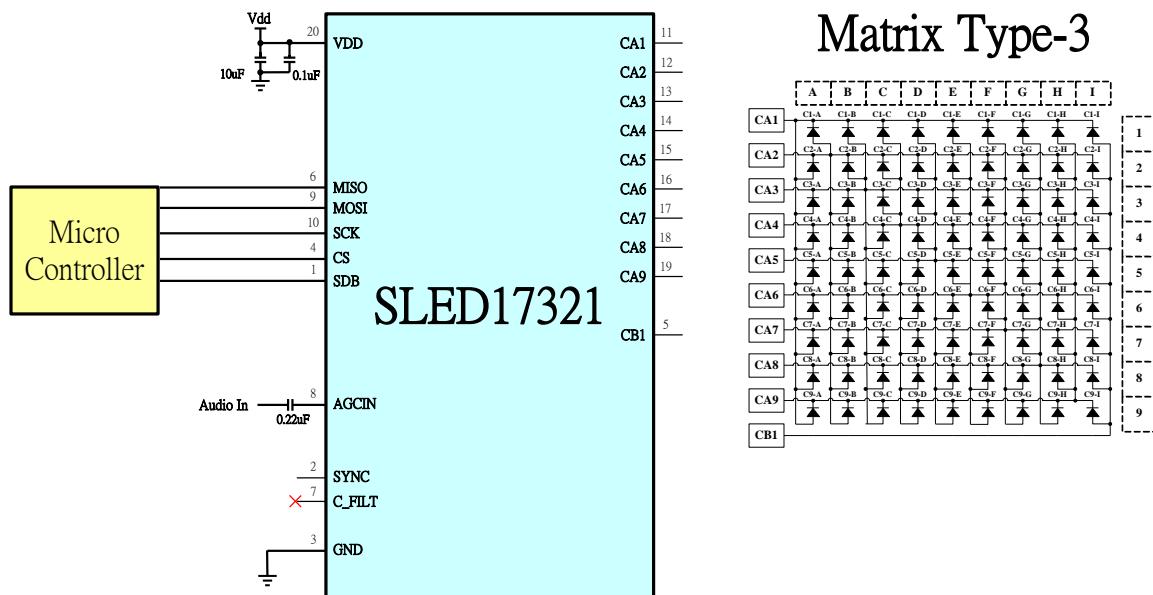
3.1.6 SLED17321 SPI INTERFACE WITH LED MATRIX TYPE-2



Matrix Type-2



3.1.7 SLED17321 SPI INTERFACE WITH LED MATRIX TYPE-3

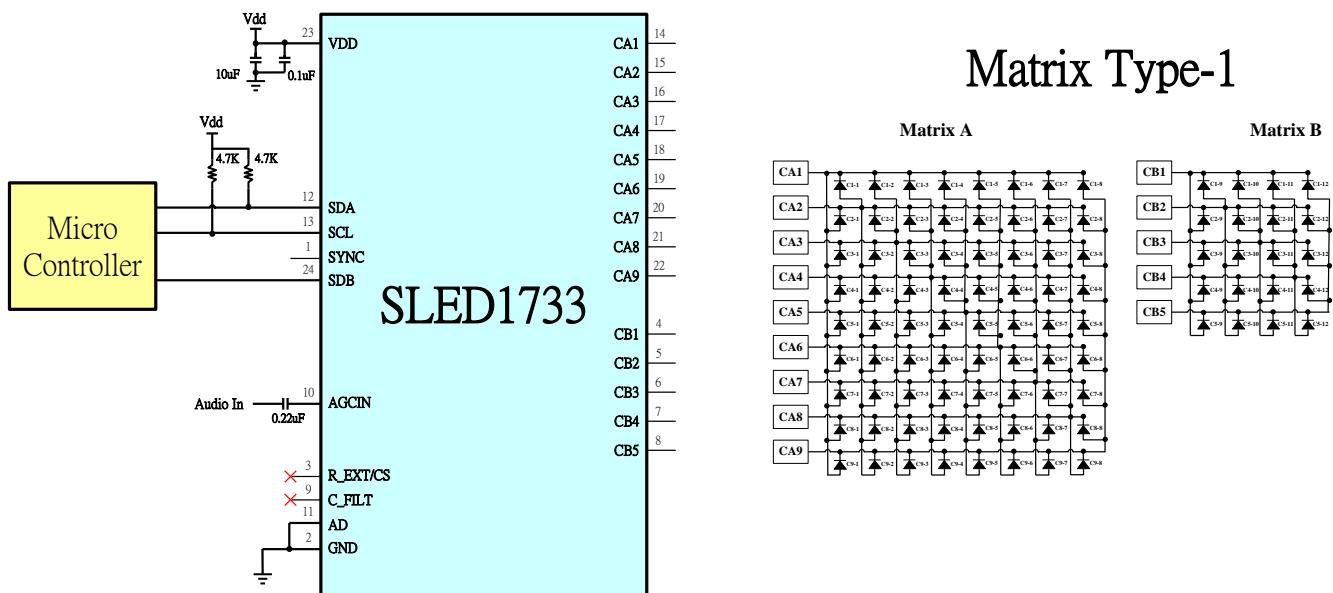


3.1.8 SLED17321 SPI INTERFACE WITH LED MATRIX TYPE-4

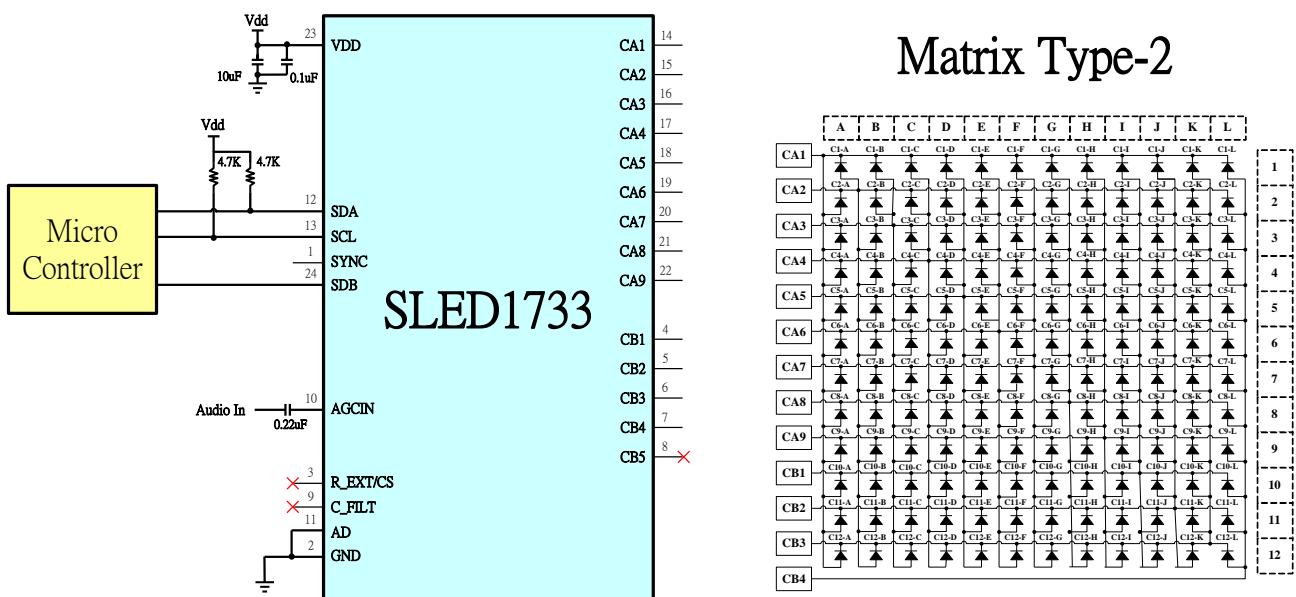
Matrix Type-4 is not supported.

3.2 LED1733/17331 INTERFACE WITH LED MATRIX

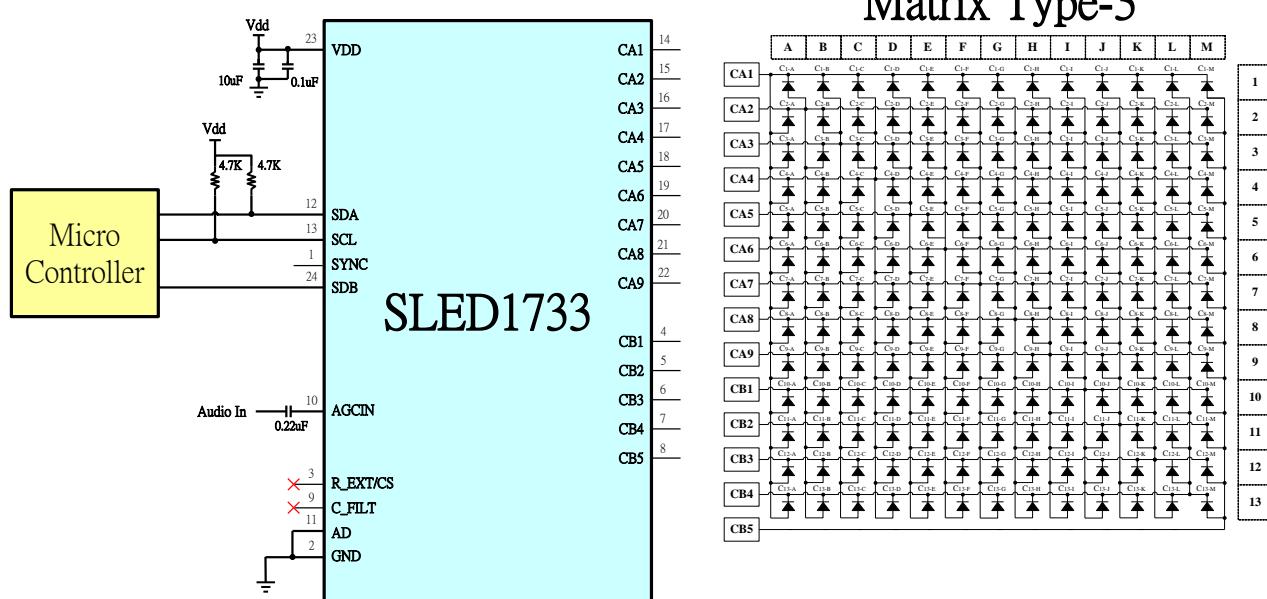
3.2.1 SLED1733 I2C INTERFACE WITH LED MATRIX TYPE-1



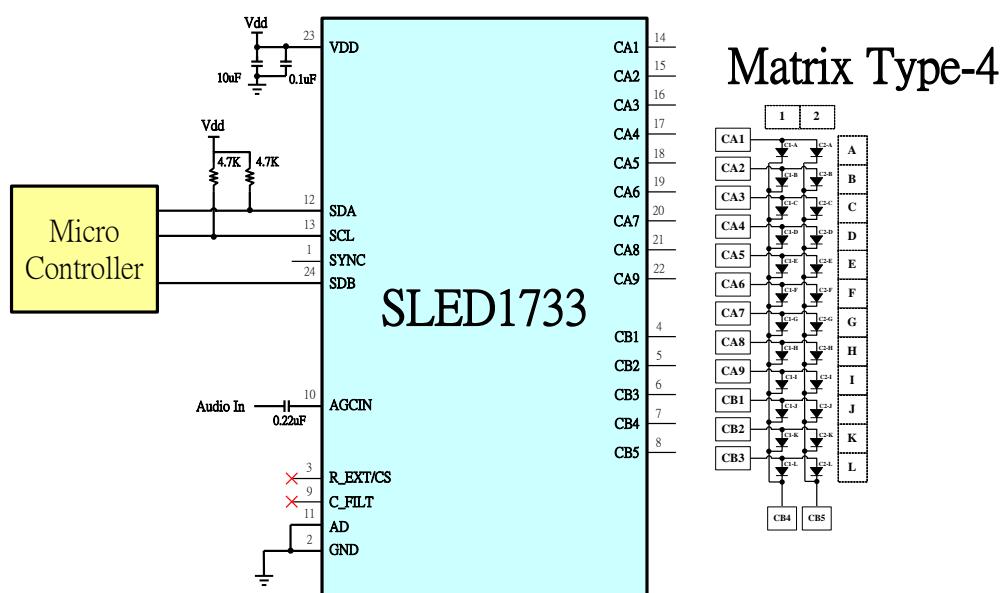
3.2.2 SLED1733 I2C INTERFACE WITH LED MATRIX TYPE-2



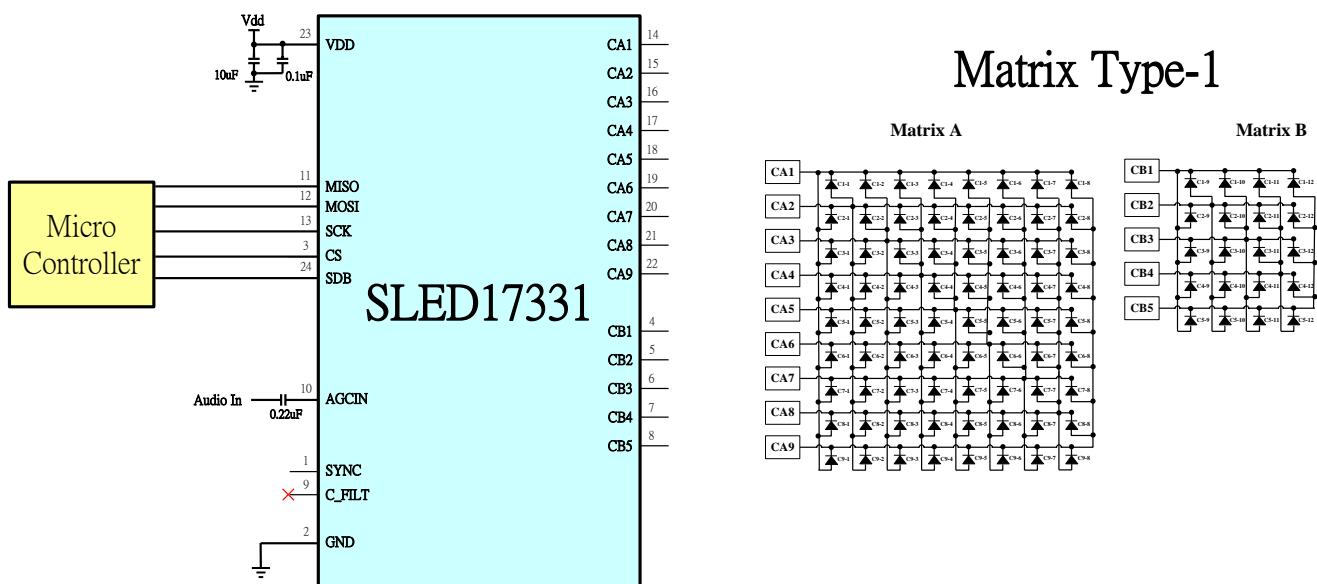
3.2.3 SLED1733 I2C INTERFACE WITH LED MATRIX TYPE-3



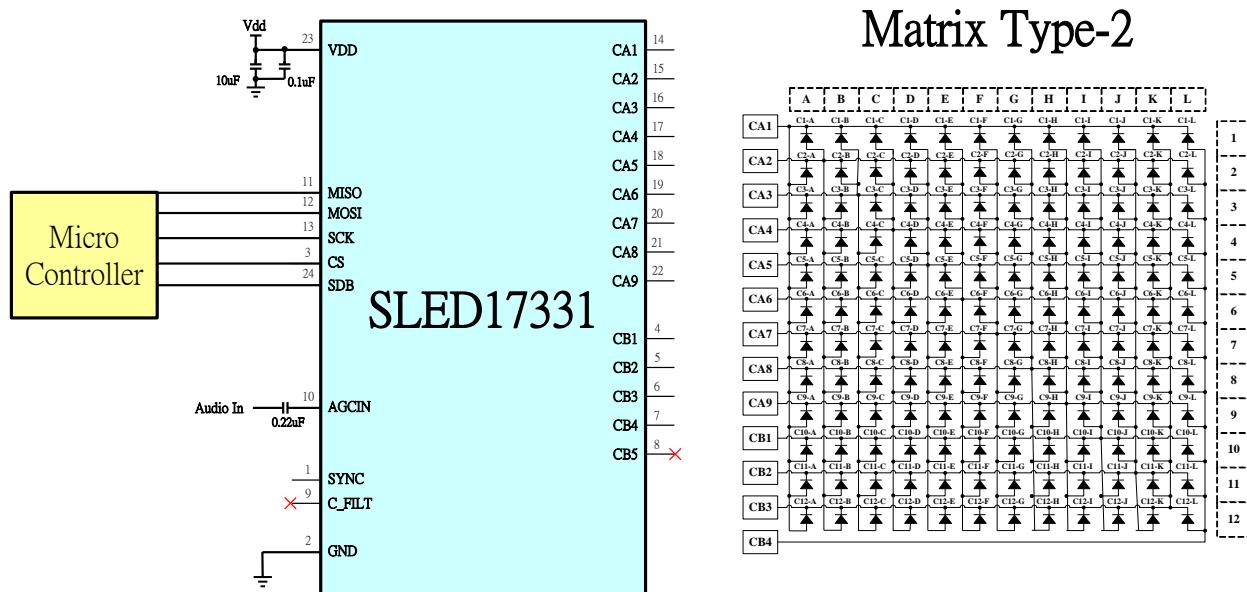
3.2.4 SLED1733 I2C INTERFACE WITH LED MATRIX TYPE-4



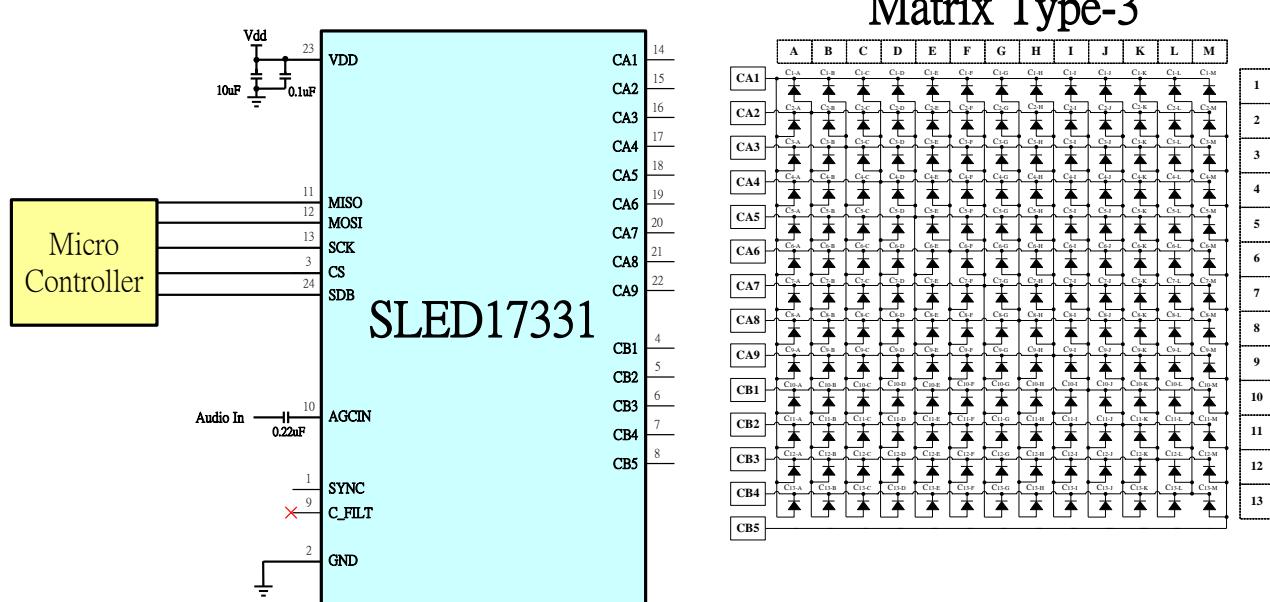
3.2.5 SLED17331 SPI INTERFACE WITH LED MATRIX TYPE-1



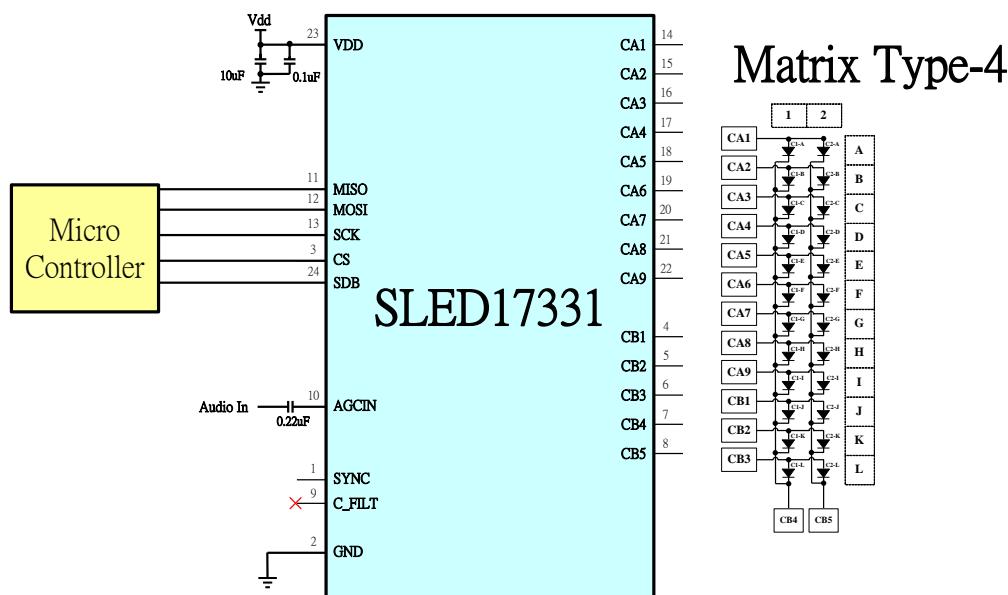
3.2.6 SLED17331 SPI INTERFACE WITH LED MATRIX TYPE-2



3.2.7 SLED17331 SPI INTERFACE WITH LED MATRIX TYPE-3

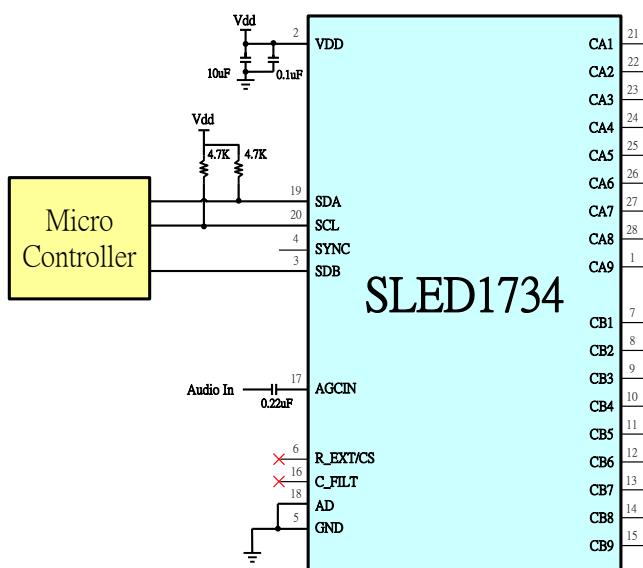


3.2.8 SLED17331 SPI INTERFACE WITH LED MATRIX TYPE-4

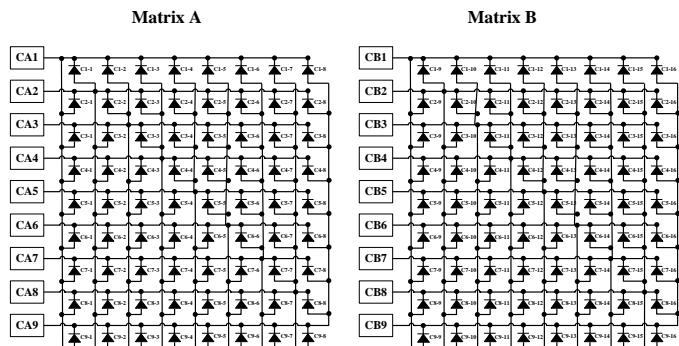


3.3 SLED1734/17341 INTERFACE WITH LED MATRIX

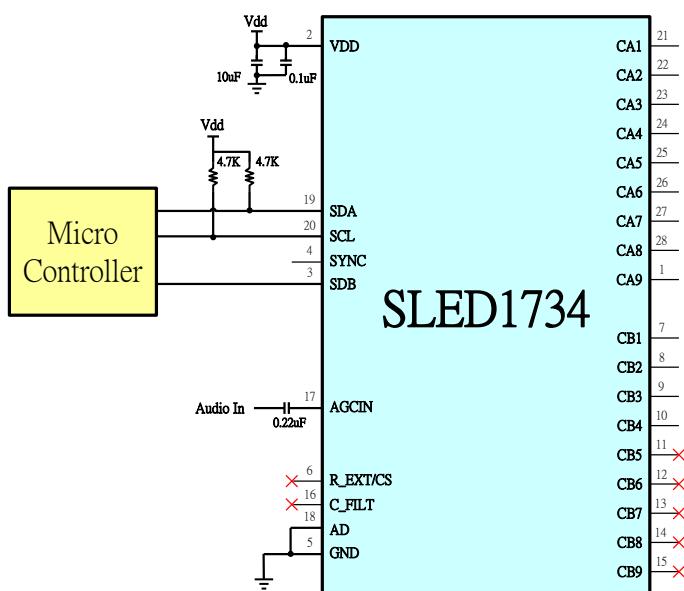
3.3.1 SLED1734 I2C INTERFACE WITH LED MATRIX TYPE-1



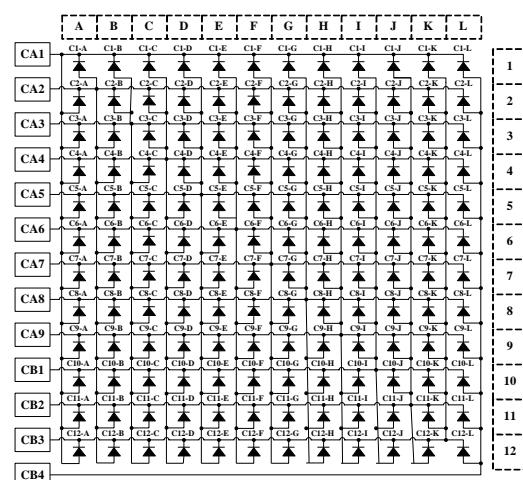
Matrix Type-1



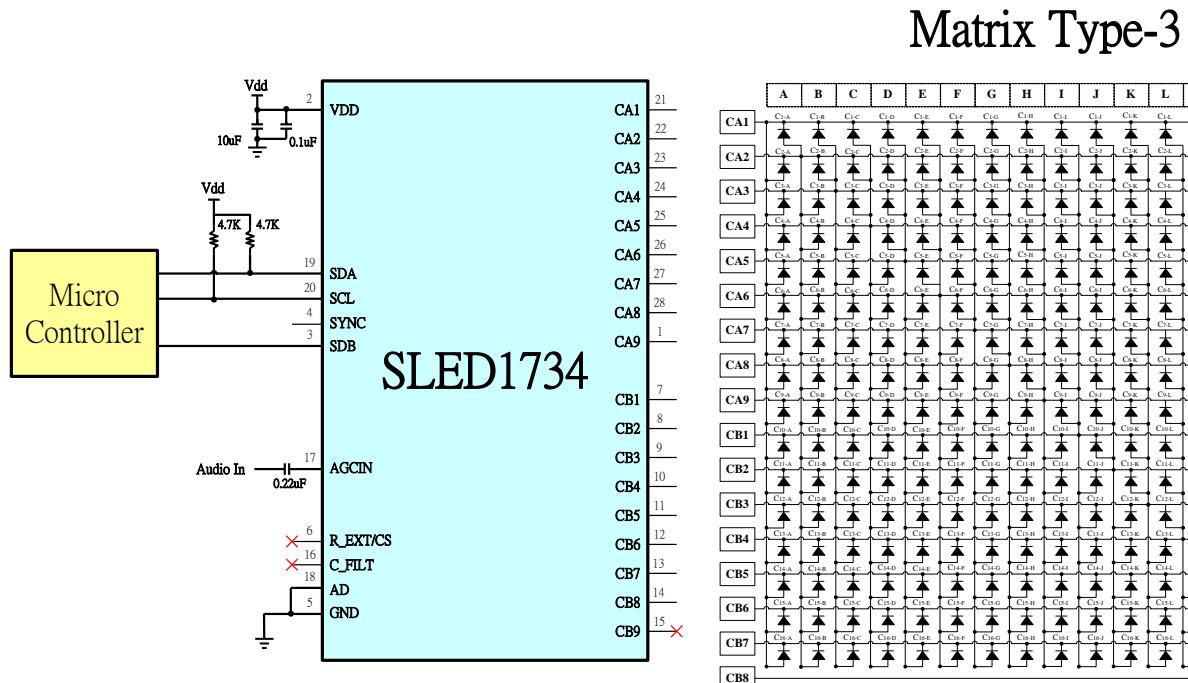
3.3.2 SLED1734 I2C INTERFACE WITH LED MATRIX TYPE-2



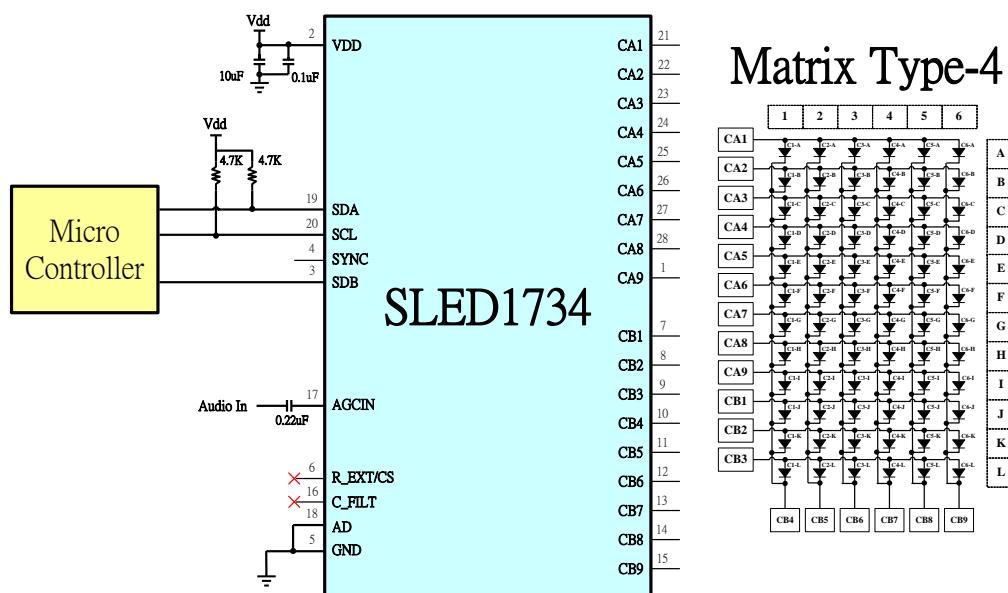
Matrix Type-2



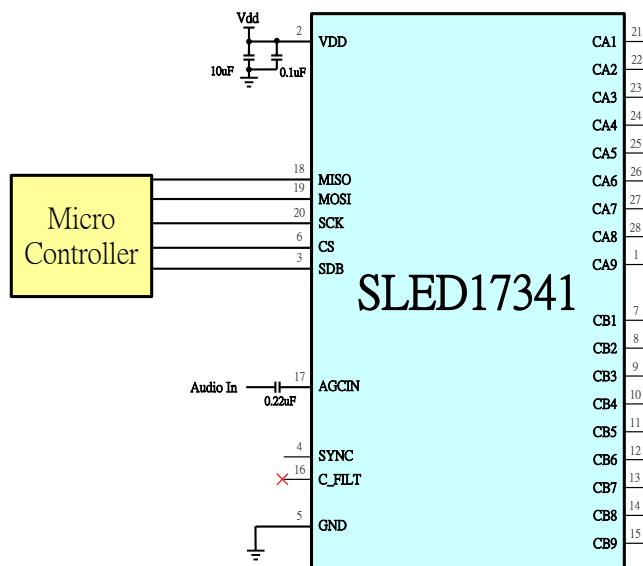
3.3.3 SLED1734 I2C INTERFACE WITH LED MATRIX TYPE-3



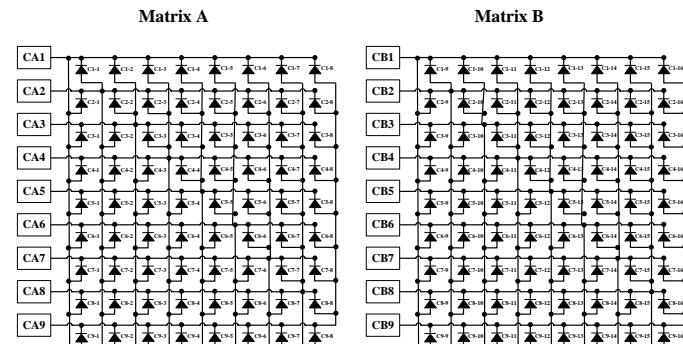
3.3.4 SLED1734 I2C INTERFACE WITH LED MATRIX TYPE-4



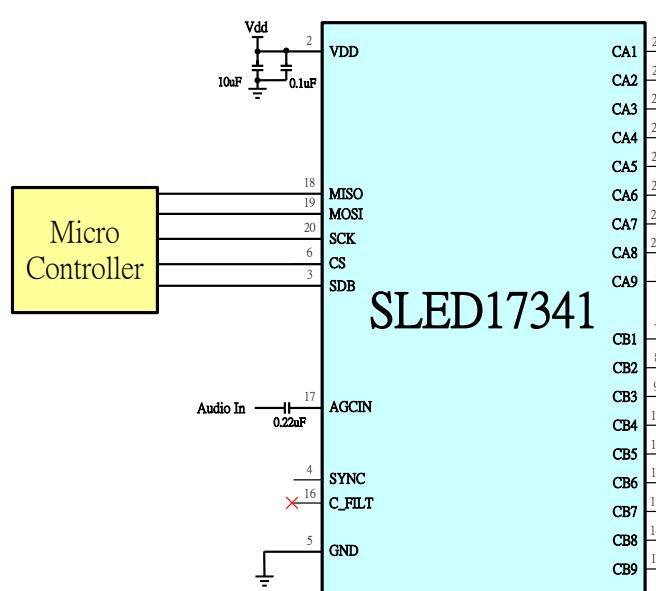
3.3.5 SLED17341 SPI INTERFACE WITH LED MATRIX TYPE-1



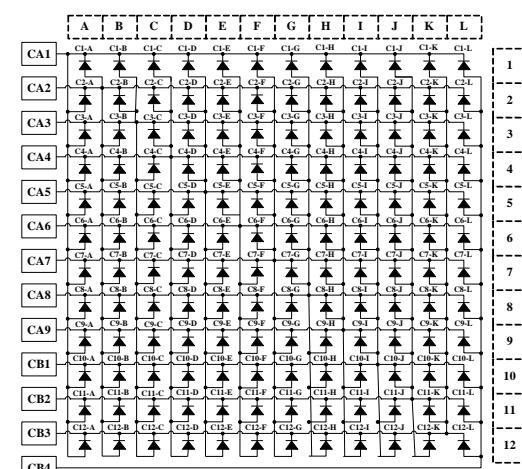
Matrix Type-1



3.3.6 SLED17341 SPI INTERFACE WITH LED MATRIX TYPE-2

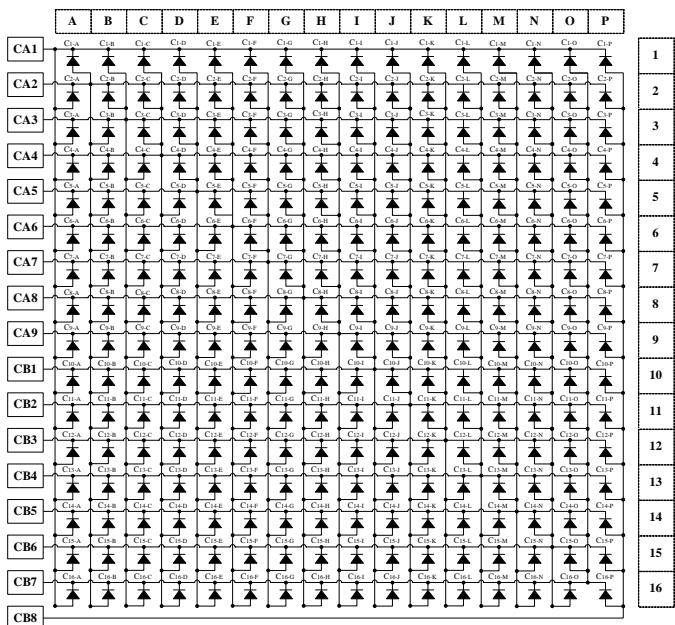
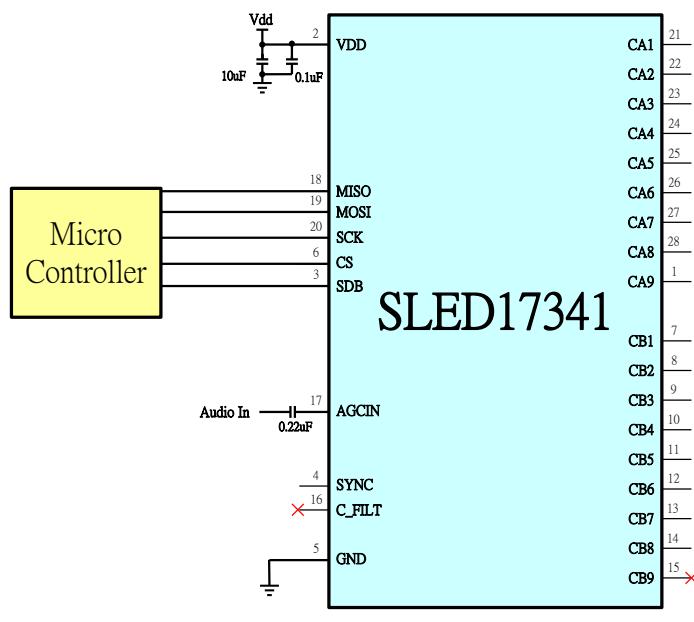


Matrix Type-2

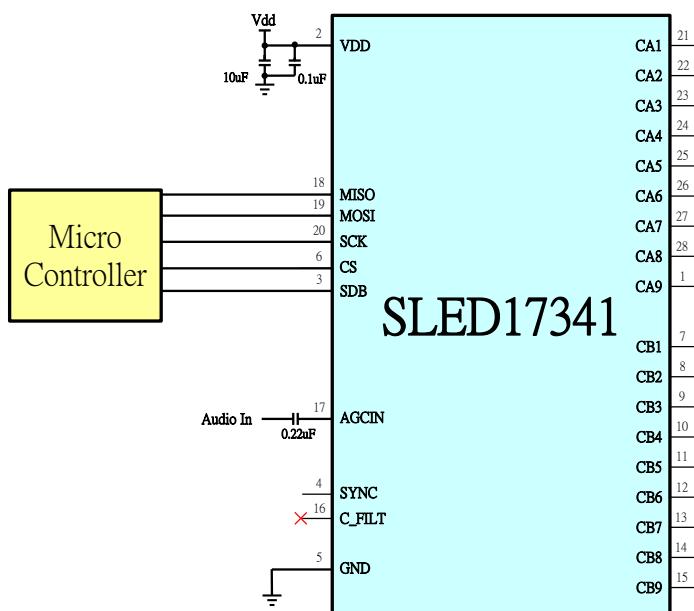


3.3.7 SLED17341 SPI INTERFACE WITH LED MATRIX TYPE-3

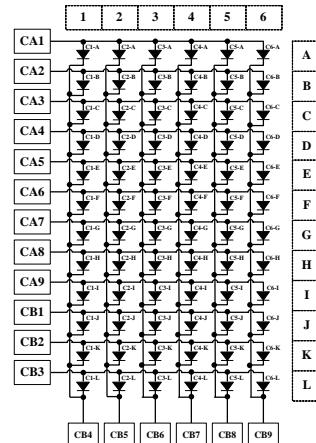
Matrix Type-3



3.3.8 SLED17341 SPI INTERFACE WITH LED MATRIX TYPE-4

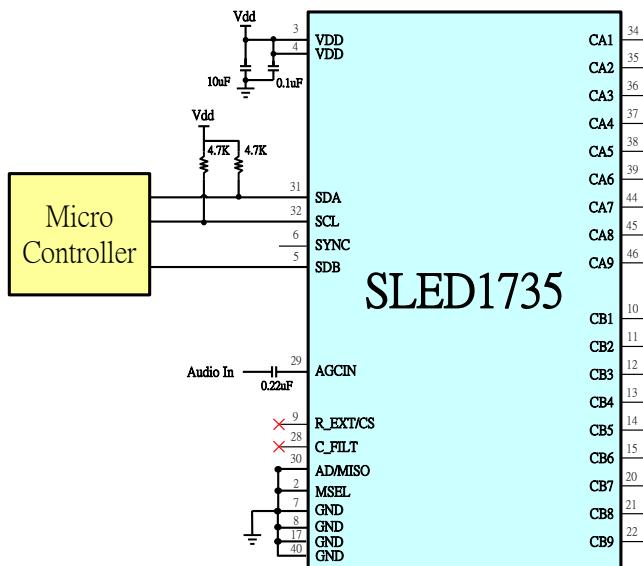


Matrix Type-4

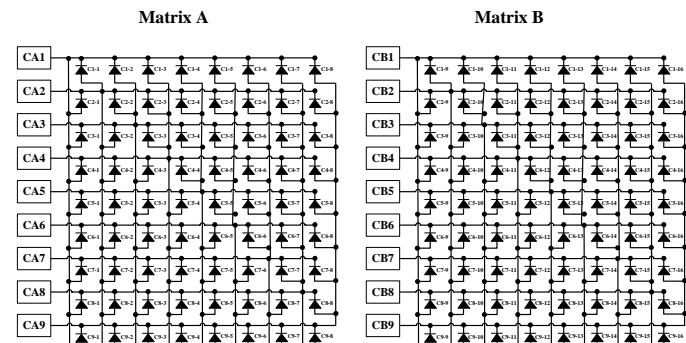


3.4 SLED1735 INTERFACE WITH LED MATRIX

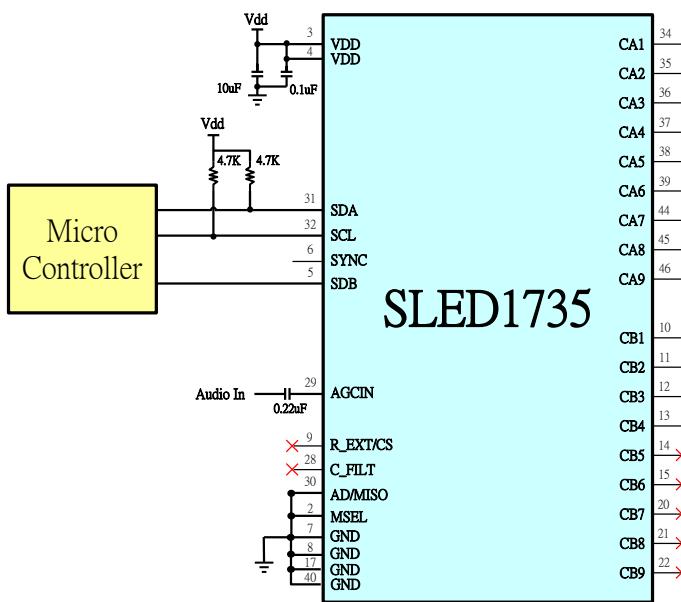
3.4.1 SLED1735 I2C INTERFACE WITH LED MATRIX TYPE-1



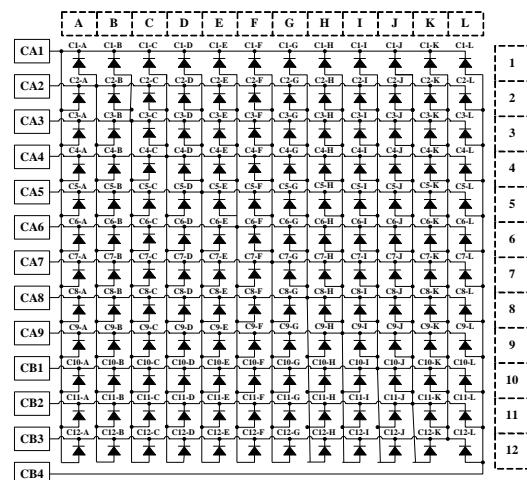
Matrix Type-1



3.4.2 SLED1735 I2C INTERFACE WITH LED MATRIX TYPE-2

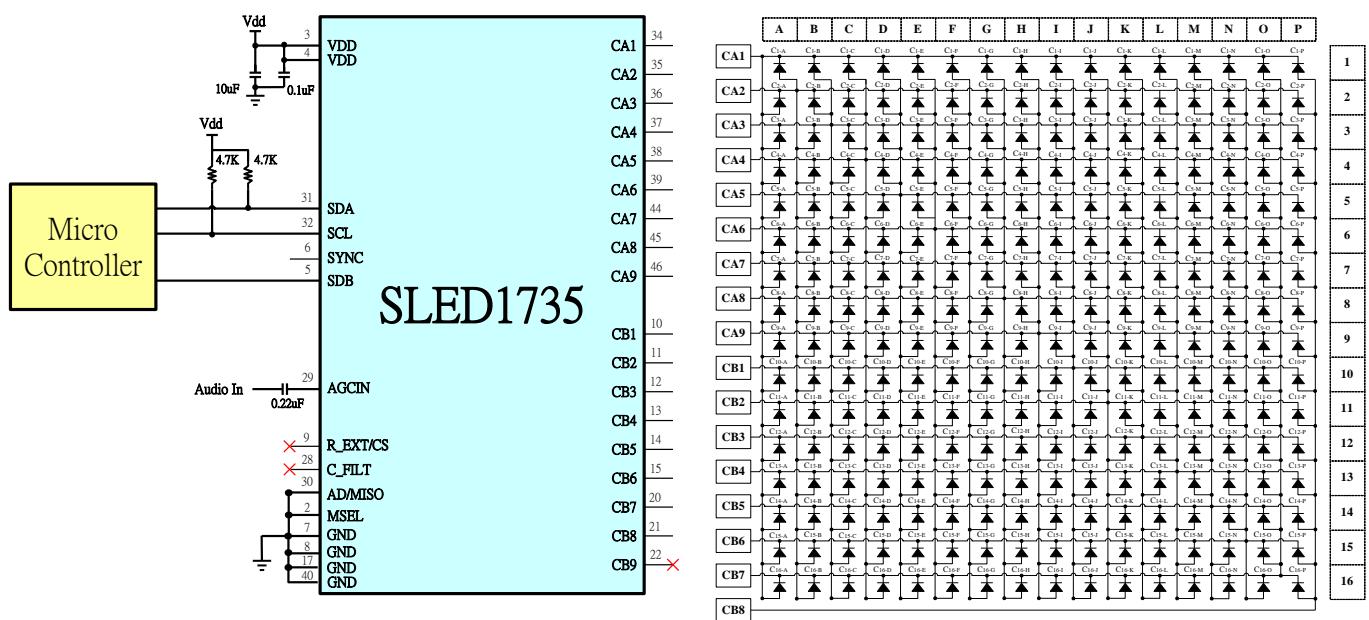


Matrix Type-2

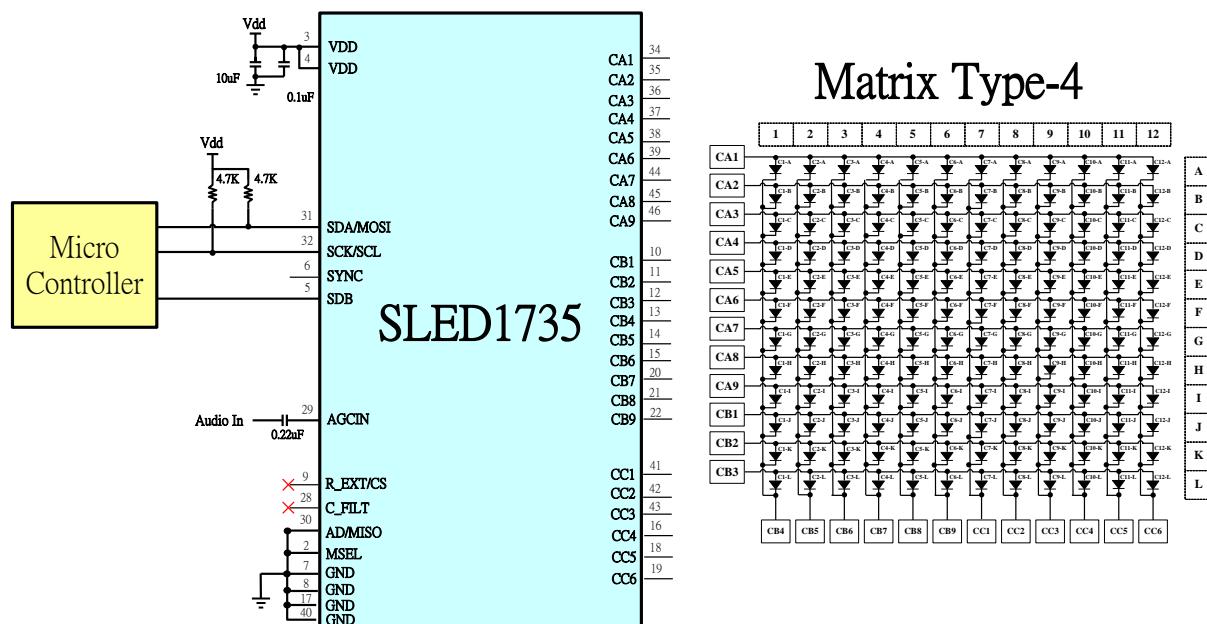


3.4.3 SLED1735 I2C INTERFACE WITH LED MATRIX TYPE-3

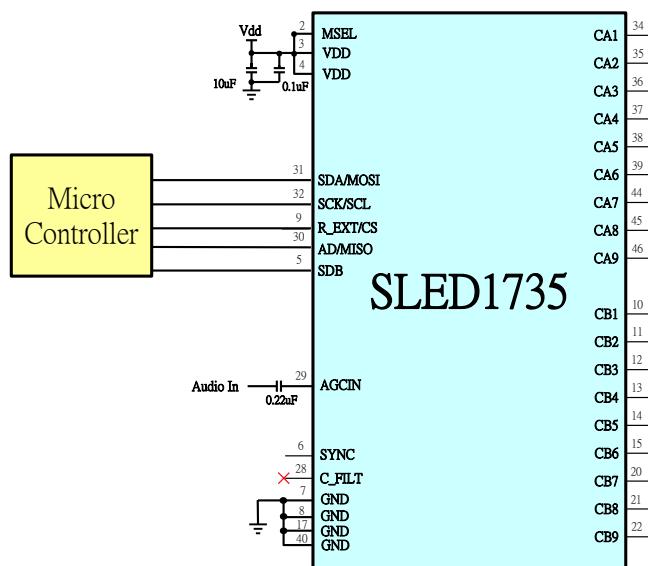
Matrix Type-3



3.4.4 SLED1735 I2C INTERFACE WITH LED MATRIX TYPE-4

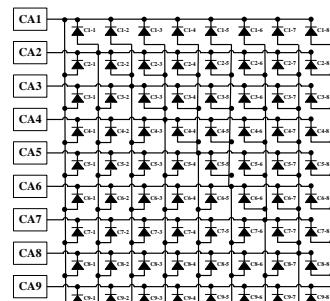


3.4.5 SLED1735 SPI INTERFACE WITH LED MATRIX TYPE-1



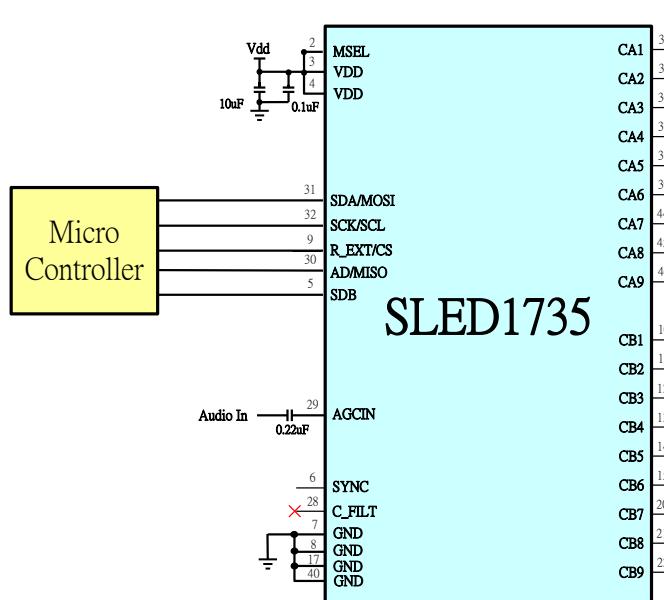
Matrix Type-1

Matrix A

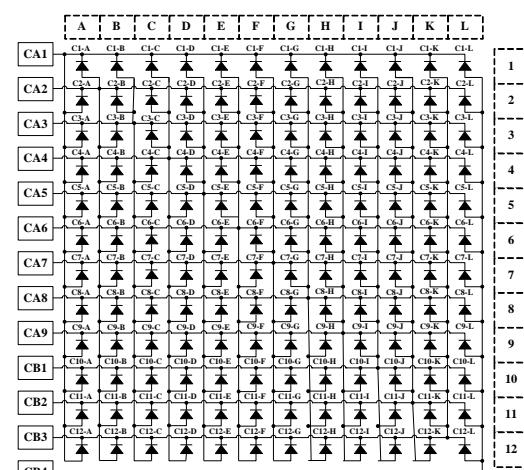


Matrix B

3.4.6 SLED1735 SPI INTERFACE WITH LED MATRIX TYPE-2

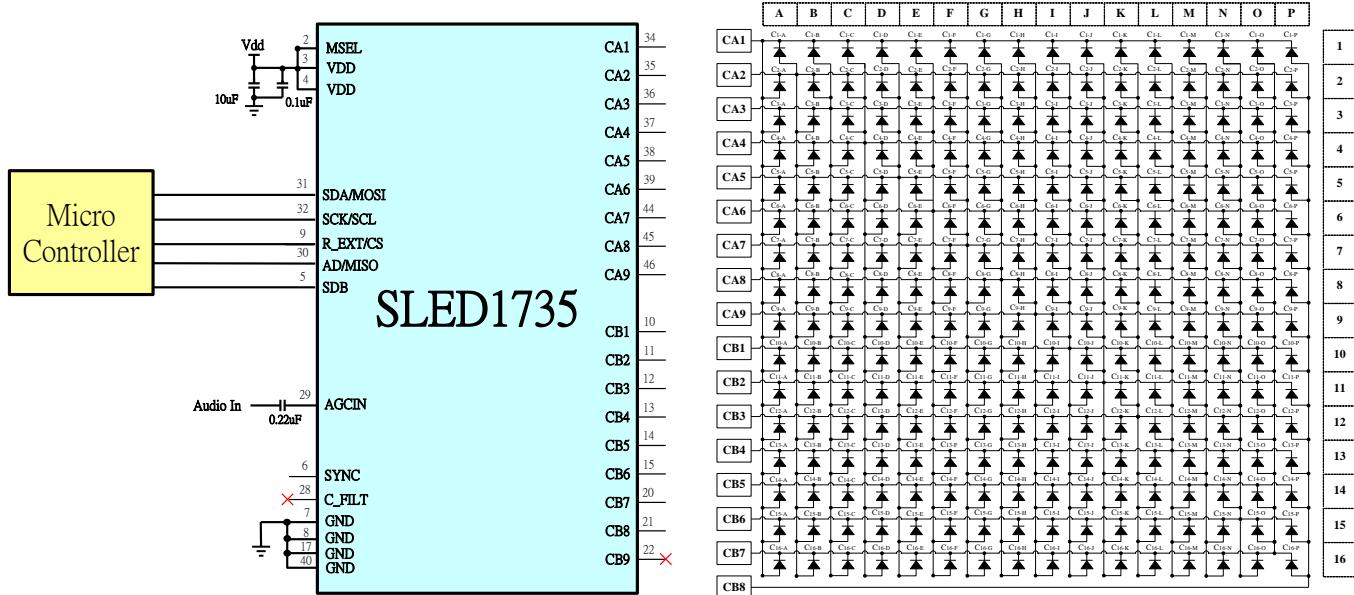


Matrix Type-2

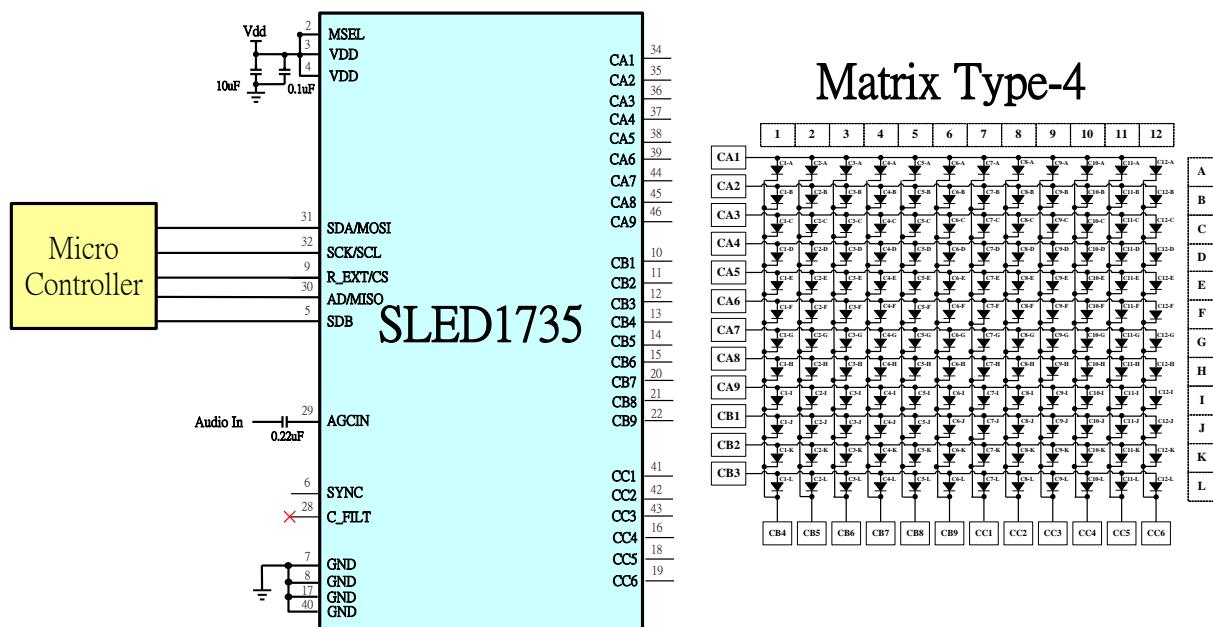


3.4.7 SLED1735 SPI INTERFACE WITH LED MATRIX TYPE-3

Matrix Type-3



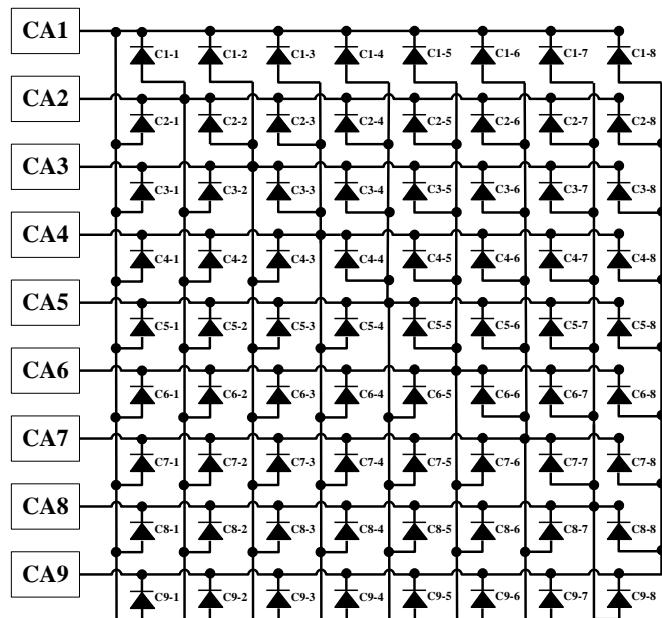
3.4.8 SLED1735 SPI INTERFACE WITH LED MATRIX TYPE-4



3.5 SLED1732/17321 RGB LED MATRIX PLACEMENT

3.5.1 SLED1732/17321 SINGLE COLOR LED IN MATRIX TYPE-1

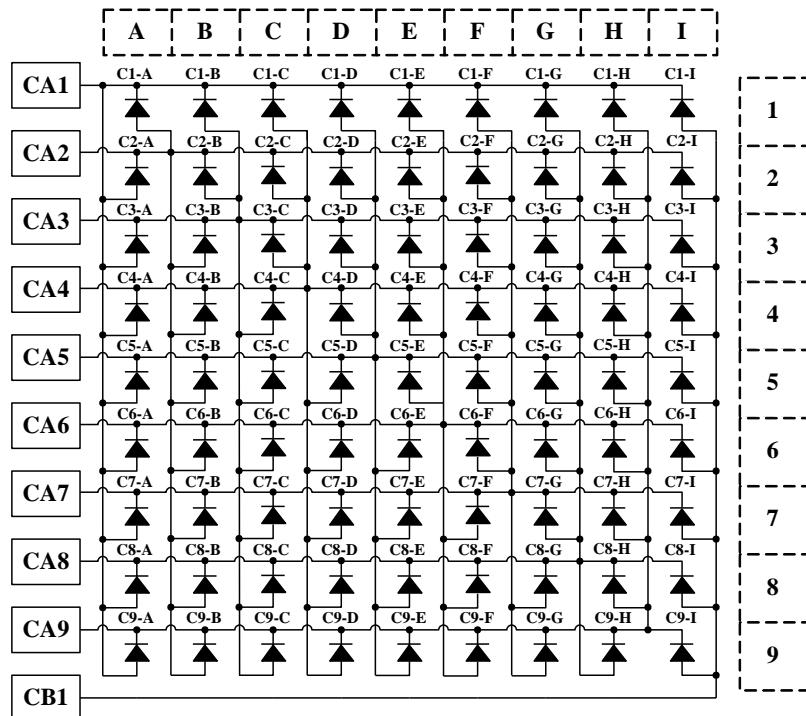
Matrix Type-1 can drive 72 single color LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-1: Matrix A (9*8)

3.5.2 SLED1732/17321 SINGLE COLOR LED IN MATRIX TYPE-2

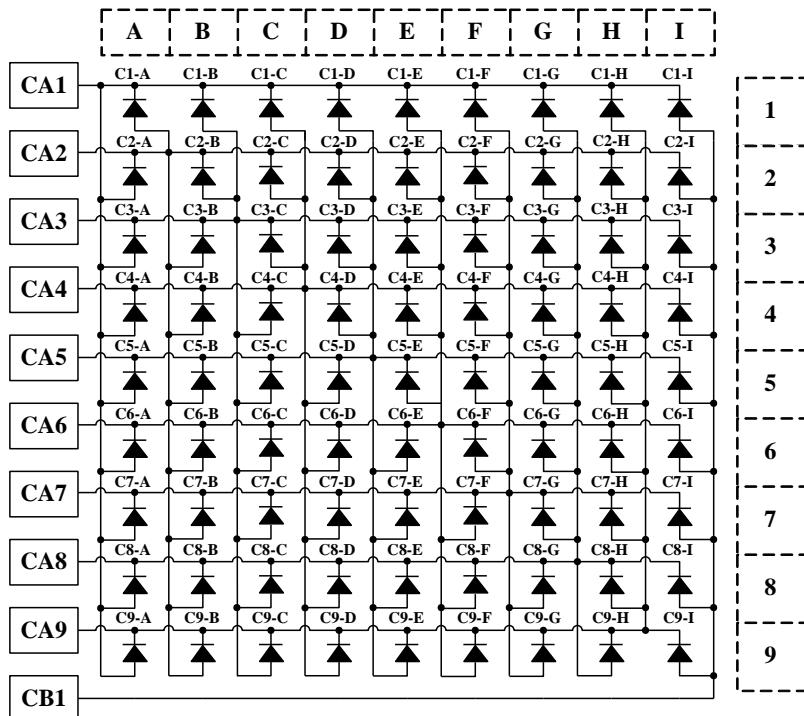
Matrix Type-2 can drive 81 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-2: 9*9

3.5.3 SLED1732/17321 SINGLE COLOR RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 81 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



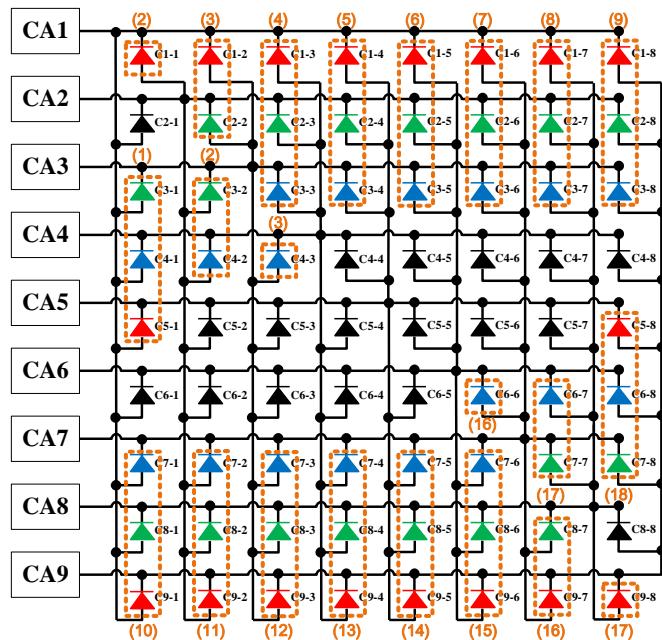
Type-3: 9*9

3.5.4 SLED1732/17321 SINGLE COLOR RGB LED IN MATRIX TYPE-4

Matrix Type-4 is not supported.

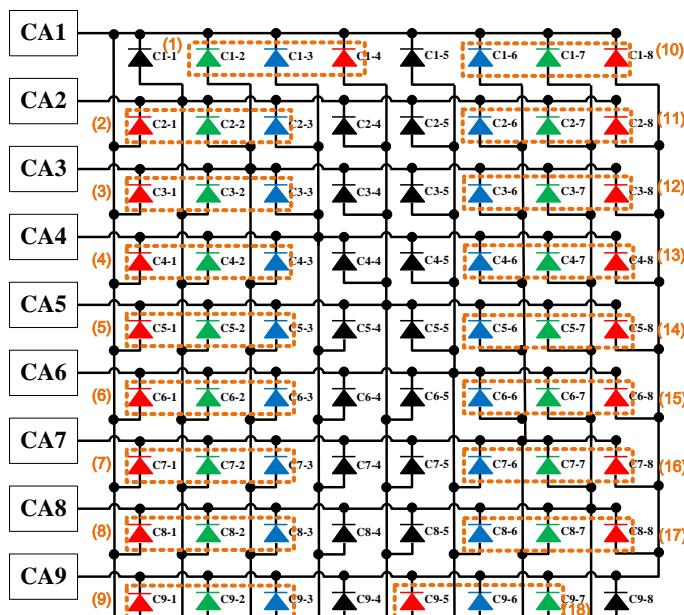
3.5.5 SLED1732/17321 COMMON ANODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 18 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



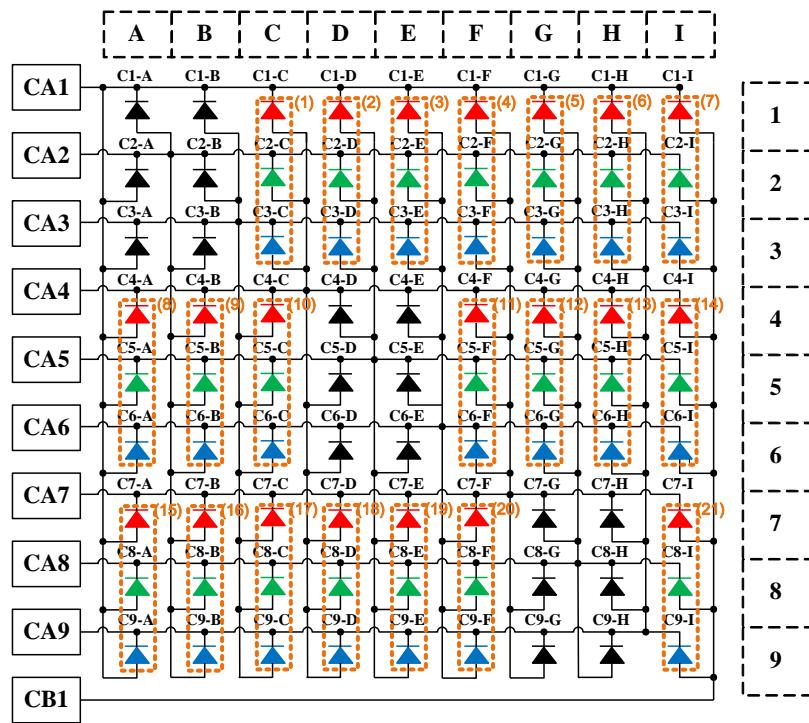
3.5.6 SLED1732/17321 COMMON CATHODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 18 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



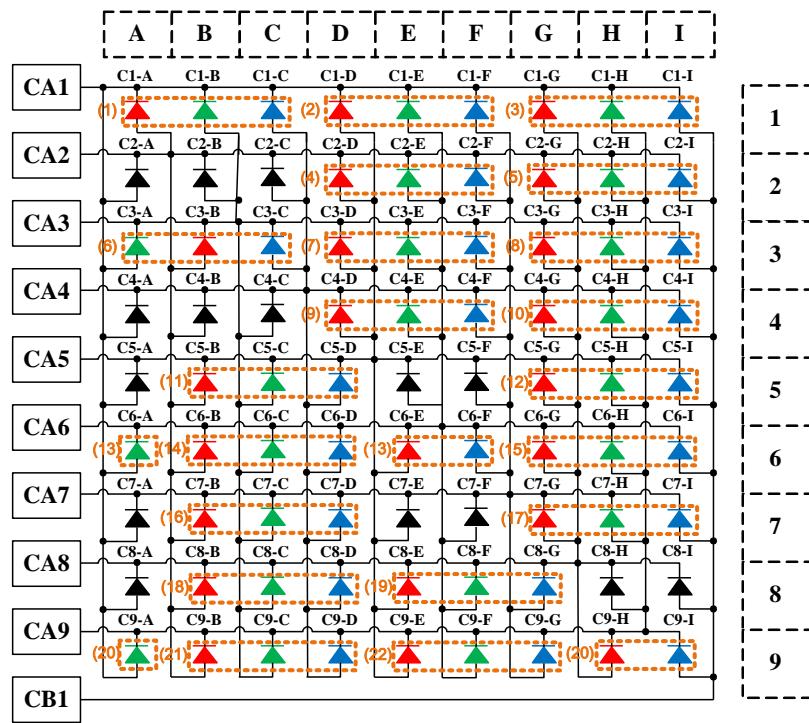
3.5.7 SLED1732/17321 COMMON ANODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 21 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



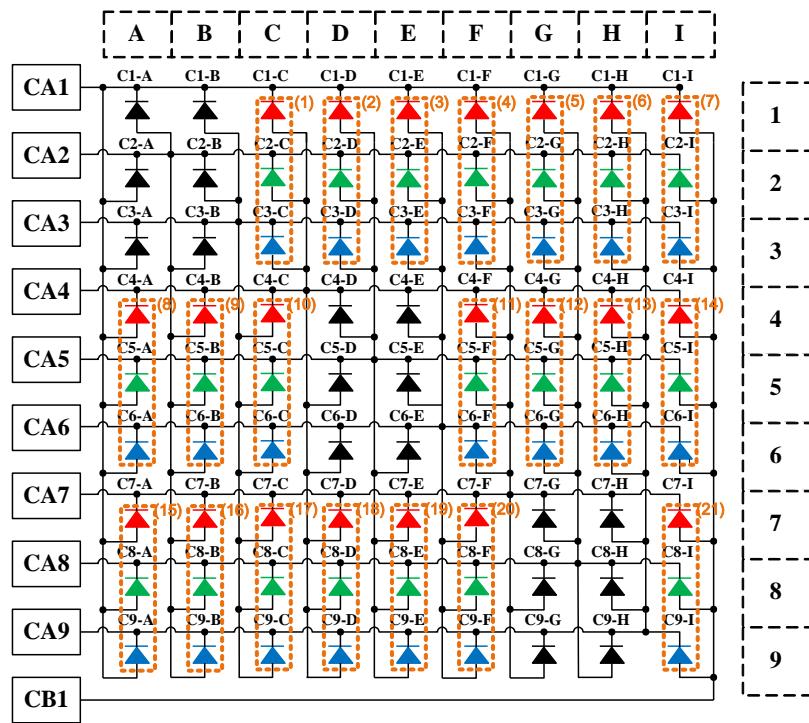
3.5.8 SLED1732/17321 COMMON CATHODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 22 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



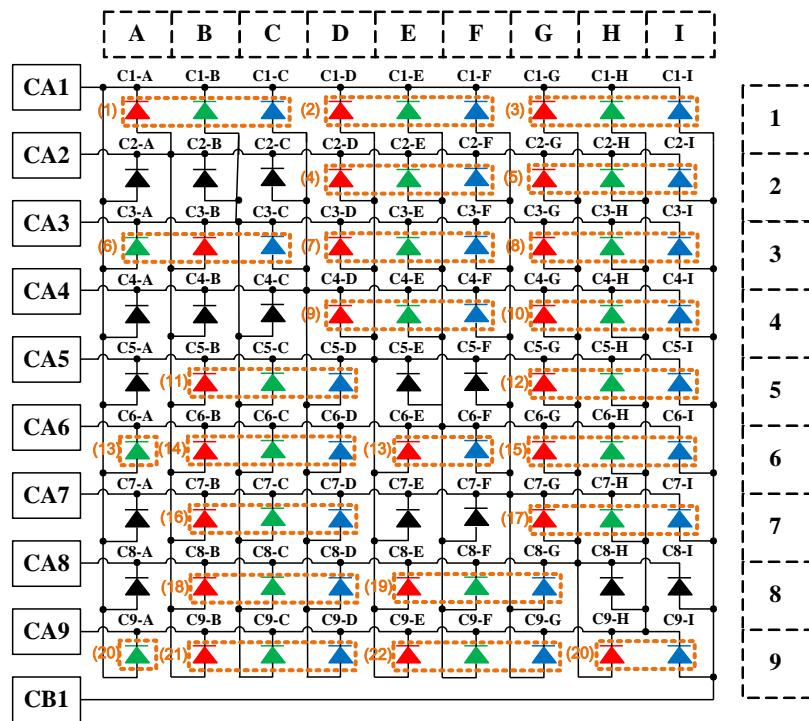
3.5.9 SLED1732/17321 COMMON ANODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 21 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



3.5.10 SLED1732/17321 COMMON CATHODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 22 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



3.5.11 SLED1732/17321 COMMON ANODE RGB LED IN MATRIX TYPE-4

Common Anode RGB LEDs of Matrix Type-4 is not supported in SLED1732/SLED17321.

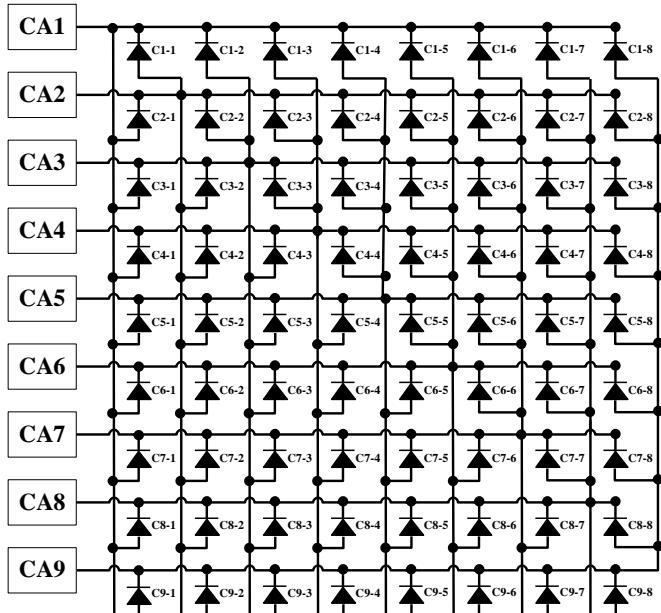
3.5.12 SLED1732/17321 COMMON CATHODE RGB LED IN MATRIX TYPE-4

Common Cathode RGB LEDs of Matrix Type-4 is not supported in SLED1732/SLED17321.

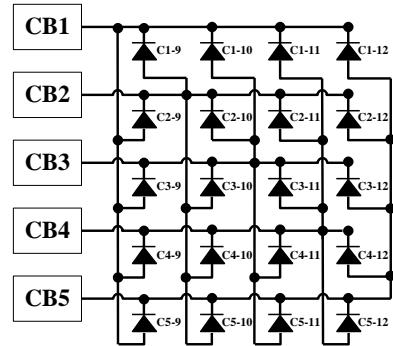
3.6 SLED1733/17331 RGB LED MATRIX PLACEMENT

3.6.1 SLED1733/17331 SINGLE COLOR LED IN MATRIX TYPE-1

Matrix Type-1 can drive 72+20 single color LEDs. The locations of single color LEDs are recommended as the circuit below.



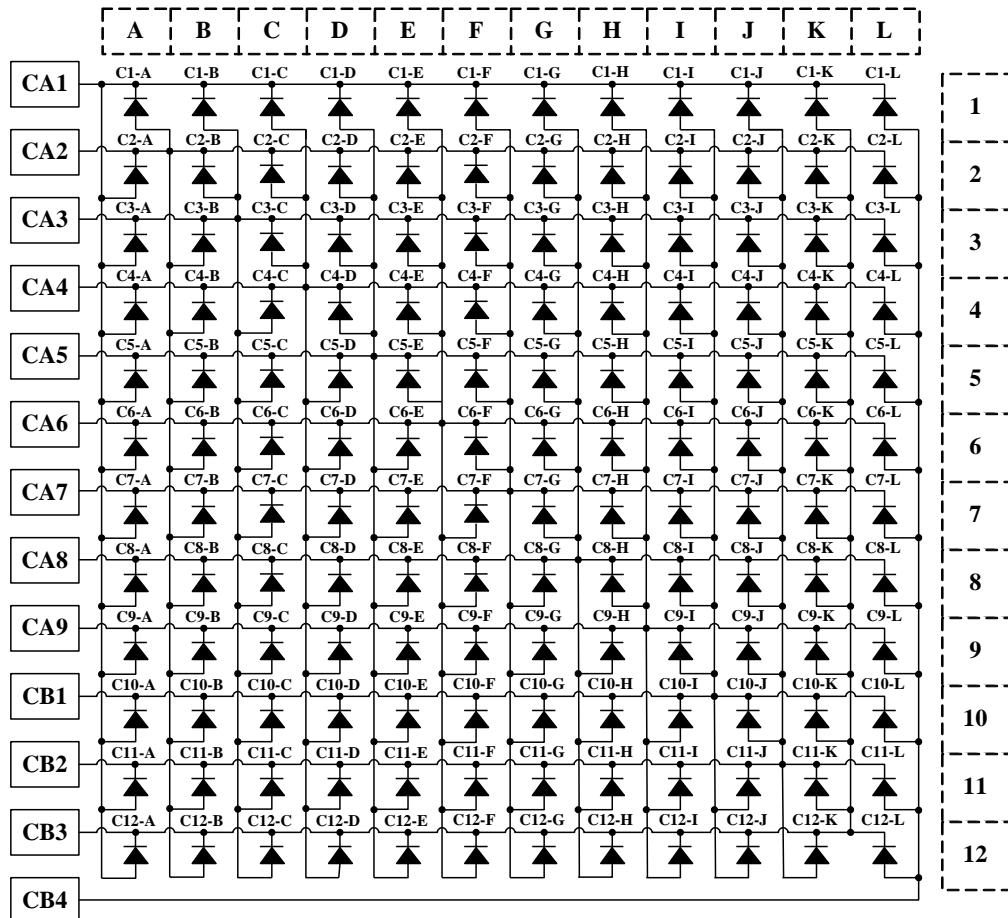
Type-1: Matrix A (9*8)



Type-1: Matrix B (5*4)

3.6.2 SLED1733/17331 SINGLE COLOR LED IN MATRIX TYPE-2

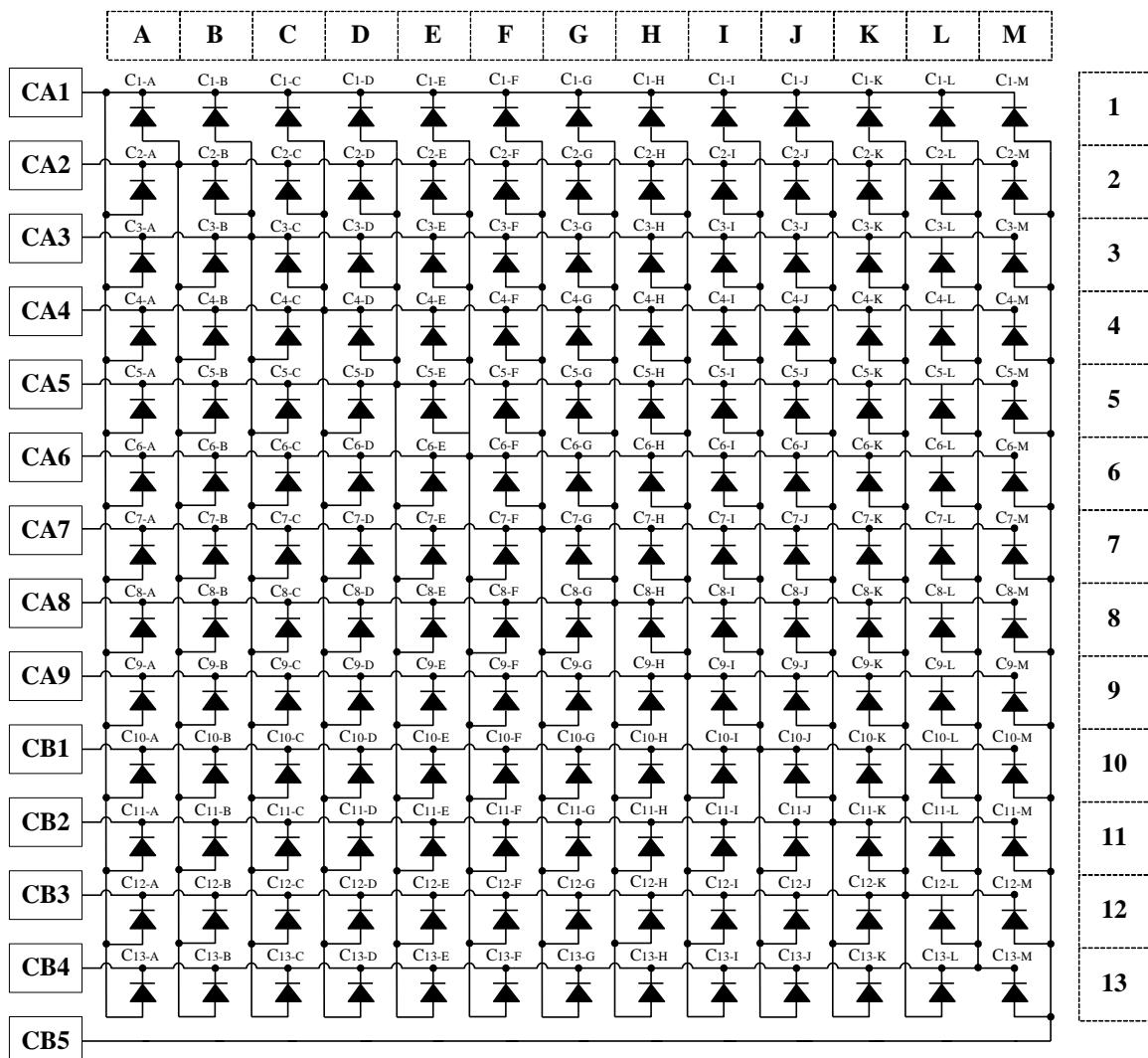
Matrix Type-2 can drive 144 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-2: 12*12

3.6.3 SLED1733/17331 SINGLE COLOR RGB LED IN MATRIX TYPE-3

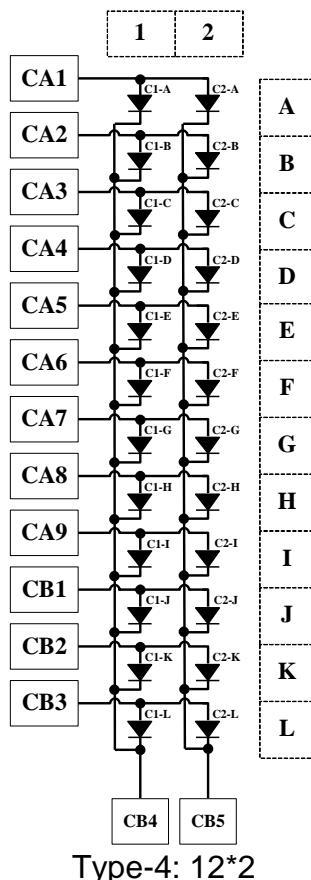
Matrix Type-3 can drive 169 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-3: 13*13

3.6.4 SLED1733/17331 SINGLE COLOR RGB LED IN MATRIX TYPE-4

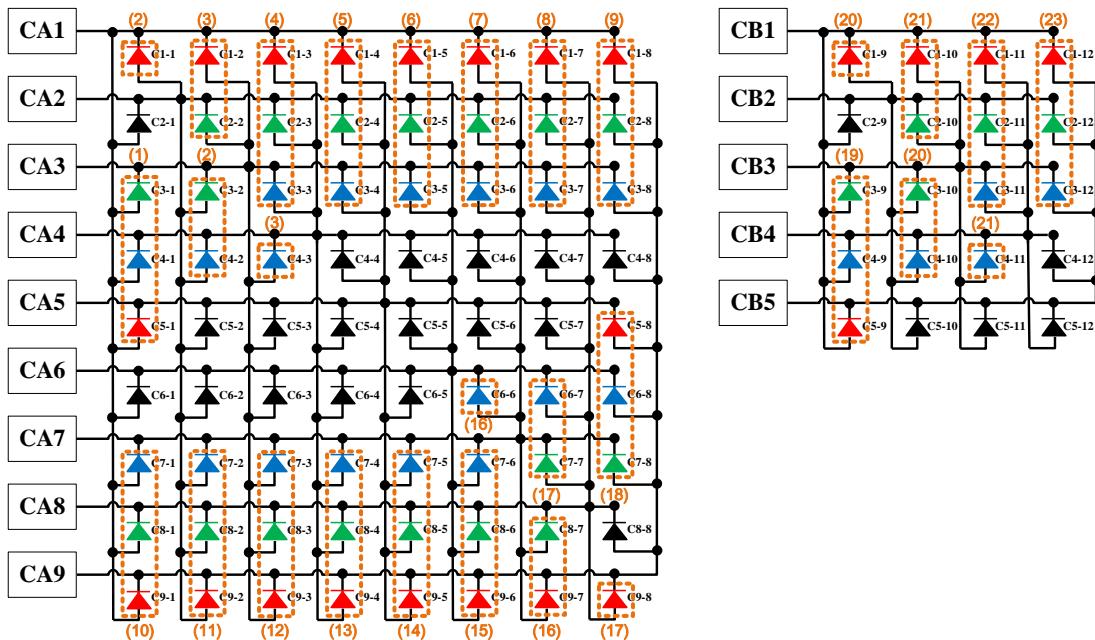
Matrix Type-4 can drive 24 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-4: 12*2

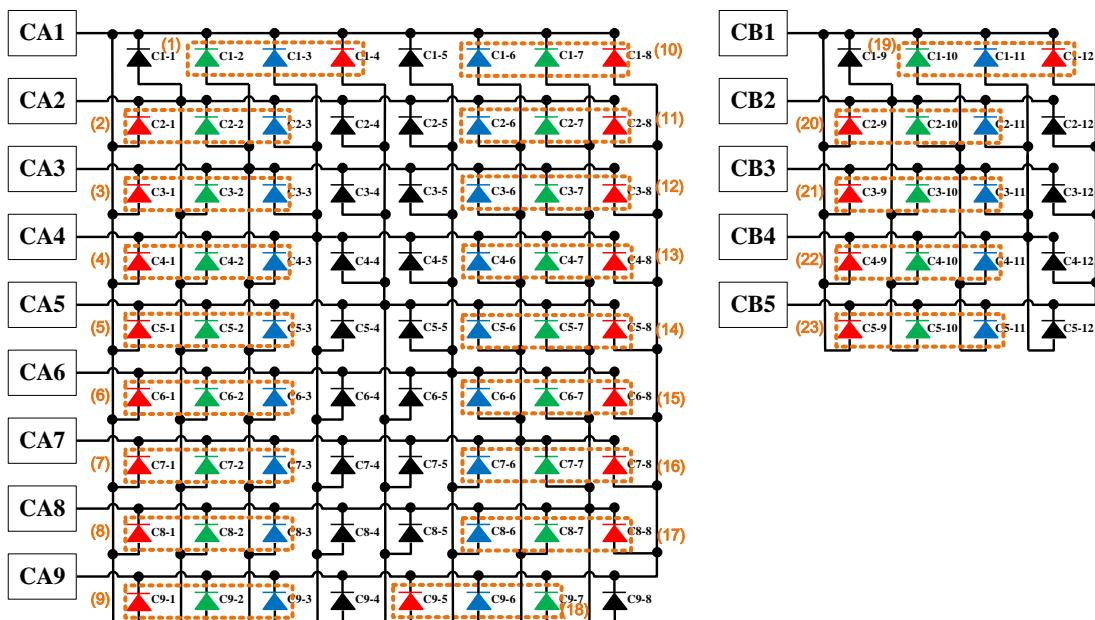
3.6.5 SLED1733/17331 COMMON ANODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 18+5 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



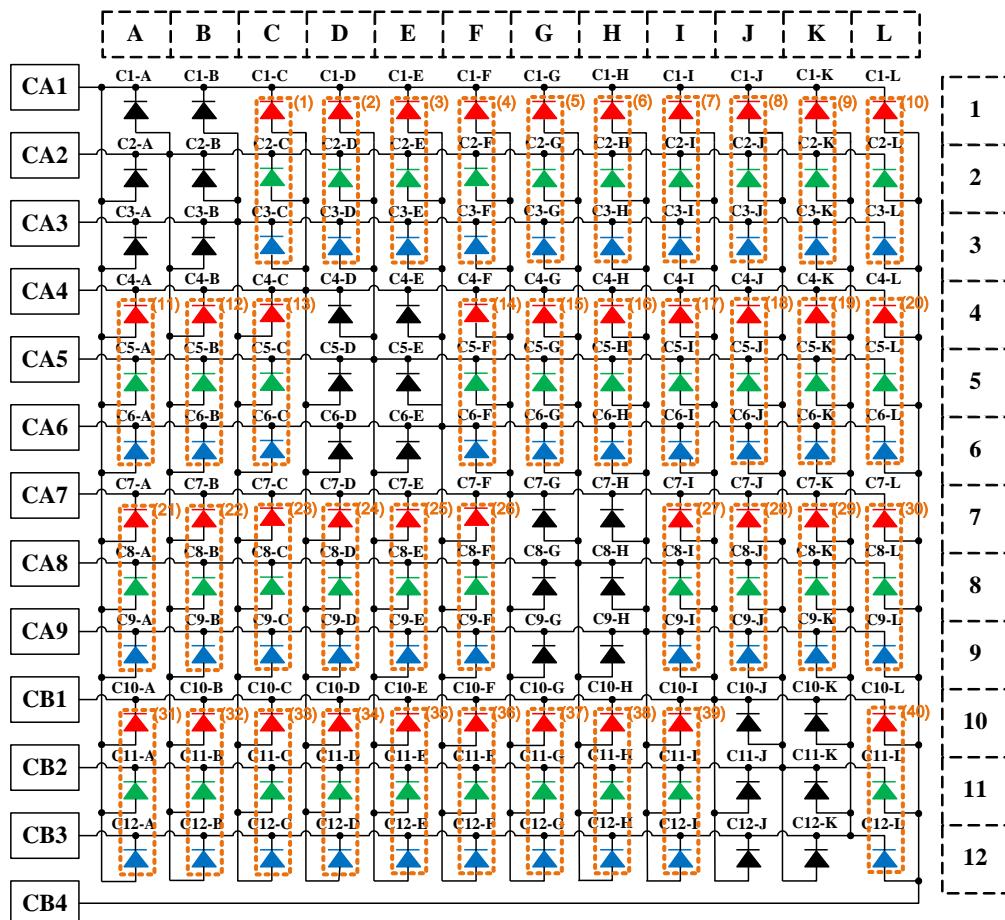
3.6.6 SLED1733/17331 COMMON CATHODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 18+5 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



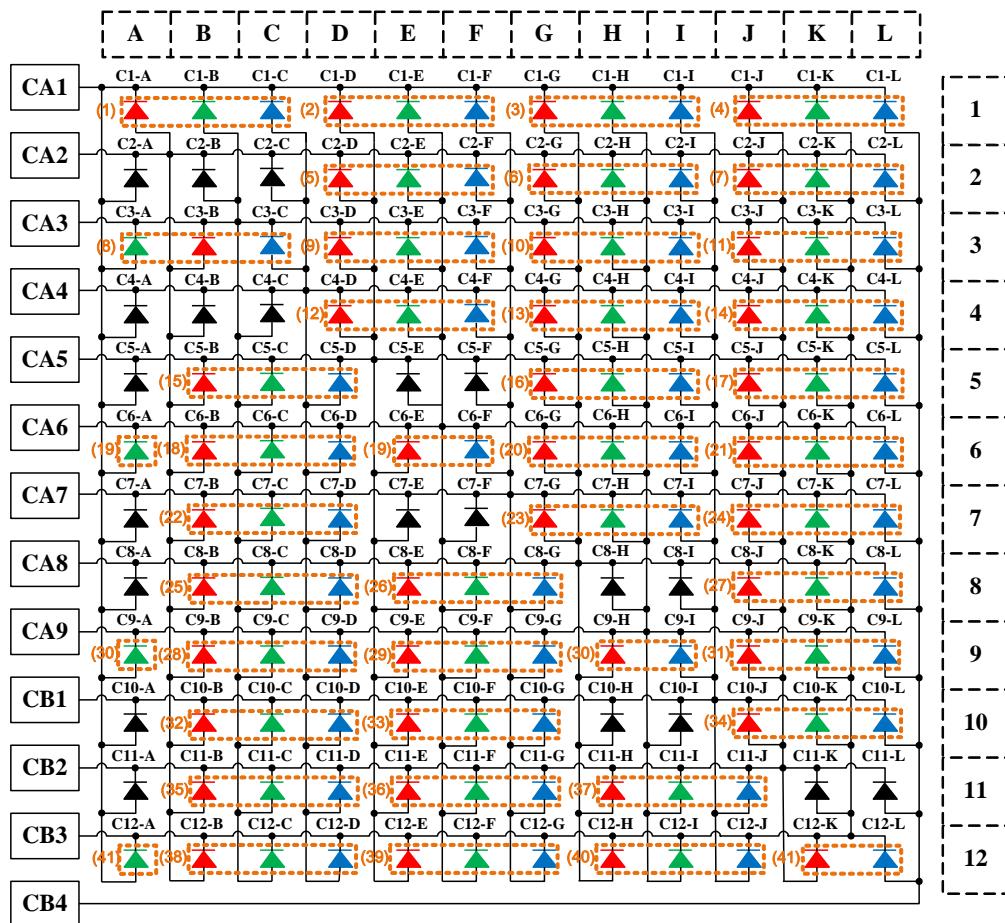
3.6.7 SLED1733/17331 COMMON ANODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 40 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



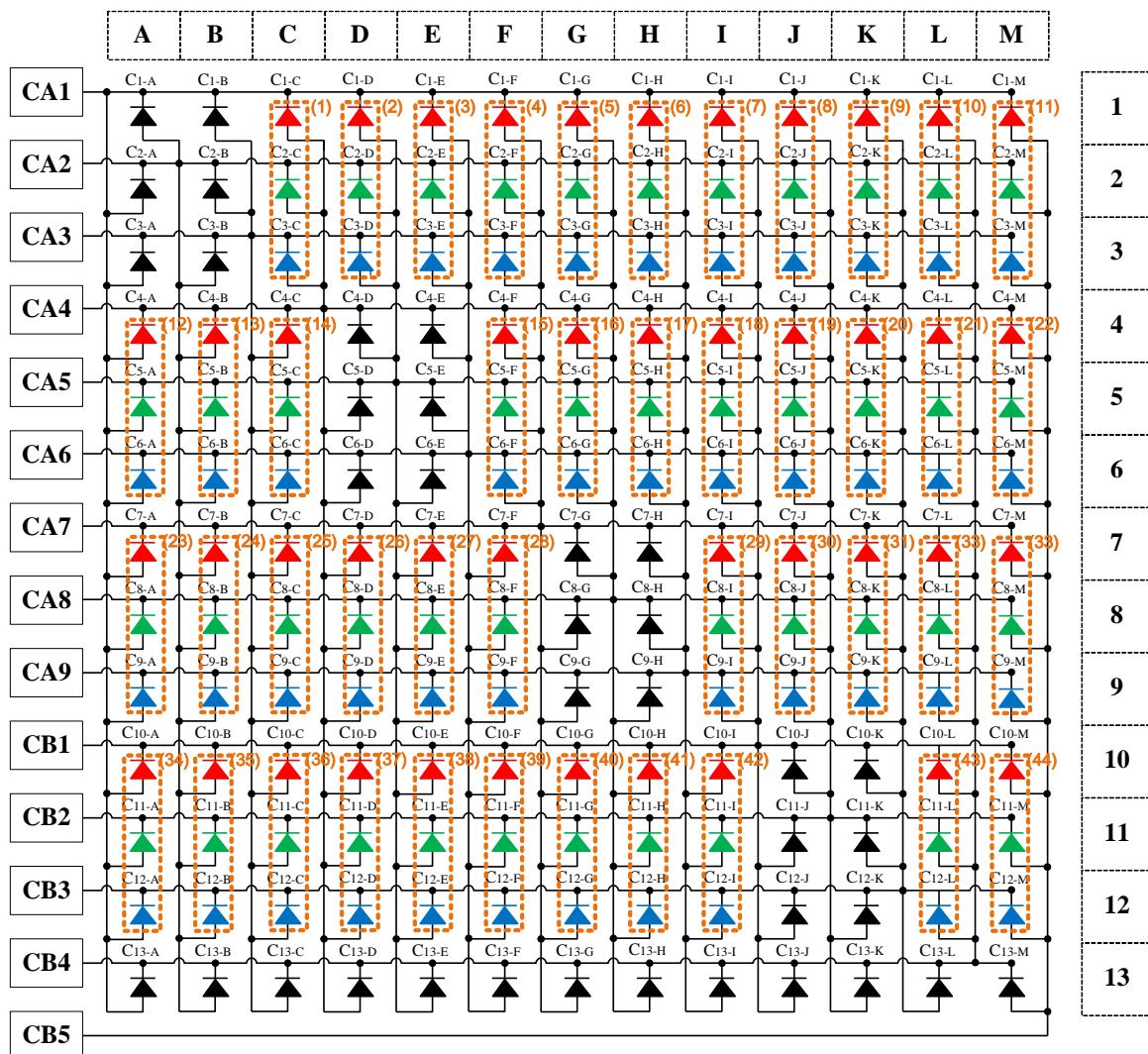
3.6.8 SLED1733/17331 COMMON CATHODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 41 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



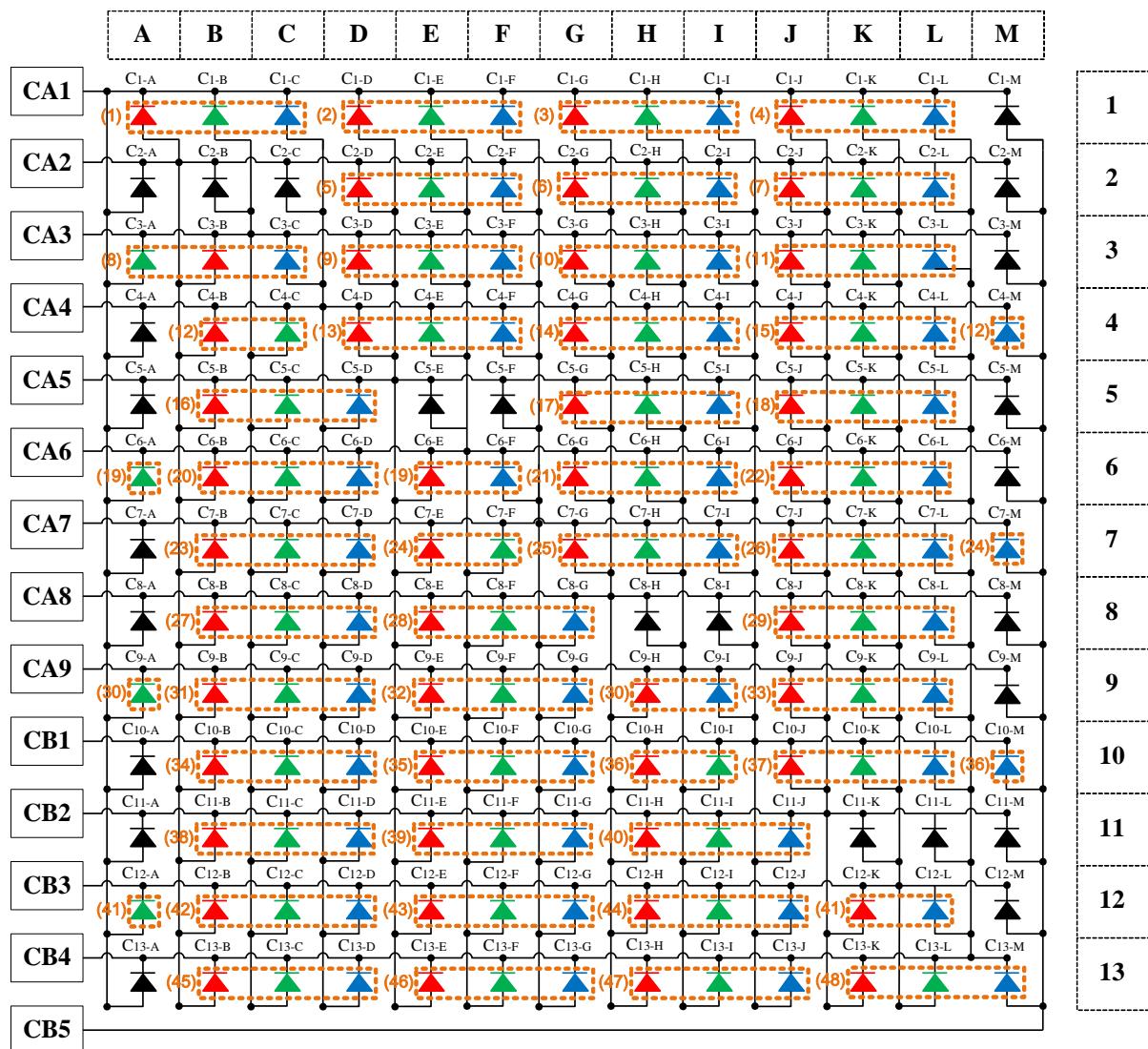
3.6.9 SLED1733/17331 COMMON ANODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 44 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



3.6.10 SLED1733/17331 COMMON CATHODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 48 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.

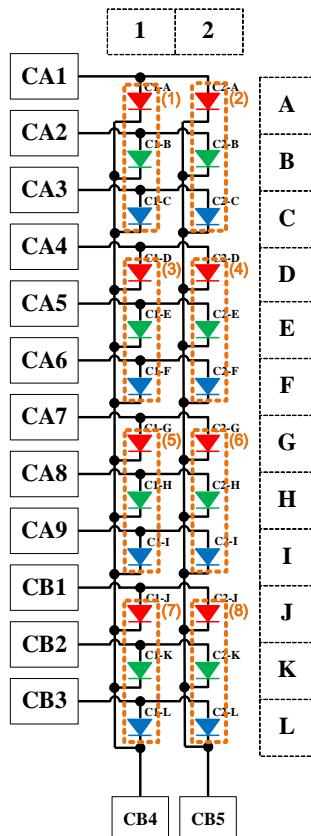


3.6.11 SLED1733/17331 COMMON ANODE RGB LED IN MATRIX TYPE-4

Common Anode RGB LEDs of Matrix Type-4 is not supported in SLED1733/SLED17331.

3.6.12 SLED1733/17331 COMMON CATHODE RGB LED IN MATRIX TYPE-4

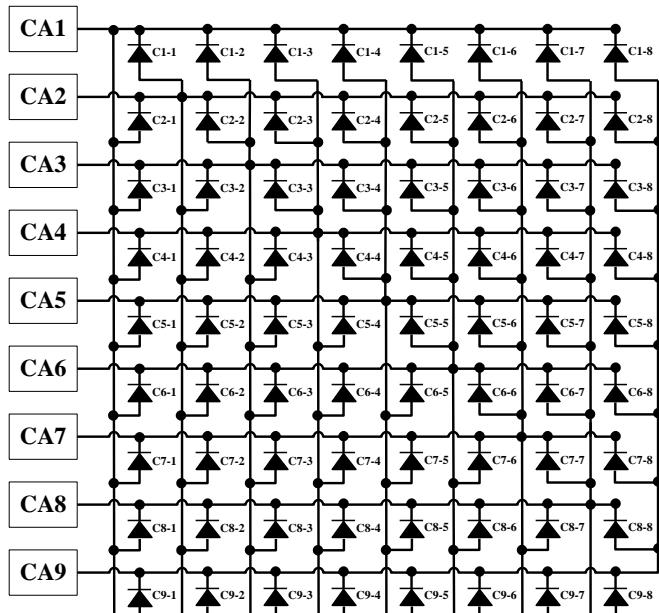
Matrix Type-4 can drive 8 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.



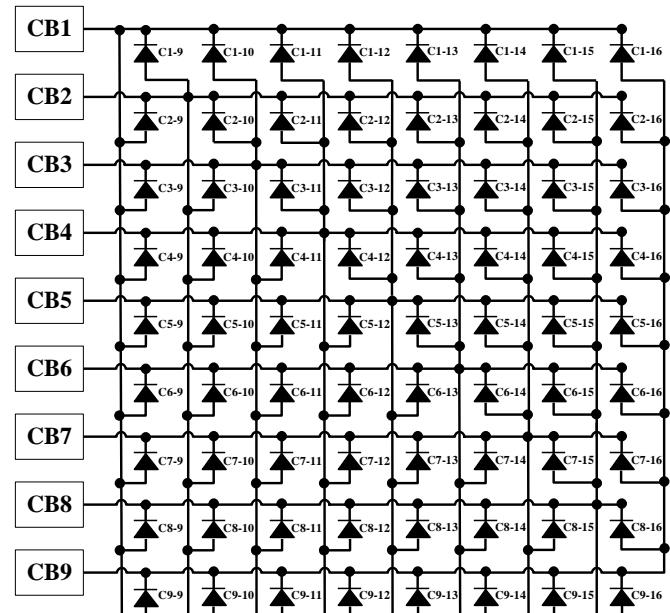
3.7 LED1734/17341 RGB LED MATRIX PLACEMENT

3.7.1 SLED1734/17341 SINGLE COLOR LED IN MATRIX TYPE-1

Matrix Type-1 can drive 144 single color LEDs. The locations of single color LEDs are recommended as the circuit below.



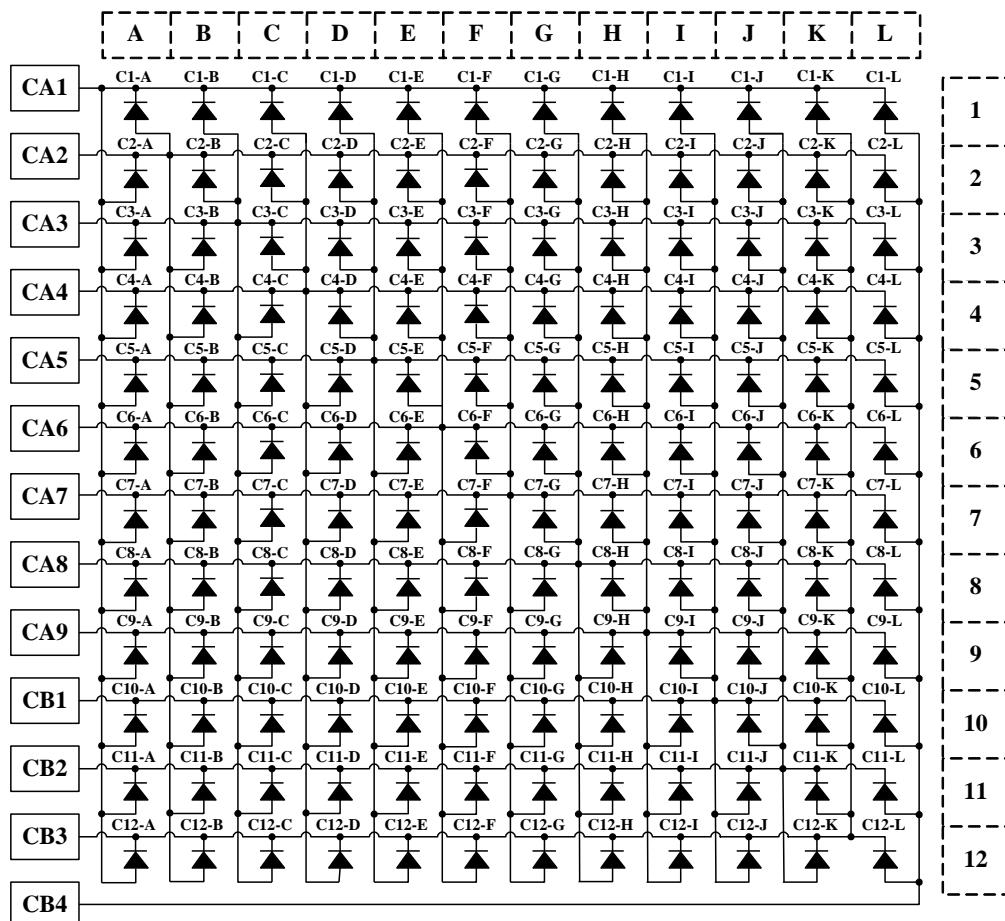
Type-1: Matrix A (9*8)



Type-1: Matrix B (9*8)

3.7.2 SLED1734/17341 SINGLE COLOR LED IN MATRIX TYPE-2

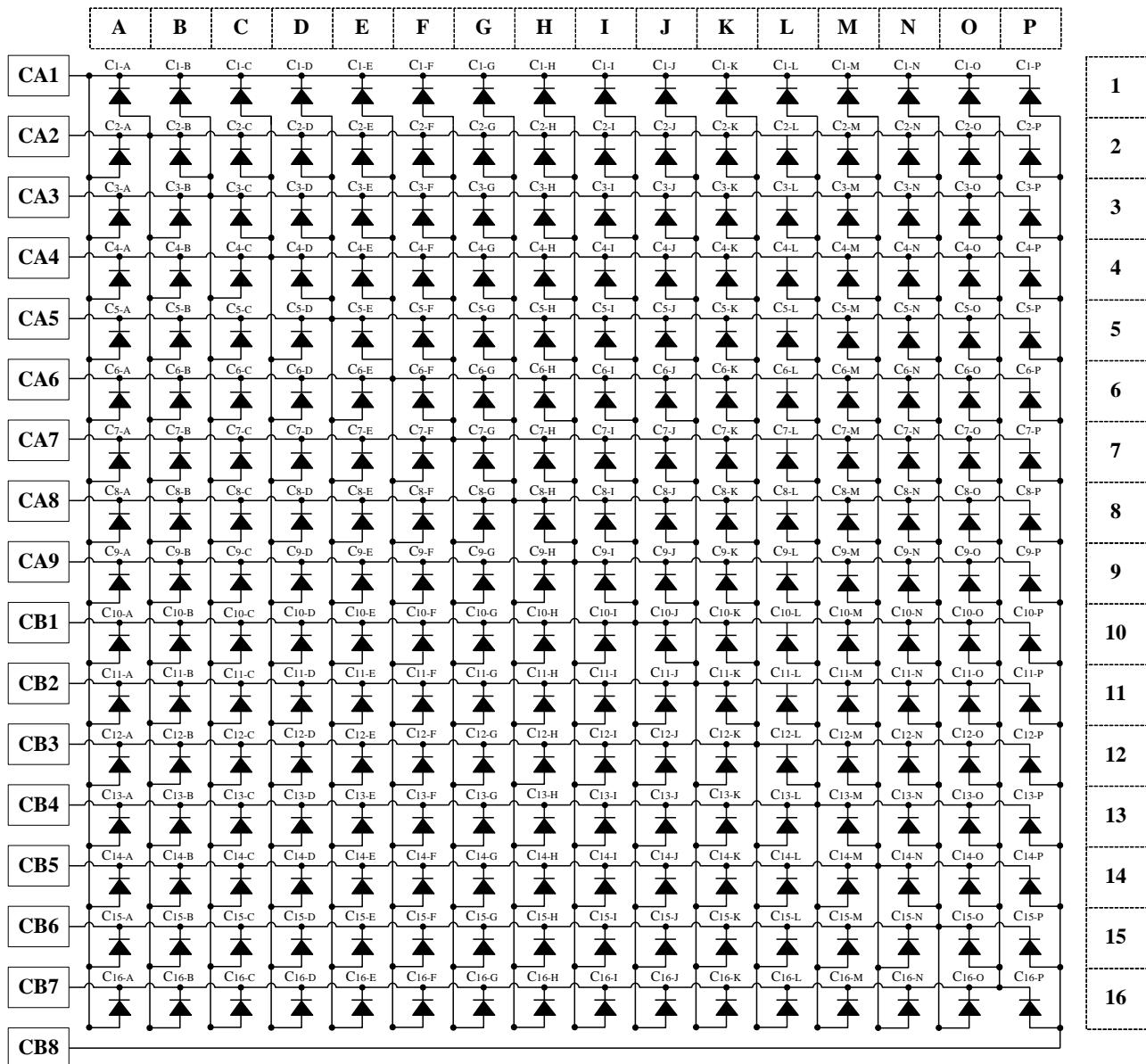
Matrix Type-2 can drive 144 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-2: 12*12

3.7.3 SLED1734/17341 SINGLE COLOR RGB LED IN MATRIX TYPE-3

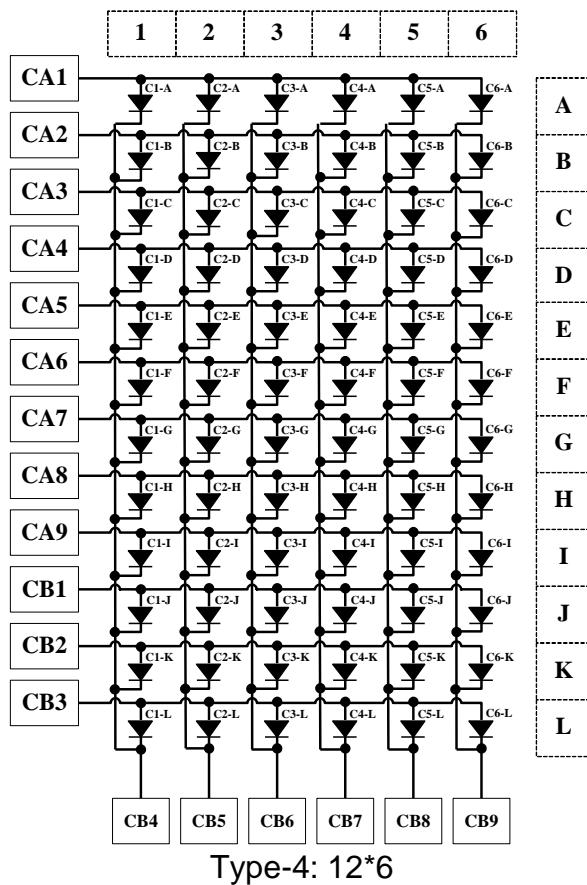
Matrix Type-3 can drive 256 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-3: 16*16

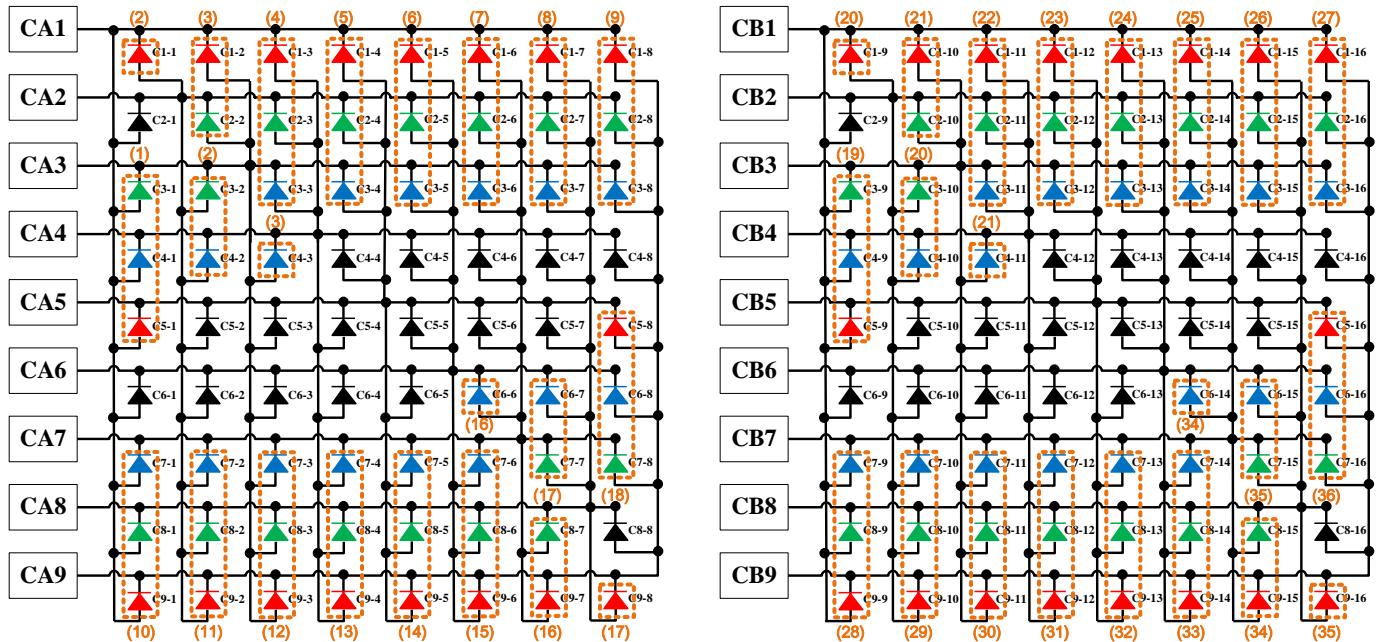
3.7.4 SLED1734/17341 SINGLE COLOR RGB LED IN MATRIX TYPE-4

Matrix Type-4 can drive 72 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



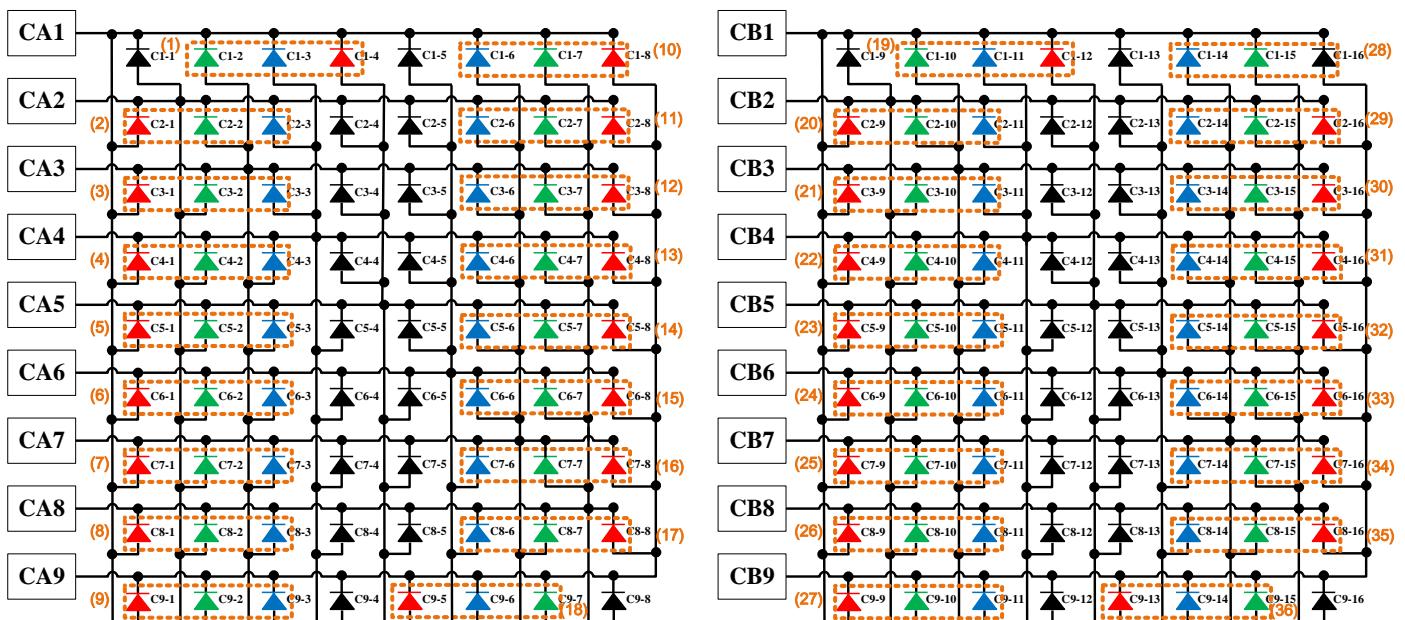
3.7.5 SLED1734/17341 COMMON ANODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 36 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



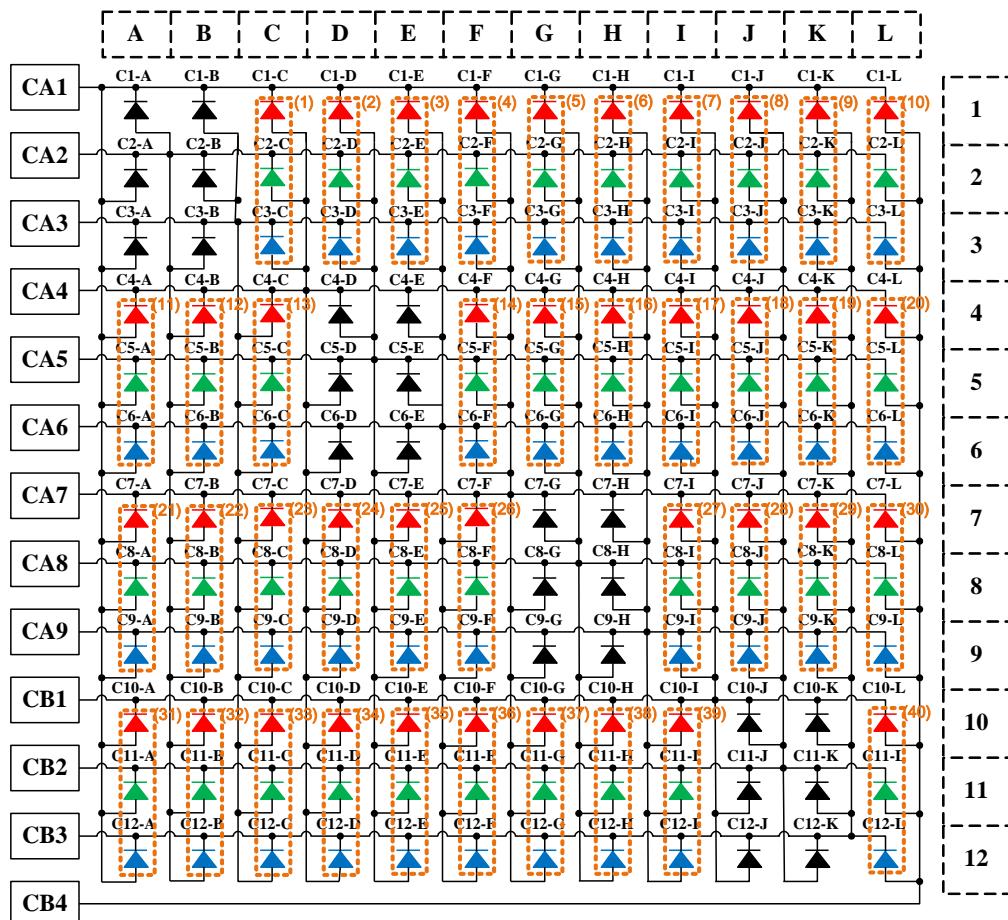
3.7.6 SLED1734/17341 COMMON CATHODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 36 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



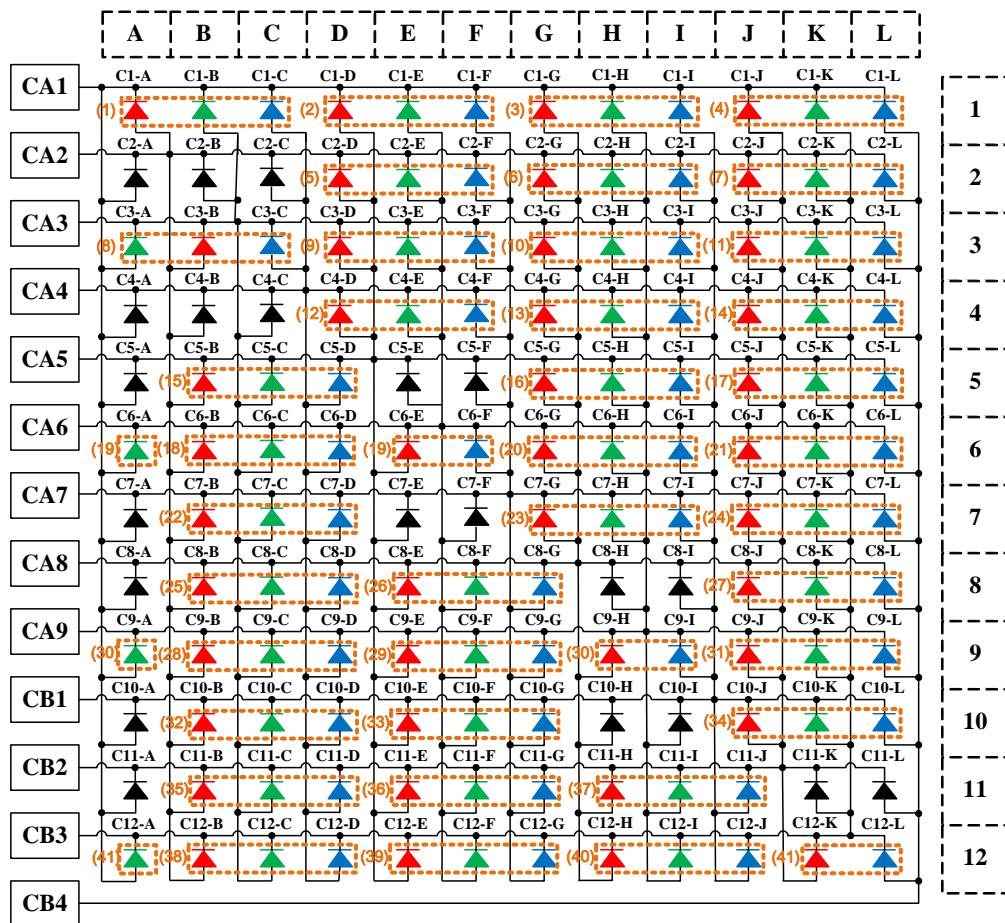
3.7.7 SLED1734/17341 COMMON ANODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 40 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



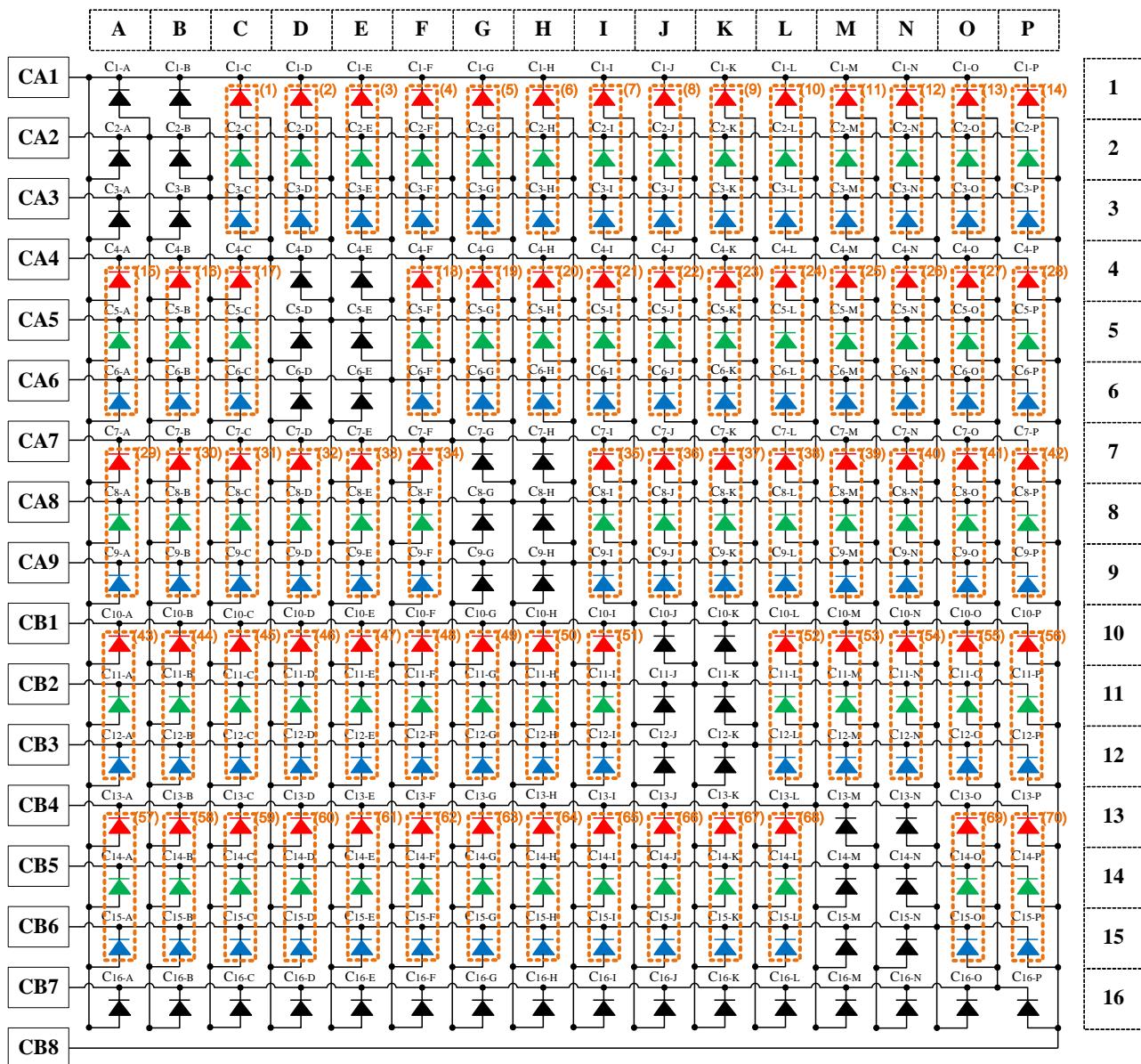
3.7.8 SLED1734/17341 COMMON CATHODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 41 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



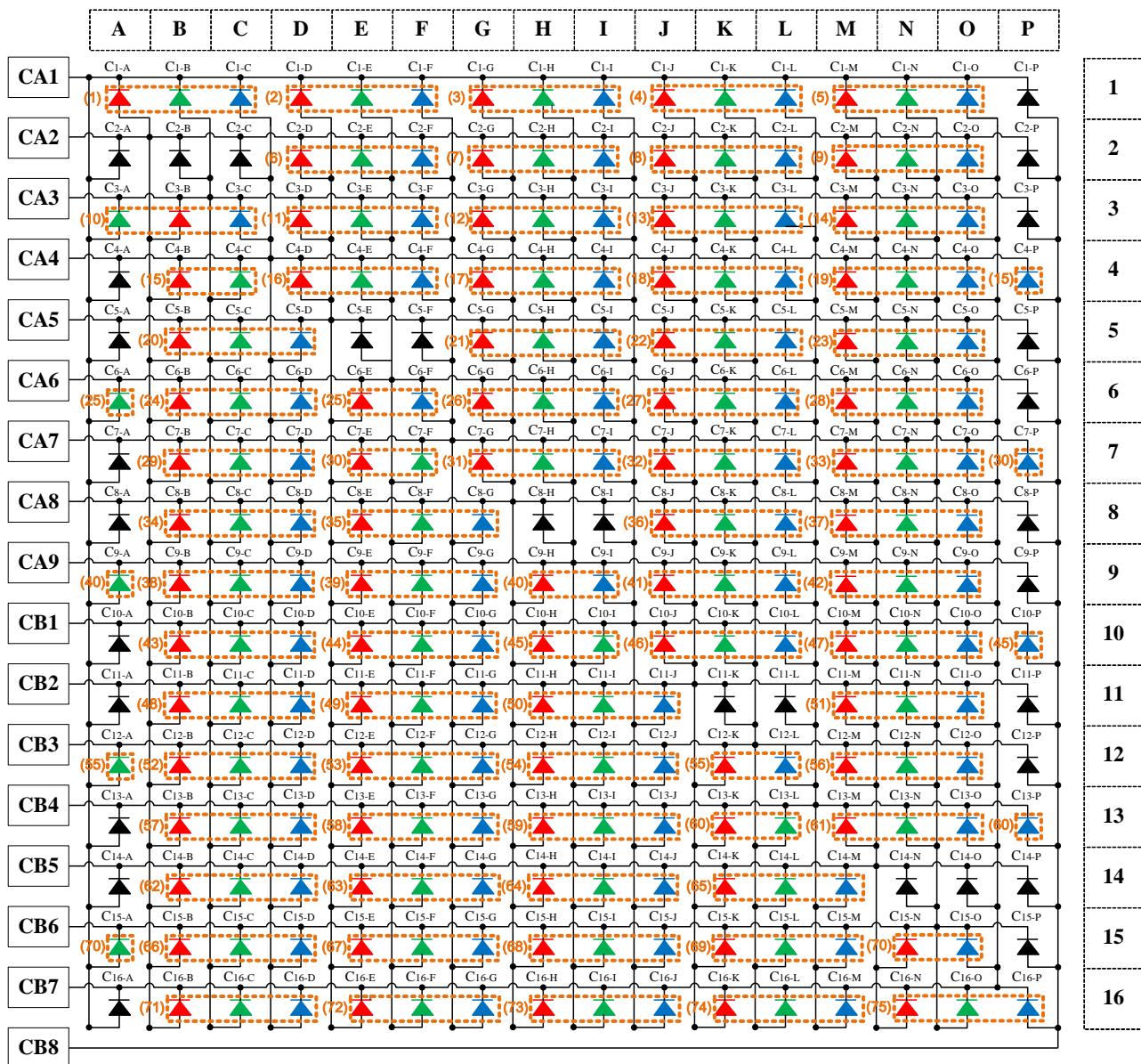
3.7.9 SLED1734/17341 COMMON ANODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 70 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



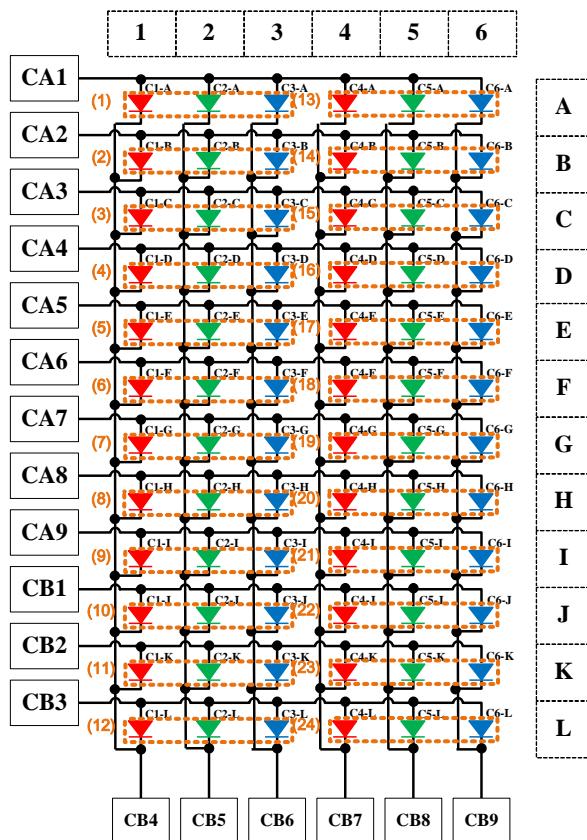
3.7.10 SLED1734/17341 COMMON CATHODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 75 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



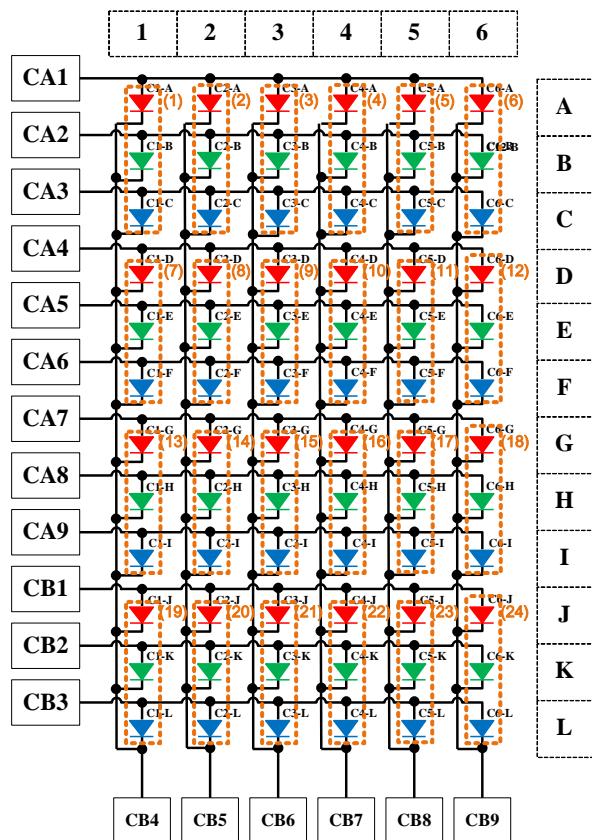
3.7.11 SLED1734/17341 COMMON ANODE RGB LED IN MATRIX TYPE-4

Matrix Type-4 can drive 24 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.



3.7.12 SLED1734/17341 COMMON CATHODE RGB LED IN MATRIX TYPE-4

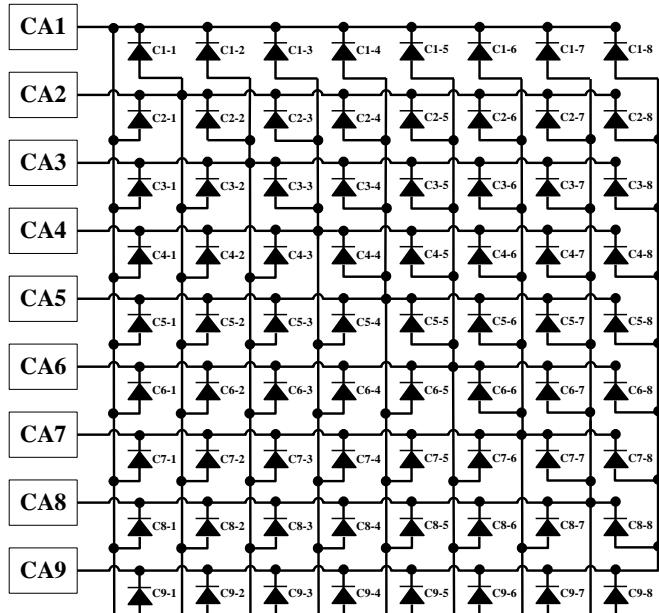
Matrix Type-4 can drive 24 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.



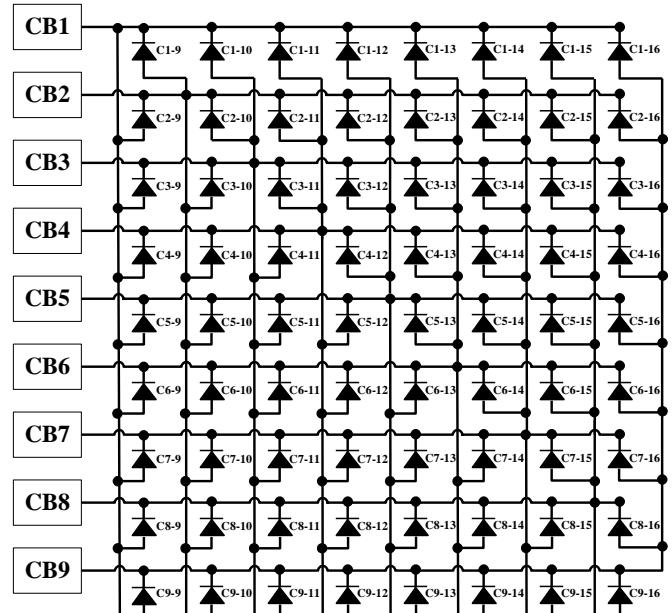
3.8 SLED1735/SLED1735 RGB LED MATRIX PLACEMENT

3.8.1 SLED1735 SINGLE COLOR LED IN MATRIX TYPE-1

Matrix Type-1 can drive 144 single color LEDs. The locations of single color LEDs are recommended as the circuit below.



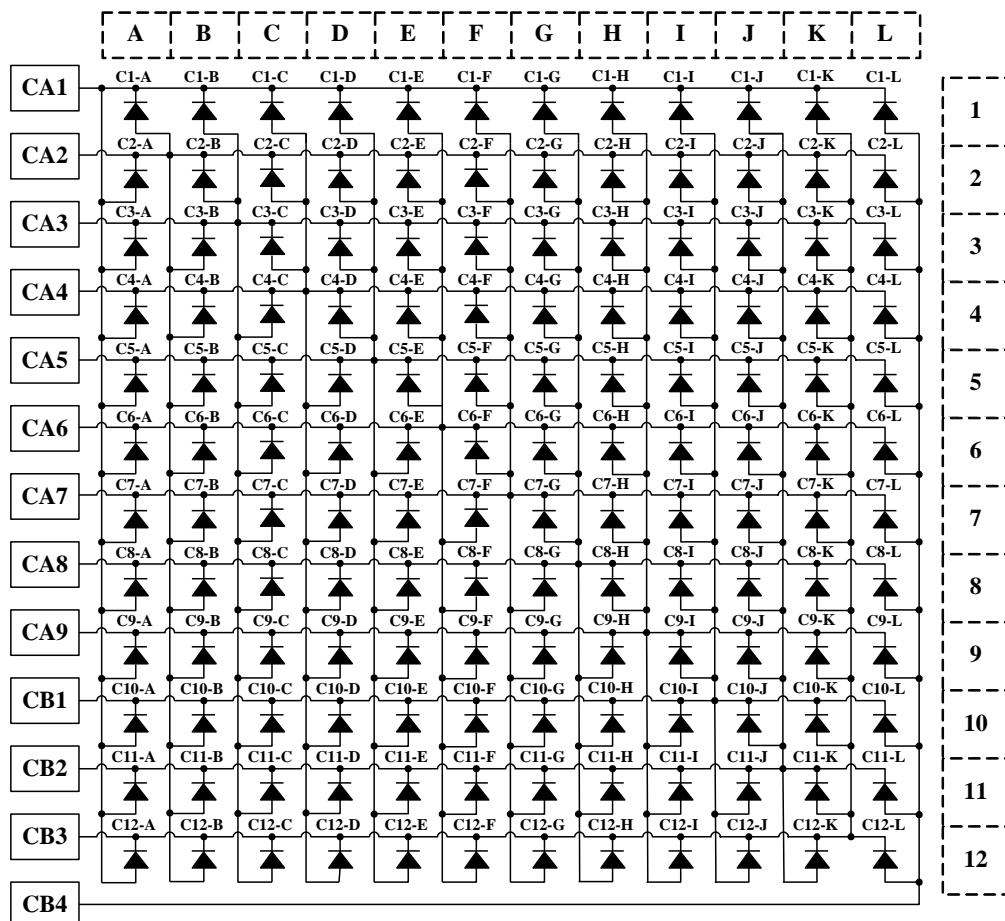
Type-1: Matrix A (9*8)



Type-1: Matrix B (9*8)

3.8.2 SLED1735 SINGLE COLOR LED IN MATRIX TYPE-2

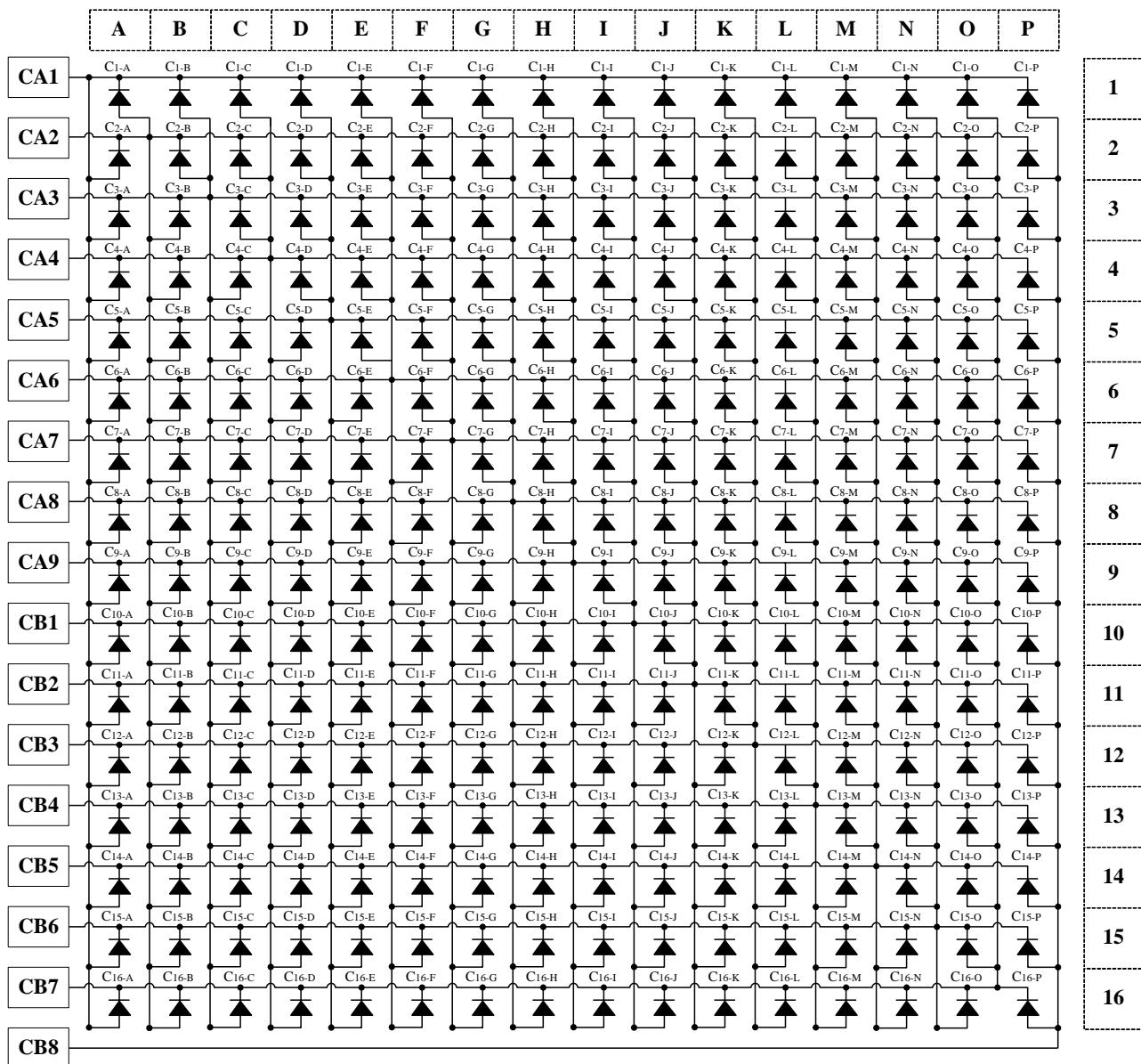
Matrix Type-2 can drive 144 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-2: 12*12

3.8.3 SLED1735 SINGLE COLOR RGB LED IN MATRIX TYPE-3

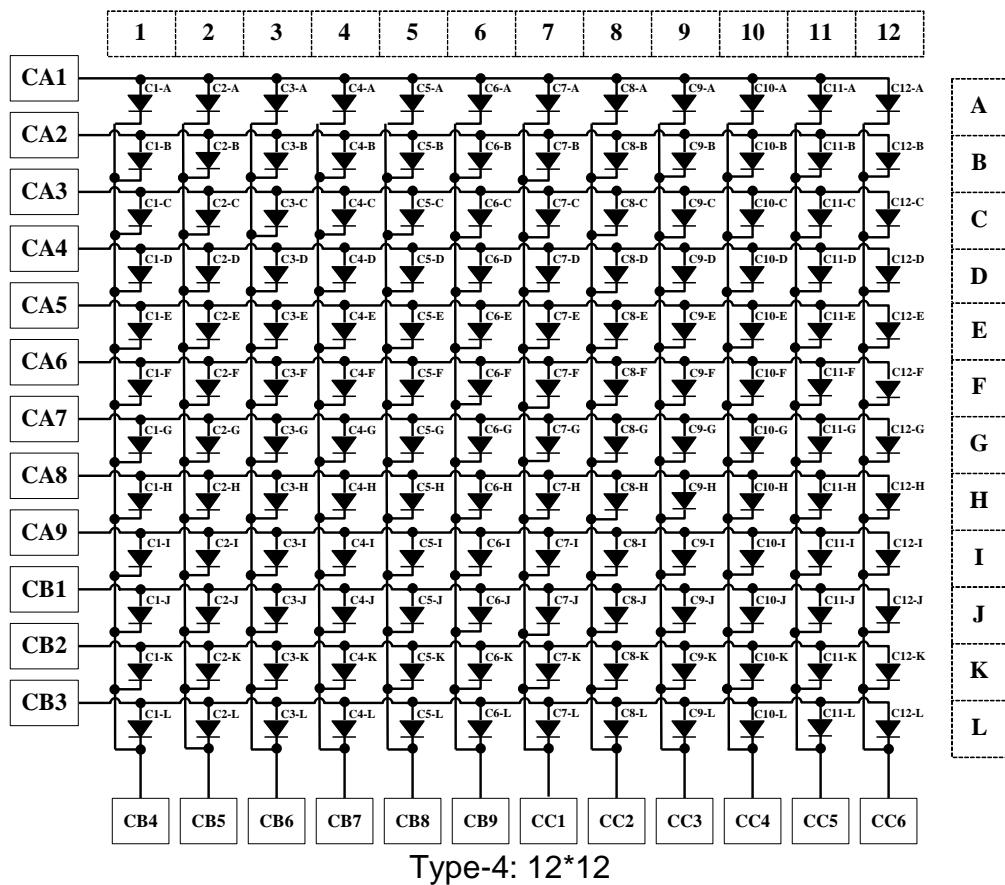
Matrix Type-3 can drive 256 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



Type-3: 16*16

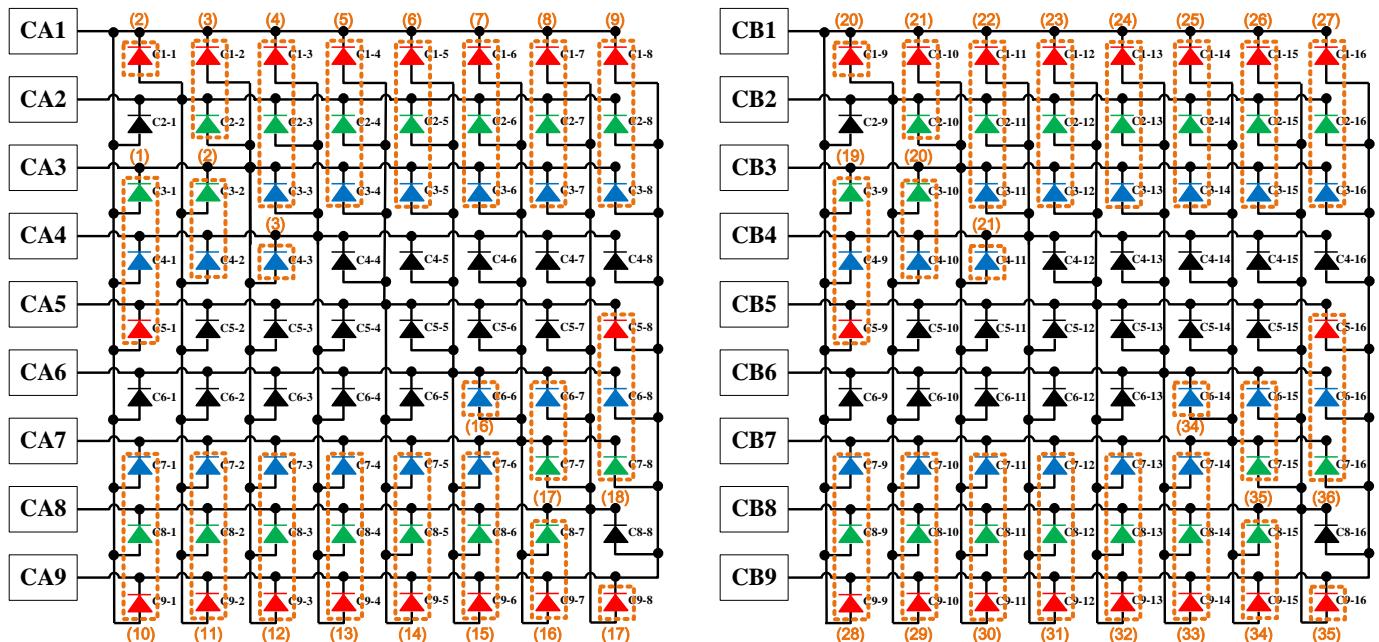
3.8.4 SLED1735 SINGLE COLOR RGB LED IN MATRIX TYPE-4

Matrix Type-4 can drive 144 single color RGB LEDs. The locations of single color LEDs are recommended as the circuit below.



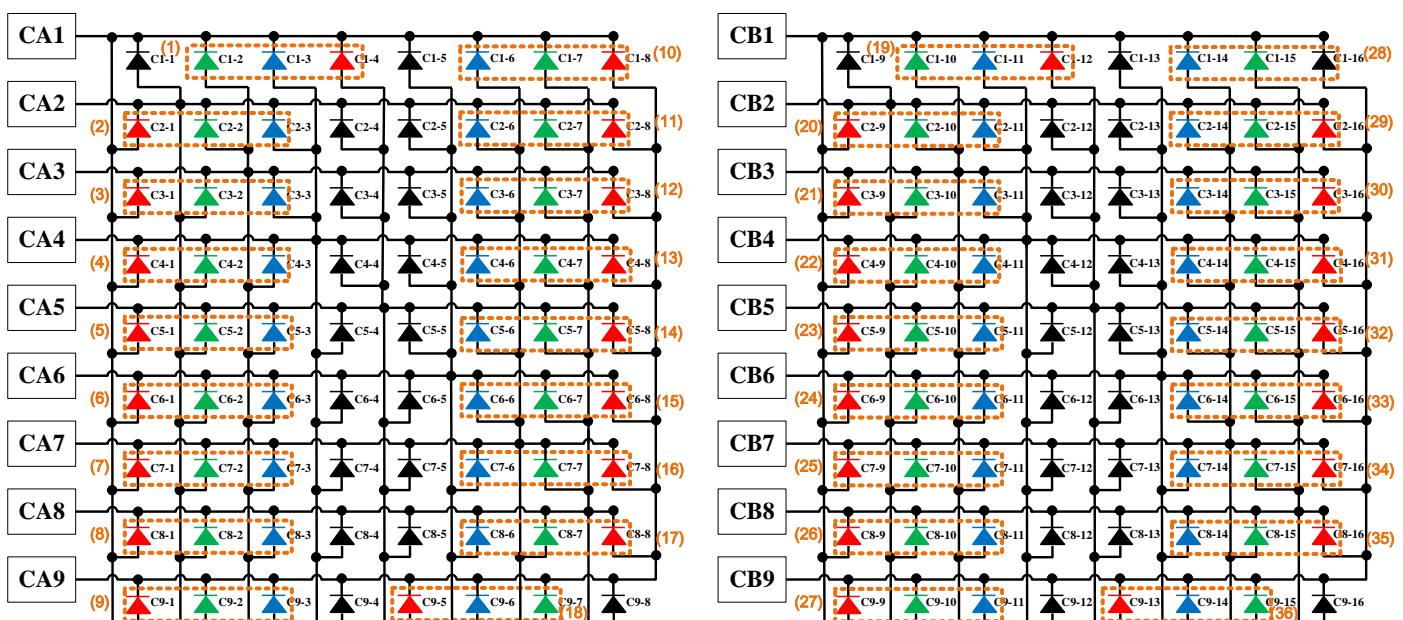
3.8.5 SLED1735 COMMON ANODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 36 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



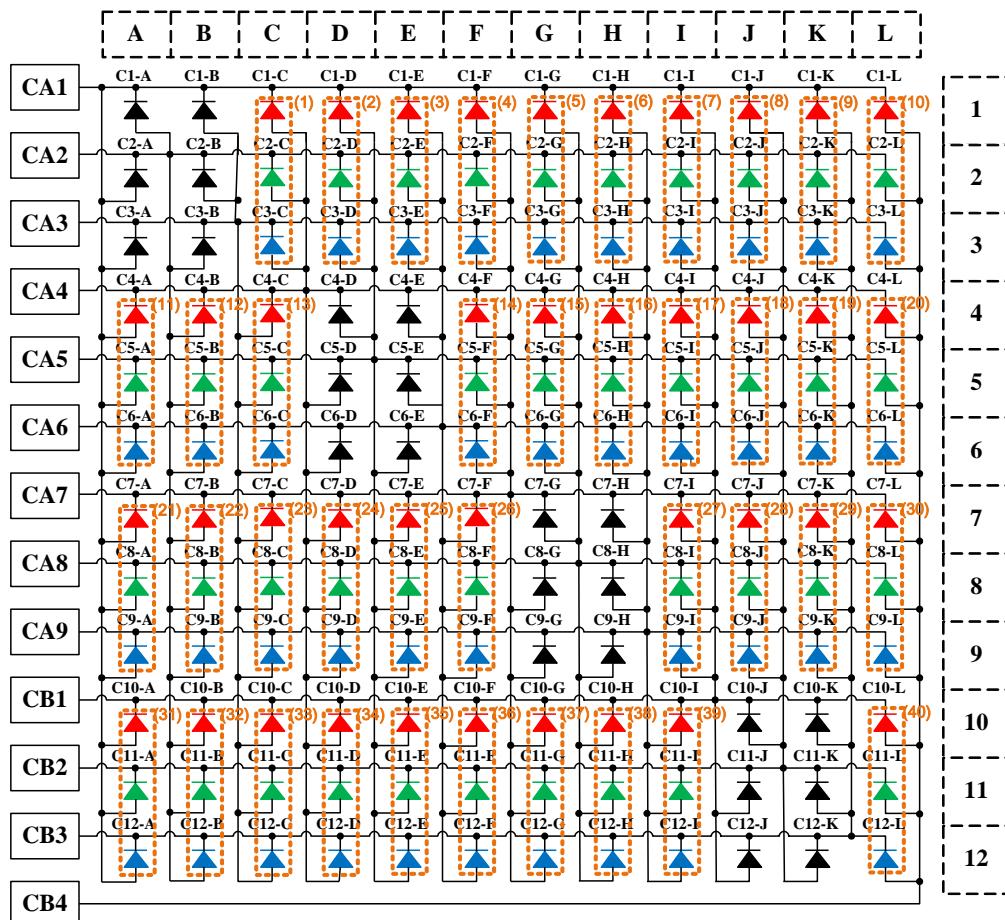
3.8.6 SLED1735 COMMON CATHODE RGB LED IN MATRIX TYPE-1

Matrix Type-1 can drive 36 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



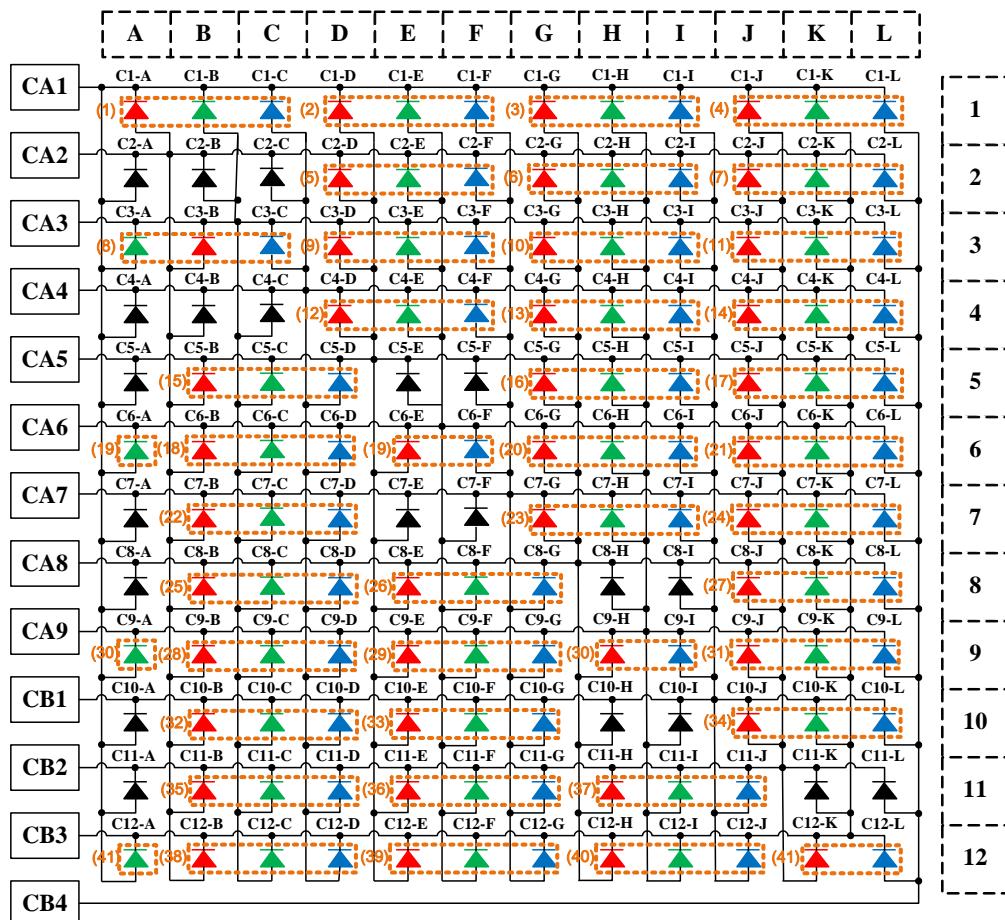
3.8.7 SLED1735 COMMON ANODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 40 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



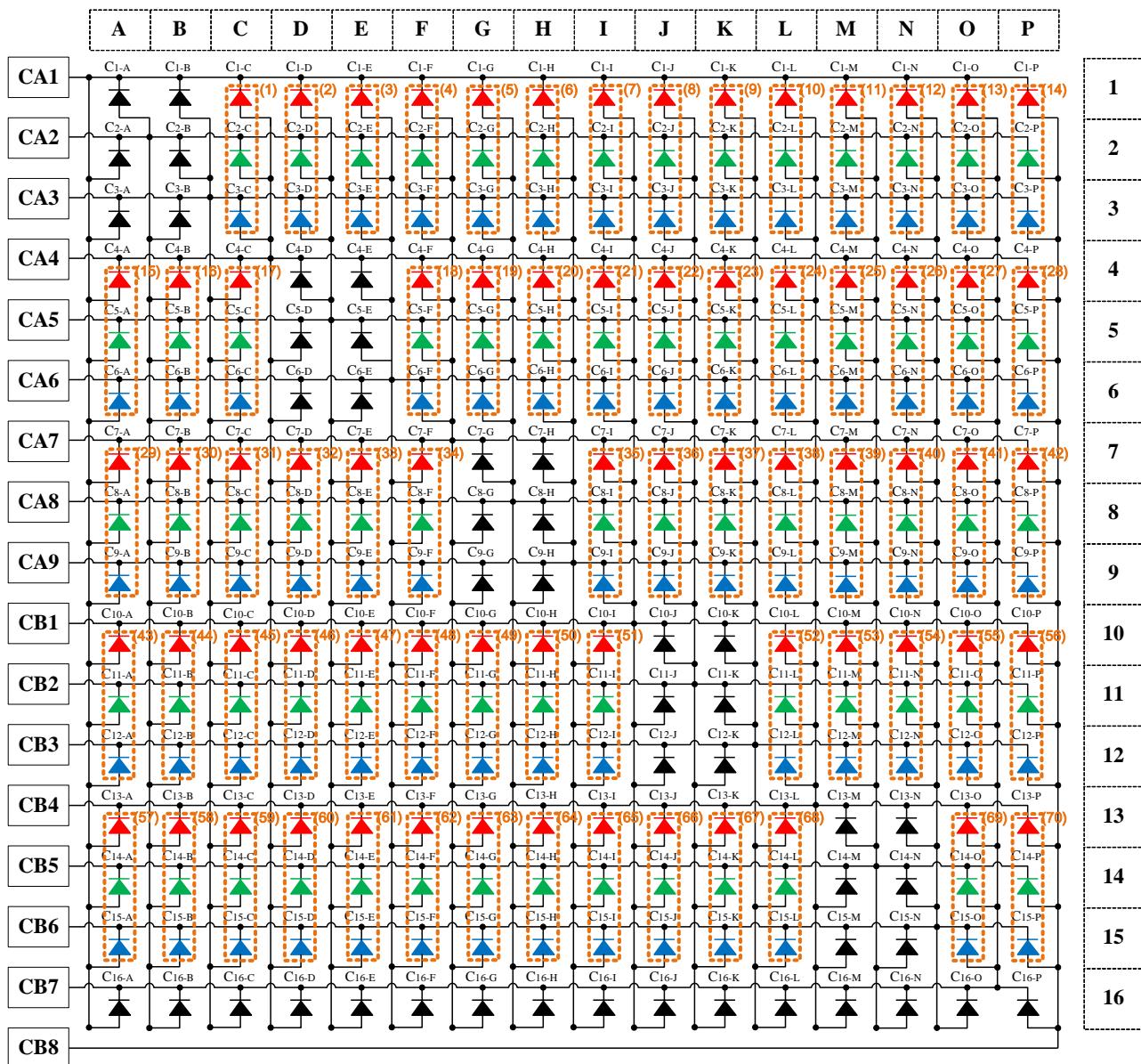
3.8.8 SLED1735 COMMON CATHODE RGB LED IN MATRIX TYPE-2

Matrix Type-2 can drive 41 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



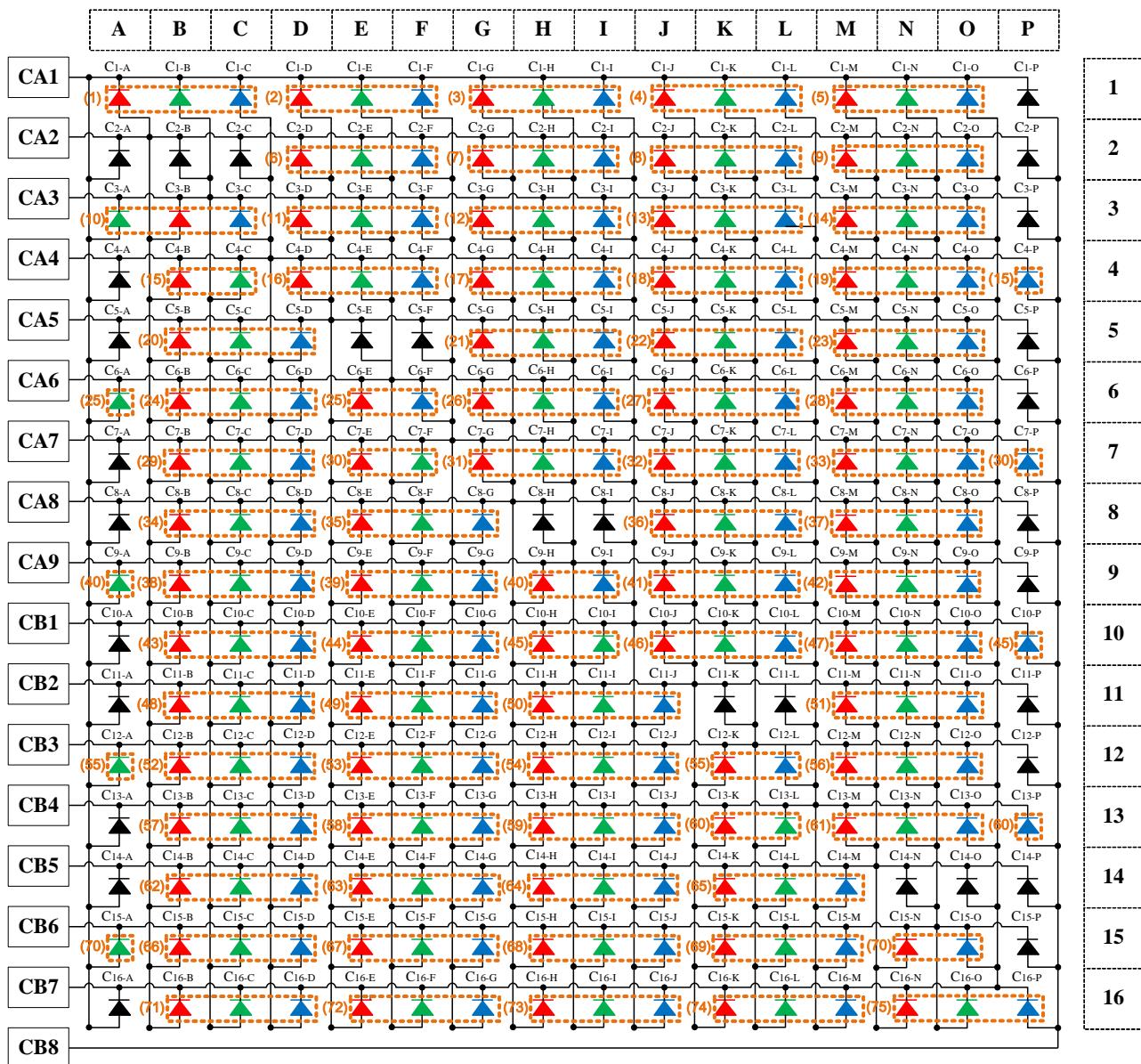
3.8.9 SLED1735 COMMON ANODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 70 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



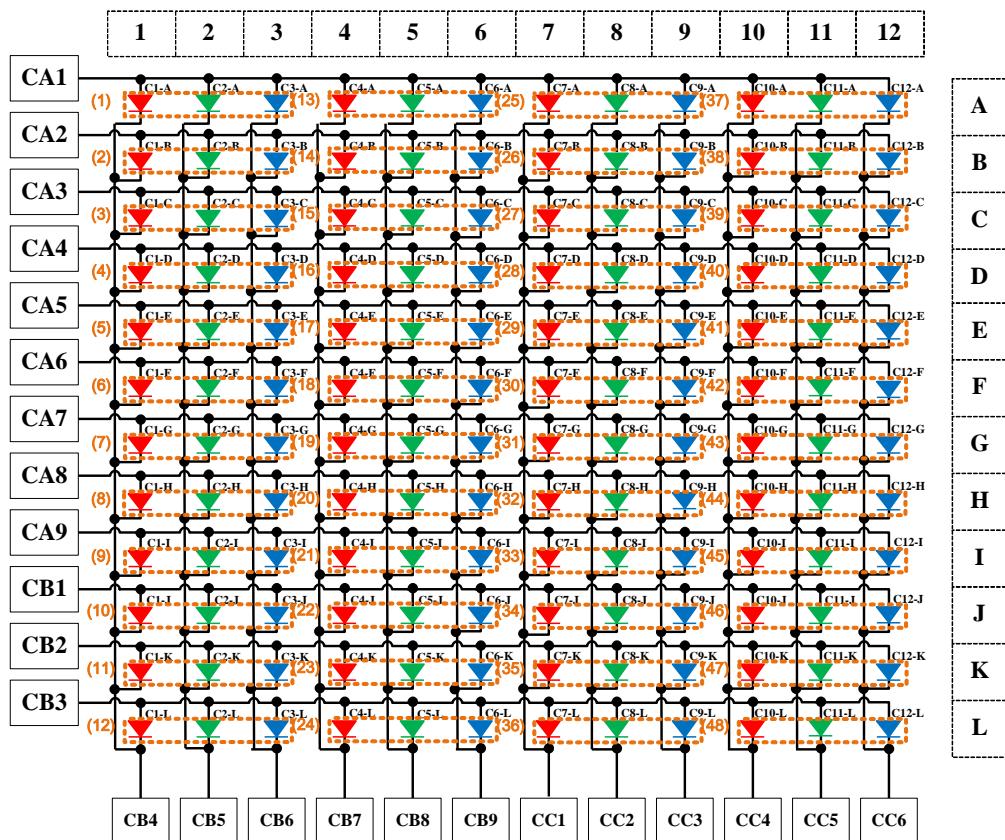
3.8.10 SLED1735 COMMON CATHODE RGB LED IN MATRIX TYPE-3

Matrix Type-3 can drive 75 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below. The LEDs in black can be Not Connected or be connected with the single color LEDs except the red one.



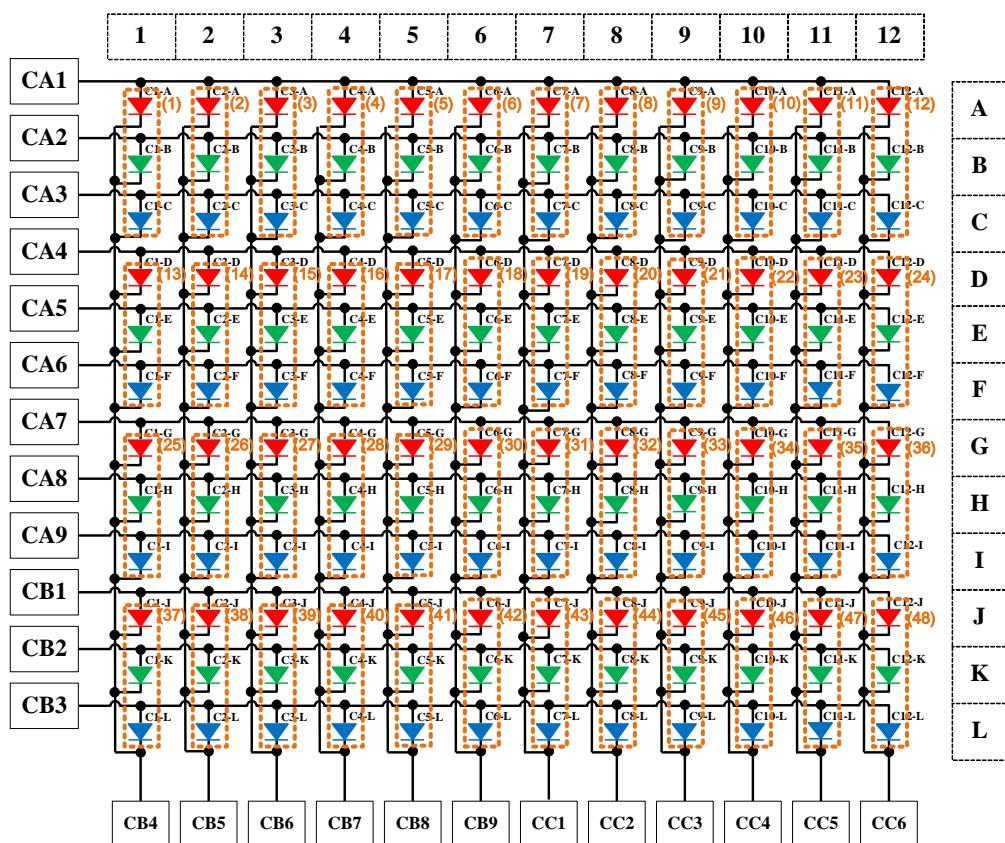
3.8.11 SLED1735 COMMON ANODE RGB LED IN MATRIX TYPE-4

Matrix Type-4 can drive 48 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.



3.8.12 SLED1735 COMMON CATHODE RGB LED IN MATRIX TYPE-4

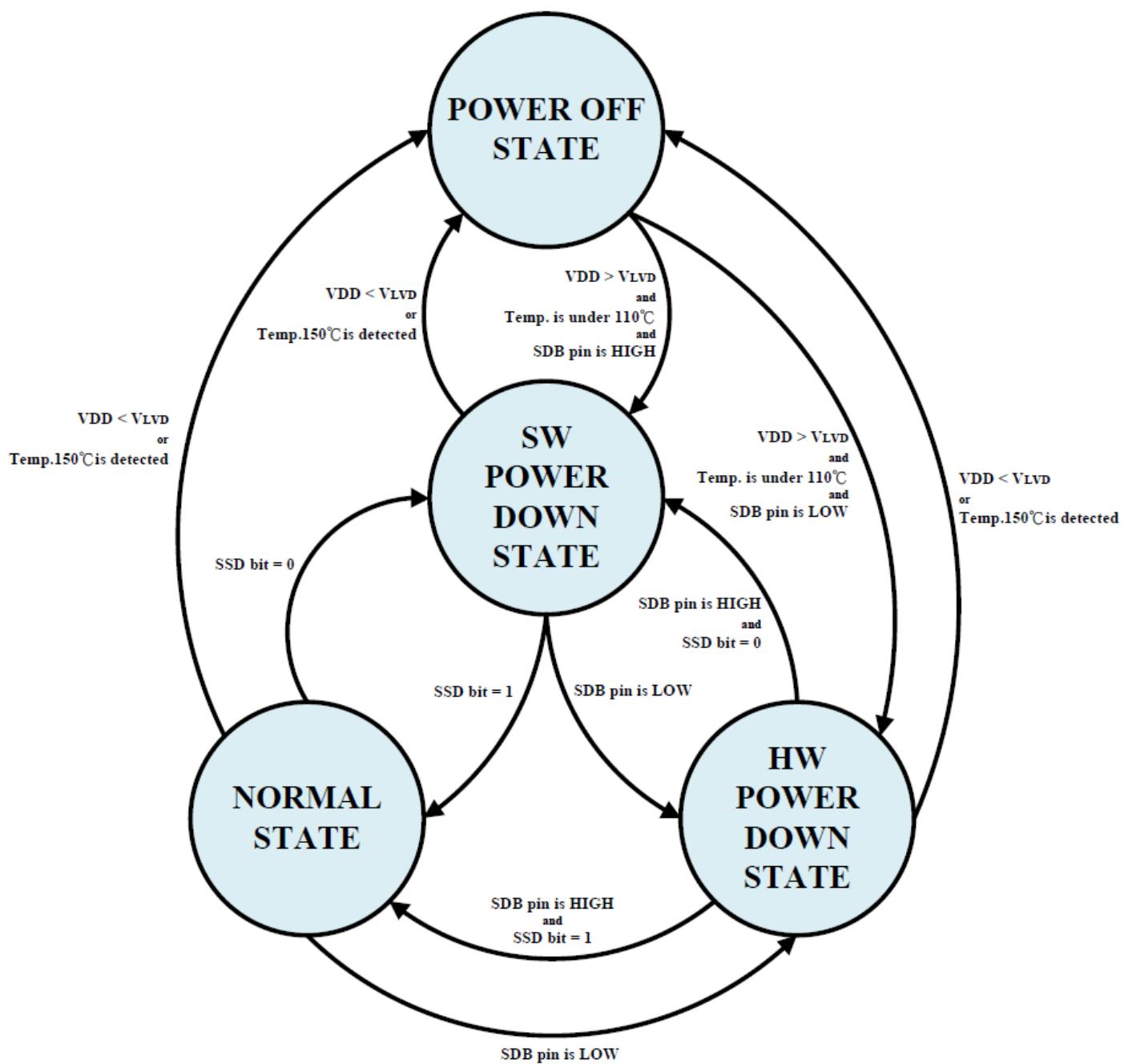
Matrix Type-4 can drive 48 common Cathode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.



4 SYSTEM OPERATION MODE

4.1 POWER STATE MACHINE FLOW CHART

Power states are determined by the VLVD threshold, the thermal detector 150°C threshold, the SDB pin state, and the software shutdown register (SSD bit) status.



4.1.1 POWER OFF STATE

When the VDD power is under VLVD threshold or the temperature is above 150°C, the system enters the POWER OFF state. In this state, the whole chip function is off. When the VDD power is above VLVD threshold or the temperature is under 110°C, a power on initial sequence is executed. During the sequence, all registers are initialized to the default

After the sequence, the system will enter the SW POWER DOWN state if SDB pin is HIGH or will enter the HW POWER DOWN state if the SDB pin is LOW.

4.1.2 SW POWER DOWN STATE

In this state, all current sources and digital drivers are switched off, so that the matrix is blanked. All registers and the SRAM data can be written or read. Normal mode requires 50 μ s into software power down mode, and 150 μ s wakeup time from software power down mode.

4.1.3 HW POWER DOWN STATE

In this state, besides all current sources and digital drivers are switched off, all registers are forbidden writing and reading. Normal mode requires 50 μ s into hardware power down mode, and 180 μ s wakeup time from hardware power down mode.

4.1.4 NORMAL STATE

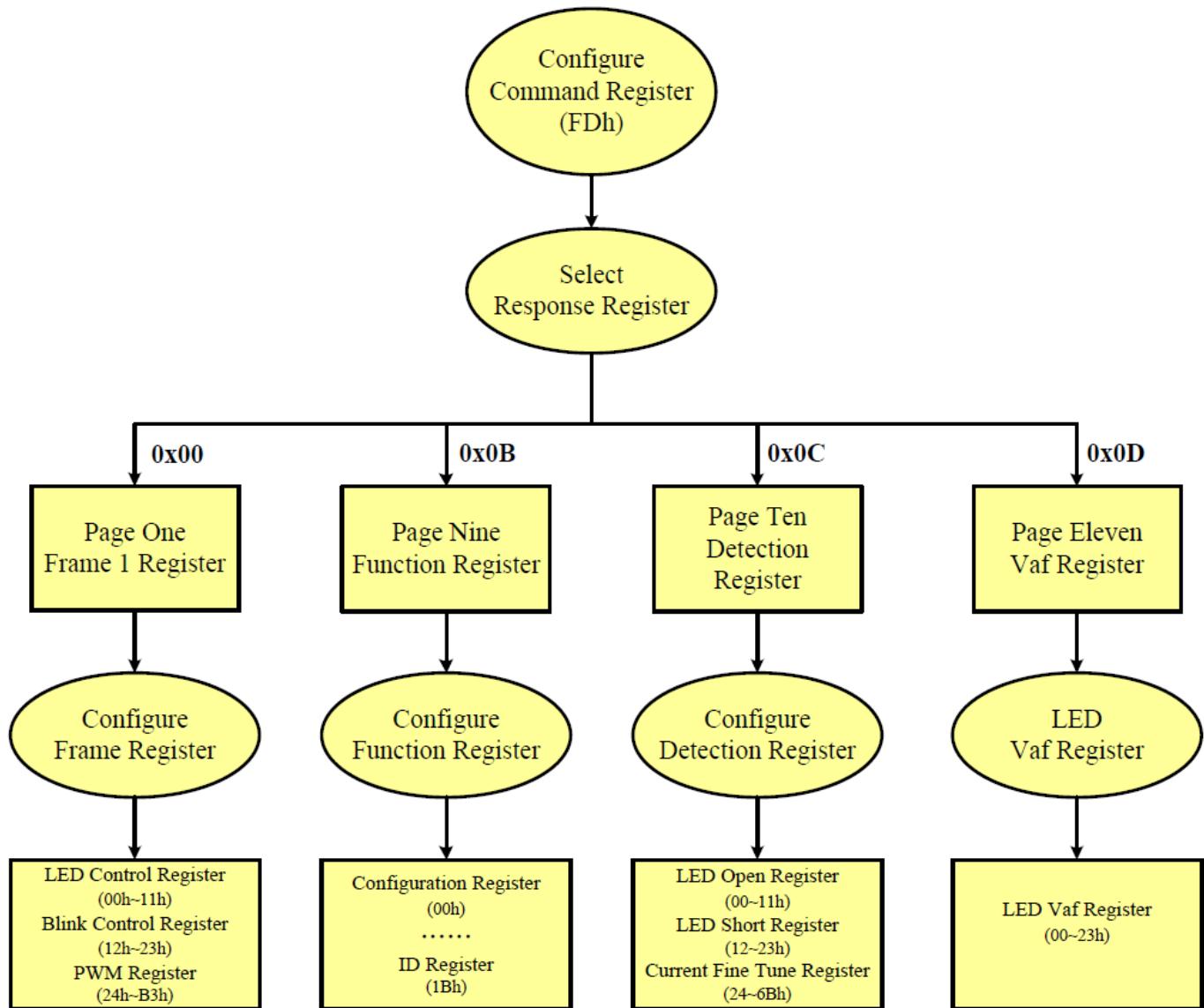
In this state, all current sources and digital drivers are operating depending on the register settings.

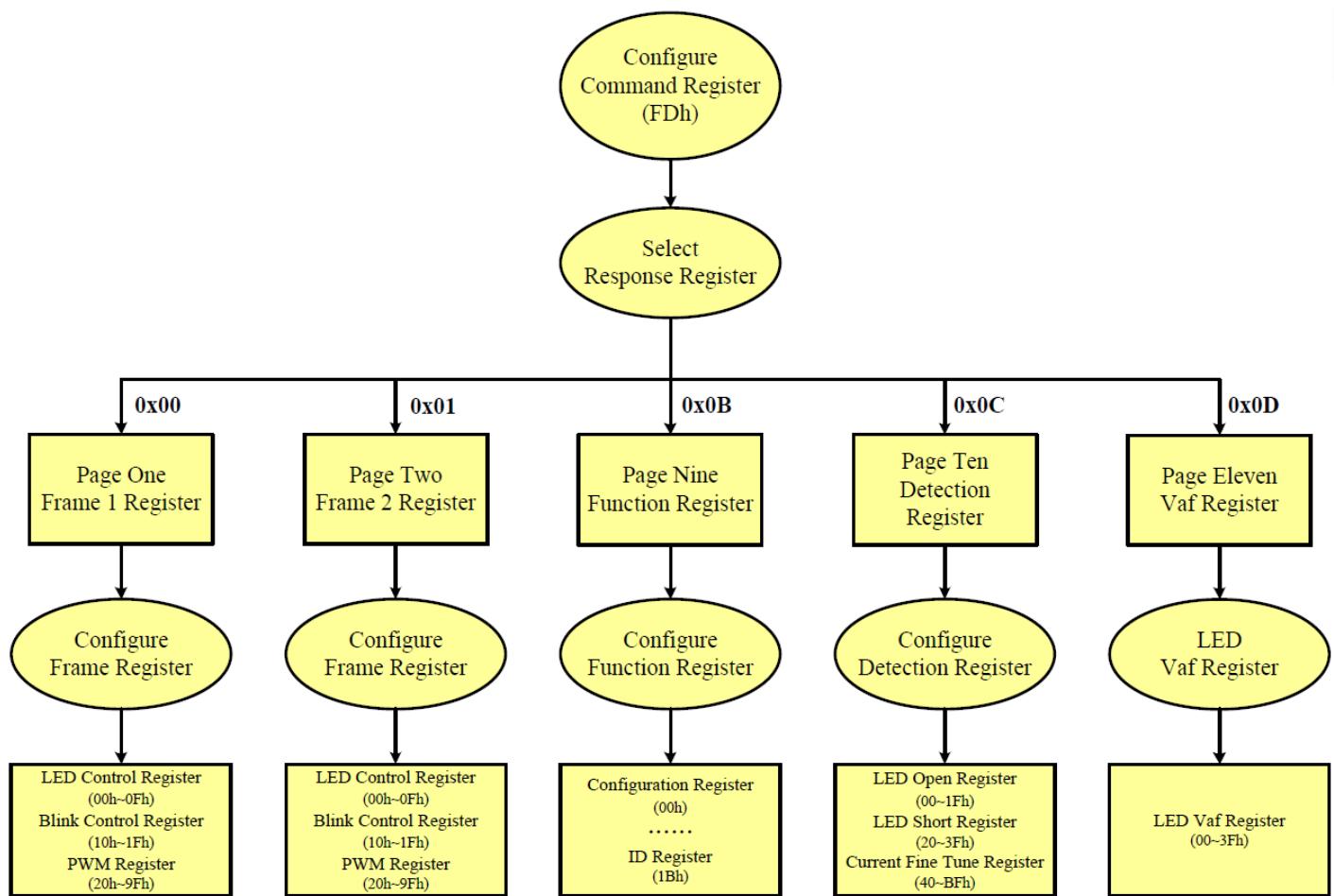
5 REGISTER DEFINITION

5.1 REGISTER CONTROL

User has to first configure the Command Register (FDh) with the following data 0x00, 0x01, 0x0B, 0x0C, or 0x0D to select the Page No., and then to configure the available registers in that Page No.

5.1.1 MATRIX TYPE 1 & 2 & 4





5.2 FDH COMMAND REGISTER

Data	Function
0x00	Point to Page One (Frame 1 Register is available)
0x01	Point to Page Two (Frame 2 Register is available)
0x0B	Point to Page Nine (Function Register is available)
0x0C	Point to Page Ten (Detection Register is available)
0x0D	Point to Page Eleven (LED Vaf Register is available)

5.3 FUNCTION REGISTER TABLE

Address	Name	Function	R/W	Default
Frame Register (Page One) for Type-1 & 2 & 4				
00h~11h	LED Control Register	Store on or off state for each LED	R/W	0000 0000b
12h~23h	Blink Control Register	Control the blink function for each LED	R/W	
24h~B3h	PWM Register	144 LEDs PWM duty cycle data register	R/W	
Frame Register (Page One) for Type-3				
00h~0Fh	LED Control Register	Store on or off state for LED C _{1-A} to C _{8-P}	R/W	0000 0000b
10h~1Fh	Blink Control Register	Control the blink function for LED C _{1-A} to C _{8-P}	R/W	
20h~9Fh	PWM Register	128 LEDs PWM duty cycle data register for LED C _{1-A} to C _{8-P}	R/W	
Frame Register (Page Two) for Type-3				
00h~0Fh	LED Control Register	Store on or off state for LED C _{9-A} to C _{16-P}	R/W	0000 0000b
10h~1Fh	Blink Control Register	Control the blink function for LED C _{9-A} to C _{16-P}	R/W	
20h~9Fh	PWM Register	128 LEDs PWM duty cycle data register for LED C _{9-A} to C _{16-P}	R/W	
Function Register (Page Nine)				
00h	Configuration Register	Configure the operation mode	R/W	0000 0000b
01h	Picture Display Register	Set the display frame in Picture Mode	R/W	
02h	Auto Play Control Register 1	Set the way of display in Auto Frame Play Mode	R/W	
03h	Auto Play Control Register 2	Set the delay time in Auto Frame Play Mode	R/W	
04h	Reserved	-	-	
05h	Display Option Register	Set the display option	R/W	
06h	Audio Synchronization Register	Set the audio synchronization function	R/W	
07h	Reserved	-	R	
08h	Breath Control Register 1	Set fade in and fade out time for breath function	R/W	
09h	Breath Control Register 2	Set the breath function	R/W	
0Ah	Shutdown Register	Set software shutdown mode	R/W	
0Bh	AGC Control	Set the AGC function and the audio gain	R/W	
0Ch	Audio ADC Rate Register	Set the ADC sample rate of the input signal	R/W	
0Dh	Staggered Delay Register	Set the staggered delay timing	R/W	
0Eh	Slew Rate Control Register	Set the slew rate control function	R/W	
0Fh	Current Control Register	Set the current source step.	R/W	0011 0001b
10h	Open Short Test Register 1	Open Short Detect	R/W	0000 0000b
11h	Open Short Test Register 2	Open Short Detect	R/W	0000 0000b
12h	Reserved	-	R	0000 0000b
13h	ADC Output	Read ADC 6-bit output	R	0000 0000b

14h	Vaf Register 1	LED anti-forward setting of Vaf1, Vaf2	R/W	0100 0100b
15h	Vaf Register 2	LED anti-forward setting of Vaf3	R/W	0000 0100b
17h	Thermal Detection Register	Temperature 70°C status	R	0010 0000b
18h	TP4Vaf Register 1	Type 4 CB4~CB7 Vaf setting.	R/W	0000 0000b
19h	TP4Vaf Register 2	Type 4 CB8~CC2 Vaf setting.	R/W	0000 0000b
1Ah	TP4Vaf Register 3	Type 4 CC3~CC6 Vaf setting.	R/W	0000 0000b
1Bh	ID Register	Chip ID	R	0111 0011b

Detection Register (Page Ten) for Type-1 & 2 & 4

00h~11h	LED Open Register	LED Open status for each LED	R	0000 0000b
12h~23h	LED Short Register	LED Short status for each LED	R	
24h~6Bh	Current Fine Tune Register	Store the current fine tune status for each LED	R/W	

Detection Register (Page Ten) for Type-3

00h~1Fh	LED Open Register	LED Open status for each LED	R	0000 0000b
20h~3Fh	LED Short Register	LED Short status for each LED	R	
40h~BFh	Current Fine Tune Register	Store the current fine tune status for each LED	R/W	

LED Location Register (Page Eleven) for Type-1 & 2 & 4

00h~23h	LED Vaf Register	Store the Vaf setting for each LED location.	R/W	0000 0000b
LED Location Register (Page Eleven) for Type-3				
00h~3Fh	LED Vaf Register	Store the Vaf setting for each LED location.	R/W	0000 0000b

5.4 FRAME REGISTER

00h~11h or 00h~0Fh	Matrix Type	Bit 7:0
LED Control Register	Type-1	$C_{n-8}:C_{n-1}$ or $C_{n-16}:C_{n-9}$, $n = 1\sim 9$
	Type-2	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
	Type-3	$C_{n-H}:C_{n-A}$, $n = 1\sim 8$ for Frame 1 $C_{n-P}:C_{n-I}$, $n = 9\sim 16$ for Frame 2
	Type-4	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
Read/Write		R/W
After Reset		0000 0000b

For Matrix Type-1, the LED Control Registers store the on or off state of each LED in the Matrix A and B;

For Matrix Type-2, the LED Control Registers store the on or off state of each LED in the 12*12 LED matrix.

For Matrix Type-3, the LED Control Registers store the on or off state of each LED in the 16*16 LED matrix.

For Matrix Type-4, the LED Control Registers store the on or off state of each LED in the 12*12 LED matrix.

The detail ordering of C_{X-Y} can be referred to section 2.3~2.6 Memory Map.

C_{X-Y}	LED State Bit
0	LED off
1	LED on

12h~23h or 10h~1Fh	Matrix Type	Bit 7:0
LED Blink Register	Type-1	$C_{n-8}:C_{n-1}$ or $C_{n-16}:C_{n-9}$, $n = 1\sim 9$
	Type-2	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
	Type-3	$C_{n-H}:C_{n-A}$ or $C_{n-P}:C_{n-I}$, $n = 1\sim 16$
	Type-4	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
Read/Write		R/W
After Reset		0000 0000b

For Matrix Type-1, the Blink Control Registers store the on or off state of each LED in the Matrix A and B;

For Matrix Type-2, the Blink Control Registers store the on or off state of each LED in the 12*12 LED matrix.

For Matrix Type-3, the Blink Control Registers store the on or off state of each LED in the 16*16 LED matrix.

For Matrix Type-4, the Blink Control Registers store the on or off state of each LED in the 12*12 LED matrix.

C_{X-Y}	Blink Control Bit
0	Disable
1	Enable

24h~B3h or 20h~9Fh	Matrix Type	Bit 7:0
PWM Register	Type-1	PWM
	Type-2	
	Type-3	
	Type-4	
Read/Write		R/W
After Reset		0000 0000b

For Matrix Type-1, 2 and 4, PWM Registers modulate the 144 LEDs in 255 steps.

For Matrix Type-3, PWM Registers modulate the 256 LEDs in 255 steps.

The detail ordering of C_{X-Y} can be referred to section 2.3~2.6 Memory Map.

Each count in PWM Register represents 416.67ns.

5.5 FUNCTION REGISTER

00h	Matrix Type	Bit 7:6	Bit 5	Bit 4	Bit 3	Bit 2:0
Configuration Register	Type-1	SYNC	-	ADCEN	MODE	-
	Type-2					
	Type-3					
	Type-4					
Read/Write		R/W	R	R/W	R/W	R
After Reset		00b	0b	0b	0b	000b

The Configuration Register sets the operating mode and synchronize mode used for cascaded LED drivers.

SYNC Synchronize Mode

00/11	High Impedance. (SYNC pin is in input pull-up state)
01	Master Mode. (SYNC pin is in output mode)
10	Slave Mode. (SYNC pin is in input mode)

ADCEN ADC Enable

0	ADC Disable, ADC value can't read in ADCO(13h).
1	ADC Enable, ADC value can read in ADCO(13h).

MODE Display Mode

0	Picture Mode Enable.
1	Picture Mode Disable, disable PWM output.

01h	Matrix Type	Bit 7:5	Bit 4:3	Bit 2:0
Picture Display Register	Type-1	-	MTYPE	-
	Type-2			
	Type-3			
	Type-4			
Read/Write		R	R/W	R
After Reset		000b	00b	000b

The Picture Display Register sets the embedded Matrix Types.

MTYPE Matrix Type

00	Matrix Type-1.
01	Matrix Type-2.
10	Matrix Type-3.
11	Matrix Type-4.

05h	Matrix Type	Bit 7:6	Bit 5:4	Bit 3	Bit 2:0
Display Option Register	Type-1	BF	-	BE	A
	Type-2				
	Type-3				
	Type-4				
Read/Write		R/W	R	R/W	R/W
After Reset		00b	00b	0	000b

The Display Option Register sets display option.

BF Blink Frame setting

00	Blink Frame is 300.
01	Blink Frame is 600.
10	Blink Frame is 75.
11	Blink Frame is 150.

BE Blink Enable

0	Disable.
1	Enable.



BPT Blink Period Time

SLED1735 Series

$$BPT = \tau \times A.$$

$$A = 0 \sim 7, \tau = 0.327\text{s}.$$

For example, when $A = 5$, $BPT = 0.327\text{s} \times 5 = 1.635\text{s}$.

The duty cycle for blink function is 50%.

Note: The Blink frame timing as bellow.

For Matrix Type-1, the Blink frame timing is 1.09ms.

For Matrix Type-2, the Blink frame timing is 1.45ms.

For Matrix Type-3, the Blink frame timing is 1.94ms.

For Matrix Type-4, the Blink frame timing is 1.45ms.

Note: The τ as below.

Blink Frame setting 00(Default), τ is 328ms(Type1), 436ms(Type2), 584ms(Type3) or 436ms(Type4).

Blink Frame setting 01, τ is 656ms (Type1), 872ms(Type2), 1164ms(Type3) or 872ms(Type4).

Blink Frame setting 10, τ is 82ms (Type1), 109ms(Type2), 146ms(Type3) or 109ms(Type4).

Blink Frame setting 11, τ is 164ms (Type1), 218ms(Type2), 292ms(Type3) or 218ms(Type4).

06h	Matrix Type	Bit 7:1	Bit 0
Audio Synchronization Register	Type-1	-	AE
	Type-2		
	Type-3		
	Type-4		
Read/Write		R	R/W
After Reset		0000 000b	0b

The Audio Synchronization Register sets the audio synchronization function.

AE Audio Synchronization Enable

0 Audio synchronization disable.

1 Enable audio signal to modulate the intensity of the matrix.

08h	Matrix Type	Bit 7	Bit 6:4	Bit 3	Bit 2:0
Breath Control Register 1	Type-1	-	A	-	B
	Type-2				
	Type-3				
	Type-4				
Read/Write		R	R/W	R	R/W
After Reset		0b	000b	0b	000b

The Breath Control Register 1 sets fade in and fade out time for breath function.

FOT Fade Out Time

$$FOT = \tau \times 2^A.$$

$$A = 0 \sim 7, \tau = 33\text{ms}. \text{ (Typical)}$$

For example, when $A = 4$, FOT is $33\text{ms} \times 2^4 = 528\text{ms}$.

FIT Fade In Time

$$FIT = \tau \times 2^B.$$

$$B = 0 \sim 7, \tau = 33\text{ms}. \text{ (Typical)}$$

For example, when $B = 4$, FOT is $33\text{ms} \times 2^4 = 528\text{ms}$.

Note: The τ calculation is as below.

For Matrix Type-1, the τ is 33ms.

For Matrix Type-2, the τ is 44ms.

For Matrix Type-3, the τ is 58ms.

For Matrix Type-4, the τ is 44ms.

09h	Matrix Type	Bit 7:6	Bit 5	Bit 4	Bit 3	Bit 2:0
Breath Control Register 2	Type-1	-	CB_EN	B_EN	-	A
	Type-2					
	Type-3					
	Type-4					
Read/Write		R	R/W	R/W	R	R/W
After Reset		000b	0b	0b	0b	000b

The Breath Control Register 2 sets the breath function.

CB_EN **Continuous Breath Enable**

0 Disable.

1 Enable continuous breath function.

B_EN **Breath Enable**

0 Disable.

1 Enable.

ET **Extinguish Time**

$$ET = \tau \times 2^A$$

A = 0~7, τ = 4.3ms. (Typical)

For example, when A = 4, ET = 4.3ms $\times 2^4$ = 68.8ms.

Note: The τ calculation is as below.

For Matrix Type-1, the τ is 4.3ms.

For Matrix Type-2, the τ is 5.8ms.

For Matrix Type-3, the τ is 7.7ms..

For Matrix Type-4, the τ is 5.8ms.

0Ah	Matrix Type	Bit 7:1	Bit 0
Shutdown Register	Type-1	-	SSD
	Type-2		
	Type-3		
	Type-4		
Read/Write		R	R/W
After Reset		0000 000b	0b

The Shutdown Register sets software shutdown mode.

SSD **Shutdown Control**

0 SW Shutdown Mode.

1 Normal Mode.

0Bh	Matrix Type	Bit 7:5	Bit 4	Bit 3	Bit 2:0
AGC Control Register	Type-1	-	AGCM	AGC	AGS
	Type-2				
	Type-3				
	Type-4				
Read/Write		R	R/W	R/W	R/W
After Reset		000b	0b	0b	000b

The AGC Control Register sets the AGC function and the audio gain.

AGCM	AGC Mode
0	Slow Mode.
1	Fast Mode.

AGC	AGC Enable
0	Disable.
1	Enable.

AGS	Audio Gain Selection
000	0dB.
001	3dB.
010	6dB.
011	9dB.
100	12dB.
101	15dB.
110	18dB.
111	21dB.

0Dh	Matrix Type	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
Staggered Delay Register	Type-1	STD4	STD3	STD2	STD1
	Type-2				
	Type-3				
	Type-4				
Read/Write		R/W	R/W	R/W	R/W
After Reset		00b	00b	00b	00b

The Staggered Delay Register sets the staggered delay timing for each current source IO.

STD1~4 Staggered Delay Timing

00	Group 1: Zero delay.
01	Group 2: Less delay.
10	Group 3: Medium delay.
11	Group 4: Maximum delay.

STD1 delay time T_{STD1} is used on CA1, CA5, CA9, CB4, and CB8.

STD2 delay time T_{STD2} is used on CA2, CA6, CB1, CB5, and CB9.

STD3 delay time T_{STD3} is used on CA3, CA7, CB2, and CB6.

STD4 delay time T_{STD4} is used on CA4, CA8, CB3, and CB7.

STD1~4 are only applicable on the state of IO current source output but not on the state of IO floating or sinking low.

0Eh	Matrix Type	Bit 7:1	Bit 0
Slew Rate Control Register	Type-1	-	SL
	Type-2		
	Type-3		
	Type-4		
Read/Write		R	R/W
After Reset		0000 000b	0b

The Slew Rate Control Register sets the slew rate of current source IO.

SL Slew Rate Enable

0	Disable.
1	Enable.

Enabling SL Register make the all current source IO have a smooth signal from floating to output high.

0Fh	Matrix Type	Bit 7	Bit 6	Bit 5:0
Current Control	Type-1	CCSEN	-	CCS
	Type-2			

Register	Type-3			
	Type-4			
Read/Write	R/W	R		R/W
After Reset	0b	0b		11 0001b

The Current Control Register sets the constant current step of all current source IOs.

CCSEN Constant Current Enable

- 0 Disable.
1 Enable.

CCS Constant Current Step

If CCS = 0, constant current control is disabled. The output current I_{out} is 8mA.

If CCS = 1~63, constant source current I_{out} is $[8 + (CCS) \times 0.5]$ mA.

For example, when CCS = 48, I_{out} is $[8 + (48) \times 0.5] = 32$ mA

10h	Matrix Type	Bit 7	Bit 6	Bit 5:0
Open Short Test Register 1	Type-1	ODS	SDS	OSDD
	Type-2			
	Type-3			
	Type-4			
Read/Write	R/W	R/W		R/W
After Reset	0b	0b		00 0000b

The Open Short Test Register 1 is used to enable the open/short detection test and latched duty.

ODS Open Detection Start

- 0 Not enable open detection test. (H/W clear automatically)
1 Start open detection test.

SDS Short Detection Start

- 0 Not enable short detection test. (H/W clear automatically)
1 Start short detection test.

OSDD Open Short Detection Duty

The PWM duty that Open Short detection is latched.

The latched duty 0 is reserved, and the usable duty ranges from 1~63.

For example, when OSDD is 16, the open short latched duty is 16.

Note: The open short detection matrix depends on the setting of MTYPE in Configuration Register.

Note: Once OSDS is set, all other operation modes are ignored and the system starts to re-run the LED matrix for the LED open short detection. And the OSDS will be cleared as '0' by H/W automatically. After the open short detection has completed scanning the full LED matrix, the OSDINT will be set as '1' by H/W automatically.

Note: To do open short detection or not depends on the LED Control Register setting. Any bit set as '0' in LED Control Register means no open short detection will run at that corresponding LED location. Also, the corresponding bit in LED Open Register and LED Short Register will be always set as '0' after open short detection is completed.

11h	Matrix Type	Bit 7	Bit 6	Bit 5:0
Open Short Test Register 2	Type-1	ODINT	SDINT	-
	Type-2			
	Type-3			
	Type-4			
Read/Write	R/W	R/W		R
After Reset	0b	0b		00 0000b

The Open Short Test Register 2 is used to indicate the open/short detection status.

ODINT	Open Detection Interrupt
0	Open detection test is not completed.
1	Open detection test is completed. (H/W set automatically)

SDINT	Short Detection Interrupt
0	Short detection test is not completed.
1	Short detection test is completed. (H/W set automatically)

13h	Matrix Type	Bit 7	Bit 6:0
ADC Output Register	Type-1	-	ADCO
	Type-2		
	Type-3		
	Type-4		
Read/Write	R		R
After Reset	0b		000 0000b

The ADC Output Register indicates the real time 6-bit ADC counts of the voltage measured from AGCIN pin with the converting rate 120 KHz.

14h	Matrix Type	Bit 7	Bit 6:4	Bit 3	Bit 2:0
VAF Register 1	Type-1	-	VAF2	-	VAF1
	Type-2				
	Type-3				
	Type-4				
Read/Write	R		R/W	R	R/W
After Reset	0b		100b	0b	100b

VAF1	Vaf1 fine tune setting.
000-011	Vaf1 voltage is decrement.
100	Default Vaf1 voltage setting.
101-111	Vaf1 voltage is increment.

VAF2	Vaf2 fine tune setting.
000-011	Vaf2 voltage is decrement.
100	Default Vaf2 voltage setting.
101-111	Vaf2 voltage is increment.

15h	Matrix Type	Bit 7:6	Bit 5:3	Bit 2:0
VAF Register 2	Type-1	FVAF	FVAFT	VAF3
	Type-2			
	Type-3			
	Type-4			
Read/Write	R/W		R/W	R/W
After Reset	00b		000b	100b

FVAF	Force Vaf control bit.
00	Enable Force Vaf.
01	Enable Force Vaf, and enable time by FVAFT.
10	Disable Force Vaf.
11	Reserved.

FVAFT	Force Vaf time Setting.
000	Default setting.
001-111	Vaf time is increment.

VAF3	Vaf3 fine tune setting.
000	Vaf3 is VDD.
001-011	Vaf3 voltage is decrement.
100	Default Vaf3 voltage setting.
101-111	Vaf3 voltage is increment.

17h	Matrix Type	Bit 7:4	Bit 3	Bit 2:0
Thermal Detection Register	Type-1		TDF	-
	Type-2			
	Type-3			
	Type-4			
Read/Write		R	R	R
After Reset		0010b	0b	000b

TDF Thermal detect Flag

0 System temperature is under 70°C.

1 System temperature reaches or is over 70°C.

18h	Matrix Type	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
TP4Vaf Register 1	Type-4	TP4VAF_CB7	TP4VAF_CB6	TP4VAF_CB5	TP4VAF_CB4
Read/Write		R/W	R/W	R/W	R/W
After Reset		00b	00b	00b	00b

19h	Matrix Type	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
TP4Vaf Register 2	Type-4	TP4VAF_CC2	TP4VAF_CC1	TP4VAF_CB9	TP4VAF_CB4
Read/Write		R/W	R/W	R/W	R/W
After Reset		00b	00b	00b	00b

1Ah	Matrix Type	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0
TP4Vaf Register 3	Type-4	TP4VAF_CC6	TP4VAF_CC5	TP4VAF_CC4	TP4VAF_CC3
Read/Write		R/W	R/W	R/W	R/W
After Reset		00b	00b	00b	00b

TP4VAF_Cxx Vaf setting for Matrix Type-4's sinking channels.

00 Vaf2.

01 Vaf1.

10 Vaf3.

11 No Vaf, floating.

1Bh	Matrix Type	Bit 7:0
ID Register	Type-1	ID
	Type-2	
	Type-3	
	Type-4	
Read/Write		R
After Reset		0111 0011b

Note: The suggested ID Register check 0x7X. (X = don't care)

5.6 DETECTION REGISTER

00h~11h or 00h~0Fh	Matrix Type	Bit 7:0
LED Open Register	Type-1	$C_{n-8}:C_{n-1}$ or $C_{n-16}:C_{n-9}$, $n = 1\sim 9$
	Type-2	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
	Type-3	$C_{n-H}:C_{n-A}$ or $C_{n-P}:C_{n-I}$, $n = 1\sim 16$
	Type-4	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
Read/Write		R/W
After Reset		0000 0000

For Matrix Type-1, the LED Open Registers store the LED open test result of each LED in the Matrix A and B;

For Matrix Type-2, the LED Open Registers store the LED open test result of each LED in the 12*12 LED matrix.

For Matrix Type-3, the LED Open Registers store the LED open test result of each LED in the 16*16 LED matrix.

For Matrix Type-4, the LED Open Registers store the LED open test result of each LED in the 12*12 LED matrix.

Cx-y LED Open State

- | | |
|---|-------------------------------------|
| 0 | This LED is detected as 'not OPEN'. |
| 1 | This LED is detected as 'OPEN'. |

Note: LED is detected as 'OPEN' state when the detected constant current output voltage at M-PWM IO is over VDD – 0.5V. And it is only valid if the corresponding bit in LED Control Register is set as '1'.

12h~23h or 20h~3Fh	Matrix Type	Bit 7:0
LED Short Register	Type-1	$C_{n-8}:C_{n-1}$ or $C_{n-16}:C_{n-9}$, $n = 1\sim 9$
	Type-2	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
	Type-3	$C_{n-H}:C_{n-A}$ or $C_{n-P}:C_{n-I}$, $n = 1\sim 16$
	Type-4	$C_{n-H}:C_{n-A}$ or $C_{(n+1)-D}:C_{n-I}$ or $C_{(n+1)-L}:C_{(n+1)-E}$, $n = 1, 3, 5, 7, 9, 11$
Read/Write		R/W
After Reset		0000 0000

For Matrix Type-1, the LED Short Registers store the LED short test result of each LED in the Matrix A and B;

For Matrix Type-2, the LED Short Registers store the LED short test result of each LED in the 12*12 LED matrix.

For Matrix Type-3, the LED Short Registers store the LED short test result of each LED in the 16*16 LED matrix.

For Matrix Type-4, the LED Short Registers store the LED short test result of each LED in the 12*12 LED matrix.

Cx-y LED Short State

- | | |
|---|--------------------------------------|
| 0 | This LED is detected as 'not SHORT'. |
| 1 | This LED is detected as 'SHORT'. |

Note: LED is detected as 'SHORT' state when the detected constant current output voltage at M-PWM IO is under VSS + 0.5V. And it is only valid if the corresponding bit in LED Control Register is set as '1'.

24h~6Bh or 40h~BFh	Matrix Type	Bit 7:4	Bit 3:0
Current Fine Tune Register	Type-1	$C_{n-(m+1)}$, $n = 1\sim 9 \& m = 1, 3, 5, 7, 9, 11, 13, 15$	C_{n-m} , $n = 1\sim 9 \& m = 1, 3, 5, 7, 9, 11, 13, 15$
	Type-2	$C_{n-(m+1)}$, $n = 1\sim 12 \& m = A, C, E, G, I, K$	C_{n-m} , $n = 1\sim 12 \& m = A, C, E, G, I, K$
	Type-3	$C_{n-(m+1)}$, $n = 1\sim 16 \& m = A, C, E, G, I, K, M, O$	C_{n-m} , $n = 1\sim 16 \& m = A, C, E, G, I, K, M, O$
	Type-4	$C_{n-(m+1)}$, $n = 1\sim 12 \& m = A, C, E, G, I, K$	C_{n-m} , $n = 1\sim 12 \& m = A, C, E, G, I, K$
Read/Write		R/W	R/W
After Reset		0000	0000

For Matrix Type-1, the Current Fine Tune Registers store the fine tune current parameter of each LED in the Matrix A and B;

For Matrix Type-2, the Current Fine Tune Registers store the fine tune current parameter of each LED in the 12*12 LED matrix.

For Matrix Type-3, the Current Fine Tune Registers store the fine tune current parameter of each LED in the 16*16 LED matrix.

For Matrix Type-4, the Current Fine Tune Registers store the fine tune current parameter of each LED in the 12*12 LED matrix.

C_{x-y}	Fine Tune Current
0000	Default current
0001	+125uA
0010	+250uA
0011	+375uA
0100	+500uA
0101	+625uA
0110	+750uA
0111	+875uA
1000	-125uA
1001	-250uA
1010	-375uA
1011	-500uA
1100	-625uA
1101	-750uA
1110	-875uA
1111	-1000uA

5.7 LED VAF REGISTER

00h~23h or 00h~3Fh	Matrix Type	Bit 7:6	Bit 3:0	Bit 3:2	Bit 1:0
LED Vaf Register	Type-1	$Vaf_C_{n-(m+3)}$	$Vaf_C_{n-(m+2)}$	$Vaf_C_{n-(m+1)}$	Vaf_C_{n-m}
				$n = 1\sim 9, m = 1, 5, 9, 13$	
	Type-2	$Vaf_C_{n-(m+3)}$	$Vaf_C_{n-(m+2)}$	$Vaf_C_{n-(m+1)}$	Vaf_C_{n-m}
				$n = 1\sim 12, m = A, E, I$	
	Type-3	$Vaf_C_{n-(m+3)}$	$Vaf_C_{n-(m+2)}$	$Vaf_C_{n-(m+1)}$	Vaf_C_{n-m}
				$n = 1\sim 16, m = A, E, I, M$	
	Type-4	$Vaf_C_{n-(m+3)}$	$Vaf_C_{n-(m+2)}$	$Vaf_C_{n-(m+1)}$	Vaf_C_{n-m}
				$n = 1\sim 12, m = A, E, I$	
Read/Write		R/W	R/W	R/W	R/W
After Reset		00b	00b	00b	00b

For Matrix Type-1, the LED Vaf Registers store the Vaf setting of each LED in the Matrix A and B;

For Matrix Type-2, the LED Vaf Registers store the Vaf setting of each LED in the 12*12 LED matrix.

For Matrix Type-3, the LED Vaf Registers store the Vaf setting of each LED in the 16*16 LED matrix.

For Matrix Type-4, the LED Vaf Registers store the Vaf setting of each LED in the 12*12 LED matrix.

Vaf_Cxx[1:0] LED Vaf Setting

00	Vaf2.
01	Vaf1.
10	Vaf3.
11	No Vaf, floating.

6 PHASE MECHANISM

6.1 PHASE SEQUENCE

6.1.1 PHASE SEQUENCE OF MATRIX TYPE-1

For Matrix Type-1, there are total 9 phases in a frame. And each phase contains two sub-phases: Current Source phase and blanking phase. The following table shows the phase sequence in order.

Phase	LED State					
	Matrix A			Matrix B		
	LED Location	Current Source IOs	Sink IO	LED Location	Current Source IOs	Sink IO
1-1	C ₁₋₁ ~C ₁₋₈	CA2~CA9	CA1	C ₁₋₉ ~C ₁₋₁₆	CB2~CB9	CB1
1-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
2-1	C ₂₋₁ ~C ₂₋₈	CA1, CA3~CA9	CA2	C ₂₋₉ ~C ₂₋₁₆	CB1, CB3~CB9	CB2
2-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
3-1	C ₃₋₁ ~C ₃₋₈	CA1~CA2, CA4~CA9	CA3	C ₃₋₉ ~C ₃₋₁₆	CB1~CB2, CB4~CB9	CB3
3-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
4-1	C ₄₋₁ ~C ₄₋₈	CA1~CA3, CA5~CA9	CA4	C ₄₋₉ ~C ₄₋₁₆	CB1~CB3, CB5~CB9	CB4
4-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
5-1	C ₅₋₁ ~C ₅₋₈	CA1~CA4, CA6~CA9	CA5	C ₅₋₉ ~C ₅₋₁₆	CB1~CB4, CB6~CB9	CB5
5-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
6-1	C ₆₋₁ ~C ₆₋₈	CA1~CA5, CA7~CA9	CA5	C ₆₋₉ ~C ₆₋₁₆	CB1~CB5, CB7~CB9	CB6
6-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
7-1	C ₇₋₁ ~C ₇₋₈	CA1~CA6, CA8~CA9	CA7	C ₇₋₉ ~C ₇₋₁₆	CB1~CB6, CB8~CB9	CB7
7-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
8-1	C ₈₋₁ ~C ₈₋₈	CA1~CA7, CA9	CA8	C ₈₋₉ ~C ₈₋₁₆	CB1~CB7, CB9	CB8
8-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf
9-1	C ₉₋₁ ~C ₉₋₈	CA1~CA8	CA9	C ₈₋₉ ~C ₈₋₁₆	CB1~CB8	CB9
9-2	-	By Vaf	By Vaf	-	By Vaf	By Vaf

6.1.2 PHASE SEQUENCE OF MATRIX TYPE-2

For Matrix Type-2, there are total 12 phases in a frame. And each phase contains two sub-phases: Current Source phase and blanking phase. The following table shows the phase sequence in order.

Phase	LED State		
	LED Location	Current Source IOs	Sink IO
1-1	C _{1-A} ~C _{1-L}	CA2~CA9, CB1~CB4	CA1
1-2	-	By Vaf	By Vaf
2-1	C _{2-A} ~C _{2-L}	CA1, CA3~CA9, CB1~CB4	CA2
2-2	-	By Vaf	By Vaf
3-1	C _{3-A} ~C _{3-L}	CA1~CA2, CA4~CA9, CB1~CB4	CA3
3-2	-	By Vaf	By Vaf
4-1	C _{4-A} ~C _{4-L}	CA1~CA3, CA5~CA9, CB1~CB4	CA4
4-2	-	By Vaf	By Vaf
5-1	C _{5-A} ~C _{5-L}	CA1~CA4, CA6~CA9, CB1~CB4	CA5
5-2	-	By Vaf	By Vaf
6-1	C _{6-A} ~C _{6-L}	CA1~CA5, CA7~CA9, CB1~CB4	CA5
6-2	-	By Vaf	By Vaf
7-1	C _{7-A} ~C _{7-L}	CA1~CA6, CA8~CA9, CB1~CB4	CA7
7-2	-	By Vaf	By Vaf
8-1	C _{8-A} ~C _{8-L}	CA1~CA7, CA9, CB1~CB4	CA8
8-2	-	By Vaf	By Vaf
9-1	C _{9-A} ~C _{9-L}	CA1~CA8, CB2~CB4	CA9
9-2	-	By Vaf	By Vaf
10-1	C _{10-A} ~C _{10-L}	CA1~CA9, CB2~CB4	CB1
10-2	-	By Vaf	By Vaf
11-1	C _{11-A} ~C _{11-L}	CA1~CA9, CB1, CB3~CB4	CB2
11-2	-	By Vaf	By Vaf
12-1	C _{12-A} ~C _{12-L}	CA1~CA9, CB1~CB2, CB4	CB3
12-2	-	By Vaf	By Vaf

6.1.3 PHASE SEQUENCE OF MATRIX TYPE-3

For Matrix Type-3, there are total 16 phases in a frame. And each phase contains two sub-phases: Current Source phase and blanking phase. The following table shows the phase sequence in order.

Phase	LED State		
	LED Location	Current Source IOs	Sink IO
1-1	C _{1-A} ~C _{1-P}	CA2~CA9, CB1~CB8	CA1
1-2	-	By Vaf	By Vaf
2-1	C _{2-A} ~C _{2-P}	CA1, CA3~CA9, CB1~CB8	CA2
2-2	-	By Vaf	By Vaf
3-1	C _{3-A} ~C _{3-P}	CA1~CA2, CA4~CA9, CB1~CB8	CA3
3-2	-	By Vaf	By Vaf
4-1	C _{4-A} ~C _{4-P}	CA1~CA3, CA5~CA9, CB1~CB8	CA4
4-2	-	By Vaf	By Vaf
5-1	C _{5-A} ~C _{5-P}	CA1~CA4, CA6~CA9, CB1~CB8	CA5
5-2	-	By Vaf	By Vaf
6-1	C _{6-A} ~C _{6-P}	CA1~CA5, CA7~CA9, CB1~CB8	CA5
6-2	-	By Vaf	By Vaf
7-1	C _{7-A} ~C _{7-P}	CA1~CA6, CA8~CA9, CB1~CB8	CA7
7-2	-	By Vaf	By Vaf
8-1	C _{8-A} ~C _{8-P}	CA1~CA7, CA9, CB1~CB8	CA8
8-2	-	By Vaf	By Vaf
9-1	C _{9-A} ~C _{9-P}	CA1~CA8, CB2~CB8	CA9
9-2	-	By Vaf	By Vaf
10-1	C _{10-A} ~C _{10-P}	CA1~CA9, CB2~CB8	CB1
10-2	-	By Vaf	By Vaf
11-1	C _{11-A} ~C _{11-P}	CA1~CA9, CB1, CB3~CB8	CB2
11-2	-	By Vaf	By Vaf
12-1	C _{12-A} ~C _{12-P}	CA1~CA9, CB1~CB2, CB8	CB3
12-2	-	By Vaf	By Vaf
13-1	C _{13-A} ~C _{13-P}	CA1~CA9, CB1~CB3, CB5~CB8	CB4
13-2	-	By Vaf	By Vaf
14-1	C _{14-A} ~C _{14-P}	CA1~CA9, CB1~CB4, CB6~CB8	CB5
14-2	-	By Vaf	By Vaf
15-1	C _{15-A} ~C _{15-P}	CA1~CA9, CB1~CB5, CB7~CB8	CB6
15-2	-	By Vaf	By Vaf
16-1	C _{16-A} ~C _{16-P}	CA1~CA9, CB1~CB6, CB8	CB7
16-2	-	By Vaf	By Vaf

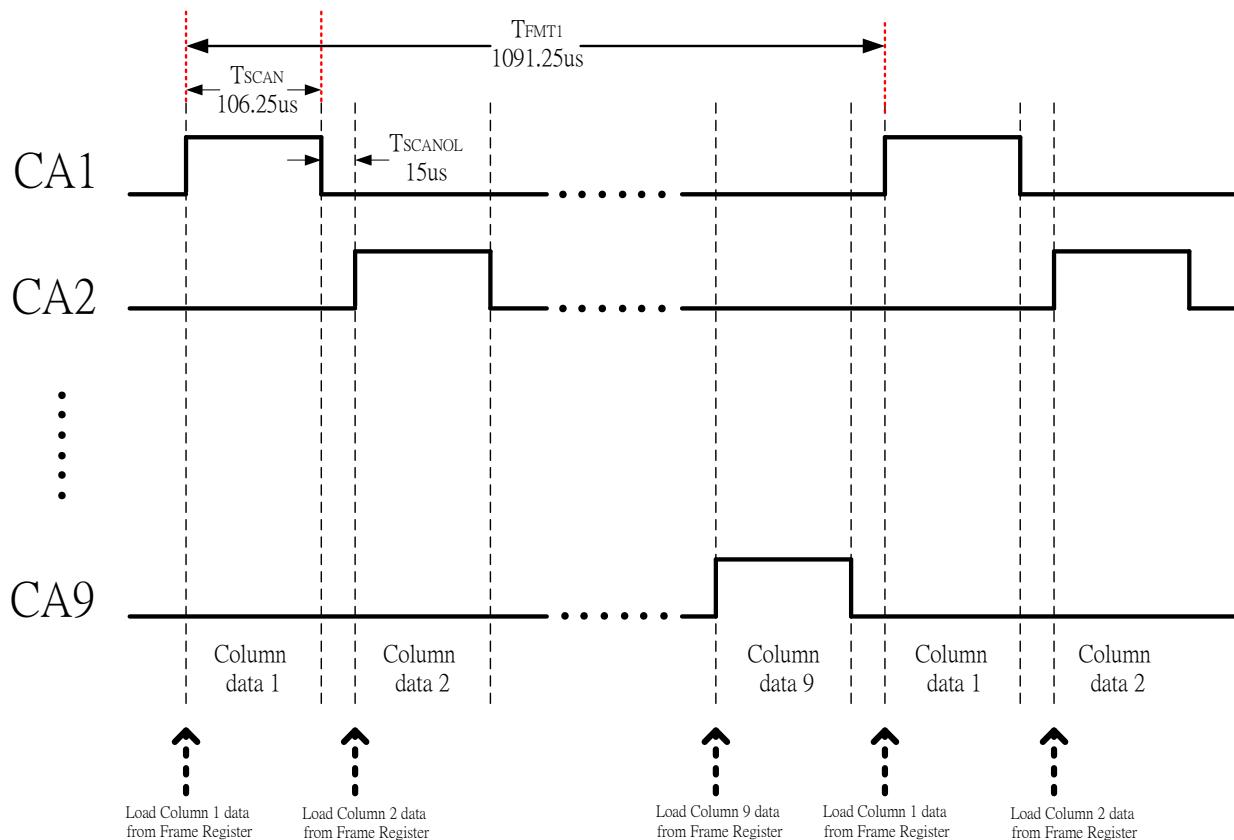
6.1.4 PHASE SEQUENCE OF MATRIX TYPE-4

For Matrix Type-4, there are total 12 phases in a frame. And each phase contains two sub-phases: Current Source phase and blanking phase. The following table shows the phase sequence in order.

Phase	LED State		
	LED Location	Current Source IOs	Sink IO
1-1	C _{1-A} ~C _{1-L}	CA1~CB3	CB4
1-2	-	By Vaf	By Vaf
2-1	C _{2-A} ~C _{2-L}	CA1~CB3	CB5
2-2	-	By Vaf	By Vaf
3-1	C _{3-A} ~C _{3-L}	CA1~CB3	CB6
3-2	-	By Vaf	By Vaf
4-1	C _{4-A} ~C _{4-L}	CA1~CB3	CB7
4-2	-	By Vaf	By Vaf
5-1	C _{5-A} ~C _{5-L}	CA1~CB3	CB8
5-2	-	By Vaf	By Vaf
6-1	C _{6-A} ~C _{6-L}	CA1~CB3	CB9
6-2	-	By Vaf	By Vaf
7-1	C _{7-A} ~C _{7-L}	CA1~CB3	CC1
7-2	-	By Vaf	By Vaf
8-1	C _{8-A} ~C _{8-L}	CA1~CB3	CC2
8-2	-	By Vaf	By Vaf
9-1	C _{9-A} ~C _{9-L}	CA1~CB3	CC3
9-2	-	By Vaf	By Vaf
10-1	C _{10-A} ~C _{10-L}	CA1~CB3	CC4
10-2	-	By Vaf	By Vaf
11-1	C _{11-A} ~C _{11-L}	CA1~CB3	CC5
11-2	-	By Vaf	By Vaf
12-1	C _{12-A} ~C _{12-L}	CA1~CB3	CC6
12-2	-	By Vaf	By Vaf

6.2 PHASE TIMING

6.2.1 PHASE TIMING OF MATRIX TYPE-1

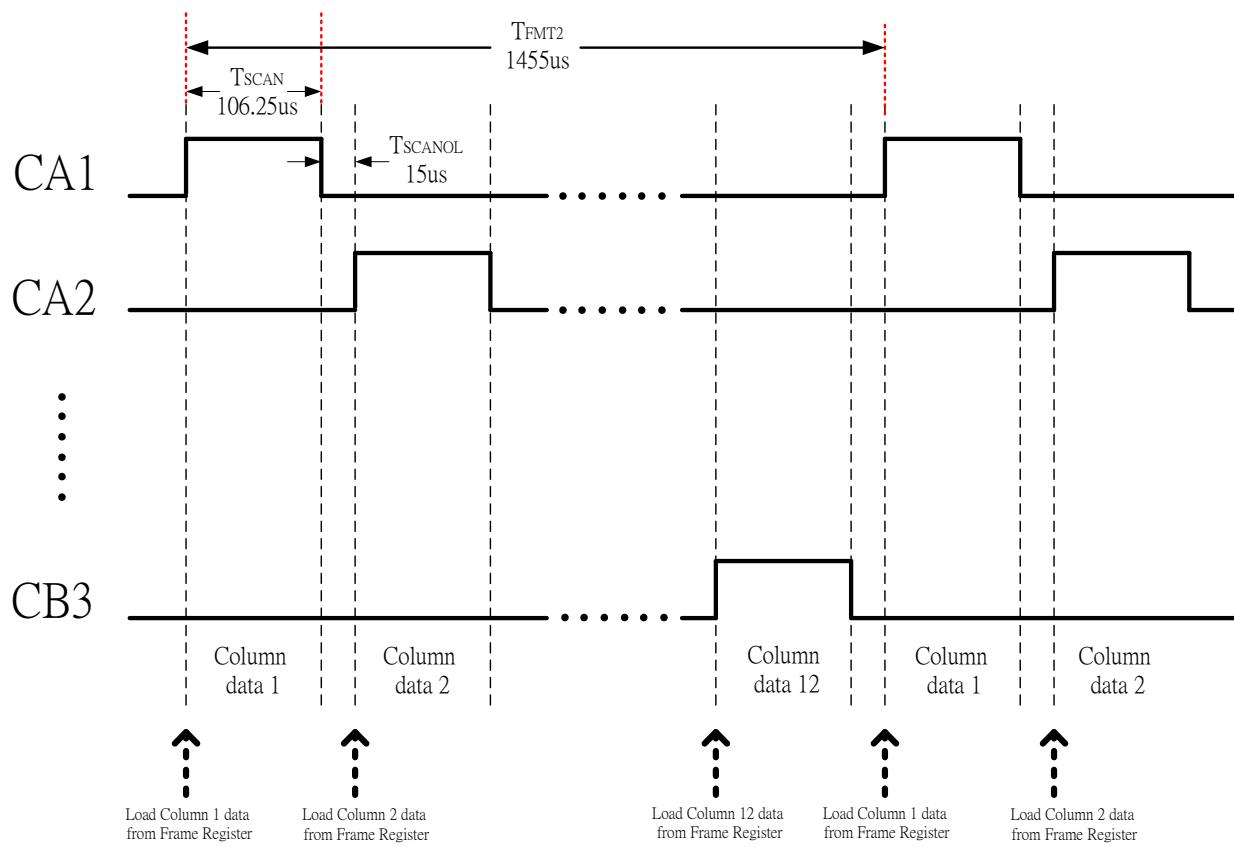


For matrix type-1, $T_{\text{FMT1}} = \text{Phase No.} \times (T_{\text{SCAN}} + T_{\text{SCANOL}}) = 9 \times (106.25\text{us} + 15\text{us}) = 1091.25\text{us}$

The LED scan time $T_{\text{SCAN}} = 106.25\text{us}$.

The blanking time $T_{\text{SCANOL}} = 15\text{us}$.

6.2.2 PHASE TIMING OF MATRIX TYPE-2

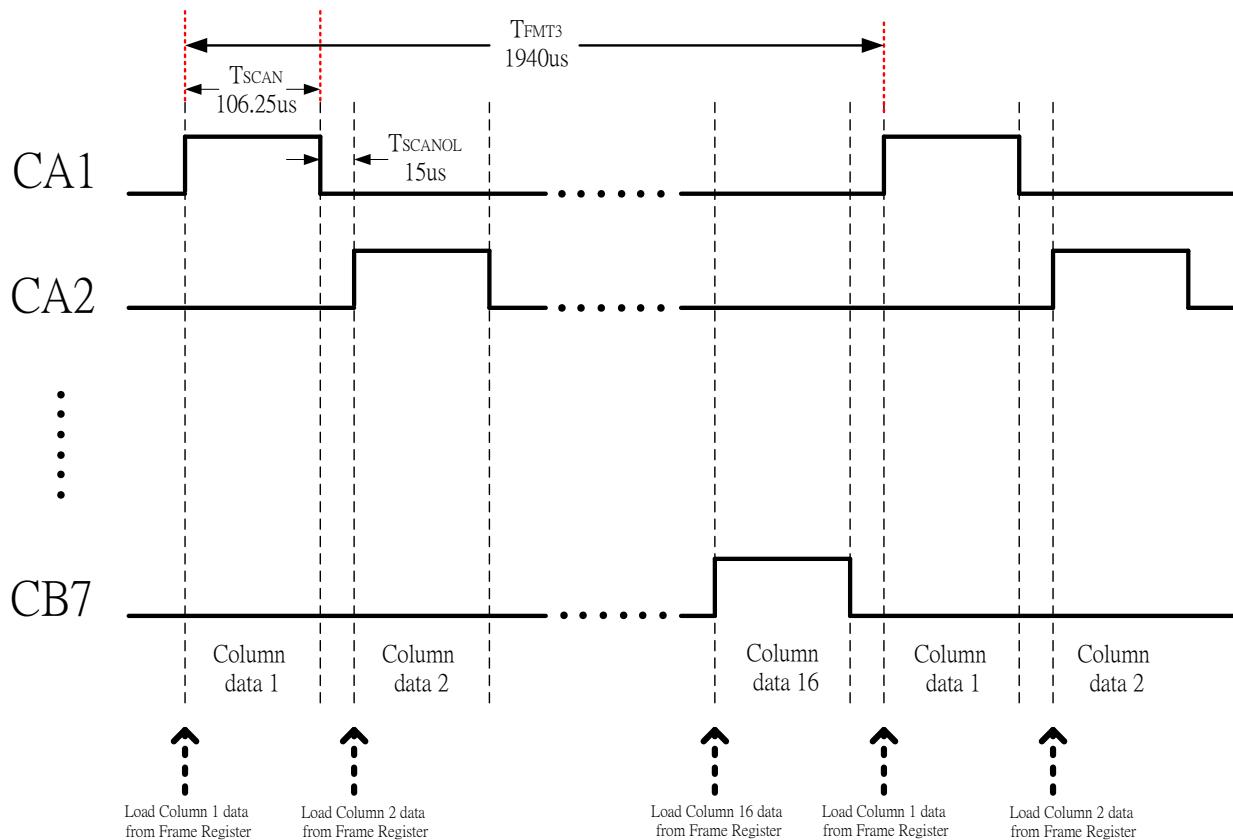


For matrix type-2, $T_{FMT2} = \text{Phase No.} \times (T_{SCAN} + T_{SCANOL}) = 12 \times (106.25\mu s + 15\mu s) = 1455\mu s$

The LED scan time $T_{SCAN} = 106.25\mu s$.

The blanking time $T_{SCANOL} = 15\mu s$.

6.2.3 PHASE TIMING OF MATRIX TYPE-3

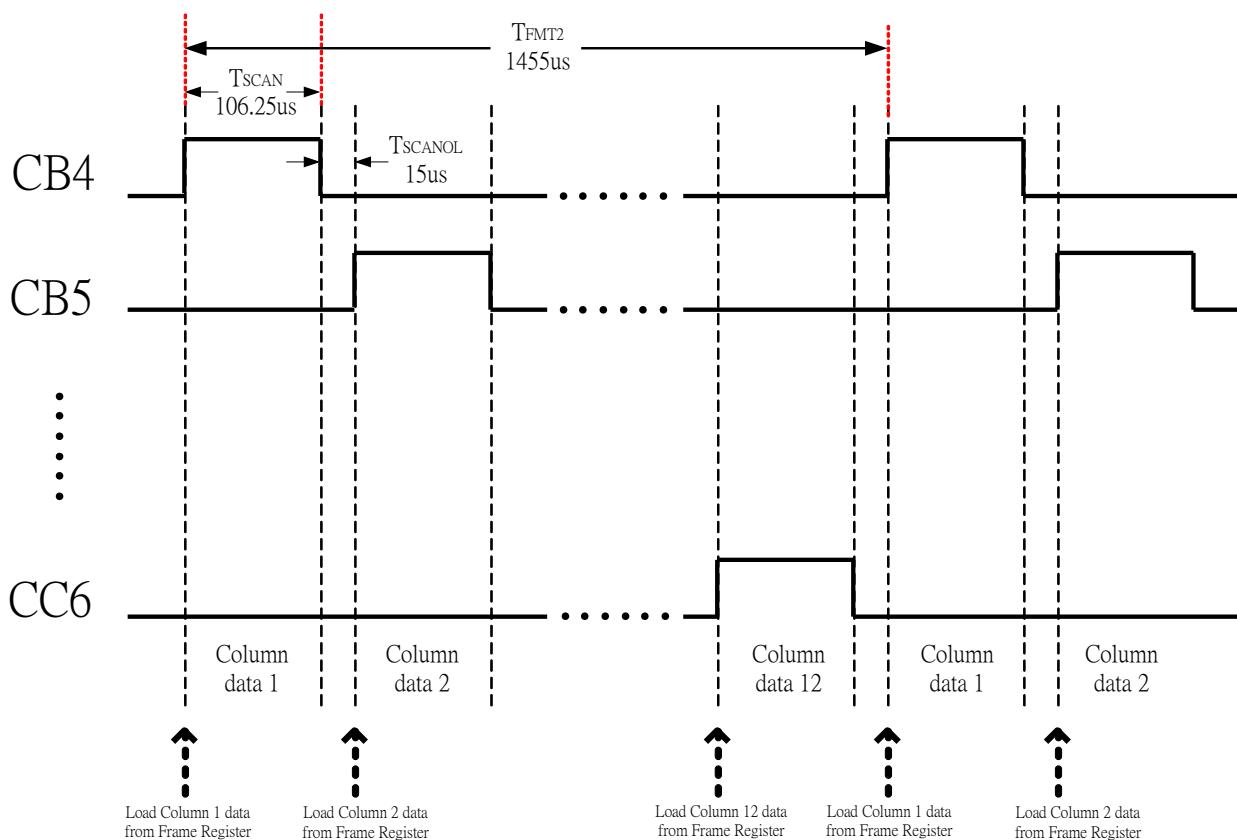


For matrix type-3, $T_{FMT3} = \text{Phase No. } x (\text{T}_{SCAN} + \text{T}_{SCANOL}) = 16 \times (106.25\text{us} + 15\text{us}) = 1940\text{us}$

The LED scan time $\text{T}_{SCAN} = 106.25\text{us}$.

The blanking time $\text{T}_{SCANOL} = 15\text{us}$.

6.2.4 PHASE TIMING OF MATRIX TYPE-4

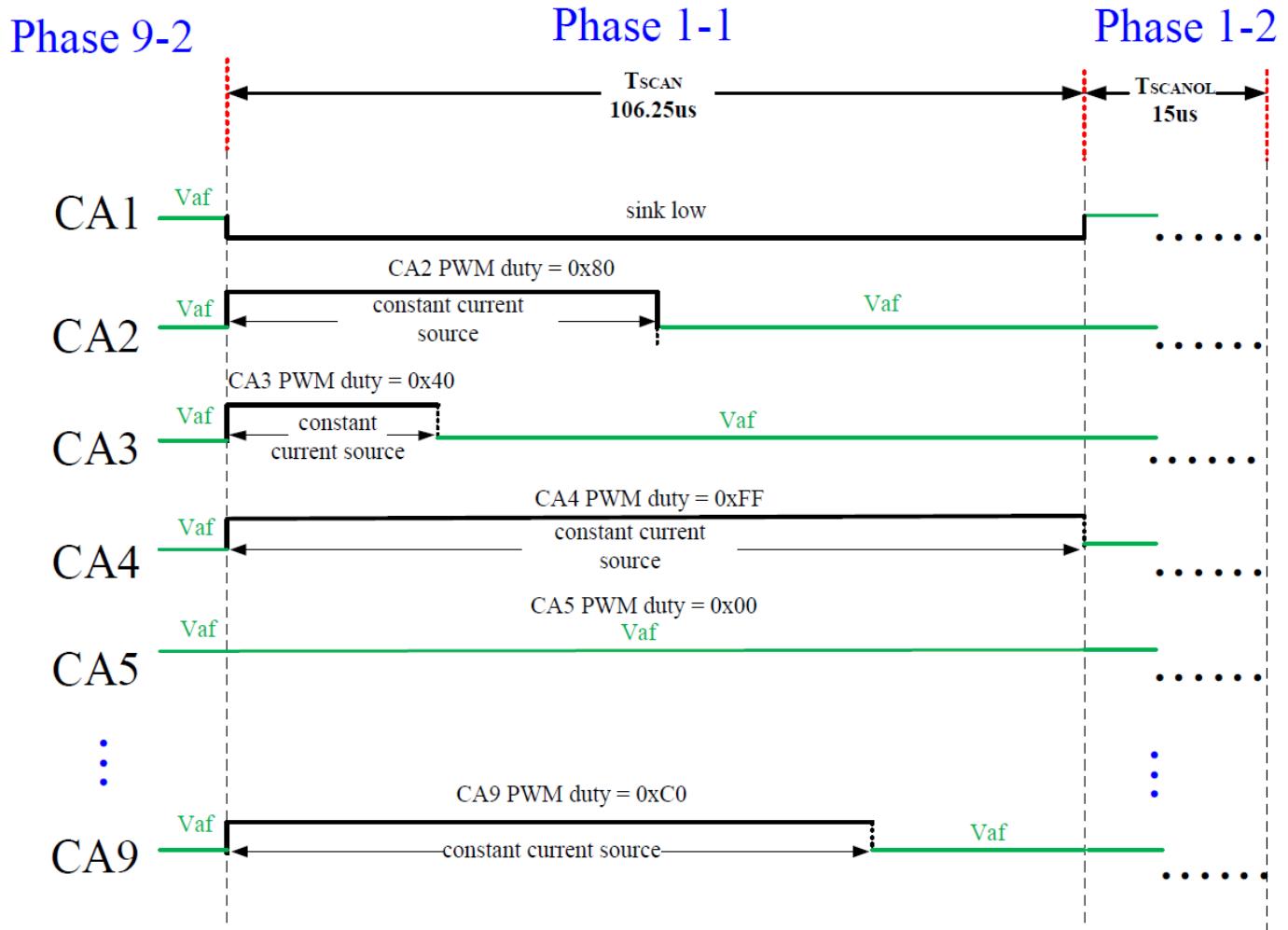


For matrix type-4, $T_{FMT2} = \text{Phase No. } x (\text{T}_{SCAN} + \text{T}_{SCANOL}) = 12 \times (106.25\text{us} + 15\text{us}) = 1455\text{us}$

The LED scan time $\text{T}_{SCAN} = 106.25\text{us}$.

The blanking time $\text{T}_{SCANOL} = 15\text{us}$.

6.2.5 LED SCAN TIME (PHASE N-1)



The figure above shows the example of the LED scan time in Phase 1-1 in matrix type-1.

In Phase 1-1, CA1 keeps sinking low during T_{SCAN} time 106.25us. And in this time, CA2~CA9 channels depending on the PWM duty setting (In PWM Register) will have constant source current output high state. And while the PWM counter reaches the PWM duty, the CA2~CA9 channels will transfer to input floating state.

For example:

CA2 PWM duty = 0x80

- ⇒ The output high time = $128 \times T_{MCLK} = 128 \times 416.67\text{ns} = 53.33\mu\text{s}$,
- ⇒ The Vaf time = $(255-128) \times T_{MCLK} = 127 \times 416.67\text{ns} = 52.92\mu\text{s}$

CA3 PWM duty = 0x40

- ⇒ The output high time = $64 \times T_{MCLK} = 64 \times 416.67\text{ns} = 26.67\mu\text{s}$,
- ⇒ The Vaf time = $(255-64) \times T_{MCLK} = 192 \times 416.67\text{ns} = 79.58\mu\text{s}$

CA4 PWM duty = 0xFF

- ⇒ The output high time = $255 \times T_{MCLK} = 255 \times 416.67\text{ns} = 106.25\mu\text{s}$,
- ⇒ The Vaf time = $(255-255) \times T_{MCLK} = 0 \times 416.67\text{ns} = 0\mu\text{s}$

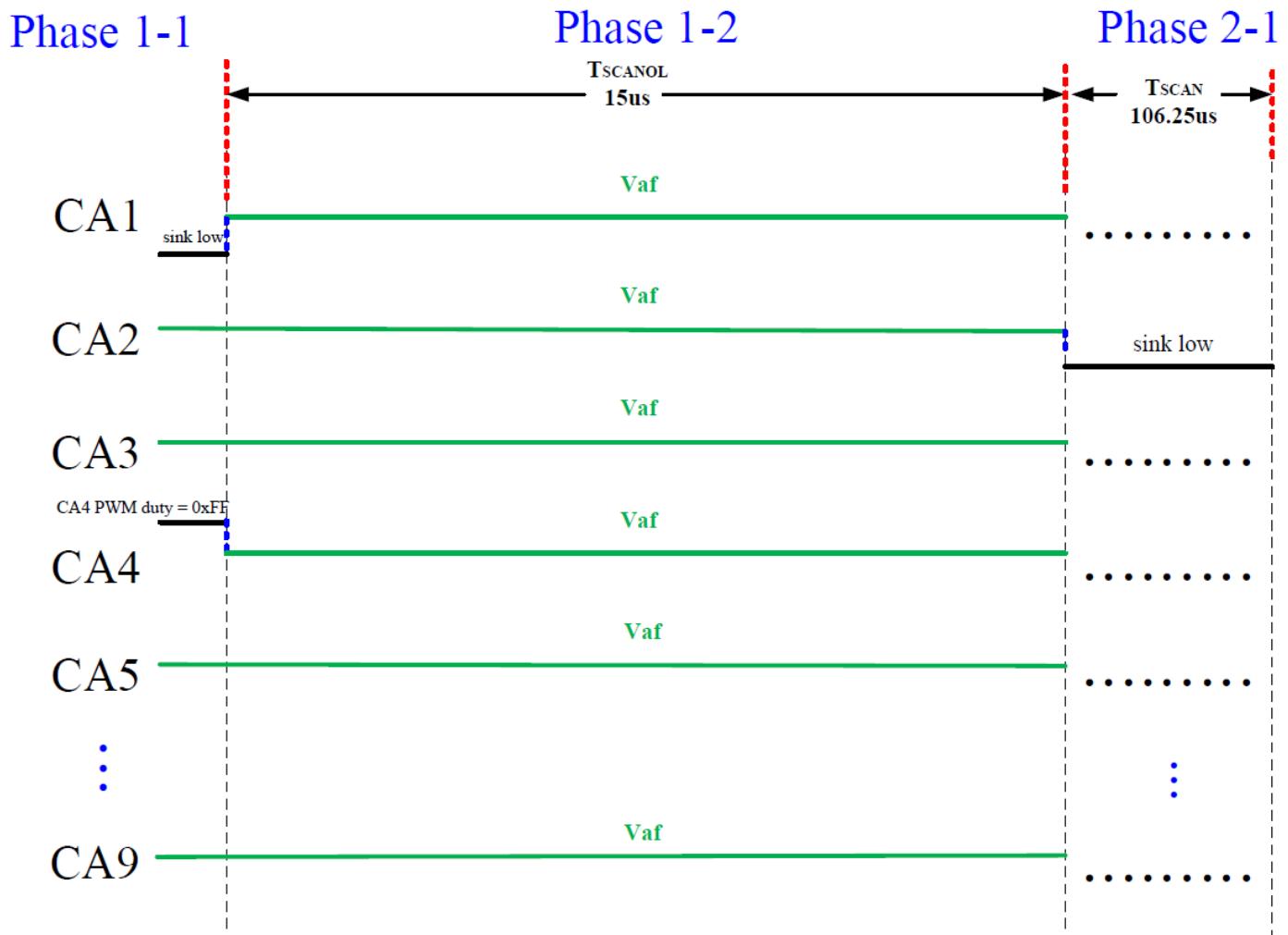
CA5 PWM duty = 0x00

- ⇒ The output high time = $0 \times T_{MCLK} = 0 \times 416.67\text{ns} = 0\mu\text{s}$,
- ⇒ The Vaf time = $(255-0) \times T_{MCLK} = 255 \times 416.67\text{ns} = 106.25\mu\text{s}$

CA9 PWM duty = 0xC0

- ⇒ The output high time = $192 \times T_{MCLK} = 192 \times 416.67\text{ns} = 80\mu\text{s}$,
- ⇒ The Vaf time = $(255-192) \times T_{MCLK} = 63 \times 416.67\text{ns} = 26.25\mu\text{s}$

6.2.6 BLANKING TIME (PHASE N-2)



The figure above shows the example of the blanking time in Phase 1-2 in matrix type-1. In Phase 1-2, all MPWM channels keep input state during T_{SCANOL} time 15us.

7

I2C SLAVE INTERFACE

For SLED1735, when MSEL pin status is low, the system is in I2C Slave mode, and disables the SPI slave function. For SLED1734, the system is always in I2C slave mode. SLED1734/SLED1735 uses a serial bus, which conforms to the I2C protocol, to control the chip's function with two wires: SCL and SDA. The 7-bit slave address (A7:A1), followed by the R/W bit A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A2 and A2 are decided by the connection of the AD pin.

Slave Address (Write only):

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	1	1	1	0	1	AD_CON	0/1	
AD Connected to GND, AD_CON = 00								
AD Connected to VDD, AD_CON = 11								
AD Connected to SCL, AD_CON = 01								
AD Connected to SDA, AD_CON = 10								

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typical 4.7Kohm). The maximum clock frequency is 400KHz. In this discussion, the master is the microcontroller and the slave is SLED1734/1735.

The timing diagram for the I2C is shown in the figure below. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

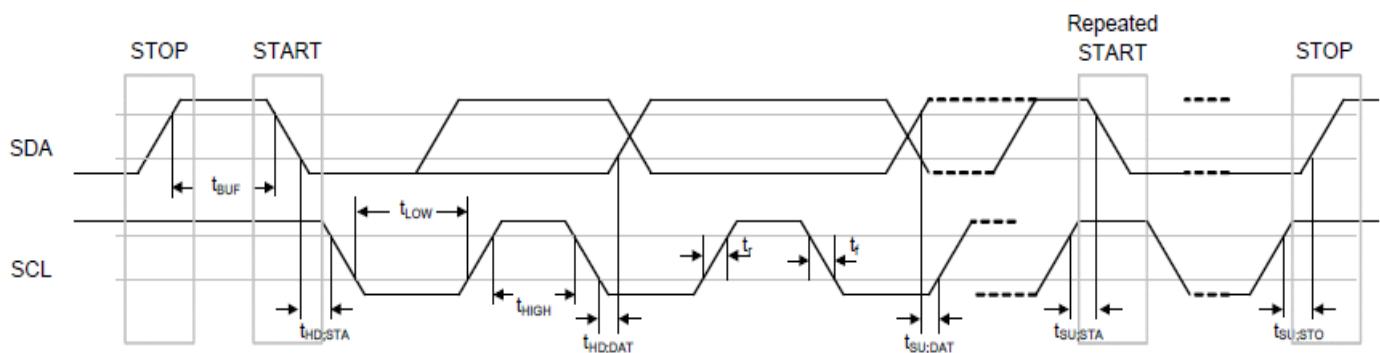
The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all device attached to the I2C bus to check the incoming address against their own slave address.

The 8-bit slave address is sent next, MSB first. Each address bit must be stable while the SCL level is high.

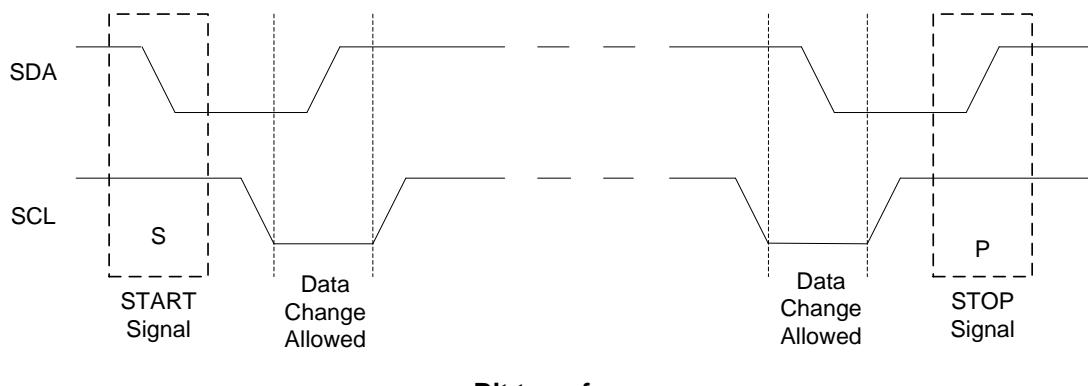
After the last bit of the chip address is sent, the master checks for the slave's acknowledge. The master releases the SDA line high (through a pull-up resistor.) Then the master sends an SCL pulse. If the slave has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal and abort the transfer. Following acknowledge of the slave, the register address byte is sent, MSB first. SLED1735 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, MSB first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the slave must generate another acknowledge to indicate that the data was received.

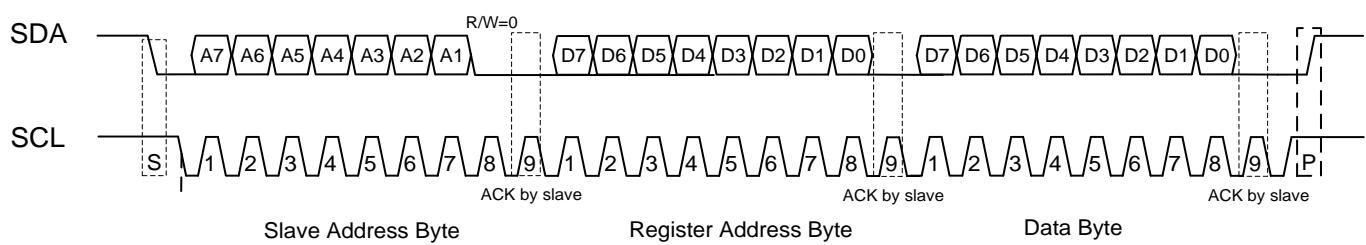
The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.



Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock frequency	-	-	400	kHz
t_{BUFS}	Bus free time between a STOP and a START condition	1.3	-	-	us
$t_{HD,STA}$	Hold Time (repeated) START condition	0.6	-	-	us
$t_{SU,STA}$	Repeated START condition setup time	0.6	-	-	us
$t_{SU,STO}$	STOP condition setup time	0.6	-	-	us
$t_{HD,DAT}$	Data hold time	-	-	0.9	us
$t_{SU,DAT}$	Data setup time	100	-	-	ns
t_{LOW}	SCL clock low period	1.3	-	-	us
t_{HIGH}	SCL clock high period	0.7	-	-	us
t_R	Rise time of both SDA and SCL signals, receiving	20	300	ns	
t_F	Fall time of both SDA and SCL signals, receiving	20	300	ns	



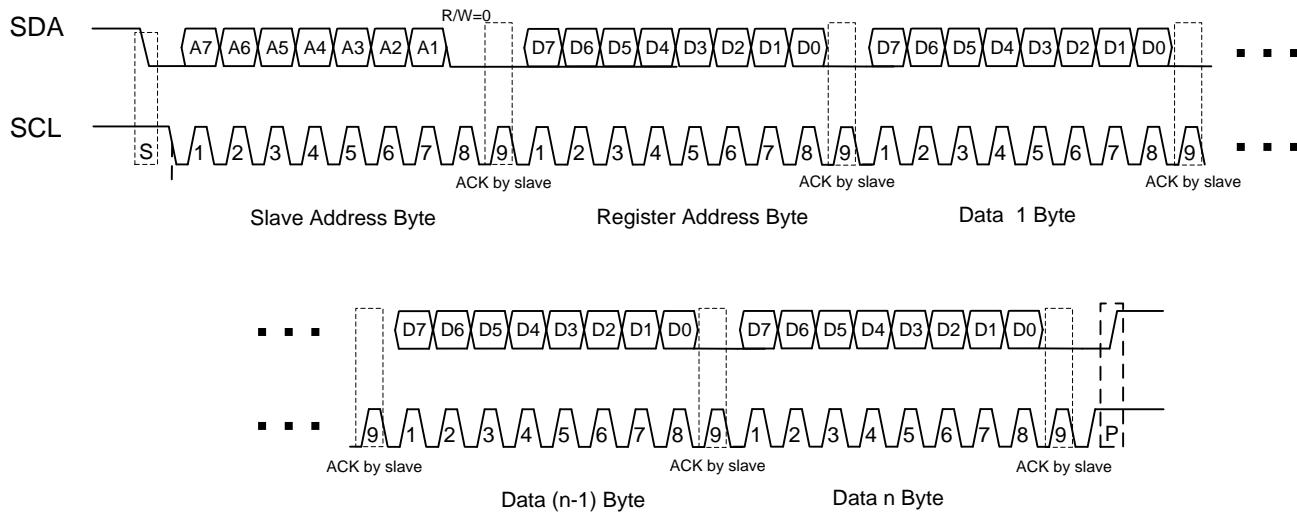
Bit transfer



Write to SLED1734/SLED1735

7.1 ADDRESS AUTO INCREMENT

To write multiple bytes of data into SLED1734/SLED1735, load the address of the data register that the first data byte is intended for. During SLED1734/SLED1735 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to SLED1734/SLED1735 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to SLED1734/SLED1735.

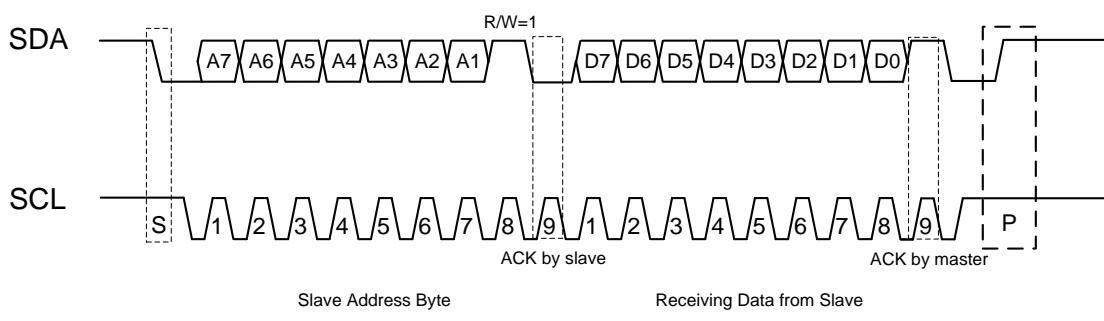


7.2 READING REGISTERS

All of registers in SLED1734/SLED1735 can be read. But frame Registers can only be read in software shutdown mode as SDB pin high. The Function Register and the Detection Register can be read in software shutdown mode or normal operating mode.

To read the device data, the bus master must follow the steps below:

- 1. Select the response register:** Send the slave address with R/W bit set to “0”, followed by the Command Register address, FDH, then send command data which determines which response register is accessed. (This step can be ignored if the current response register is the same as the new one to be set.)
- 2. Set the address of the data to be read:** Send the slave address with R/W bit set to “0”, followed by the address byte of the data to be read.
- 3. Read the data:** Send the slave address with R/W bit set to “1” and then read the data.



8 SPI SLAVE INTERFACE

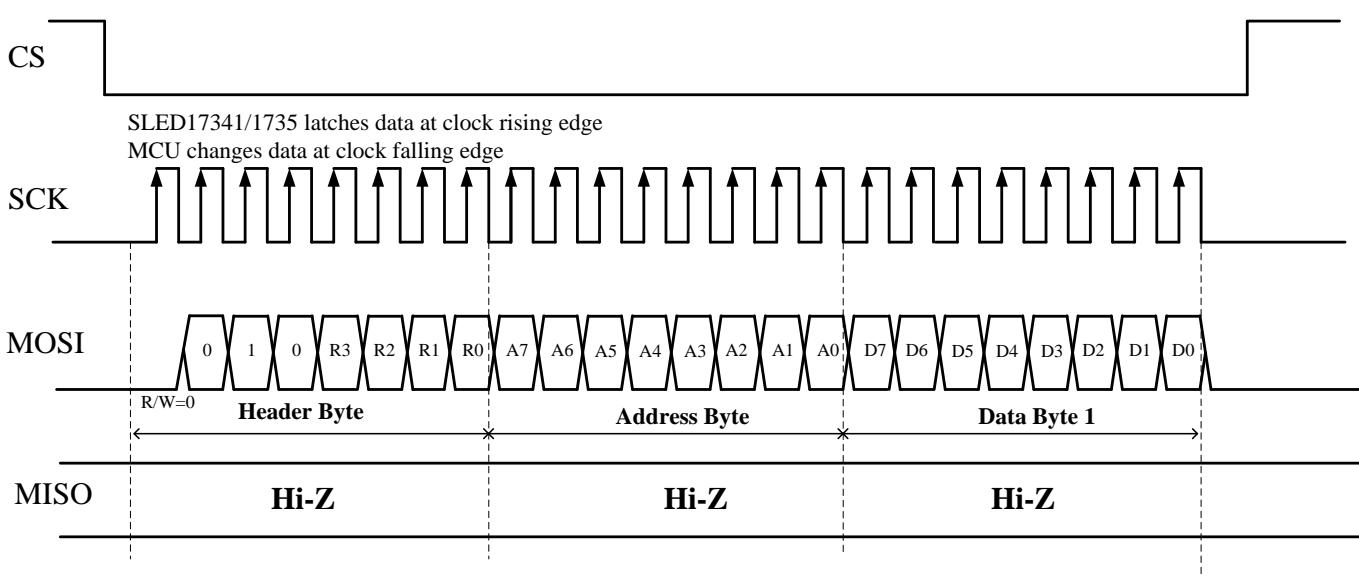
For SLED1735, when MSEL pin status is high, the system is in SPI Slave mode, and disables the I2C slave function. For SLED17341, the system is always in SPI slave mode. SLED17341/1735 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI, and MISO. SPI transfer starts from CS pin from high to low controlled by Master (microcontroller), and SLED17341/1735 latches the data when clock rising.

The SPI data format is 8-bit length. The first header byte composite of 1-bit R/W bit, 3-bit checking pattern and 4-bit Response Register must be sent first, and is followed by the following address byte that the data is to be accessed is sent. And if the R/W bit is "0", meaning a write operation, Master (micro-controller) can write the data byte to the address.

The maximum SCK frequency supported in SLED17341/1735 is 2.4MHz.

Header byte (Write only):

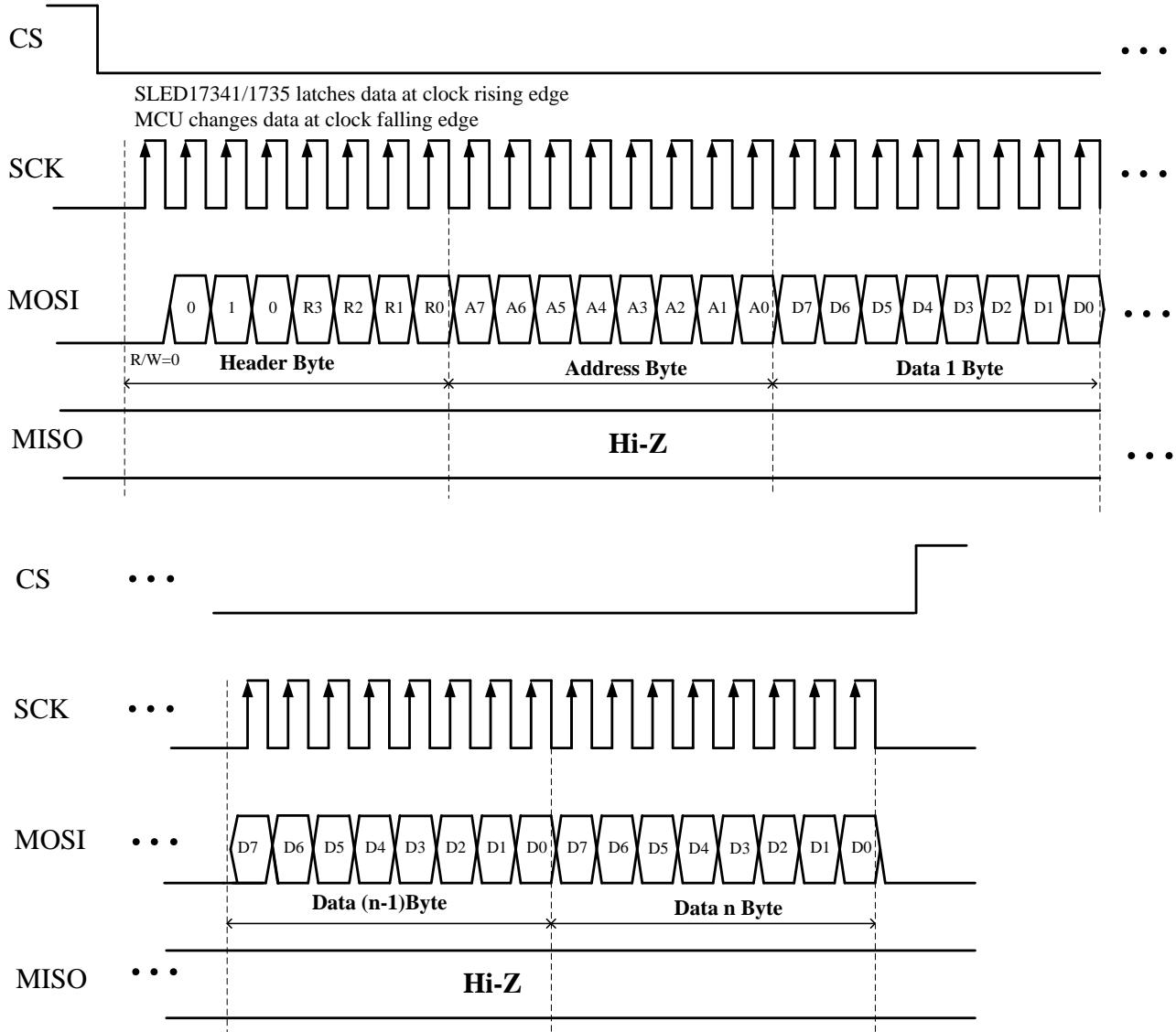
Name	R/W Bit	Checking Pattern	Response Register
Bit	Bit 7	Bit 6:4	Bit 3:0
Value	0: Write operation 1: Read operation	010 (Fixed)	0x0, Point to Page One (Frame 1 Register is available) 0x1, Point to Page Two (Frame 2 Register is only available in Type-3 mode) 0xB, Point to Page Nine (Function Register is available) 0xC, Point to Page Ten (Detection Register is available) 0xD, Point to Page Eleven (LED Location Register is available)



8.1 ADDRESS AUTO INCREMENT

To write multiple bytes of data into SLED17341/1735, load the address of the data register that the first data byte is intended for. After SLED17341/1735 receiving the data byte, the internal address pointer will increment by one. The next data byte sent to SLED17341/1735 will be placed in the new address, and so on. The auto increment of the address will

continue as long as data continues to be written to SLED17341/1735.



Write to SLED17341/SLED1735 (Automatic address increment)

8.2 READING REGISTERS

All of registers in SLED17341/1735 can be read. But frame Registers can only be read in software shutdown mode as SDB pin high. The Function Register and the Detection Register can be read in software shutdown mode or normal operating mode.

To read the device data, the bus master must first send the SLED17341/1735 header byte with R/W bit set to “1”, checking pattern and the Response Register, and then send the Address Byte. SLED17341/1735 will then transmit the data byte addressed by the Address Byte to MCU.

CS

SLED17341/1735 latches data at clock rising edge
MCU changes data at clock falling edge

SCK

MOSI

MISO

</

9 ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd).....	- 0.3V ~ 5.5V
Input in voltage (Vin).....	Vss - 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr).....	0°C ~ + 70°C
Storage ambient temperature (Tstor)	-40°C ~ + 125°C

9.2 ELECTRICAL CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V,, ambient temperature is 25°C unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vdd		2.7*	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset	0.05	-	-	V/ms
Input Low Voltage	ViL		Vss	-	0.3*Vdd	V
Input High Voltage	ViH	SDB, SCK/SCL, SDA/MOSI, AD/MISO pins	0.7*Vdd	-	Vdd	V
Input Low Voltage	ViL		Vss	-	0.1*Vdd	V
Input High Voltage	ViH	MSEL, SYNC, R_EXT/CS, pins	0.9*Vdd	-	Vdd	V
I/O port input leakage current	Ilekg	Vin = Vdd	-	-	2	uA
Default output current	Iout	Output current of CA1~CA9, CB1~CB9, Vds=0.5V. The Constant Current Step setting is 11 0001b.	-	32	-	mA
Current sink headroom voltage	VHR1	Isink = 270mA	-	-	400	mV
Current source headroom voltage	VHR1	Isource = 32mA	-	-	400	mV
I/O output source current sink current	IoH	Vop = Vdd - 0.5V			-	mA
	IoL	Vop = Vss + 0.5V			-	mA
Supply Current (Disable ADC)	Idd1	Normal Mode	Vdd= 5V	-	6.5	mA
	Idd2	Soft Shutdown Mode	Vdd= 5V	-	1	mA
	Idd3	Hardware Shutdown Mode	Vdd= 5V	-	10	uA
LVD Voltage	VLVD	Low voltage reset/indicator level	-	2.55	-	V

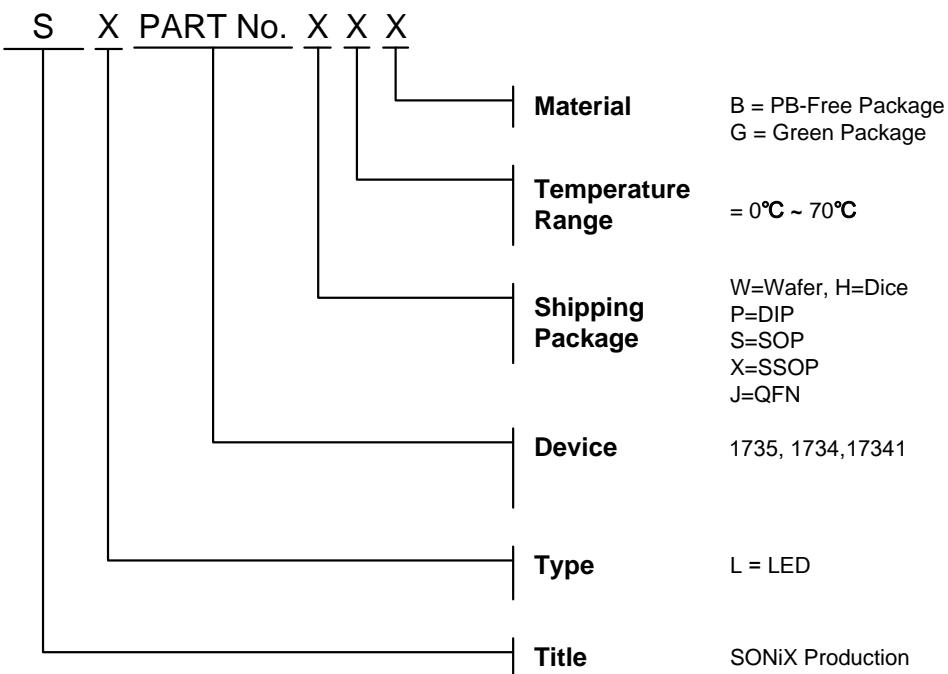
Note 1: Blue LED and Green LED has higher forward voltage. Suggest operating voltage is above 4V.

10 MARKING DEFINITION

10.1 INTRODUCTION

There are many different types in production line. This note lists the production definition of MCU for order or obtain information.

10.2 MARKING IDENTIFICATION SYSTEM



10.3 MARKING EXAMPLE

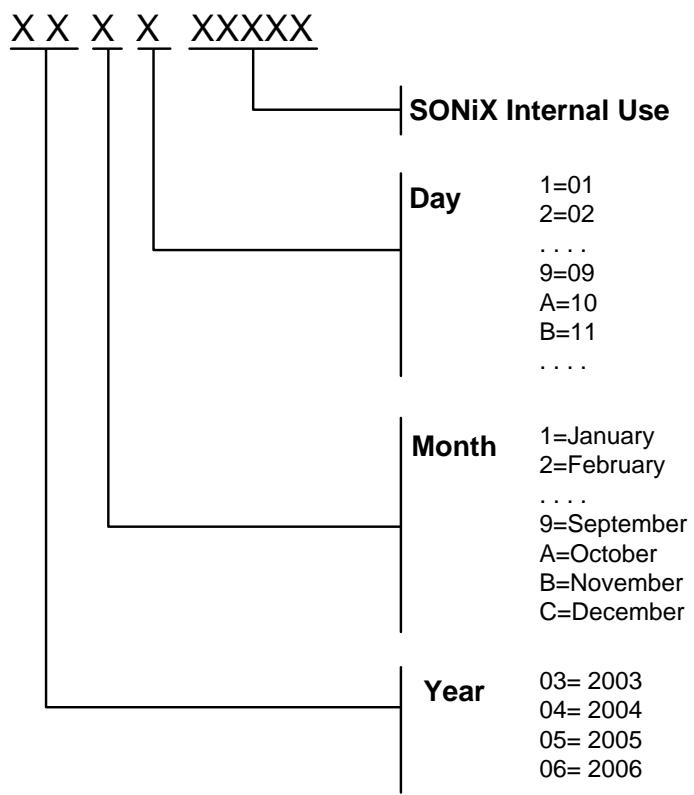
- ### ● Wafer, Dice:

Name	Type	Device	Package	Temperature	Material
SLED1735W	ASIC	SLED1735	Wafer	0°C~70°C	-
SLED1735H	ASIC	SLED1735	Dice	0°C~70°C	-

- **Green Package:**

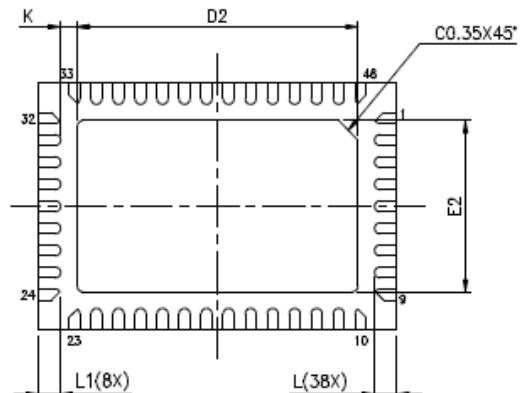
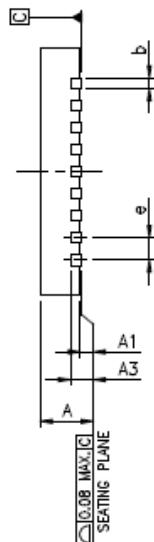
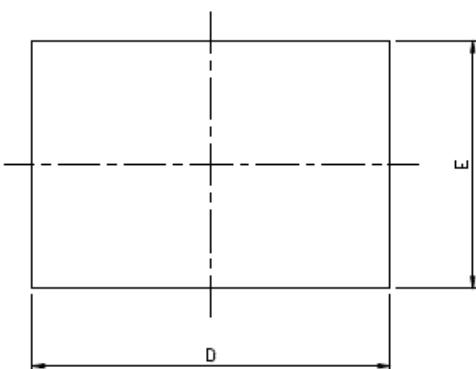
Name	Type	Device	Package	Temperature	Material
SLED1735J	ASIC	SLED1735	QFN	0°C~70°C	Green Package
SLED1734J	ASIC	SLED1735	QFN	0°C~70°C	Green Package
SLED1734X	ASIC	SLED1735	SSOP	0°C~70°C	Green Package
SLED17341J	ASIC	SLED1735	QFN	0°C~70°C	Green Package
SLED17341X	ASIC	SLED1735	SSOP	0°C~70°C	Green Package
SLED1733S	ASIC	SLED1735	SOP	0°C~70°C	Green Package
SLED17331S	ASIC	SLED1735	SOP	0°C~70°C	Green Package
SLED1732S	ASIC	SLED1735	SOP	0°C~70°C	Green Package
SLED17321S	ASIC	SLED1735	SOP	0°C~70°C	Green Package

10.4 DATECODE SYSTEM



11 PACKAGE INFORMATION

11.1 QFN 46 PIN



PAD SIZE : 213X13* MIL

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

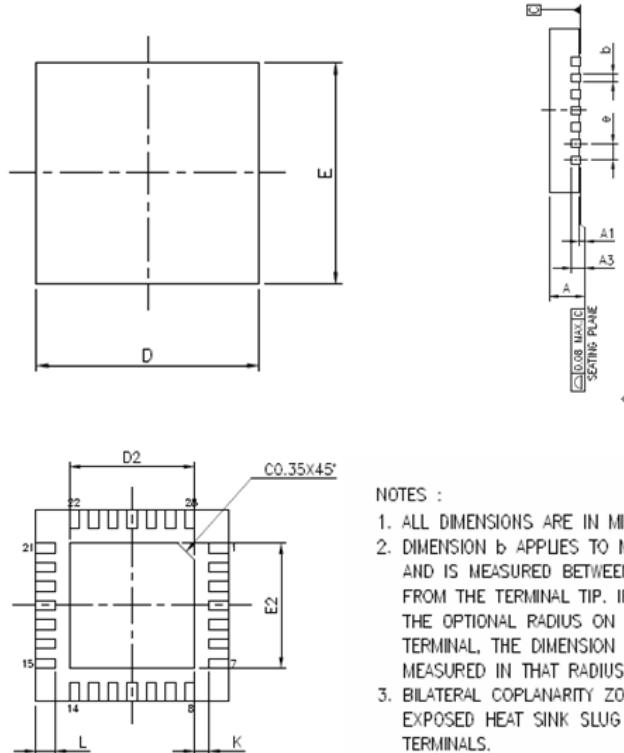
JEDEC OUTLINE	PACKAGE TYPE		
	N/A		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.50 BSC		
E	4.50 BSC		
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			L1			LEAD FINISH	JEDEC CODE
	MIN.	NOM.	MAX.											
212X13* MIL	5.05	5.10	5.15	3.05	3.10	3.15	0.35	0.40	0.45	0.33	0.38	0.43	V	X

"k" 表示汎用字元，此汎用字元可能被其它不同字元所取代，實際的字元請參照bonding diagram所示。

"k" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

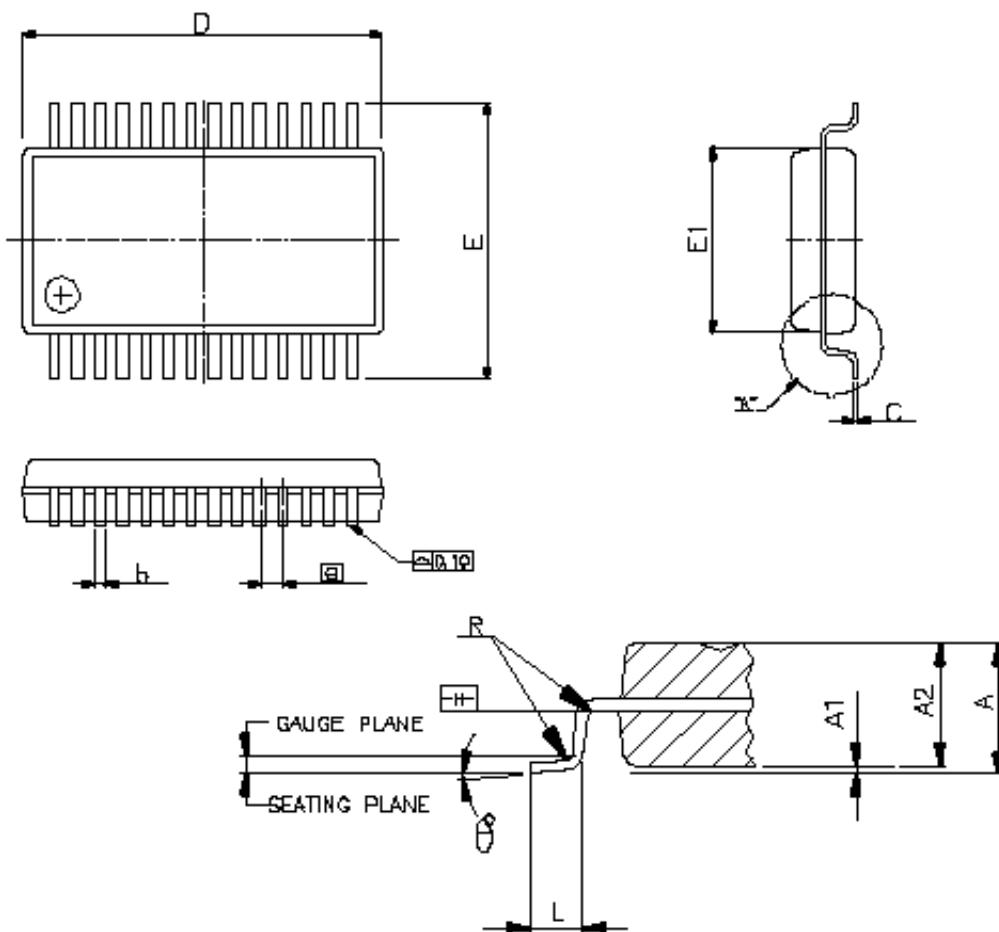
11.2 QFN 28 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	0.003	0.030	0.031	0.07	0.75	0.80
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF.			0.20 REF.		
b	0.006	0.008	0.010	0.15	0.20	0.25
D	0.16 BSC			4.00 BSC		
E	0.16 BSC			4.00 BSC		
e	0.016 BSC			0.40 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45
K	0.008	-	-	0.20	-	-

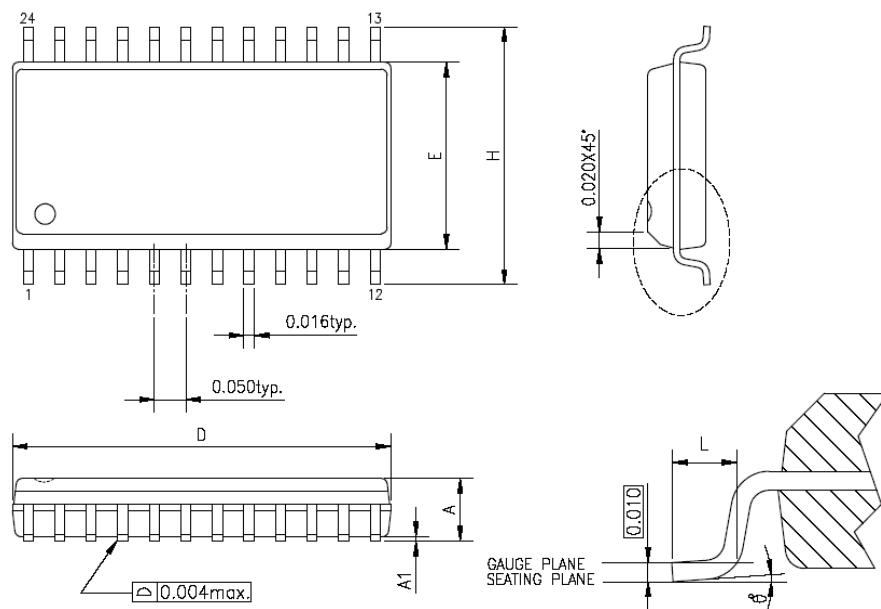
PAD SIZE	D2 (mm)			E2 (mm)		
	MIN	NOR	MAX	MIN	NOR	MAX
115x115 MIL	2.50	2.60	2.65	2.50	2.60	2.65

11.3 SSOP 28 PIN

DETAIL A

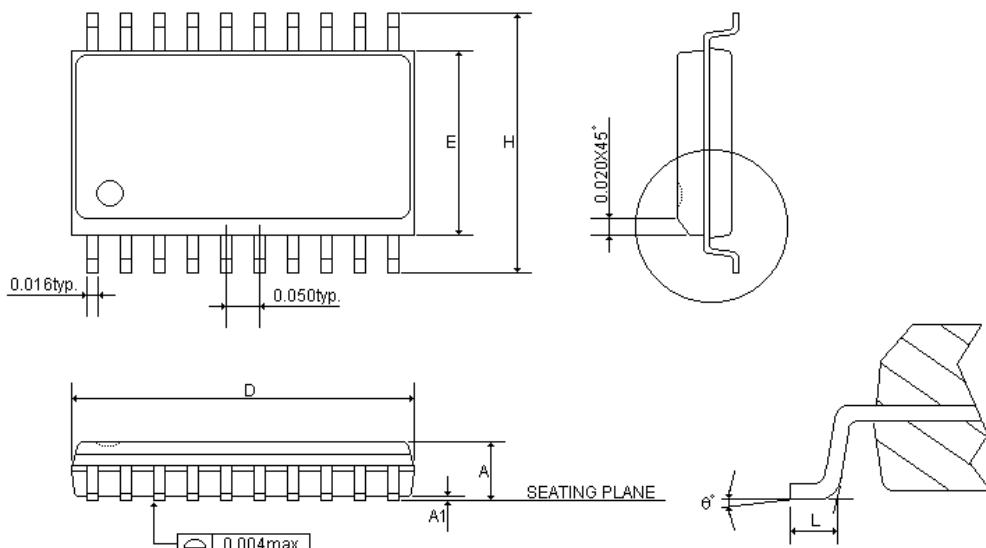
SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.08	-	-	2.13
A1	0.00	-	0.01	0.05	-	0.25
A2	0.06	0.07	0.07	1.63	1.75	1.88
b	0.01	-	0.01	0.22	-	0.38
C	0.00	-	0.01	0.09	-	0.20
D	0.39	0.40	0.41	9.90	10.20	10.50
E	0.29	0.31	0.32	7.40	7.80	8.20
E1	0.20	0.21	0.22	5.00	5.30	5.60
[e]	0.0259BSC			0.65BSC		
L	0.02	0.04	0.04	0.63	0.90	1.03
R	0.00	-	-	0.09	-	-
θ°	0°	4°	8°	0°	4°	8°

11.4 SOP 24 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.069	-	-	1.753
A1	0.004	-	0.010	0.102	-	0.254
D	0.612	0.618	0.624	15.545	15.697	15.850
E	0.292	0.296	0.299	7.417	7.518	7.595
H	0.405	0.412	0.419	10.287	10.465	10.643
L	0.021	0.031	0.041	0.533	0.787	1.041
θ°	0°	4°	8°	0°	4°	8°

11.5 SOP 20 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	0.093	0.099	0.104	2.362	2.502	2.642
A1	0.004	0.008	0.012	0.102	0.203	0.305
D	0.496	0.502	0.508	12.598	12.751	12.903
E	0.291	0.295	0.299	7.391	7.493	7.595
H	0.394	0.407	0.419	10.008	10.325	10.643
L	0.016	0.033	0.050	0.406	0.838	1.270
θ°	0°	4°	8°	0°	4°	8°

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