

PRODUCT OVERVIEW

FEATURES

- ◆ Support I2C/SPI slave communication
- ◆ Built-in four LED Matrix Types
 - LED Matrix Type-1**

Achieve 9x8+9x8 LED matrix by CA1~CA9 and CB1~CB9.
Maximum to 144 LEDs are supported.
Maximum to 36 anode RGB LEDs are supported.
Maximum to 36 cathode RGB LEDs are supported.
 - LED Matrix Type-2**

Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.
Maximum to 144 LEDs are supported.
Maximum to 40 anode RGB LEDs are supported.
Maximum to 41 cathode RGB LEDs are supported.
 - LED Matrix Type-3**

Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8
Maximum to 256 LEDs are supported.
Maximum to 75 anode RGB LEDs are supported.
Maximum to 75 cathode RGB LEDs are supported.
 - LED Matrix Type-4**

Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9, CB1~CB9, and CC1~CC6.
Maximum to 144 LEDs are supported.
Maximum to 48 anode RGB LEDs are supported.
Maximum to 48 cathode RGB LEDs are supported.
- ◆ LED Controls

Each LED has the on/off control.
Each LED has the blink enable/disable control.
Each LED has the 8-bit programmable PWM duty.
Each LED has the open/short detection status.
Each LED has the anti-forward control (Vaf) to prevent the ghost LED effects.
Each LED has the +/-6% current fine tune control.
Support global 8mA~40mA constant current source control.
- ◆ MPWM IO (CA1~CA9, CB1~CB9, and CC1~CC6)

Each MPWM IO has sink current of 320mA.
Each MPWM IO supports staggered delay.
Each MPWM IO supports slew rate control.
Each MPWM IO except CC1~CC6 has the precise current skew under +/-2%.
Current skew between chips is under +/-2%.
- ◆ System Clock Synchronization for cascaded LED drivers

Support SYNC output in master mode.
Support SYNC input in slave mode.
- ◆ I2C Slave

Maximum to 400KHz
Support four auto-selective slave addresses by which AD pin is connected to. (VDD/VSS/SCL/SDA)
- ◆ SPI Slave

Maximum to 2.4MHz
- ◆ Matrix Control Engine

Support Type 1~4 matrixes by register setting.
The frame time depending on Matrix Type has different phase number.
Type-1 has the frame time 1098us including 9 phases.
Type-2 and Type-4 have the frame time 1464us including 12 phases.
Type-3 has the frame time 1952us including 16 phases.
Each phase includes the PWM duty time 107us and the blanking time 15us.
Support auto-breath control.
Support auto-blink control.
Support Audio-IN synchronous to auto-brightness control.
- ◆ Audio In Gain Control

Support register configurable gain for Audio-IN: 0dB, 3dB, 6dB, 9dB, 12dB, 15dB, 18dB, and 21dB.
Support auto-gain control.
- ◆ Thermal Detection

Support thermal shutdown at 150°C
Support thermal flag at 70°C
- ◆ Power Modes

Normal Mode
Software power down mode
Hardware power down mode.
- ◆ Package

QFN28/SSOP28/QFN46.

SSOP 28pins): I2C Interface

CA9	1	U	28	CA8
VDD	2		27	CA7
SDB	3		26	CA6
SYNC	4		25	CA5
GND	5		24	CA4
R_EXT	6		23	CA3
CB1	7		22	CA2
CB2	8		21	CA1
CB3	9		20	SCL
CB4	10		19	SDA
CB5	11		18	AD
CB6	12		17	AGCIN
CB7	13		16	C_FILT
CB8	14		15	CB9

VS12L03A
SSOP 28pins): SPI Interface

CA9	1	U	28	CA8
VDD	2		27	CA7
SDB	3		26	CA6
SYNC	4		25	CA5
GND	5		24	CA4
CS	6		23	CA3
CB1	7		22	CA2
CB2	8		21	CA1
CB3	9		20	SCK
CB4	10		19	MOSI
CB5	11		18	MISO
CB6	12		17	AGCIN
CB7	13		16	C_FILT
CB8	14		15	CB9

VS12L03A

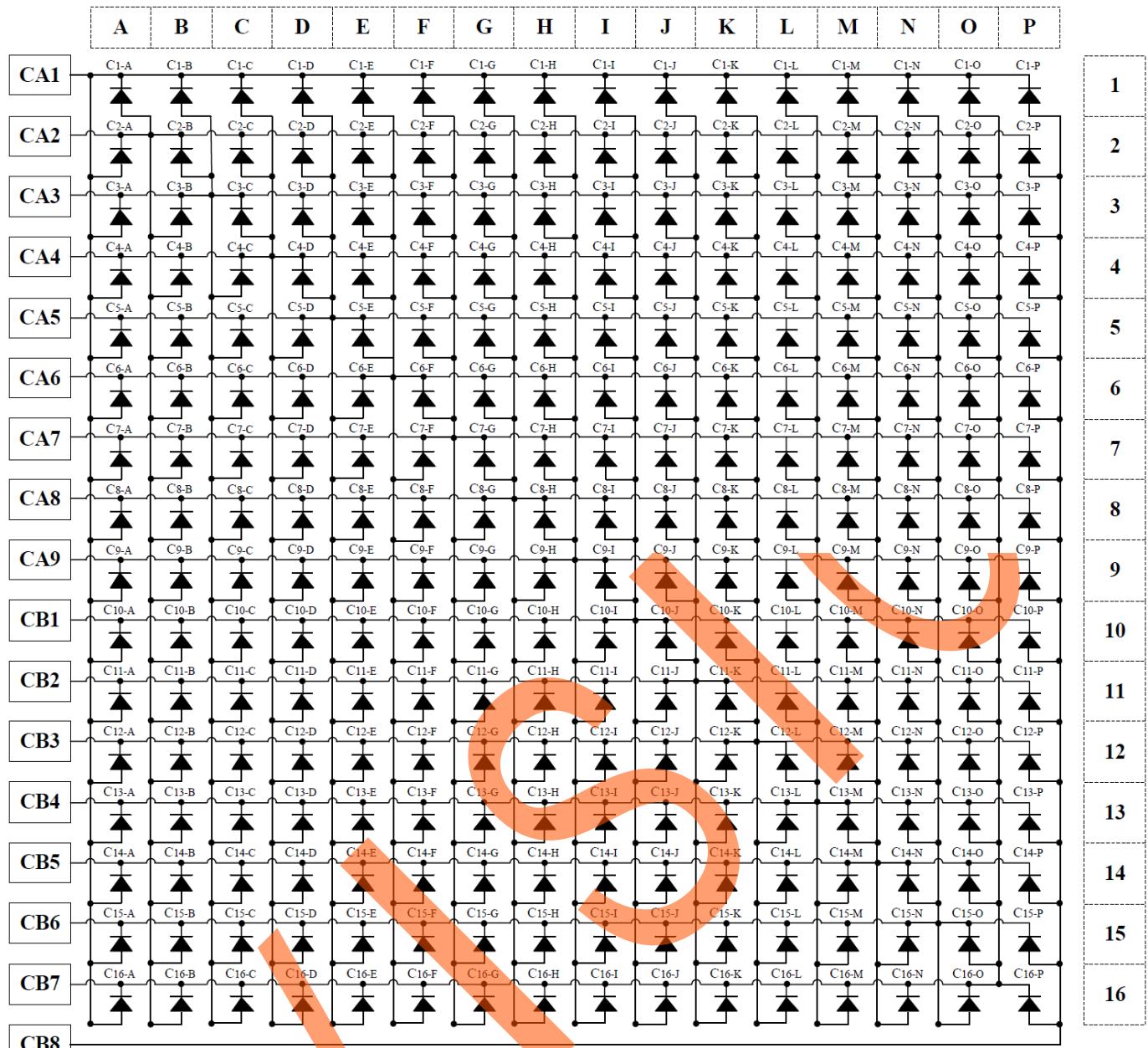
PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pin for digital and analog circuit.
		Power supply input pin for digital and analog circuit.
		Power supply input pins for digital and analog circuit.
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. MSEL = 0 : I2C, pMSEL = 1 : SPI.
SDB	I	Schmitt trigger structure as input mode with internal pull-down resistor. Shutdown the chip when pull to low.
SYNC	I/O	Clock synchronous input or output pin. Schmitt trigger structure as input mode.
R_EXT/CS	I	R_EXT: Input only with internal pull down resistor in I2C mode. No external pull-down resistor is required.
		CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.
C_FILT	O	Used for filter audio-in noise.
AGCIN	I	Audio-IN Input.
AD/MISO	I/O	AD: I2C slave address selection pin. Schmitt trigger structure as input mode. MISO: SPI Master-Input-Slave-Output pin.
SDA/MOSI	I/O	SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode. MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.
SCL/SCK	I/O	SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode. SCK: SPI Clock input pin. Schmitt trigger structure as input mode.
CA1~CA9	O	PWM IO with sink 320mA and constant current source.
CB1~CB9	O	PWM IO with sink 320mA and constant current source.
CC1~CC6	O	PWM IO with sink 320mA.

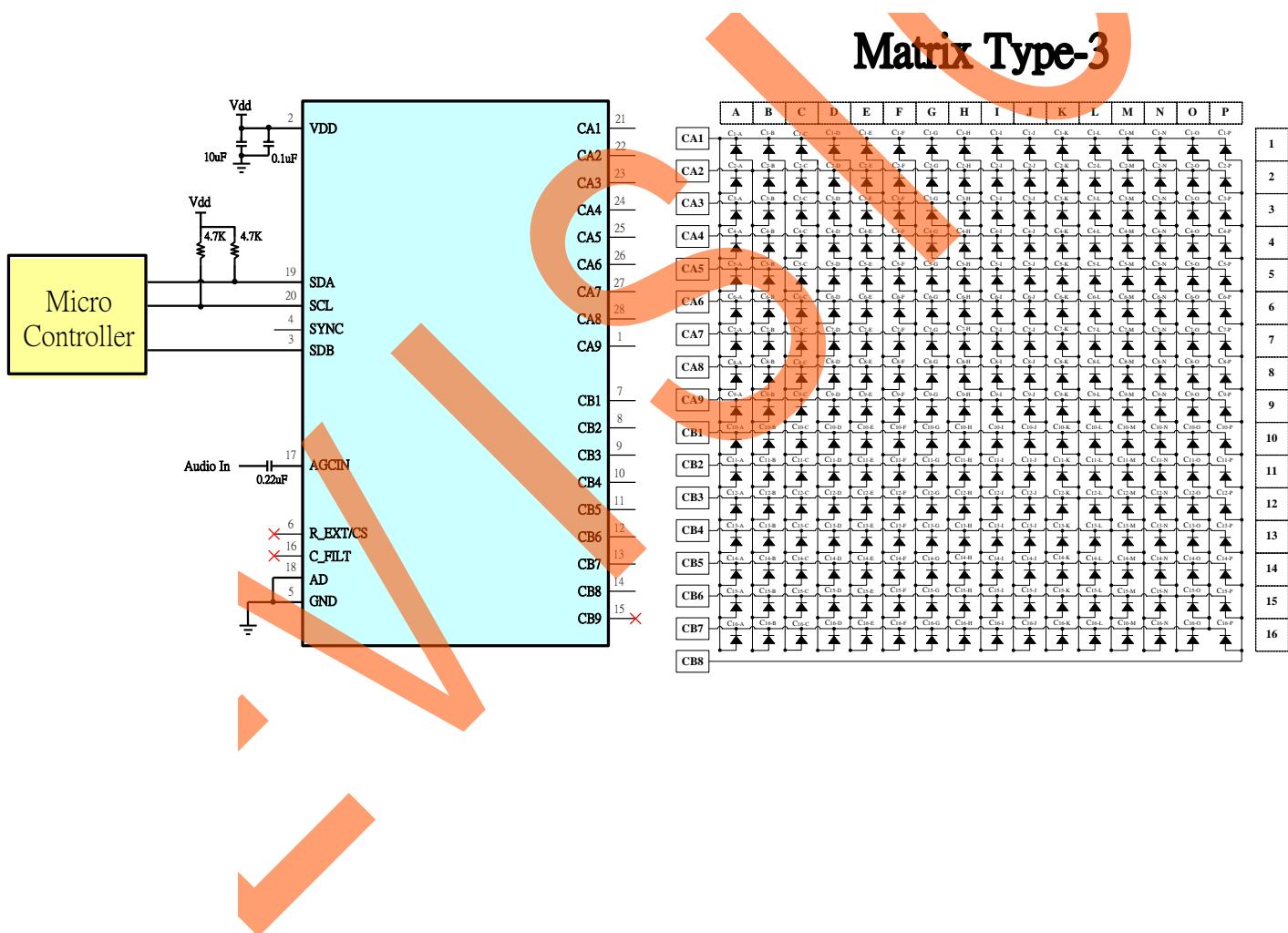


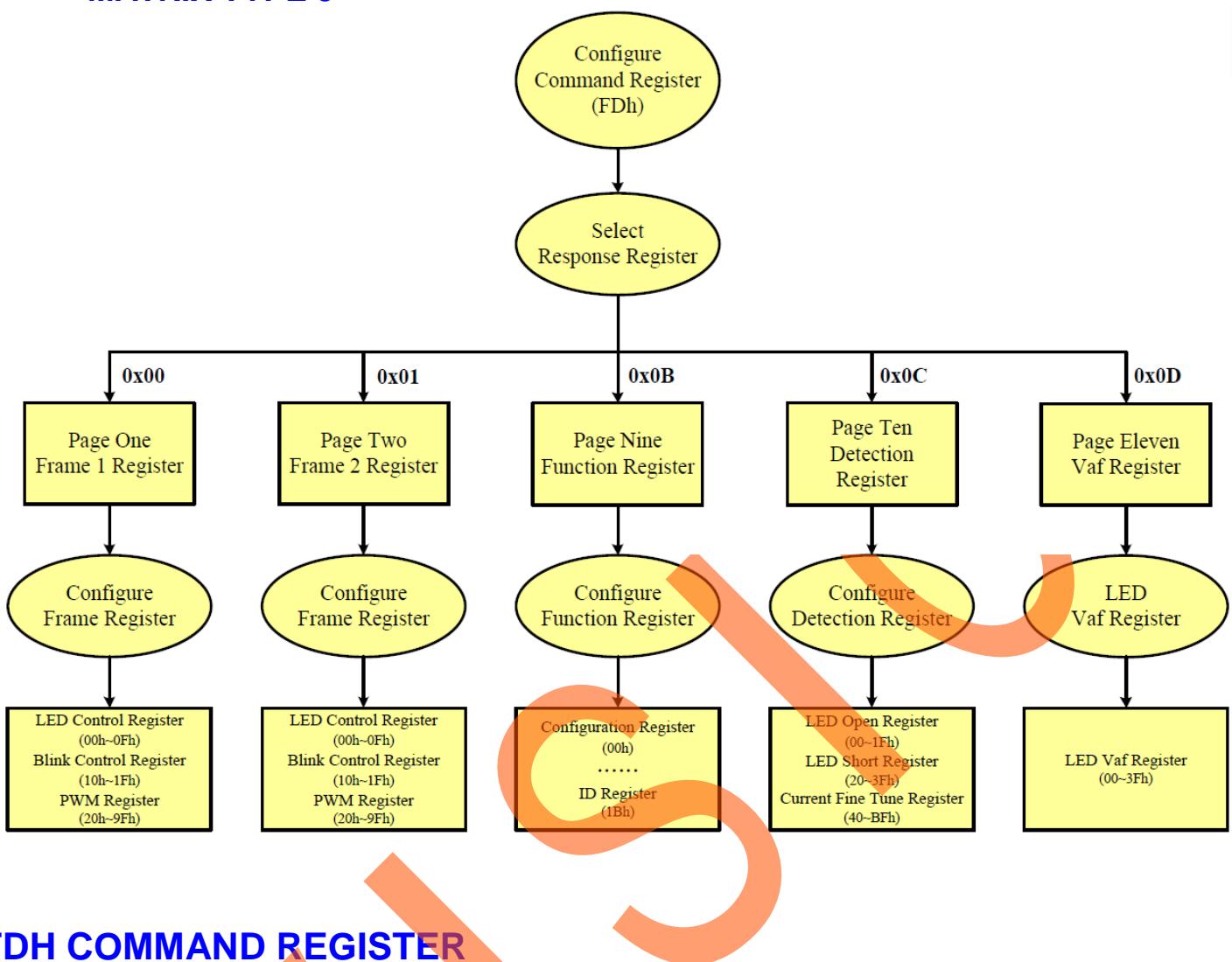
MATRIX TYPE-3 RAM MAP

Type-3 (16*16)						
	Frame 1			Frame C		
LED Location	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA1(C1-A~C1-P)	00h~01h	10h~11h	20h~2Fh	00h~01h	20h~21h	40h~47h
CA2(C2-A~C2-P)	02h~03h	12h~13h	30h~3Fh	02h~03h	22h~23h	48h~4Fh
CA3(C3-A~C3-P)	04h~05h	14h~15h	40h~4Fh	04h~05h	24h~25h	50h~57h
CA4(C4-A~C4-P)	06h~07h	16h~17h	50h~5Fh	06h~07h	26h~27h	58h~5Fh
CA5(C5-A~C5-P)	08h~09h	18h~19h	60h~6Fh	08h~09h	28h~29h	60h~67h
CA6(C6-A~C6-P)	0Ah~0Bh	1Ah~1Bh	70h~7Fh	0Ah~0Bh	2Ah~2Bh	68h~6Fh
CA7(C7-A~C7-P)	0Ch~0Dh	1Ch~1Dh	80h~8Fh	0Ch~0Dh	2Ch~2Dh	70h~77h
CA8(C8-A~C8-P)	0Eh~0Fh	1Eh~1Fh	90h~9Fh	0Eh~0Fh	2Eh~2Fh	78h~7Fh
	Frame 2			Frame C		
LED Location	LED Control Register	Blink Control Register	PWM Register	LED Open Register	LED Short Register	Current Fine Tune Register
CA9(C9-A~C9-P)	00h~01h	10h~11h	20h~2Fh	10h~11h	30h~31h	80h~87h
CB1(C10-A~C10-P)	02h~03h	12h~13h	30h~3Fh	12h~13h	32h~33h	88h~8Fh
CB2(C11-A~C11-P)	04h~05h	14h~15h	40h~4Fh	14h~15h	34h~35h	90h~97h
CB3(C12-A~C12-P)	06h~07h	16h~17h	50h~5Fh	16h~17h	36h~37h	98h~9Fh
CB4(C13-A~C13-P)	08h~09h	18h~19h	60h~6Fh	18h~19h	38h~39h	A0h~A7h
CB5(C14-A~C14-P)	0Ah~0Bh	1Ah~1Bh	70h~7Fh	1Ah~1Bh	3Ah~3Bh	A8h~AFh
CB6(C15-A~C15-P)	0Ch~0Dh	1Ch~1Dh	80h~8Fh	1Ch~1Dh	3Ch~3Dh	B0h~B7h
CB7(C16-A~C16-P)	0Eh~0Fh	1Eh~1Fh	90h~9Fh	1Eh~1Fh	3Eh~3Fh	B8h~BFh
	Frame D					
LED Location	LED Vaf Register					
CA1(C1-A~C1-P)	00h~03h					
CA2(C2-A~C2-P)	04h~07h					
CA3(C3-A~C3-P)	08h~0Bh					
CA4(C4-A~C4-P)	0Ch~0Fh					
CA5(C5-A~C5-P)	10h~13h					
CA6(C6-A~C6-P)	14h~17h					
CA7(C7-A~C7-P)	18h~1Bh					
CA8(C8-A~C8-P)	1Ch~1Fh					
CA9(C9-A~C9-P)	20h~23h					
CB1(C10-A~C10-P)	24h~27h					
CB2(C11-A~C11-P)	28h~2Bh					
CB3(C12-A~C12-P)	2Ch~2Fh					
CB4(C13-A~C13-P)	30h~33h					
CB5(C14-A~C14-P)	34h~37h					
CB6(C15-A~C15-P)	38h~3Bh					
CB7(C16-A~C16-P)	3Ch~3Fh					



I2C INTERFACE WITH LED MATRIX TYPE-3



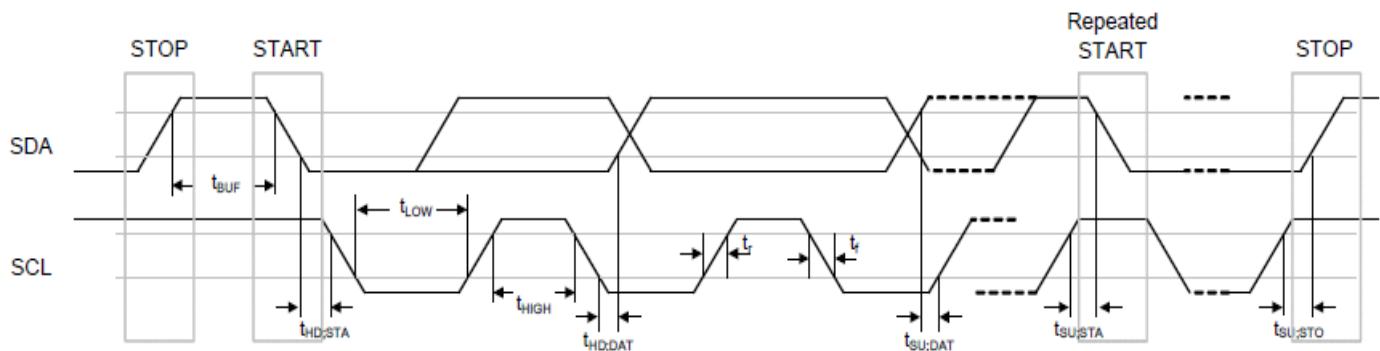
MATRIX TYPE 3

FDH COMMAND REGISTER

Data	Function
0x00	Point to Page One (Frame 1 Register is available)
0x01	Point to Page Two (Frame 2 Register is available)
0x0B	Point to Page Nine (Function Register is available)
0x0C	Point to Page Ten (Detection Register is available)
0x0D	Point to Page Eleven (LED Vaf Register is available)

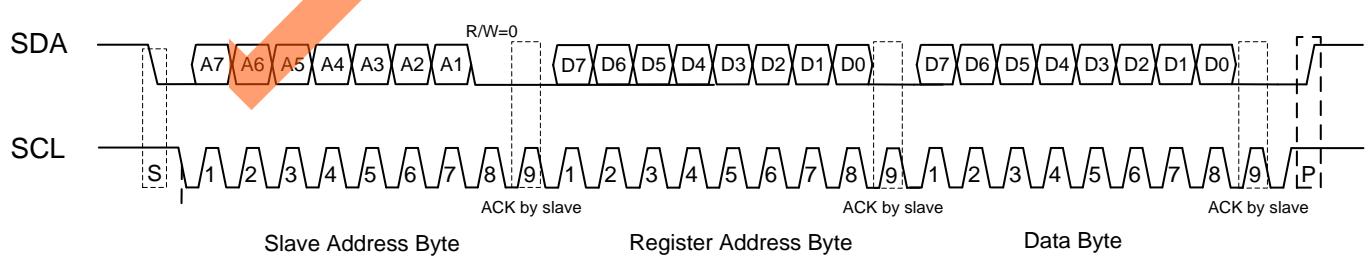
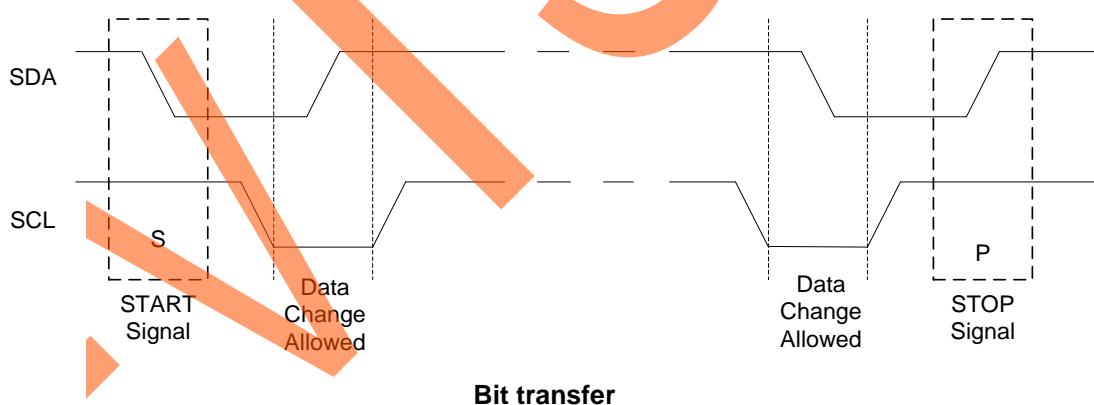
PHASE SEQUENCE OF MATRIX TYPE-3

For Matrix Type-3, there are total 16 phases in a frame. And each phase contains two sub-phases: Current Source phase and blanking phase. The following table shows the phase sequence in order.

Phase	LED State		
	LED Location	Current Source IOs	Sink IO
1-1	C _{1-A} ~C _{1-P}	CA2~CA9, CB1~CB8	CA1
1-2	-	By Vaf	By Vaf
2-1	C _{2-A} ~C _{2-P}	CA1, CA3~CA9, CB1~CB8	CA2
2-2	-	By Vaf	By Vaf
3-1	C _{3-A} ~C _{3-P}	CA1~CA2, CA4~CA9, CB1~CB8	CA3
3-2	-	By Vaf	By Vaf
4-1	C _{4-A} ~C _{4-P}	CA1~CA3, CA5~CA9, CB1~CB8	CA4
4-2	-	By Vaf	By Vaf
5-1	C _{5-A} ~C _{5-P}	CA1~CA4, CA6~CA9, CB1~CB8	CA5
5-2	-	By Vaf	By Vaf
6-1	C _{6-A} ~C _{6-P}	CA1~CA5, CA7~CA9, CB1~CB8	CA5
6-2	-	By Vaf	By Vaf
7-1	C _{7-A} ~C _{7-P}	CA1~CA6, CA8~CA9, CB1~CB8	CA7
7-2	-	By Vaf	By Vaf
8-1	C _{8-A} ~C _{8-P}	CA1~CA7, CA9, CB1~CB8	CA8
8-2	-	By Vaf	By Vaf
9-1	C _{9-A} ~C _{9-P}	CA1~CA8, CB2~CB8	CA9
9-2	-	By Vaf	By Vaf
10-1	C _{10-A} ~C _{10-P}	CA1~CA9, CB2~CB8	CB1
10-2	-	By Vaf	By Vaf
11-1	C _{11-A} ~C _{11-P}	CA1~CA9, CB1, CB3~CB8	CB2
11-2	-	By Vaf	By Vaf
12-1	C _{12-A} ~C _{12-P}	CA1~CA9, CB1~CB2, CB8	CB3
12-2	-	By Vaf	By Vaf
13-1	C _{13-A} ~C _{13-P}	CA1~CA9, CB1~CB3, CB5~CB8	CB4
13-2	-	By Vaf	By Vaf
14-1	C _{14-A} ~C _{14-P}	CA1~CA9, CB1~CB4, CB6~CB8	CB5
14-2	-	By Vaf	By Vaf
15-1	C _{15-A} ~C _{15-P}	CA1~CA9, CB1~CB5, CB7~CB8	CB6
15-2	-	By Vaf	By Vaf
16-1	C _{16-A} ~C _{16-P}	CA1~CA9, CB1~CB6, CB8	CB7
16-2	-	By Vaf	By Vaf



Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock frequency	-	-	400	kHz
t_{BUFS}	Bus free time between a STOP and a START condition	1.3	-	-	us
$t_{HD,STA}$	Hold Time (repeated) START condition	0.6	-	-	us
$t_{SU,STA}$	Repeated START condition setup time	0.6	-	-	us
$t_{SU,STO}$	STOP condition setup time	0.6	-	-	us
$t_{HD,DAT}$	Data hold time	-	-	0.9	us
$t_{SU,DAT}$	Data setup time	100	-	-	ns
t_{LOW}	SCL clock low period	1.3	-	-	us
t_{HIGH}	SCL clock high period	0.7	-	-	us
t_R	Rise time of both SDA and SCL signals, receiving	20	-	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	20	-	300	ns



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING

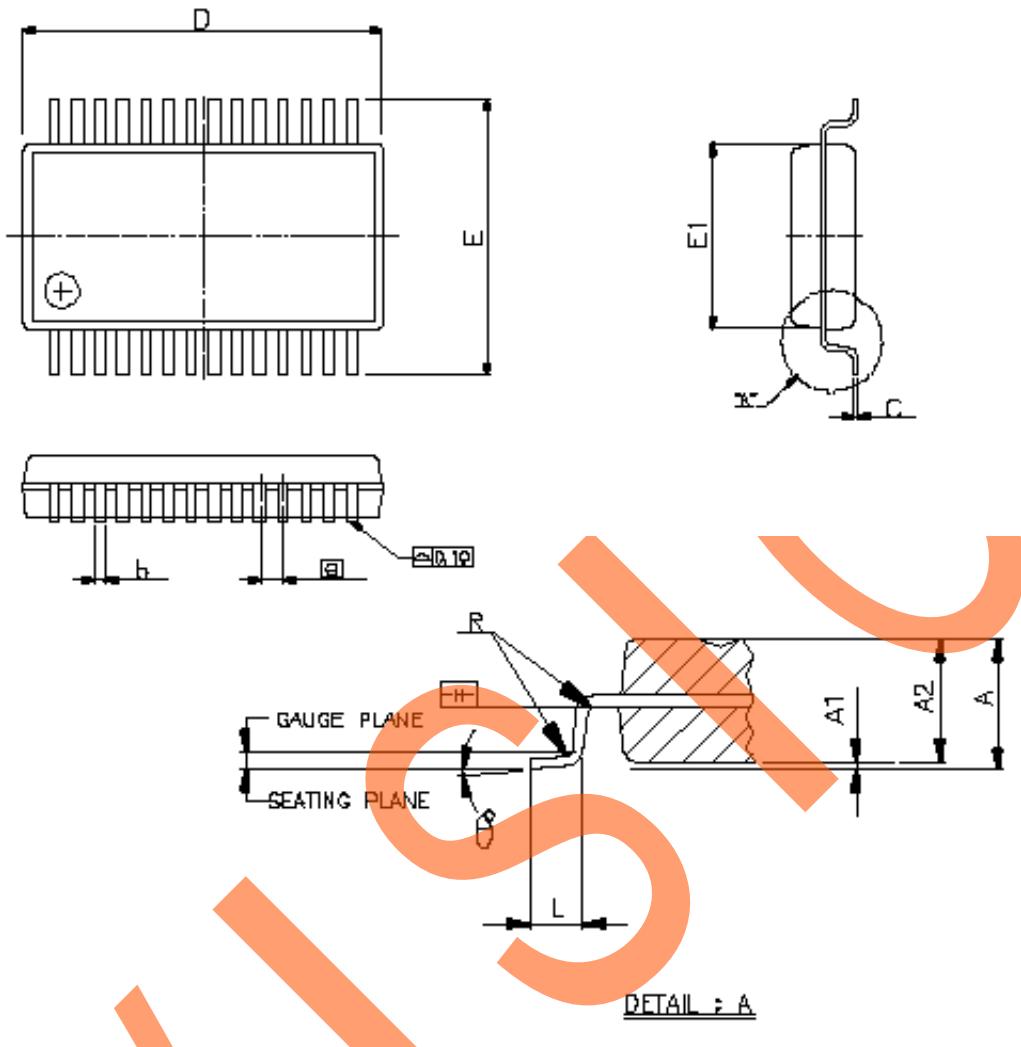
Supply voltage (Vdd).....	- 0.3V ~ 5.5V
Input in voltage (Vin).....	Vss - 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr).....	0°C ~ + 70°C
Storage ambient temperature (Tstor)	-40°C ~ + 125°C

ELECTRICAL CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V,, ambient temperature is 25°C unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd		2.7	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset	0.05	-	-	V/ms
Input Low Voltage	ViL	MSEL, SDB, SYNC, R_EXT/CS,	Vss	-	0.3*Vdd	V
Input High Voltage	ViH	SCK/SCL, SDA/MOSI, AD/MISO pins	0.7*Vdd	-	Vdd	V
I/O port input leakage current	Ilekg	Vin = Vdd	-	-	2	uA
Default output current	Iout	Output current of CA1~CA9, CB1~CB9 The Constant Current Step setting is 11 0001b	-	32	-	mA
Current sink headroom voltage	VHR1	Isink = 270mA	-	-	400	mV
Current source headroom voltage	VHR1	Isource = 32mA	-	-	400	mV
I/O output source current sink current	IoH	Vop = Vdd - 0.5V			-	mA
	IoL	Vop = Vss + 0.5V			-	
Supply Current (Disable ADC)	Idd1	Normal Mode Vdd= 5V	-	TBD	-	mA
	Idd2	Soft Shutdown Mode Vdd= 5V	-	TBD	-	uA
	Idd3	Hardware Shutdown Mode Vdd= 5V	-	TBD	-	uA
LVD Voltage	VLVD	Low voltage reset/indicator level	2.4	2.55	2.7	V

11.3 SSOP 28 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.08	-	-	2.13
A1	0.00	-	0.01	0.05	-	0.25
A2	0.06	0.07	0.07	1.63	1.75	1.88
b	0.01	-	0.01	0.22	-	0.38
C	0.00	-	0.01	0.09	-	0.20
D	0.39	0.40	0.41	9.90	10.20	10.50
E	0.29	0.31	0.32	7.40	7.80	8.20
E1	0.20	0.21	0.22	5.00	5.30	5.60
[e]	0.0259BSC			0.65BSC		
L	0.02	0.04	0.04	0.63	0.90	1.03
R	0.00	-	-	0.09	-	-
θ°	0°	4°	8°	0°	4°	8°