深圳维盛半导体科技有限公司

VS12L08A 参考手册

Evision Matrix LED Driver IC

1 PRODUCT OVERVIEW

1.1 FEATURES

- **Support I2C/SPI slave communication**

- **Built-in four LED Matrix Types**
- **LED Matrix Type-1**
  Achieve 9x8+9x8 LED matrix by CA1~CA9 and CB1~CB9.
  Maximum to 144 LEDs are supported.
  Maximum to 36 anode RGB LEDs are supported.
  Maximum to 36 cathode RGB LEDs are supported.
- **LED Matrix Type-2**
  Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.
  Maximum to 144 LEDs are supported.
  Maximum to 40 anode RGB LEDs are supported.
  Maximum to 41 cathode RGB LEDs are supported.
- **LED Matrix Type-3**
  Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8
  Maximum to 256 LEDs are supported.
  Maximum to 75 anode RGB LEDs are supported.
  Maximum to 75 cathode RGB LEDs are supported.
- **LED Matrix Type-4**
  Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9, CB1~CB9, and CC1~CC6.
  Maximum to 144 LEDs are supported.
  Maximum to 48 anode RGB LEDs are supported.
  Maximum to 48 cathode RGB LEDs are supported.

- **LED Controls**
  Each LED has the on/off control.
  Each LED has the blink enable/disable control.
  Each LED has the 8-bit programmable PWM duty.
  Each LED has the open/short detection status.
  Each LED has the anti-forward control (Vaf) to prevent the ghost LED effects.
  Each LED has the +/-6% current fine tune control.
  Support global 8mA~40mA constant current source control.

- **MPWM IO (CA1~CA9, CB1~CB9, and CC1~CC6)**
  Each MPWM IO has sink current of 320mA.
  Each MPWM IO supports staggered delay.
  Each MPWM IO supports slew rate control.
  Each MPWM IO except CC1~CC6 has the precise current skew under +/-2%.
  Current skew between chips is under +/-2%.

- **System Clock Synchronization for cascaded LED drivers**
  Support SYNC output in master mode.
  Support SYNC input in slave mode.

- **I2C Slave**
  Maximum to 400KHz
  Support four auto-selective slave addresses by which AD pin is connected to. (VDD/VSS/SCL/SDA)

- **SPI Slave**
  Maximum to 2.4MHz

- **Matrix Control Engine**
  Support Type 1~4 matrixes by register setting.
  The frame time depending on Matrix Type has different phase number.
  Type-1 has the frame time 1098us including 9 phases.
  Type-2 and Type-4 have the frame time 1464us including 12 phases.
  Type-3 has the frame time 1952us including 16 phases.
  Each phase includes the PWM duty time 107us and the blanking time 15us.
  Support auto-breath control.
  Support auto-blink control.
  Support Audio-IN synchronous to auto-brightness control.

- **Audio In Gain Control**
  Support register configurable gain for Audio-IN: 0dB, 3dB, 6dB, 9dB, 12dB, 15dB, 18dB, and 21dB.
  Support auto-gain control.

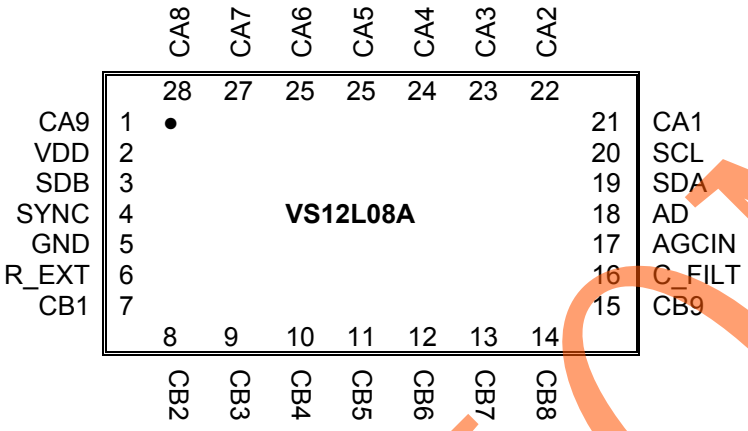
- **Thermal Detection**
  Support thermal shutdown at 150℃
  Support thermal flag at 70℃

- **Power Modes**
  Normal Mode
  Software power down mode
  Hardware power down mode.

- **Package**
  QFN28.

1.2 PIN ASSIGNMENT

VS12L08A (QFN 28pins): I2C Interface



1.3 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pin for digital and analog circuit.
		Power supply input pin for digital and analog circuit.
		Power supply input pins for digital and analog circuit.
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. MSEL = 0 : I2C, pMSEL = 1 : SPI.
SDB	I	Schmitt trigger structure as input mode with internal pull-down resistor. Shutdown the chip when pull to low.
SYNC	I/O	Clock synchronous input or output pin. Schmitt trigger structure as input mode.
R_EXT/CS	I	R_EXT: Input only with internal pull down resistor in I2C mode. No external pull-down resistor is required.
		CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.
C_FILT	O	Used for filter audio-in noise.
AGCIN	I	Audio-IN Input.
AD/MISO	I/O	AD: I2C slave address selection pin. Schmitt trigger structure as input mode.
		MISO: SPI Master-Input-Slave-Output pin.
SDA/MOSI	I/O	SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode.
		MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.
SCL/SCK	I/O	SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode.
		SCK: SPI Clock input pin. Schmitt trigger structure as input mode.
CA1~CA9	O	PWM IO with sink 320mA and constant current source.
CB1~CB9	O	PWM IO with sink 320mA and constant current source.
CC1~CC6	O	PWM IO with sink 320mA.

2 ARCHITECTURE DESCRIPTOR

2.1 RAM MAPPING FOR MATRIX TYPE 1 & 2 & 4

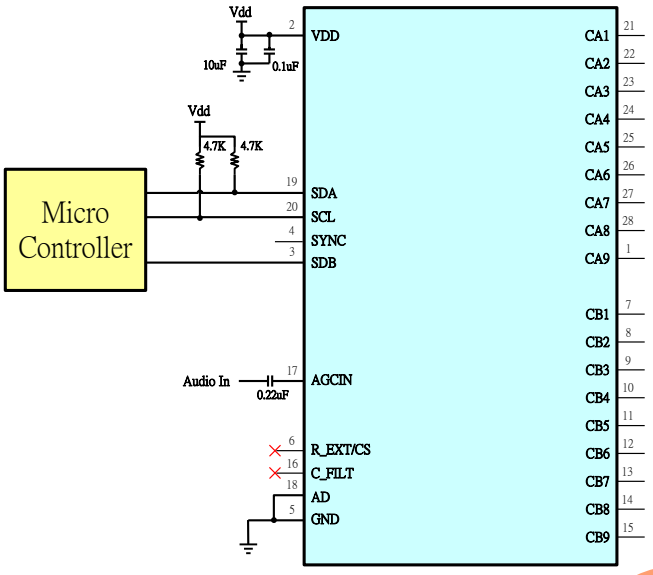
Frame No.	User Address	*Register Segment*	Comment
↑	000H … 011H	***LED Control Register***	18-byte
Frame 1	012H … 023H	***Blink Control Register***	18-byte
	024H … 0B3H ↓	***PWM Register***	144-byte
↑	000H … 011H	***LED Open Register***	18-byte
Frame C	012H … 023H	***LED Short Register***	18-byte
	024H … 06BH ↓	***Current Fine Tune Register***	72-byte
↑ **Frame D** ↓	000H … 023H	***LED Vaf Register***	36-byte

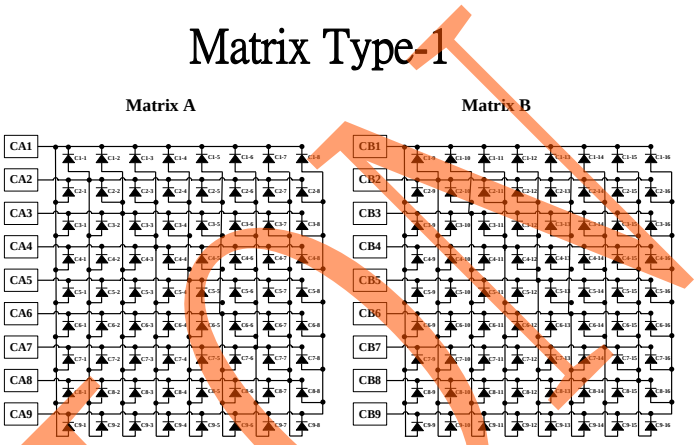
2.2 RAM MAPPING FOR MATRIX TYPE 3

Frame No.	User Address	*Register Segment*	Comment
↑	000H . . . 00FH	***LED Control Register L***	16-byte
Frame 1	010H . . . 01FH	***Blink Control Register L***	16-byte
	020H . . . 09FH	***PWM Register L***	128-byte
↑	000H . . . 00FH	***LED Control Register H***	16-byte
Frame 2	010H . . . 01FH	***Blink Control Register H***	16-byte
	020H . . . 09FH	***PWM Register H***	128-byte
↑	000H . . . 01FH	***LED Open Register***	32-byte
Frame C	020H . . . 03FH	***LED Short Register***	32-byte
	040H . . . 0BFH	***Current Fine Tune Register***	128-byte
↑ **Frame D**	000H . . . 03FH	***LED Vaf Register***	64-byte

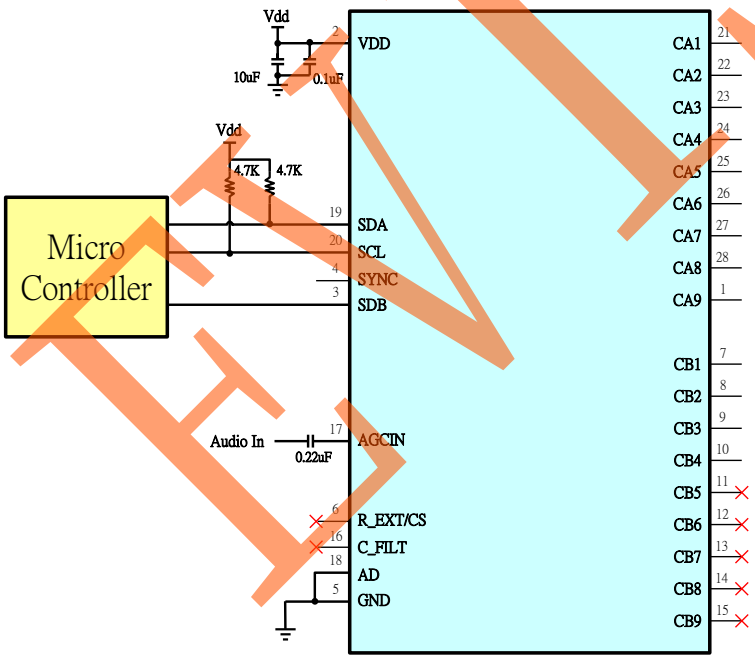
3 APPLICATION CIRCUIT

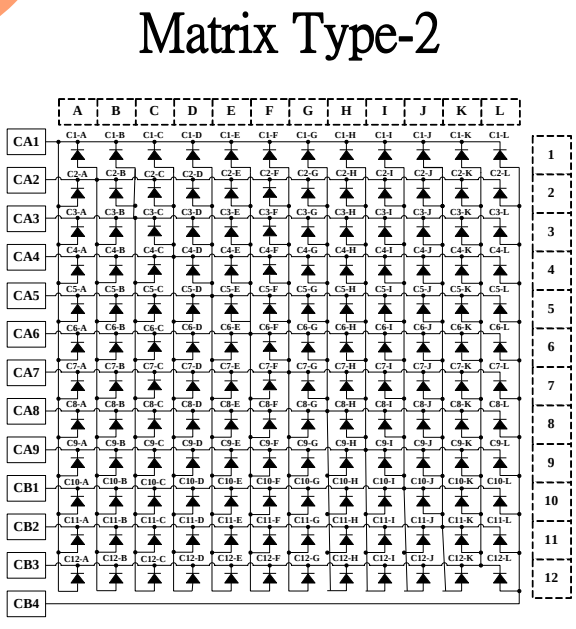
3.1 I2C INTERFACE WITH LED MATRIX TYPE-1



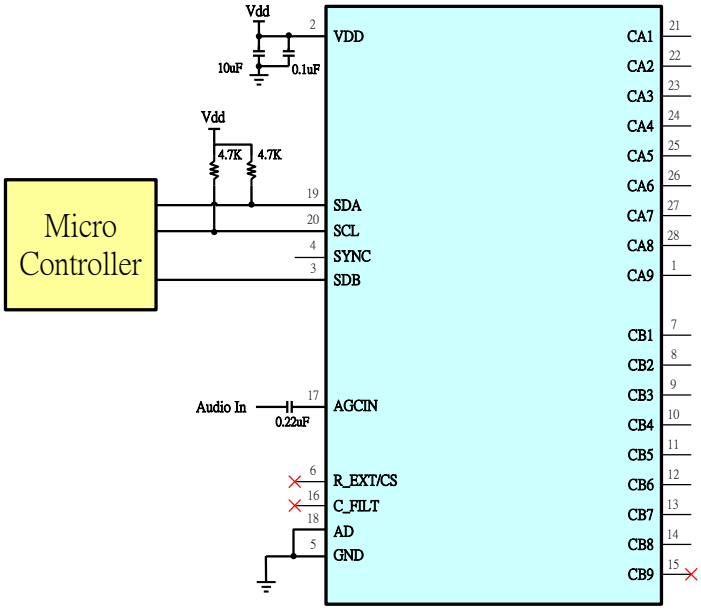


3.2 I2C INTERFACE WITH LED MATRIX TYPE-2

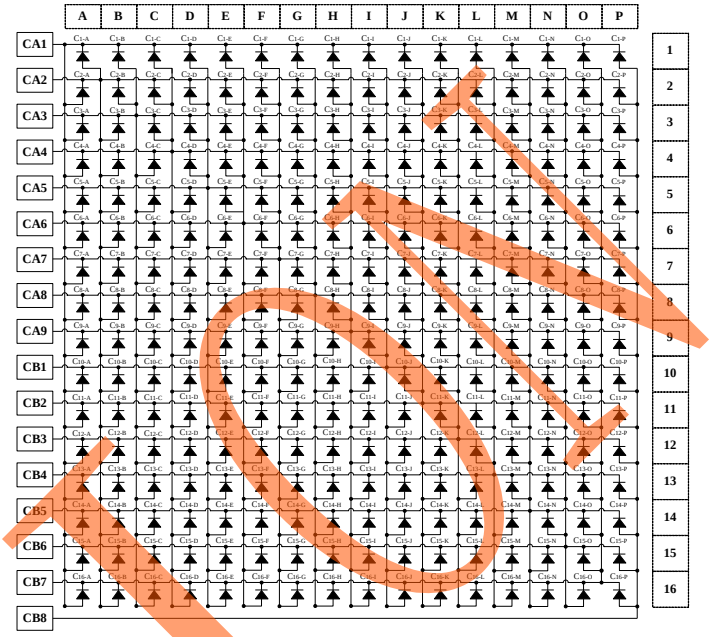




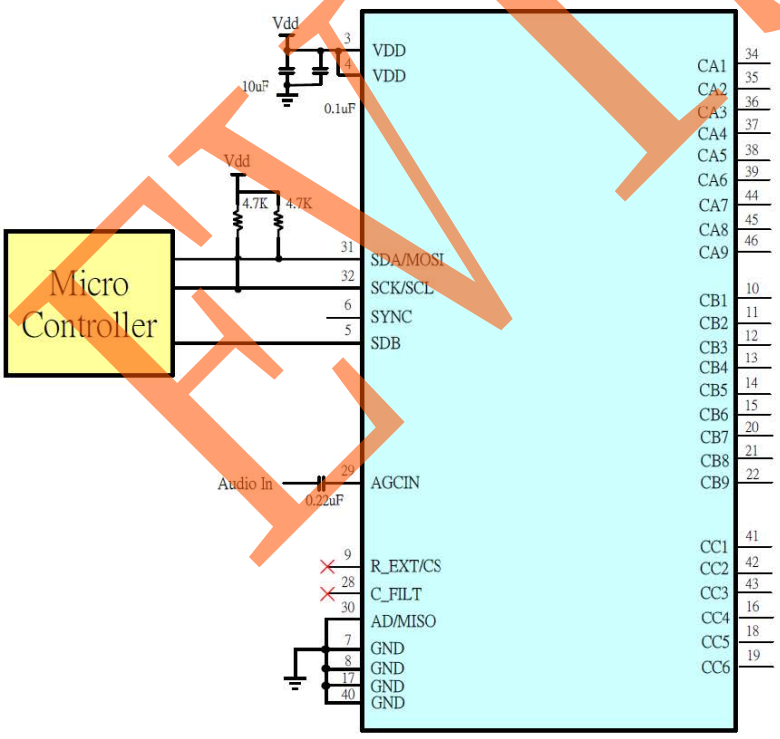
3.3 I2C INTERFACE WITH LED MATRIX TYPE-3



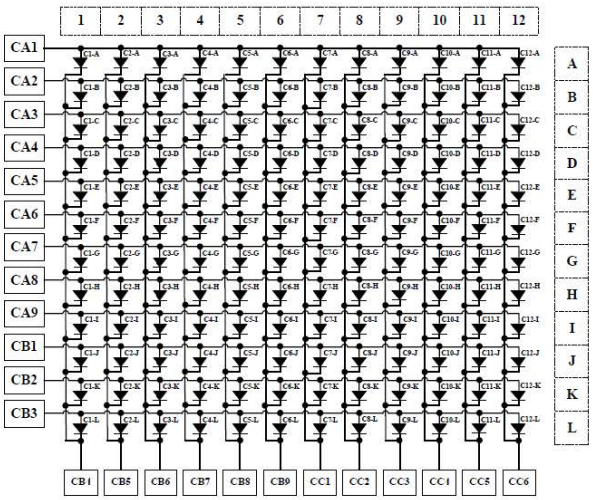
Matrix Type-3



3.4 I2C INTERFACE WITH LED MATRIX TYPE-4



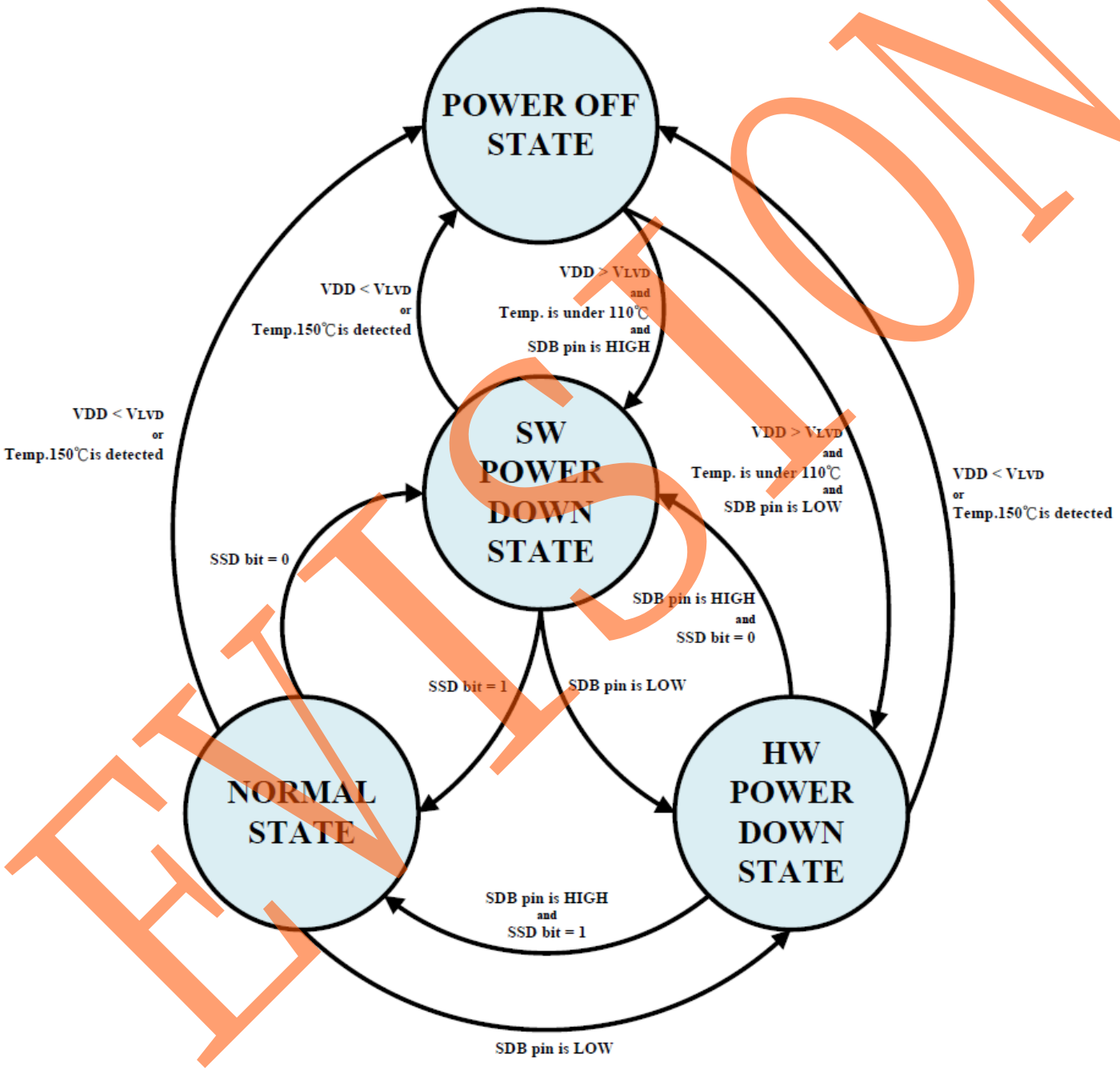
Matrix Type-4



4 SYSTEM OPERATION MODE

4.1 POWER STATE MACHINE FLOW CHART

Power states are determined by the VLVD threshold, the thermal detector 150℃ threshold, the SDB pin state, and the software shutdown register (SSD bit) status.



5 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... 0°C ~ + 70°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

5.2 ELECTRICAL CHARACTERISTIC

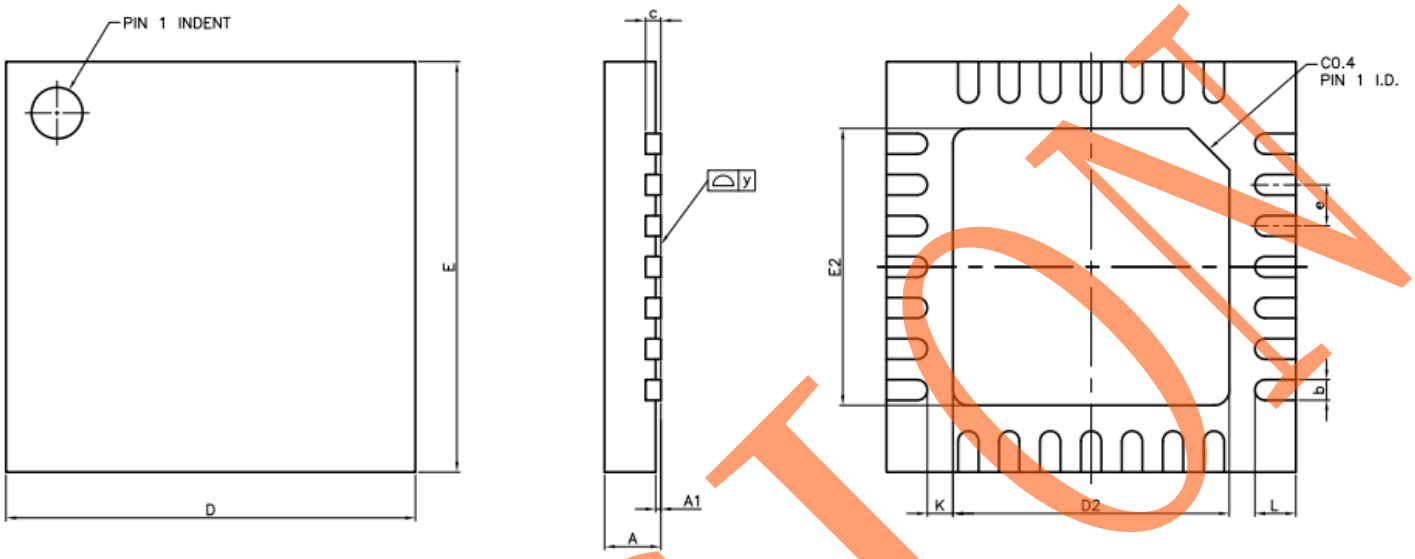
- **DC CHARACTERISTIC**

(All of voltages refer to Vss, Vdd = 5.0V,,ambient temperature is 25℃ unless otherwise

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd			2.7	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset		0.05	-	-	V/ms
Input Low Voltage	ViL	MSEL, SDB, SYNC, R_EXT/CS, SCK/SCL, SDA/MOSI, AD/MISO pins		Vss	-	0.3*Vdd	V
Input High Voltage	ViH			0.7*Vdd	-	Vdd	V
I/O port input leakage current	Ilekg	Vin = Vdd		-	-	2	uA
Default output current	Iout	Output current of CA1~CA9, CB1~CB9 The Constant Current Step setting is 11 0001b		-	32	-	mA
Current sink headroom voltage	V_{HR1}	Isink = 270mA		-	-	400	mV
Current source headroom voltage	V_{HR1}	Isource = 32mA		-	-	400	mV
I/O output source current sink current	IoH	Vop = Vdd – 0.5V				-	mA
	IoL	Vop = Vss + 0.5V				-	
Supply Current (Disable ADC)	Idd1	Normal Mode	Vdd= 5V	-	TBD	-	mA
	Idd2	Soft Shutdown Mode	Vdd= 5V	-	TBD	-	uA
	Idd3	Hardware Shutdown Mode	Vdd= 5V	-	TBD	-	uA
LVD Voltage	V_{LVD}	Low voltage reset/indicator level		2.4	2.55	2.7	V

6 PACKAGE INFORMATION

6.1 QFN 28 PIN



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.57	0.60	0.63
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	---	0.15 REF.	---
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e	---	0.40	---
K	---	0.25 REF.	---
L	0.35	0.40	0.45
y	0.00	---	0.075