

深圳维盛半导体科技有限公司

VS12L09A 参考手册





1 PRODUCT OVERVIEW

1.1 FEATURES

♦ Support I2C/SPI slave communication

♦ Built-in four LED Matrix Types

◆ LED Matrix Type-1

Achieve 9x8+9x8 LED matrix by CA1~CA9 and CB1~CB9.

Maximum to 144 LEDs are supported.

Maximum to 36 anode RGB LEDs are supported.

Maximum to 36 cathode RGB LEDs are supported.

♦ LED Matrix Type-2

Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.

Maximum to 144 LEDs are supported.

Maximum to 40 anode RGB LEDs are supported.

Maximum to 41 cathode RGB LEDs are supported.

◆ LED Matrix Type-3

Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8 Maximum to 256 LEDs are supported.

Maximum to 75 anode RGB LEDs are supported. Maximum to 75 cathode RGB LEDs are supported.

♦ LED Matrix Type-4

Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9, CB1~CB9, and CC1~CC6.

Maximum to 144 LEDs are supported.

Maximum to 48 anode RGB LEDs are supported.

Maximum to 48 cathode RGB LEDs are supported.

LED Controls

Each LED has the on/off control.

Each LED has the blink enable/disable control.

Each LED has the 8-bit programmable PWM duty.

Each LED has the open/short detection status.

Each LED has the anti-forward control (Vaf) to

prevent the ghost LED effects.

Each LED has the +/-6% current fine tune control. Support global 8mA~40mA constant current source control.

♦ MPWM IO (CA1~CA9, CB1~CB9, and CC1~CC6)

Each MPWM IO has sink current of 320mA.

Each MPWM IO supports staggered delay.

Each MPWM IO supports slew rate control.

Each MPWM IO except CC1~CC6 has the precise

current skew under +/-2%.

Current skew between chips is under +/-2%.

System Clock Synchronization for cascaded LED drivers

Support SYNC output in master mode. Support SYNC input in slave mode.

I2C Slave

Maximum to 400KHz

Support four auto-selective slave addresses by which AD pin is connected to. (VDD/VSS/SCL/SDA)

♦ SPI Slave

Maximum to 2.4MHz

♦ Matrix Control Engine

Support Type 1~4 matrixes by register setting.

The frame time depending on Matrix Type has different phase number.

Type-1 has the frame time 1098us including 9 phases. Type-2 and Type-4 have the frame time 1464us including 12 phases.

Type-3 has the frame time 1952us including 16 phases.

Each phase includes the PWM duty time 107us and the blanking time 15us.

Support auto-breath control.

Support auto-blink control.

Support Audio-IN synchronous to auto-brightness control.

♦ Audio In Gain Control

Support register configurable gain for Audio-IN: 0dB, 3dB, 6dB, 9dB, 12dB, 15dB, 18dB, and 21dB. Support auto-gain control.

▲ Thermal Detection

Support thermal shutdown at 150° C Support thermal flag at 70° C

♦ Power Modes

Normal Mode Software power down mode Hardware power down mode.

Package

QFN28/SSOP28.



1.2 PIN ASSIGNMENT

(SSOP 28pins): I2C Interface

CA9	1	U	28	CA8
VDD	2		27	CA7
SDB	3		26	CA6
SYNC	4		25	CA5
GND	5		24	CA4
R_EXT	6		23	CA3
CB1	7		22	CA2
CB2	8		21	CA1
CB3	9		20	SCL
CB4	10		19	SDA
CB5	11		18	AD
CB6	12		17	AGCIN
CB7	13		16	C_FILT
CB8	14		15	CB9

1.3 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION	
VDD, VSS	Р	Power supply input pin for digital and analog circuit. Power supply input pin for digital and analog circuit. Power supply input pins for digital and analog circuit.	
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. MSEL = 0 : I2C, pMSEL = 1 : SPI.	
SDB	I	Schmitt trigger structure as input mode with internal pull-down resistor. Shutdown the chip when pull to low.	
SYNC	I/O	Clock synchronous input or output pin. Schmitt trigger structure as input mode.	
R_EXT/CS		R_EXT: Input only with internal pull down resistor in I2C mode. No external pull-down resistor is required. CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.	
C_FILT	0	Used for filter audio-in noise.	
AGCIN	I	Audio-IN Input.	
AD/MISO	AD: I2C slave address selection pin. Schmitt trigger structure as input mode		
SDA/MOSI I/O SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as inc		SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode. MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.	
		SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode. SCK: SPI Clock input pin. Schmitt trigger structure as input mode.	
CA1~CA9	0	PWM IO with sink 320mA and constant current source.	
CB1~CB9	0	PWM IO with sink 320mA and constant current source.	
CC1~CC6	0	PWM IO with sink 320mA.	



2 ARCHITECTURE DESCRIPTOR

2.1 RAM MAPPING FOR MATRIX TYPE 1 & 2 & 4

Frame No.	User Address	Register Segment	Comment		
↑	000H				
		LED Control Register	18-byte		
	011H				
	012H				
Frame 1		Blink Control Register	18-byte		
	023H				
	024H				
		PWM Register	144-byte		
	0B3H				
↑	000H				
		LED Open Register	18-byte		
	011H				
	012H		•		
Frame C	•••	LED Short Regi <mark>ste</mark> r	18-byte		
	023H				
	024H				
		Current Fine	72-byte		
	06BH	Tune Register			
<u> </u>	000H				
Frame D		LED Vaf Register	36-byte		
	023H				





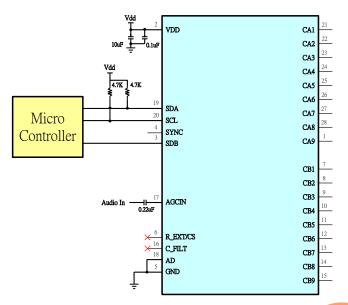
2.2 RAM MAPPING FOR MATRIX TYPE 3

Frame No.	User Address	Register Segment	Comment	
↑	000H			
		LED Control Register L	16-byte	
_	00FH			
	010H			
Frame 1		Blink Control Register L	16-byte	
	01FH			
	020H			
		PWM Register L	128-byte	
	09FH			
↑	000H			
		LED Control Register H	16-byte	
	00FH			
	010H			
Frame 2		Blink Control Register H	16-byte	
	01FH			
	020H			
		PWM Register H	128-byte	
	09FH			
↑	000H			
		LED Open Register	32-byte	
	01FH			
	020H			
Frame C		LED Short Register	32-byte	
	03FH			
	040H			
		Current Fine Tune Register	128-byte	
	0BFH			
†	000H			
Frame D		LED Vaf Register	64-byte	
	03FH			

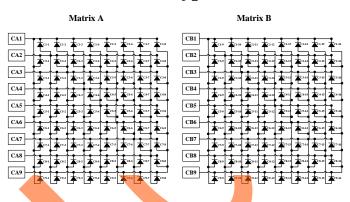


3 APPLICATION CIRCUIT

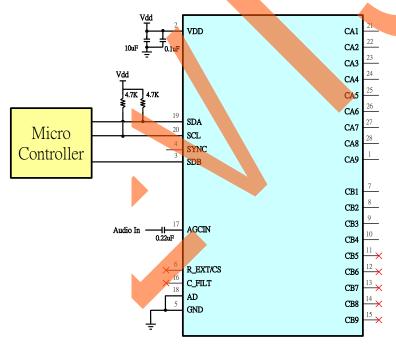
3.1 I2C INTERFACE WITH LED MATRIX TYPE-1



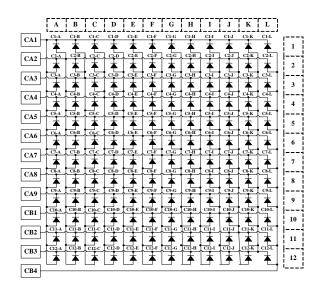
Matrix Type-1



3.2 I2C INTERFACE WITH LED MATRIX TYPE-2



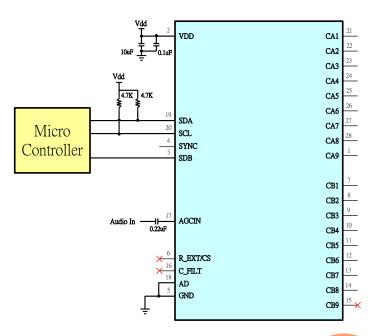
Matrix Type-2

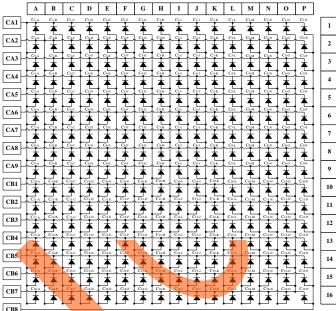




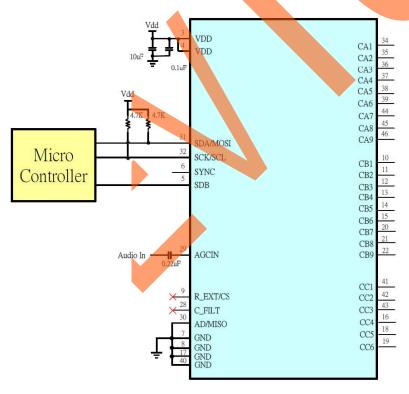
3.3 I2C INTERFACE WITH LED MATRIX TYPE-3

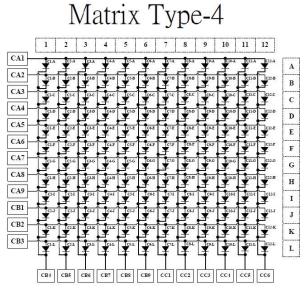
Matrix Type-3





3.4 I2C INTERFACE WITH LED MATRIX TYPE-4





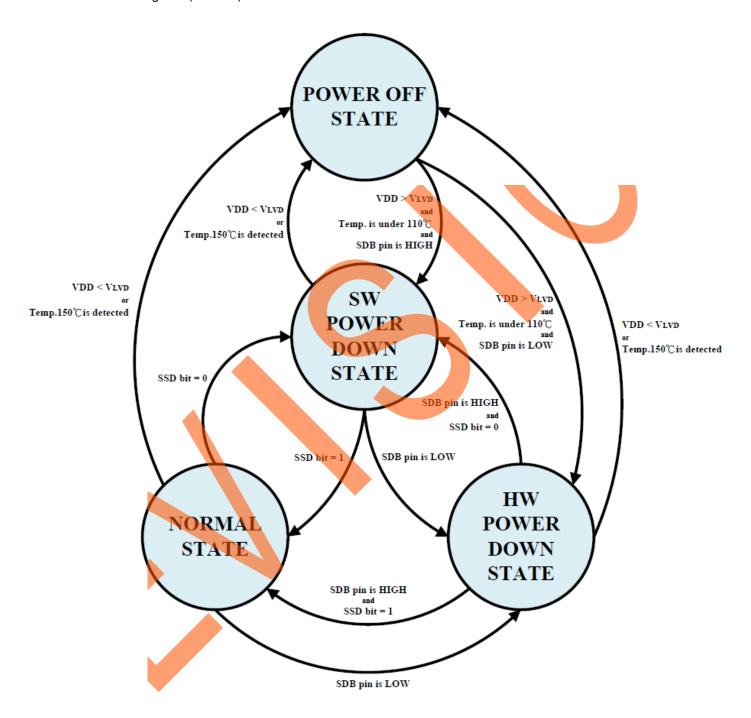


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SYSTEM OPERATION MODE

4.1 POWER STATE MACHINE FLOW CHART

Power states are determined by the VLVD threshold, the thermal detector 150°C threshold, the SDB pin state, and the software shutdown register (SSD bit) status.





5 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATING

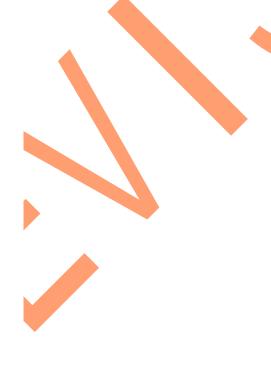
Supply voltage (Vdd)	0.3V ~ 5.5V
Input in voltage (Vin)	
Operating ambient temperature (Topr)	
Storage ambient temperature (Tstor)	40°C ~ + 125°C

5.2 ELECTRICAL CHARACTERISTIC

DC CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V,,ambient temperature is 25°C unless otherwise

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd		2.7	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset	0.05	-	-	V/ms
Input Low Voltage	ViL	MSEL, SDB, SYNC, R_EXT/CS,	Vss	-	0.3*Vdd	V
Input High Voltage	ViH	SCK/SCL, SDA/MOSI, AD/MISO pins	0.7*Vdd	-	Vdd	V
I/O port input leakage current	llekg	Vin = Vdd		-	2	uA
Default output current	lout	Output current of CA1~CA9, CB1~CB9 The Constant Current Step setting is 11 0001b		32	-	mA
Current sink headroom voltage	VHR1	Isink = 270mA	-)	400	mV
Current source headroom voltage	VHR1	Isource = 32mA	-	-	400	mV
I/O output source current	ΙοΗ	Vop = Vdd - 0.5V			-	mA
sink current	loL	IoL Vop = Vss + 0.5V			-	ША
	ldd1	Normal Mode Vdd= 5V	-	TBD	-	mΑ
Supply Current (Disable ADC)	ldd2	Soft Shutdown Mode Vdd= 5V		TBD	-	uA
(2.332.37.20)	ldd3	Hardware Shutdown Mode Vdd= 5V	-	TBD	-	uA
LVD Voltage	VLVD	Low voltage reset/indicator level	2.4	2.55	2.7	V

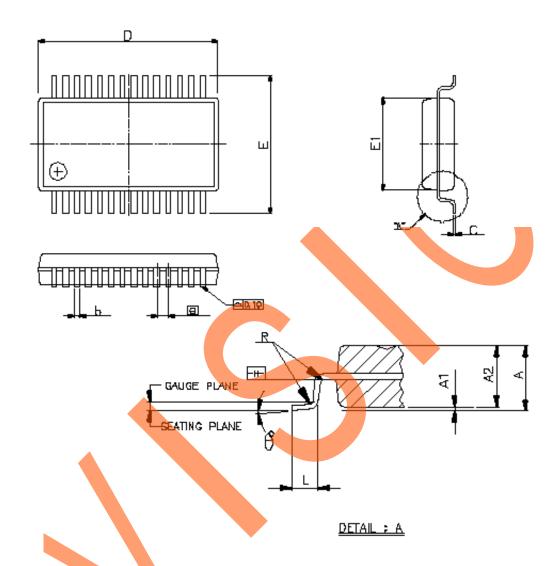




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6 PACKAGE INFORMATION

6.1 SSOP 28 PIN



CVMDOLC	MIN	NOR	MAX	MIN	NOR	MAX		
SYMBOLS		(inch)				(mm)		
Α	-	-	0.08	-	-	2.13		
A1	0.00	-	0.01	0.05	-	0.25		
A2	0.06	0.07	0.07	1.63	1.75	1.88		
b	0.01	-	0.01	0.22	-	0.38		
C	0.00	•	0.01	0.09	-	0.20		
D	0.39	0.40	0.41	9.90	10.20	10.50		
E	0.29	0.31	0.32	7.40	7.80	8.20		
E1	0.20	0.21	0.22	5.00	5.30	5.60		
[e]	0.0259BSC				0.65BSC			
L	0.02	0.04	0.04	0.63	0.90	1.03		
R	0.00	-	1	0.09	-	-		
θ°	0 °	4 °	8°	0 °	4 °	8°		