

PRODUCT OVERVIEW

FEATURES

◆ Memory configuration

Flash ROM size: 32KB.
User RAM: 2KB.
USB FIFO RAM: 256 bytes.

◆ Operation Frequency up to 48MHz

◆ Interrupt sources

ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).

◆ I/O pin configuration

Bi-directional: P0, P1, P2, P3.
Wakeup: P0, P1, P2, P3 level change.
Pull-up resistors: P0, P1, P2, P3.
20mA Sink/8mA Drive: P0, P1, P2, P3.

◆ Programmable WatchDog Timer (WDT)

Programmable watchdog frequency with watchdog clock source and divider.

◆ System tick timer

24-bit timer.
The system tick timer clock is fixed to the frequency of the system clock.
The SysTick timer is intended to generate a fixed 10-ms interrupt.

◆ LVD with separate thresholds

Reset: 2.4V/3.6V for VDD.

◆ Full Speed USB 2.0

3.3v regulator output for D+ internal 1.5k pull-up resistor.
Supports one Full speed USB device address.
Supports PS/2 mode.
One control EP and 4 configurable INT/BULK Endpoints.
EP0 supports 64-byte FIFO depth.
Programmable EP1~EP4 FIFO depth.
Total 5 endpoints share 256-byte USB RAM.

◆ Working voltage 2.5V ~ 5.5V

◆ Timer

One 16-bit general purpose timer CT16B0 with CAP0.
One 16-bit general purpose timer CT16B1 with 23-ch PWM.

◆ Interfaces: I2C & SIO

- One I2C controller supporting I2C-bus specification.
- One SPI controller supporting SPI protocol.

◆ System clocks

Internal high clock: RC type 48MHz.
Internal low clock: RC type 32KHz.

◆ Serial Wire Debug (SWD)

◆ Operating modes

Normal, Sleep, and Deep-sleep.

◆ Fcpu (Instruction cycle)

$F_{CPU} = F_{HCLK} = F_{SYSCLK}/1, F_{SYSCLK}/2, F_{SYSCLK}/4, \dots, F_{SYSCLK}/128$.

◆ In-System-Programming (ISP) supported

◆ 3.3V Regulator output

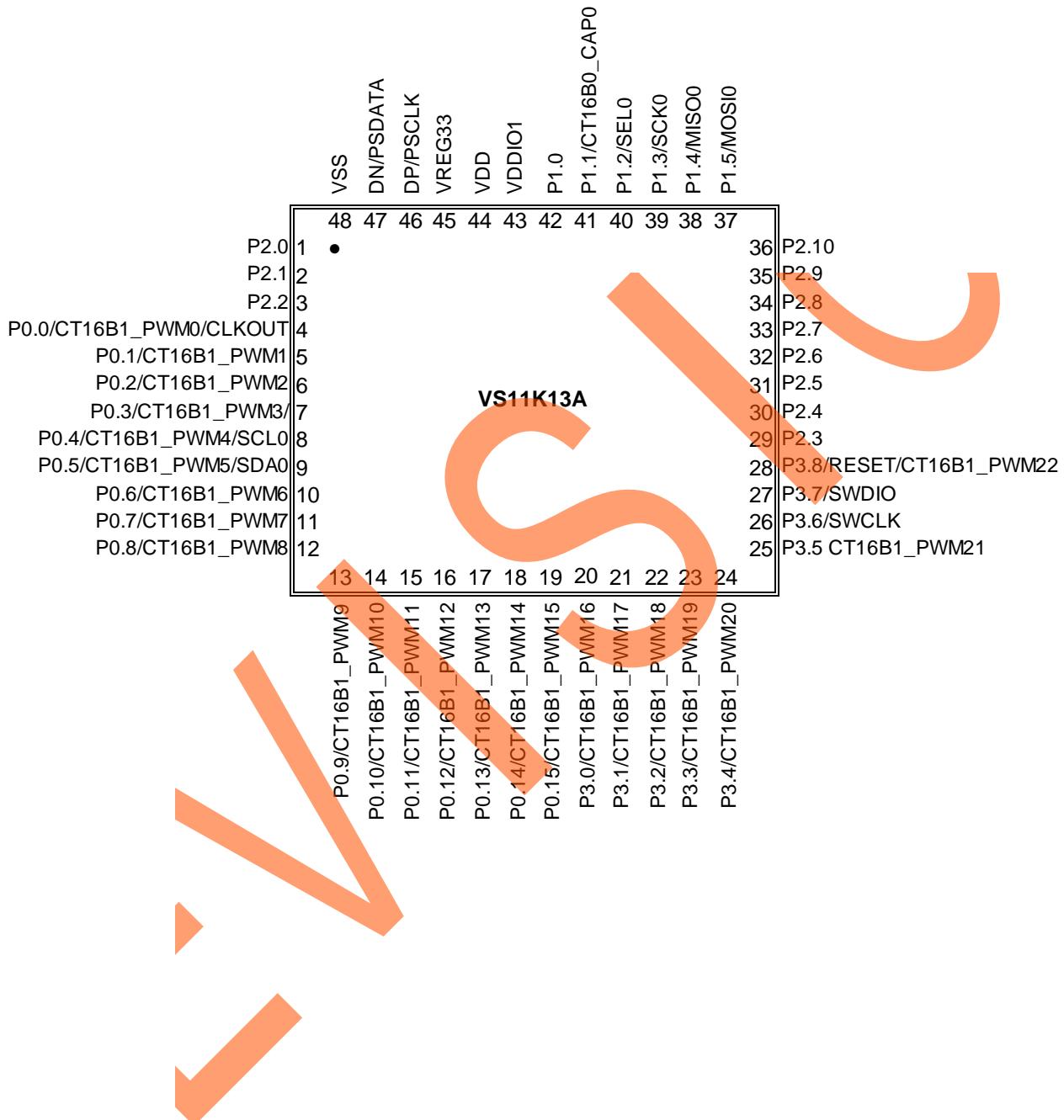
Driving current 60mA
Power for USB D+ internal pull-up resistor.
Can be IO power for P1.0~P1.5. (3.3V IOs)
Can be power source for peripheral 3.3V devices.

◆ Package (Chip form support)

LQFP48 pin
SOP28/SSOP28 pin

PIN ASSIGNMENT

VS11K13A (LQFP 48 pins)



PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital circuit.
VREG33	O	3.3v voltage output from USB 3.3v regulator.
DP/PSCLK	I/O	D+ — USB Differential signal line.
	I/O	PSCLK — PS/2 clock pin with internal 5K pull-up resistor.
DN/PSDATA	I/O	D- — USB Differential signal line.
	I/O	PSDATA — PS/2 data pin with internal 5K pull-up resistor.
VDDIO1	P	Power supply input pad for the IO power of P1.0~P1.5.
P0.0/CT16B1_PWM0/ CLKOUT	I/O	P0.0 — General purpose digital input/output pin.
	O	CT16B1_PWM0 — PWM output 0 for CT16B1.
	O	CLKOUT — Clockout pin.
P0.1/CT16B1_PWM1/ PGDCLK	I/O	P0.1 — General purpose digital input/output pin.
	O	CT16B1_PWM1 — PWM output 1 for CT16B1.
	I/O	PGDCLK — Flash clock pin in programming mode.
P0.2/CT16B1_PWM2	I/O	P0.2 — General purpose digital input/output pin.
	O	CT16B1_PWM2 — PWM output 2 for CT16B1.
P0.3/CT16B1_PWM3	I/O	P0.3 — General purpose digital input/output pin.
	O	CT16B1_PWM3 — PWM output 3 for CT16B1.
P0.4/CT16B1_PWM4/ SCL0	I/O	P0.4 — General purpose digital input/output pin.
	I/O	CT16B1_PWM4 — PWM output 4 for CT16B1.
	I/O	SCL0 — I2C clock input/output.
P0.5/CT16B1_PWM5/ SDA0	I/O	P0.5 — General purpose digital input/output pin.
	I/O	CT16B1_PWM5 — PWM output 5 for CT16B1.
	I/O	SDA0 — I2C data input/output.
P0.6~P0.15/CT16B1_ PWM6~15	I/O	P0.6~P0.15 — General purpose digital input/output pin.
	O	CT16B1_PWM6~15 — PWM output 6~15 for CT16B1.
P1.0	I/O	P1.0 — General purpose digital input/output pin.
P1.1/CT16B0_CAP0	I/O	P0.5 — General purpose digital input/output pin.
	I	CT16B0_CAP0 — Capture input 0 for CT16B0.
P1.2/SEL0	I/O	P0.6~P0.15 — General purpose digital input/output pin.
	I	SEL0 — Slave Select for SPI.
P1.3/SCK0	I/O	P1.3 — General purpose digital input/output pin.
	I/O	SCK0 — Serial clock for SPI.
P1.4/MISO0	I/O	P1.4 — General purpose digital input/output pin.

	I/O	MISO0 — Master In Slave Out for SPI.
P1.5/MOSI0	I/O	P1.5 — General purpose digital input/output pin.
	I/O	MOSI0 — Master Out Slave In for SPI.
P2.0~P2.10	I/O	P2.0~P2.10 — General purpose digital input/output pin.
P.3.0~P3.5/CT16B1_ PWM16~21	I/O	P3.0~P3.5 — General purpose digital input/output pin.
	O	CT16B1_PWM16~21 — PWM output 16~21 for CT16B1.
P3.6/SWCLK	I/O	P3.6 — General purpose digital input/output pin.
	I	SWCLK — Serial Wire Clock pin.
P3.7/SWDIO	I/O	P3.7 — General purpose digital input/output pin.
	I/O	SWDIO — Serial Wire Data input/output pin.
P3.8/RESET/CT16B1 _PWM22	I/O	P3.8 — General purpose digital input/output pin.
	I	RESET — External Reset input. Schmitt trigger structure, active “Low”, normally stay “High”.
	O	CT16B1_PWM22 — PWM output 22 for CT16B1.



PACKAGE INFORMATION

LQFP 48 PIN

