1.PRODUCT OVERVIEW

1.1 FEATURES

- **Support I2C/SPI slave communication**

- **Built-in four LED Matrix Types**
- **LED Matrix Type-1**
  Achieve 9x8+9x8 LED matrix by CA1~CA9 and CB1~CB9.
  Maximum to 144 LEDs are supported.
  Maximum to 36 anode RGB LEDs are supported.
  Maximum to 36 cathode RGB LEDs are supported.
- **LED Matrix Type-2**
  Achieve 12x12 LED matrix by CA1~CA9 and CB1~CB4.
  Maximum to 144 LEDs are supported.
  Maximum to 40 anode RGB LEDs are supported.
  Maximum to 41 cathode RGB LEDs are supported.
- **LED Matrix Type-3**
  Achieve 16x16 LED matrix by CA1~CA9 and CB1~CB8
  Maximum to 256 LEDs are supported.
  Maximum to 75 anode RGB LEDs are supported.
  Maximum to 75 cathode RGB LEDs are supported.
- **LED Matrix Type-4**
  Achieve conventional COM x SEG (12x12) LED matrix by CA1~CA9, CB1~CB9, and CC1~CC6.
  Maximum to 144 LEDs are supported.
  Maximum to 48 anode RGB LEDs are supported.
  Maximum to 48 cathode RGB LEDs are supported.

- **LED Controls**
  Each LED has the on/off control.
  Each LED has the blink enable/disable control.
  Each LED has the 8-bit programmable PWM duty.
  Each LED has the open/short detection status.
  Each LED has the anti-forward control (Vaf) to prevent the ghost LED effects.
  Each LED has the +/-6% current fine tune control.
  Support global 8mA~40mA constant current source control.

- **MPWM IO (CA1~CA9, CB1~CB9, and CC1~CC6)**
  Each MPWM IO has sink current of 320mA.
  Each MPWM IO supports staggered delay.
  Each MPWM IO supports slew rate control.
  Each MPWM IO except CC1~CC6 has the precise current skew under +/-2%.
  Current skew between chips is under +/-2%.

- **System Clock Synchronization for cascaded LED drivers**
  Support SYNC output in master mode.
  Support SYNC input in slave mode.

- **I2C Slave**
  Maximum to 400KHz
  Support four auto-selective slave addresses by which AD pin is connected to. (VDD/VSS/SCL/SDA)

- **SPI Slave**
  Maximum to 2.4MHz

- **Matrix Control Engine**
  Support Type 1~4 matrixes by register setting.
  The frame time depending on Matrix Type has different phase number.
  Type-1 has the frame time 1098us including 9 phases.
  Type-2 and Type-4 have the frame time 1464us including 12 phases.
  Type-3 has the frame time 1952us including 16 phases.
  Each phase includes the PWM duty time 107us and the blanking time 15us.
  Support auto-breath control.
  Support auto-blink control.
  Support Audio-IN synchronous to auto-brightness control.

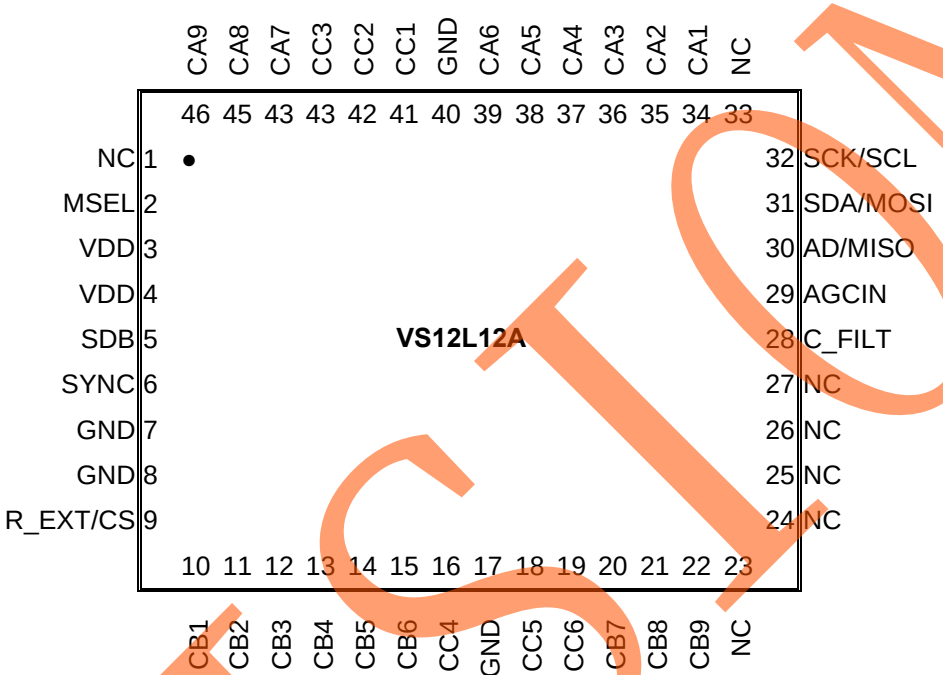
- **Audio In Gain Control**
  Support register configurable gain for Audio-IN: 0dB, 3dB, 6dB, 9dB, 12dB, 15dB, 18dB, and 21dB.
  Support auto-gain control.

- **Thermal Detection**
  Support thermal shutdown at 150℃
  Support thermal flag at 70℃

- **Power Modes**
  Normal Mode
  Software power down mode
  Hardware power down mode.

- **Package**
  QFN46.

VS12L12A (QFN 46pins): I2C & SPI Interface

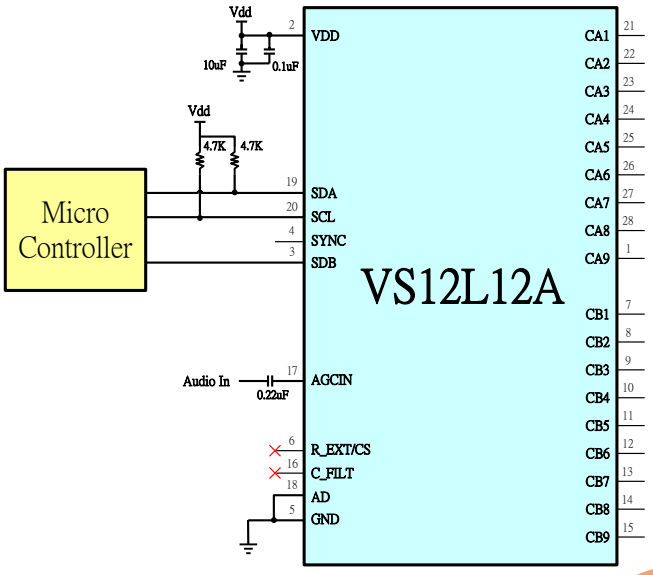


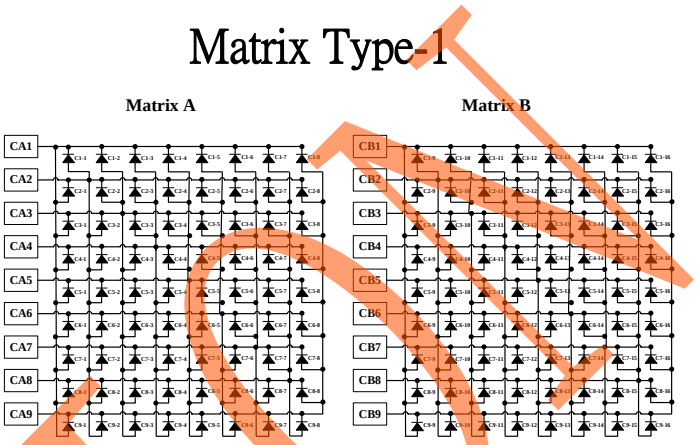
1.2 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pin for digital and analog circuit.
		Power supply input pin for digital and analog circuit.
		Power supply input pins for digital and analog circuit.
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. MSEL = 0 : I2C, pMSEL = 1 : SPI.
SDB	I	Schmitt trigger structure as input mode with internal pull-down resistor. Shutdown the chip when pull to low.
SYNC	I/O	Clock synchronous input or output pin. Schmitt trigger structure as input mode.
R_EXT/CS	I	R_EXT: Input only with internal pull down resistor in I2C mode. No external pull-down resistor is required.
		CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.
C_FILT	O	Used for filter audio-in noise.
AGCIN	I	Audio-IN Input.
AD/MISO	I/O	AD: I2C slave address selection pin. Schmitt trigger structure as input mode.
		MISO: SPI Master-Input-Slave-Output pin.
SDA/MOSI	I/O	SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode.
		MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.
SCL/SCK	I/O	SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode.
		SCK: SPI Clock input pin. Schmitt trigger structure as input mode.
CA1~CA9	O	PWM IO with sink 320mA and constant current source.
CB1~CB9	O	PWM IO with sink 320mA and constant current source.
CC1~CC6	O	PWM IO with sink 320mA.

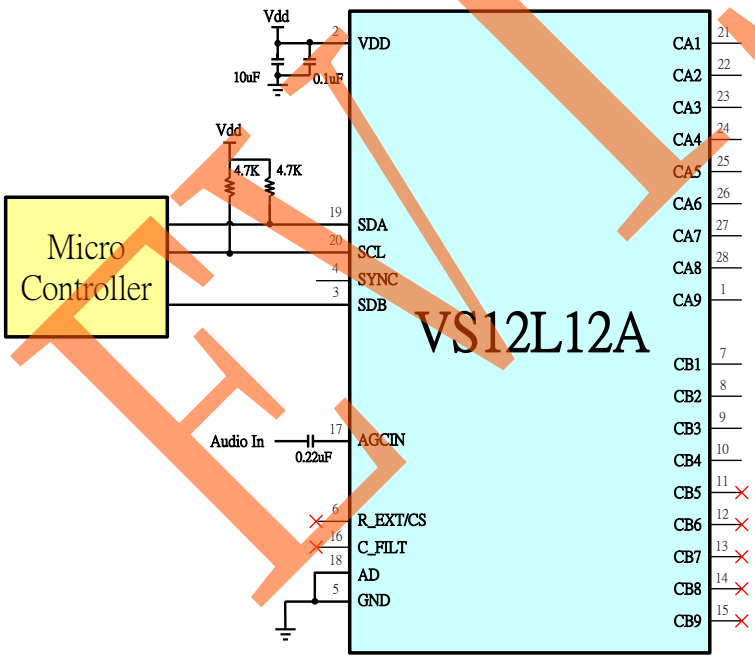
2.APPLICATION CIRCUIT

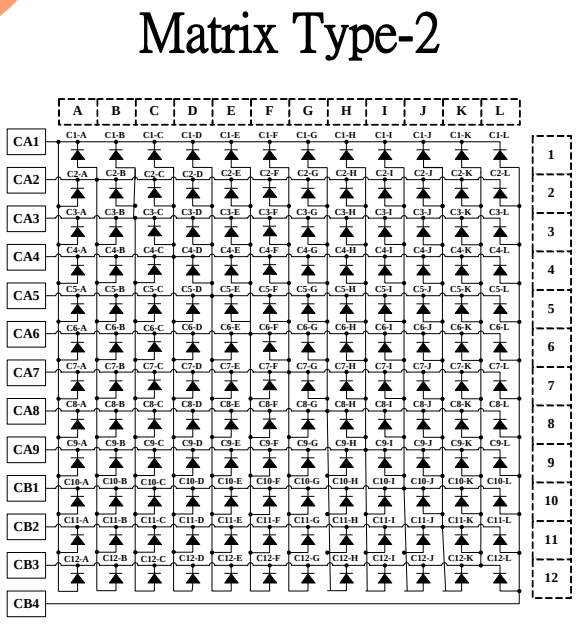
2.1 I2C INTERFACE WITH LED MATRIX TYPE-1



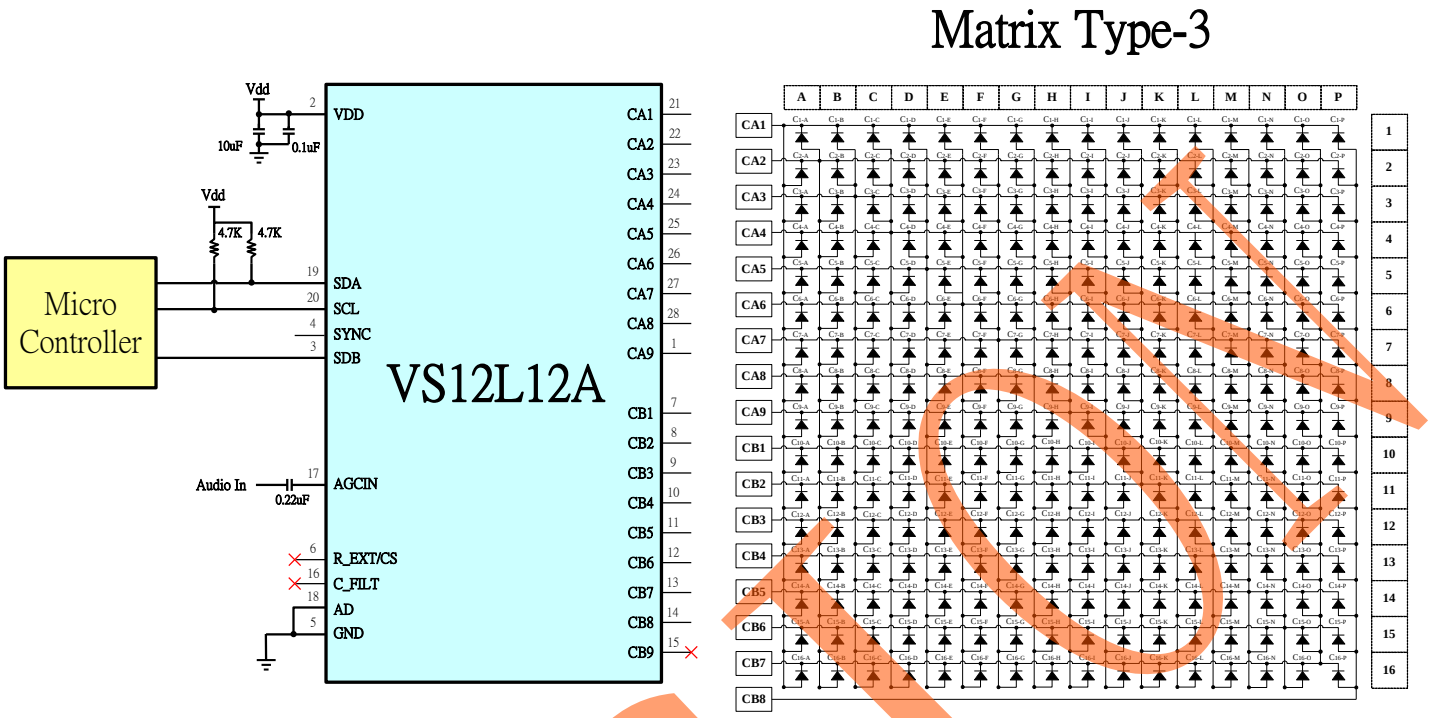


2.2 I2C INTERFACE WITH LED MATRIX TYPE-2

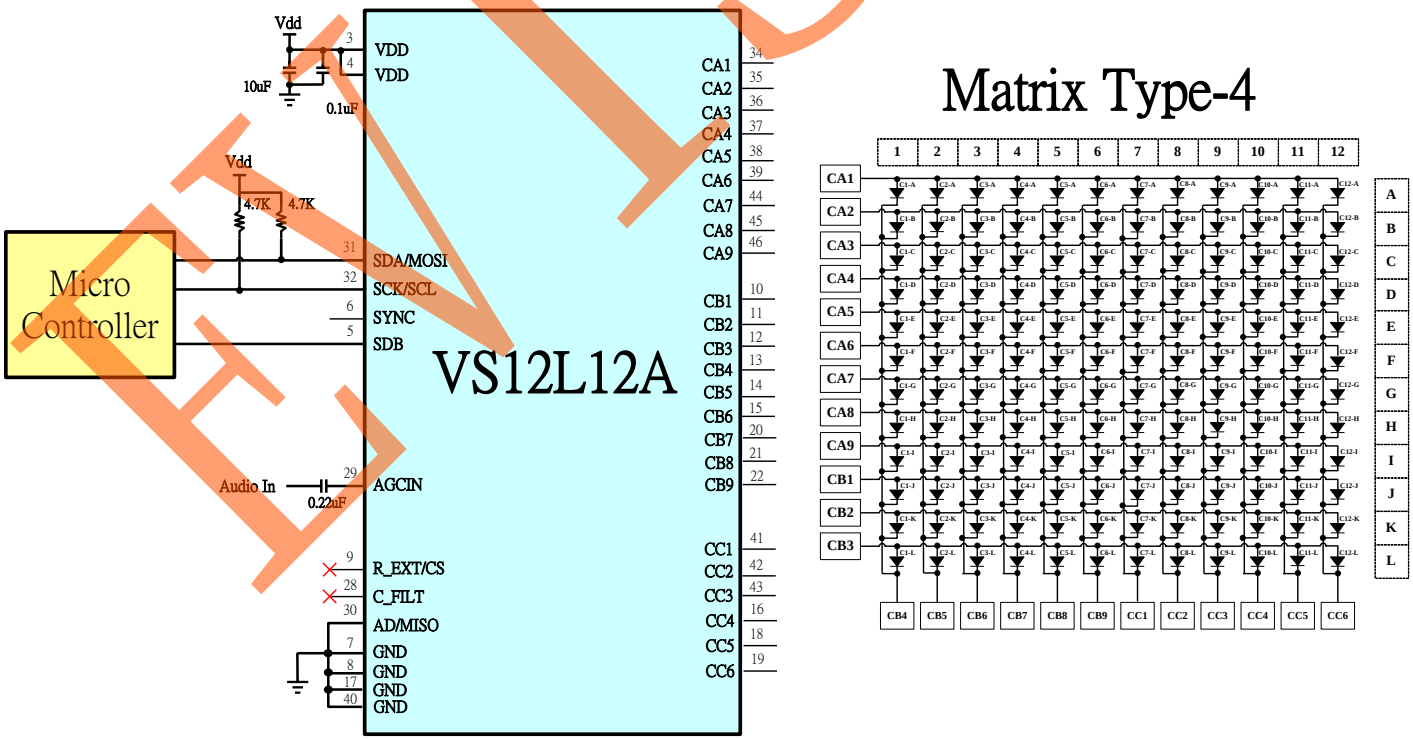




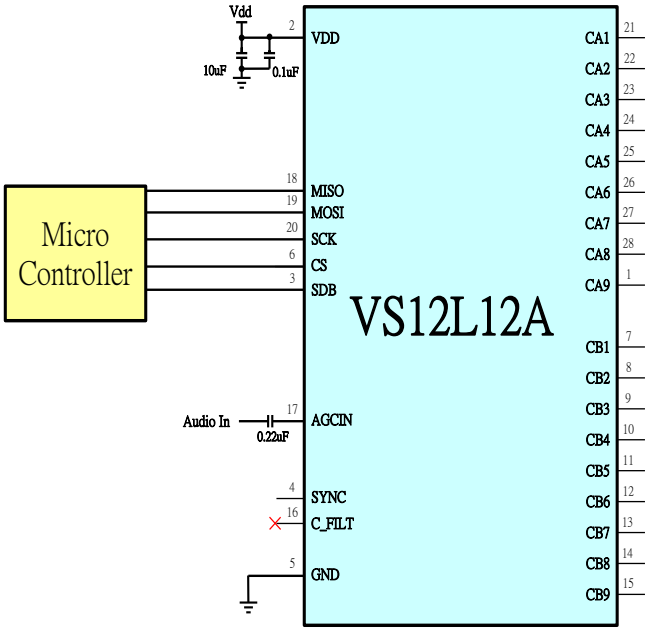
2.3 I2C INTERFACE WITH LED MATRIX TYPE-3

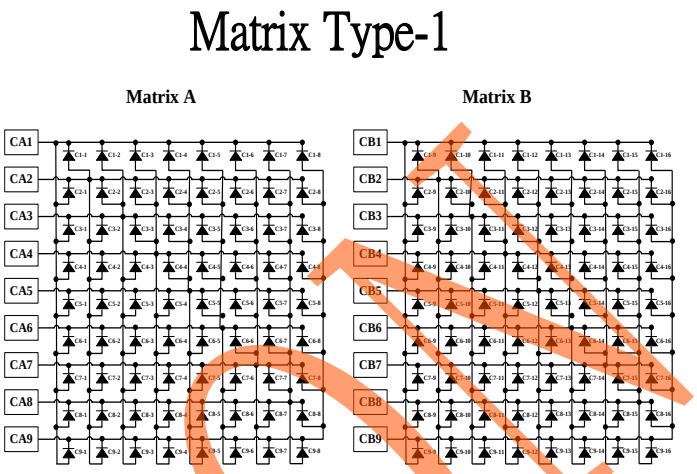


2.4 I2C INTERFACE WITH LED MATRIX TYPE-4

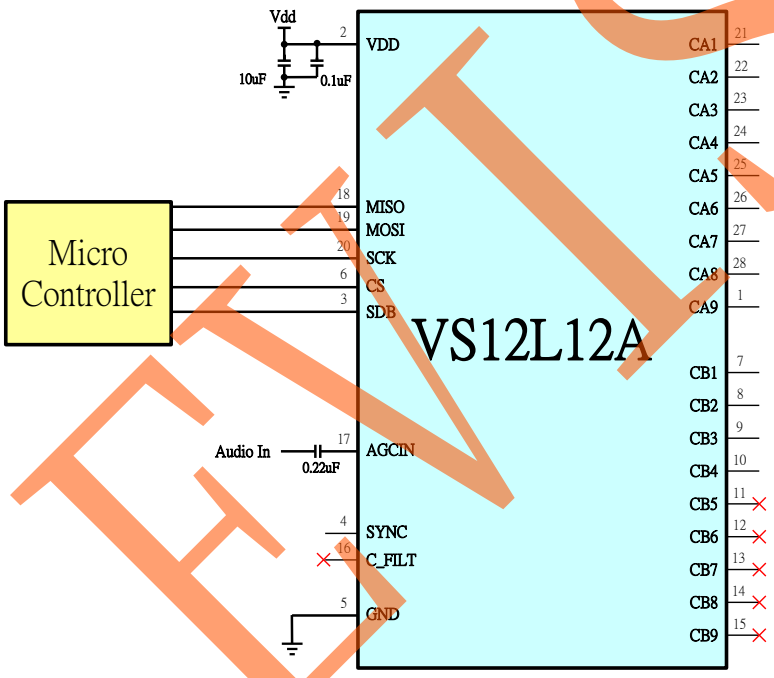


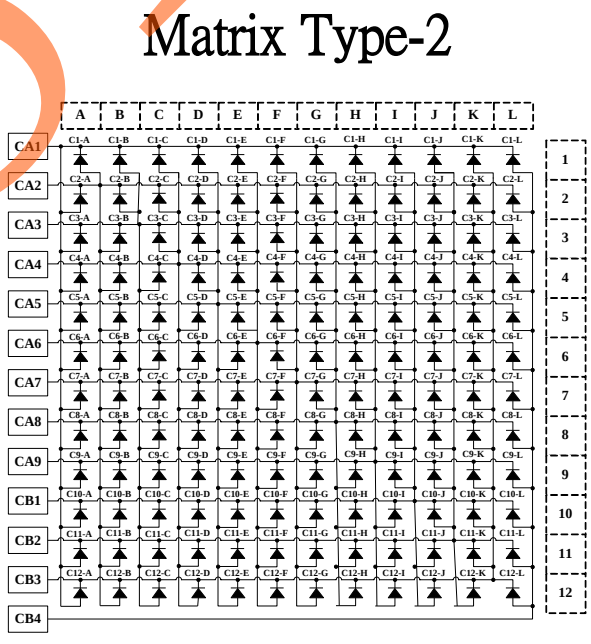
2.5 SPI INTERFACE WITH LED MATRIX TYPE-1



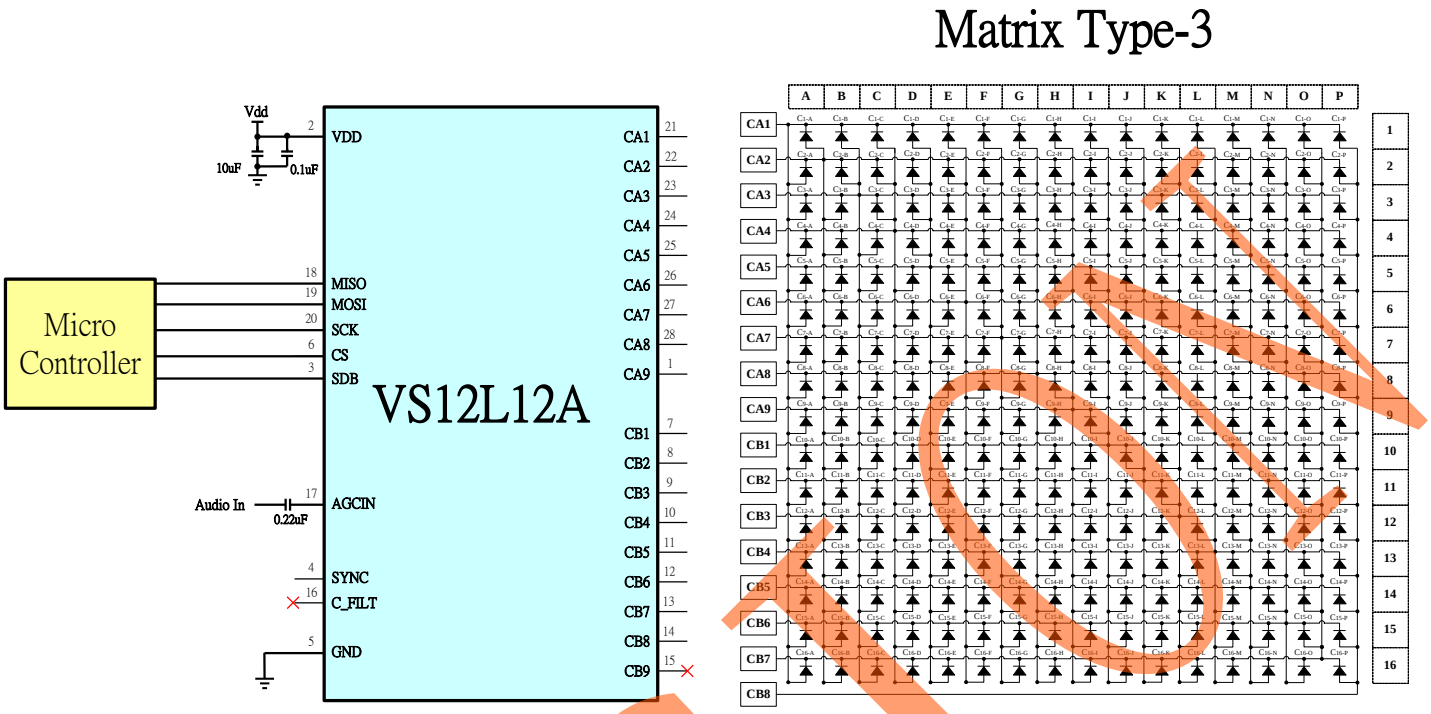


2.6 SPI INTERFACE WITH LED MATRIX TYPE-2

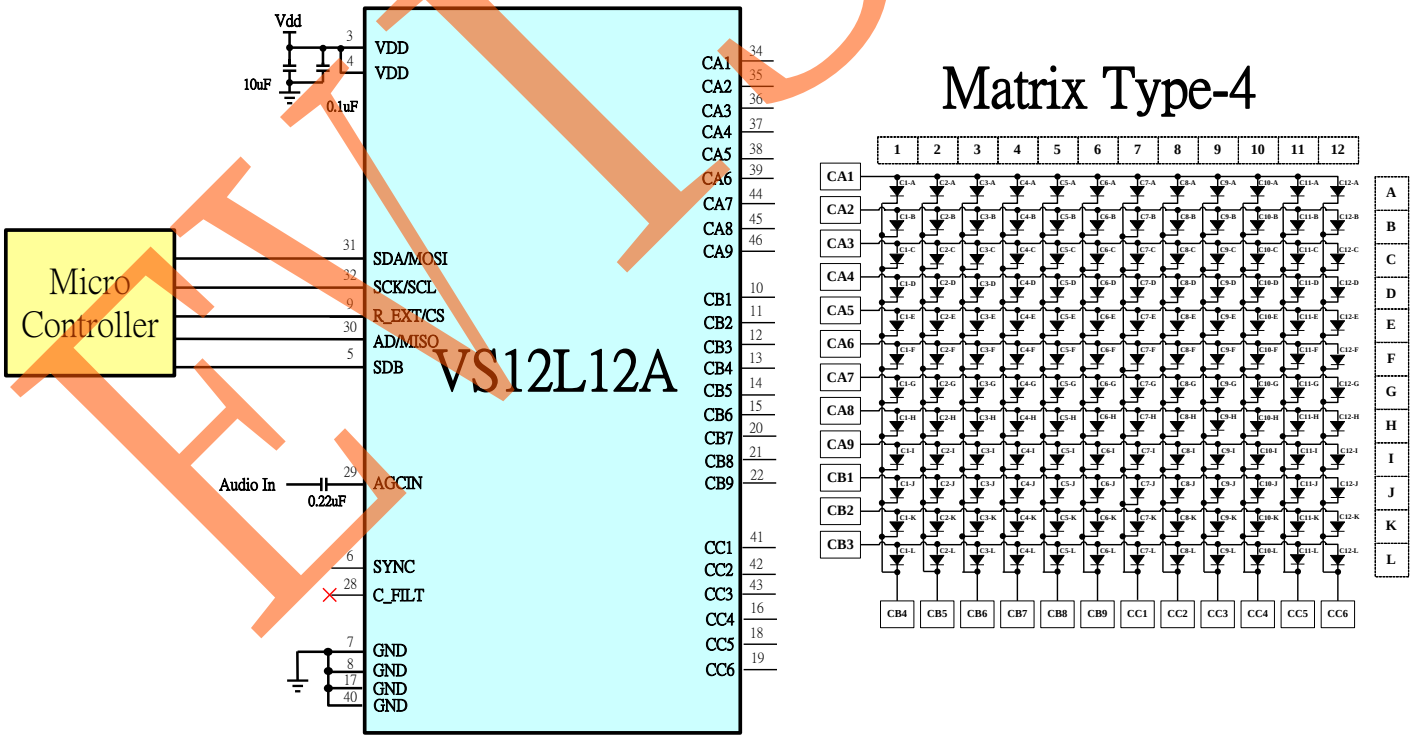




2.7 SPI INTERFACE WITH LED MATRIX TYPE-3



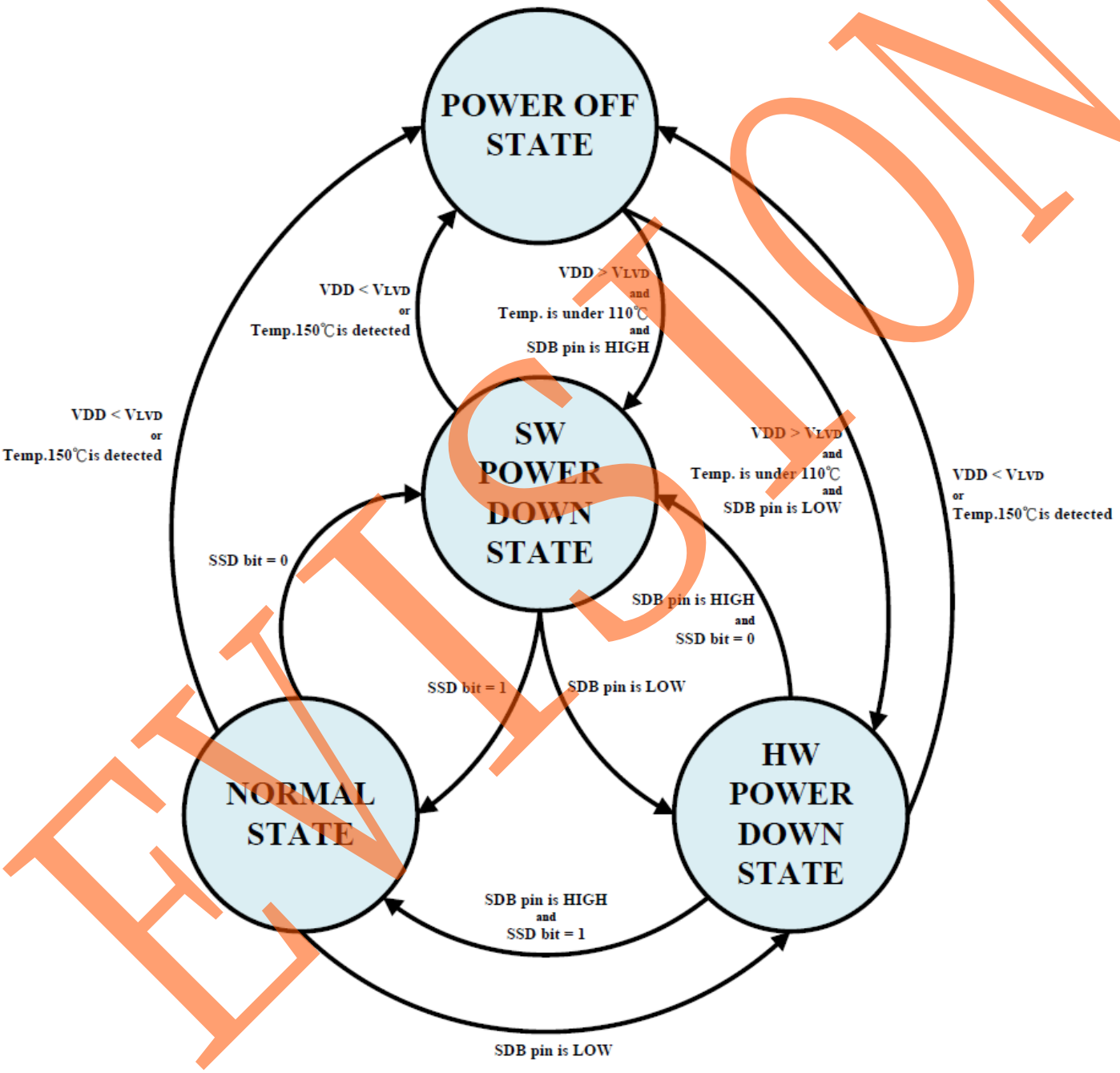
2.8 SPI INTERFACE WITH LED MATRIX TYPE-4



3.SYSTEM OPERATION MODE

3.1 POWER STATE MACHINE FLOW CHART

Power states are determined by the VLVD threshold, the thermal detector 150℃ threshold, the SDB pin state, and the software shutdown register (SSD bit) status.



3.1.1 POWER OFF STATE

When the VDD power is under VLVD threshold or the temperature is above 150℃, the system enters the POWER OFF state. In this state, the whole chip function is off. When the VDD power is above VLVD threshold or the temperature is under 110℃, a power on initial sequence is executed. During the sequence, all registers are initialized to the default

value.
After the sequence, the system will enter the SW POWER DOWN state if SDB pin is HIGH or will enter the HW POWER DOWN state if the SDB pin is LOW.

3.1.2 SW POWER DOWN STATE

In this state, all current sources and digital drivers are switched off, so that the matrix is blanked. All registers and the SRAM data can be written or read.

3.1.3 HW POWER DOWN STATE

In this state, besides all current sources and digital drivers are switched off, all registers are forbidden writing and reading.

3.1.4 NORMAL STATE

In this state, all current sources and digital drivers are operating depending on the register settings.

4.ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... 0°C ~ + 70°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

4.2 ELECTRICAL CHARACTERISTIC

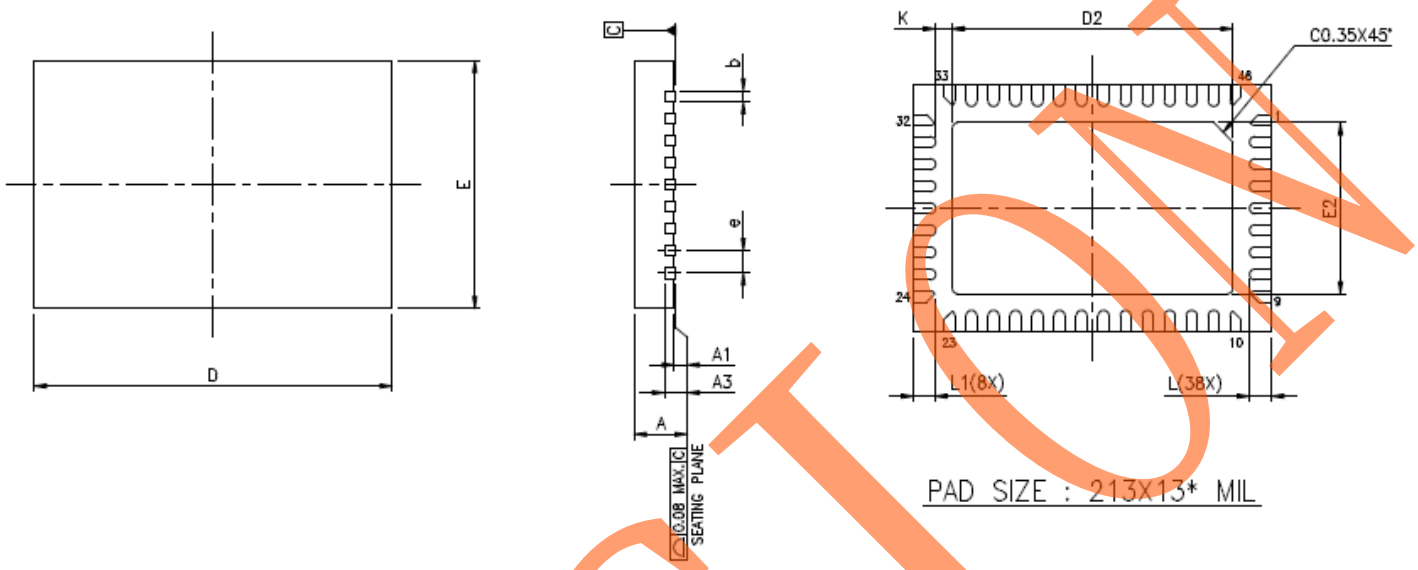
- **VS12L12A DC CHARACTERISTIC**

(All of voltages refer to Vss, Vdd = 5.0V,,ambient temperature is 25℃ unless otherwise

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd			2.7	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset		0.05	-	-	V/ms
Input Low Voltage	ViL	MSEL, SDB, SYNC, R_EXT/CS, SCK/SCL, SDA/MOSI, AD/MISO pins		Vss	-	0.3*Vdd	V
Input High Voltage	ViH			0.7*Vdd	-	Vdd	V
I/O port input leakage current	Ilekg	Vin = Vdd		-	-	2	uA
Default output current	Iout	Output current of CA1~CA9, CB1~CB9 The Constant Current Step setting is 11 0001b		-	32	-	mA
Current sink headroom voltage	V_{HR1}	Isink = 270mA		-	-	400	mV
Current source headroom voltage	V_{HR1}	Isource = 32mA		-	-	400	mV
I/O output source current sink current	IoH	Vop = Vdd – 0.5V				-	mA
	IoL	Vop = Vss + 0.5V				-	
Supply Current (Disable ADC)	Idd1	Normal Mode	Vdd= 5V	-	TBD	-	mA
	Idd2	Soft Shutdown Mode	Vdd= 5V	-	TBD	-	uA
	Idd3	Hardware Shutdown Mode	Vdd= 5V	-	TBD	-	uA
LVD Voltage	V_{LVD}	Low voltage reset/indicator level		2.4	2.55	2.7	V

5.PACKAGE INFORMATION

QFN 46 PIN



PAD SIZE : 213X13* MIL

	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.50 BSC		
E	4.50 BSC		
e	0.40 BSC		
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L			L1			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠ 212X13* MIL	5.05	5.10	5.15	3.05	3.10	3.15	0.35	0.40	0.45	0.33	0.38	0.43	V	X	N/A

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.