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A Hybrid Topology for Frequency Divider using PLL Application

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Abstract

In this paper, we present a new type of odd integer divider topology which consume low power and it uses Mod-N counter, DFF and OR gate. In existing methodology divide by 2 topologies involves only D Flip-Flops (DFF), which realized mostly Common Mode Logic DFF (CML) or True Single Phase Clock (TSPC) based DFF. These were high-speed dividers but no flexibility in this topology i.e. it divides the only power of N. So the proposed divider gives more flexibility to the topology like divided by any real odd integer. While designing a new topology the limitations are operating frequency range, a number of transistor and power consumption. Based on this consideration the 3T NAND and TSPC based Flip-Flop are investigated. The maximum operating frequency of the TSPC divide by 2 is reaches at 2.4 GHz with 1.1931 mw power consumption and is 50% low power consumption compared to the NAND_DFF based frequency divider. Similarly, divide by 3, divide by 5 and divide by 7 also consume low power with less number of transistor compare to the NAND_DFF based frequency divider. So the results show the TSPC is DFF's more preferable for PLL application and RFIC. The TSPC_DFF based frequency divider designed using 0.18 um CMOS process technology.

Keywords: Frequency Divider, Low Power, Mod-N Counter, PLL, TSCP DFF, 3T NAND Gate

1. Introduction

Frequency dividers are mandatory in many communication applications such as synthesizers, data recovery circuits, clock generations and PLL. The design of frequency divider is an important factor in the performance of PLL in the feedback path so locking gets difficult. Basic gates and Flip-Flops can be used to design digital frequency dividers.

A pulse swallow topology[1] or modular frequency topology[2] gives integer value division but it requires more hardware to reduce this complexity proper Prescaler unit is a need[3]. The Prescaler unit has some own limitation to alleviates, we proposed Hybrid topology. This proposed structure provides some flexibility to the circuit and requires less amount of hardware. New topology needs efficient components like Flip-Flops and basic gates. The requirement of efficient building block is solved by the use of 3T NAND[4] gate and TPSC DFF. In order to use the efficient component helps to achieve low power and reduce the number of transistors.

The organisation of this paper is as follows: This paper starts with Section 2 that includes a detailed explanation of basic building blocks and implemented schematic were shown, which we were used i.e. 3T NAND gate, NANDDFF, TSPC DFF and Asynchronous Mod-Ncounter. Section 3 deals with existing method i.e. frequency by 2 topologies[5]. Section 4 describes working and modification of proposed topology. Section 5 contains simulation outputs and measurements that are pictorially represented. Finally, Section 6 concludes the paper.

2. Basic Building Block

In VLSI technology, we follow either top down or bottom up approach. Both ways need building blocks here top module is frequency divider and building blocks are NAND, D Flip- Flop and Counter. In this paper,

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we employed two different DFF both have their own advantage and disadvantages. Based on this DFF, we construct Mod-N counter and divider so the impact of DFF performance will be reflecting the overall architecture.

All fundamental blocks are implemented using cadence virtuoso EDA tool with 180 nm process technology.

2.1 3T NAND

Figure 1 shows new low power NAND gate. In this design, three transistors only (2 PMOS and 1 NMOS) involve a combination of pass transistor with inverter logic. The functionality can be explained as follow, the PMOS M0 and NMOS M0 modified CMOS inverter i.e. if input 'A' value is high mean it works as an ordinary inverter. Therefore, the output was the complement of 'B'. Remaining input values output leads to undefined state due to the status (on or off) of the transistor so maintain the proper (W/L) ratio of all three transistors. (i.e. PM1 = 6 x PM0 = 3 x N0). It helps the circuit to achieve maximum exact output voltage levels.

2.2 D Flip-Flop

2.2.1 NAND based

Figure 2 shows a widely used classical positive edge trigger DFF. This circuit consists of three SR NAND Latches. The whole circuit divided into two parts - one is input side which deals with clock, data and reset with the help of two SR NAND latches. Another one is output side SR NAND latches which involve output change with respect to clock and reset. If a reset is low and the clock is trigger high to low means output is maintain the previous value, when clock signal goes low to high only Q is either set or reset then next clock cycle also it happened till the reset is applied if reset is high means Q is reset regardless of input data D.

In Figure 2 circuit, the main modification was instead of using normal 4T NAND gate replace with the 3T NAND gate. Generally, classical method requires 26 transistors (without reset) if reset embed mean it require 32 transistors. When we use 3T NAND means it gives less area (21, 30 transistors respectively) as well as low power consumption. The difficulty of this circuit is to maintain the output voltage level. This modified DFF is the basic building block of Asynchronous Mod-N counter and odd integer divider circuit.

2.2.2 TPSC DFF

A conventional CMOS DFF requires clock signals andits complementary clock signal. In nowadays result of some research avoids the complementary signal. So TSPC FF[6] replaces the inverter for produce complementary clock. Figure 3 shows TSPC DFF these are often used in

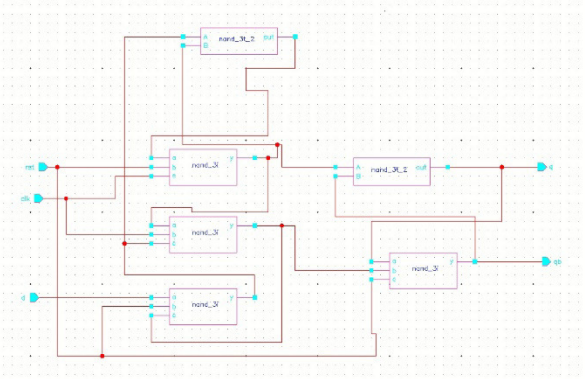

Figure 2. Schematic and implemented diagram NAND DFF.

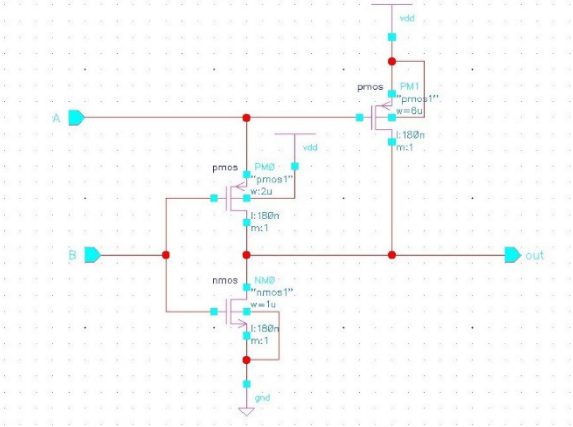

Figure 1. Schematic and implemented 3T NAND gate.

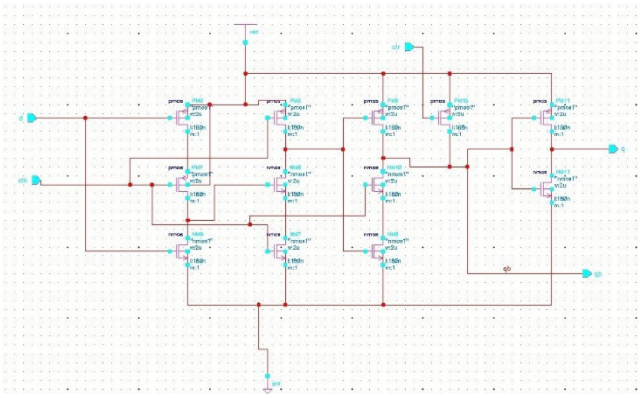

Figure 3. Schematic and implemented TSPC DFF.

high-speed CMOS circuits. A dynamic logic the parasitic capacitance enough to cause the Flip-Flop to enter invalid states. In this TPSC DFF has 11 transistors only and consume low power compare to other logic, one transistor needs to use clear the output. However, TPSC DFF will typically not perform well at the low clock rate.

A dynamic logic famiy have two phases, the first phase is precharge in this period PMOS is on and the second phase is evaluation phase decides the output either high or low depend on the input value.

2.3 Asynchronous Mod counter

2.3.1 mod-3

The asynchronous counter is one which each DFF is clocked output of the previous DFF. Compared to other design, Asynchronous counter are easy to design and require minimum hardware. Figure 4 shows MOD 3 counter. This counter was two bit counter so it requires two TFF which made up of DFF i.e. is feedback to D. The clock is fed into first DFF and output of the first DFF is into the clock input of next DFF. The first stage DFF is toggled every clock cycle and second stage DFF is toggled every two clock cycle. All the reset pin is connected together after counting 3 reset pulse clear the Flip-Flop again it starts with the initial stage before start counting also reset apply. The reset logic role is very significant here because based on this only Mod-N (mod-3 (11), mod-5(101), mod-7(111)) counter are designed and frequency divider also designed so reset logic have the vital role here.

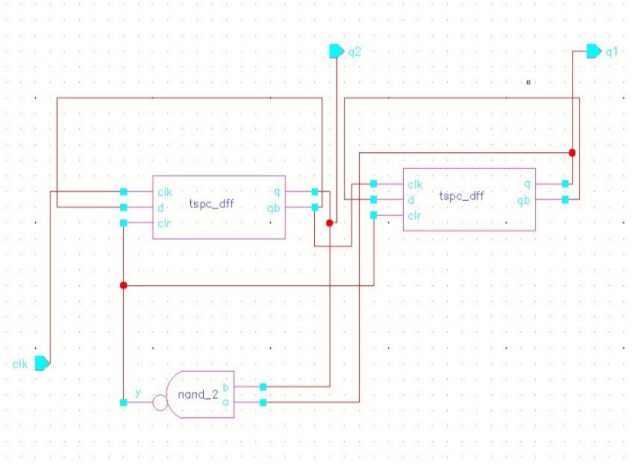

Figure 4. Schematic and implemented MOD-3 counter.

3. Existing Frequency Divider Architecture

The existing and most familiar divided-by-2 shows Figure 5. This was a straightforward[5–8] ways to implement a divide-by-2 digital frequency divider. In this method DFF was used as frequency divider, negative output (QB) was feedback to input DFF (D) remaining things as it is, output is taken from Q. Here the Q value equals to clk/2 so we extended this logic like to pad another DFF tab in cascade manner mean we got clk/4 it directly shows it produce 2 power of n values. Therefore, the freedom of this method is that the division ratio will be constrained to be a power of 2. So to overcome this limitation we proposed a hybrid approach, generally pulse shallow counter based divider uses as integer divider to produce division ratio to any integer value but it required more complex circuit and hardware. VCO output frequency first scales down largely means it needs simple and less hardware module then followed by pulse shallow counter architecture mean its consumption less power. Per-scaling value to any integer mean to achieve more accurate and resolution with low power[9,10] instead of using traditional f to use proposed hybrid odd integer divider preferable.

4. Hybrid Topology

Generally, digital frequency divider employs primary gates, counter and latches so basic building blocks are D Flip-Flop, instead of using traditional D Flip-Flop use low power TSPC DFF (with reset logic). Somodified D Flip-Flop which consumption low power and high speed. In this architecture use both synchronous and asynchronous logic.

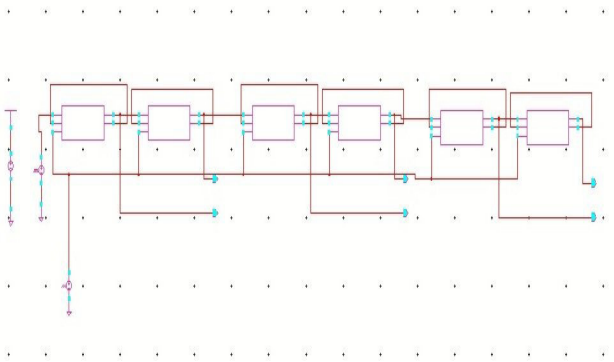

Figure 5. Schematic diagram power 2 ^ N topology.

A Figure 6 shows the proposed approach to dividing the frequency of a clock by a non-power by 2 division ratio is to implement a counter with an appropriate reset logic. That part is called asynchronous part, then followed by synchronous part. In this synchronous part consist of D Flip-Flop (modified) and primary OR gate. One important note was DFF either use a positive edge trigger or negative edge trigger. i.e. Positive edge trigger DFF produce one cycle delay and negative edge trigger DFF produces half cycle delay to the architecture.

4.1 Mod-3 based F÷3 Design

Figure 7 has Mod-3 counter and OR gate and D Flip-Flop. The Mod-N counter is reset for every four state so MSB bit which holds the half of change value and same change value is delayed by half unit using D Flip-Flop further MSB (Q1) and delayed MSB value was OR mean its gives the output which frequency was divided by 3 value that is every three clock cycle one cycle. The main advantage of above model circuits is low power model because the mod-N counter design was asynchronous so it not requires full clocking toggle rate so which consumption low power and D Flip-Flop also modified so total model circuit consumption low power compare to other architecture.

The drawback of above models circuit is 50% duty cycle and glitch accumulation.

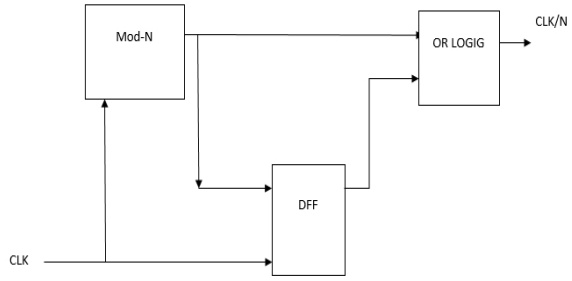

Figure 6. Proposed hybrid topology.

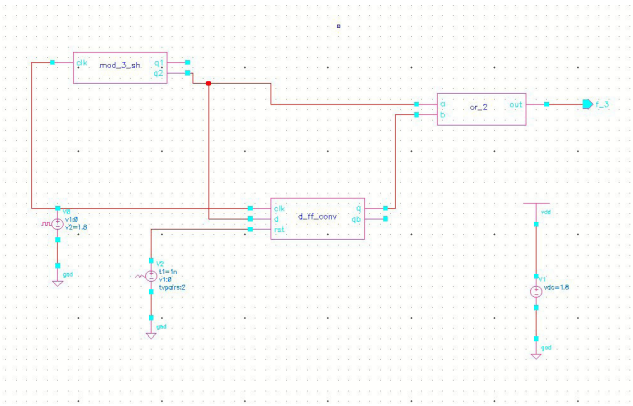

Figure 7. Block diagram frequency by 3.

4.2 Mod-5 based F÷5 Design

The Figure 9 has similar to f÷3 the main difference was a Mod-5 counter. The counter is reset for every six cycle so q1 (middle) bit which hold the half of change value and same change value is delayed by half unit using TSPC DFF further (Q1) and delayed (Q1 value) was added mean its gives the output which frequency was divided by 5 value. F_5 has running synchronous but the main counter design was asynchronous so which consumption low power and D Flip-Flop also modified (TPSC DFF) so total circuit consumption low power compares to traditional architecture.

The drawback of above architecture produces only 33.3% duty cycle and glitch accumulation.

4.3 Mod-7 based F÷7 Design

This was one more example, Figure 11 has a Mod-7 counter, OR gate and D Flip-Flop. The counter is reset for

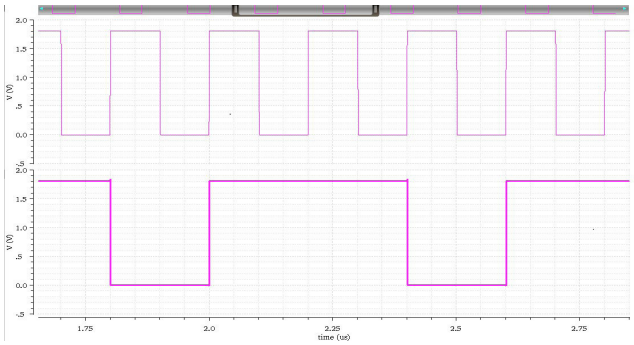

Figure 8. Output waveform for f÷3.

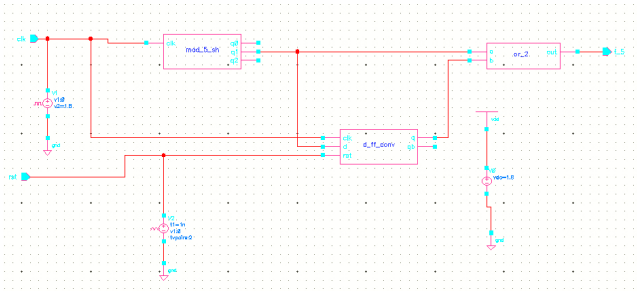

Figure 9. Block diagram frequency by 5.

every seven cycles so MSB bit which holds four off and three on value so using Q2 produce f_7. If Q1 was used mean need extra hardware.

The drawback of above architecture produces only 28.5% duty cycle and glitch accumulation.

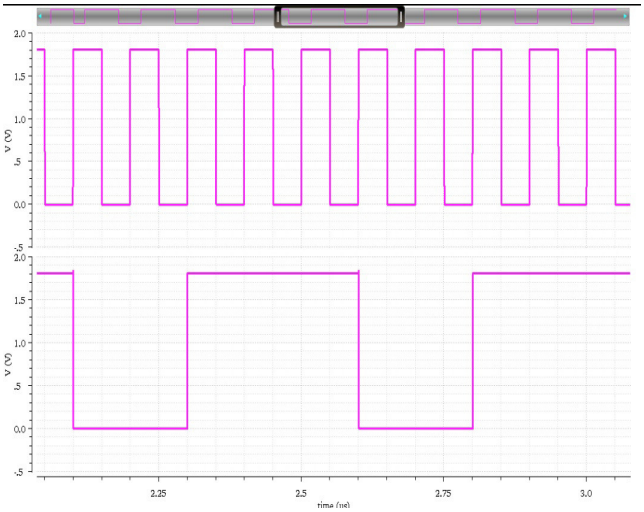

Figure 10. Output waveform for f÷5.

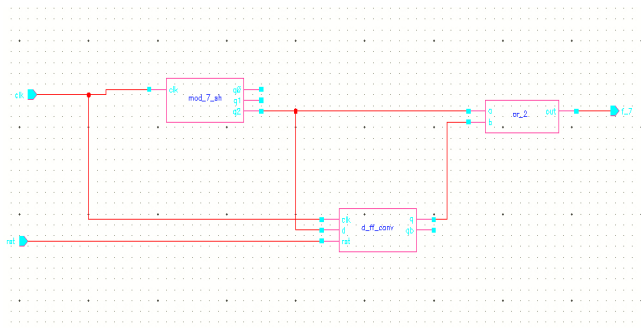

Figure 11. Block diagram frequency by 7.

5. Measurement and Analysis

Here we have implemented same hybrid approach but using two different types of DFF based, such as NAND based and TPSC based.

Implementation part start with the design of asynchronous counters (mod-3, 5, 7). These counters were made by either NAND based DFF or TSPC based DFF.

After implementation to verify functionality for both versions and Table 1 shows pros and cons for each version. Respected simulation output was shown in Figures 8, 10 and 12. All simulation was performed the same configuration i.e. supply voltage is 1.8 v, operating frequency is 2 Ghz, using 180 nm technology and simulation run time is 5 us.

A Figure 13 shows power consumption between NAND_DFF and TSPC_DFF for different modes of frequency divide. A Figure 14 shows the transistor count comparison between NAND_DFF and TSPC_DFF.

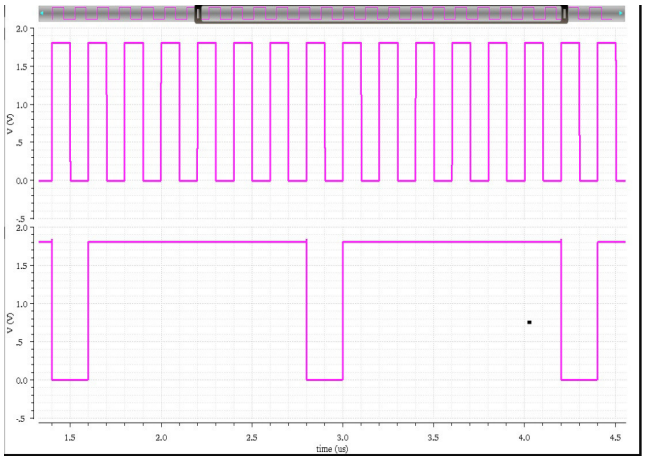

Figure 12. Output waveform for f÷7.

Table 1. Performance analysis

Design Types	NAND Based DFF-Frequency divider				TSPC Based DFF-Frequency divider			
Parameter	F/2	F/3	F/5	F/7	F/2	F/3	F/5	F/7
Power (mW)	2.4	4.42	6.9	5.03	1.19	3.82	5.35	3.392
No. of Transistor	32	103	134	134	12	42	54	54

Figure 13. Power comparison chart.

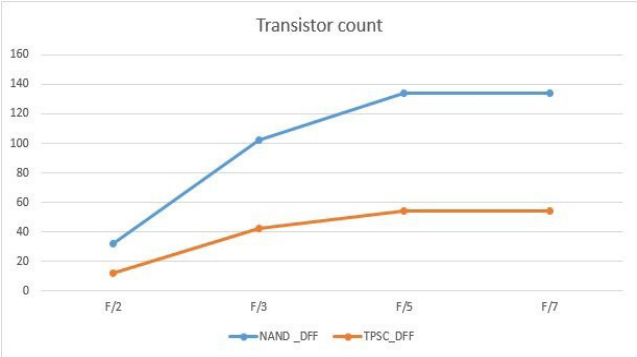

Figure 14. No. of transistor comparison chart.

6. Conclusion and Future Work

This paper mainly focuses on divider topology and suitable hardware needed. We have designed and implemented F/3, F/5 and F/7 with NAND and TDPC. Based on the performance of TSPC DFF based hybrid odd integer are more suitable which occupy less area and consume low power. Further enhancement of this proposed architecture will be to overcome duty cycle problem and glitch accumulation.

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