Design and Implementation of Sequential Circuit Based On Low Power Using 45nm Technology

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Abstract:A low power voltage CMOS frequency divider using power gating technique, that's why it reduces the overall power consumption of circuit and increases the efficiency of circuit. .A memory element consumes 70 percent of total power in an integrated circuit. As flip-flops are the main area of memory elements used on any portable device, the major concern to reduce flip-flop energy consumption will help reduce power consumption in an I In we designed a flip-flop using CMOS logic; it consumes less energy than conventional gates designed. Transistors switching occurs when input and clock is applied. proposed clocked D flip-flop is used in frequency divider circuit .The frequency divider is design by use the technique of low power CMOS designs. Here number of transistor is reduced in proposed and demonstrate various parameters and shows reduced leakage power , Delay andnoise margin of the circuit to analyze its performance in 45nm technology with power gating and pass transistor technology. The simulation results were done with cadence tool virtuoso environment at room temperature 27ºC with various supply voltage ranges (0.7 to 1.2 V).

Keywords: Frequency divider, Set value, XOR gate, T flip fop,Leakage power, Area, Delay, 45nm technology, Cadence.

I.INTRODUCTION

Sequential circuits are logic circuit whose output in any occurrence of the time depends not only on current input but emits past. Sequential circuits are of two types: locked andunlocked. The simplest type of sequential circuit is a memory cell with two states. It can be 1 or 0. These two state circuits are called sequential flip-flop, as it moves from one state to another and then fall back.Flip-flops are used as memory elements which are the basic elements of an integrated circuit[1-4].Frequency dividers are useful circuit in many communication applications for example frequency synthesizers, Timing Recovery circuits and clock generations. It also works functional in many communication applications. The approaching of frequency divider CMOS technologies for high-speed applications has established in numbers of circuits.

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Low-voltage and power operation of CMOS dividers makes them attractive integration of communication system. Common prototype for dividers are static, Dynamic, injection locked and regenerative frequency divider. Injection-locked frequency divider employs an oscillator with center tape frequency is locked to harmonic incoming signal frequency. Dynamic and injection-locked dividers can achieve high frequencies and low power, they have a narrow frequency ranges. Static dividers with inductive peaking have also been shown to achieve higher frequencies, but they require large inductor area[5-10]. The ½ frequency dividers are form two D flipflop in configurations with negative feedback. The design of frequency divider that can be applied toward massively parallel I/Os, which imparts broad frequency ranges, area, and power, are key criteria. . Wireless communication industry currently experiencing tremendous growth in Wireless LAN application, multiple standards has widely adopted in short-range communication.In particular, high speed frequency dividers consumption of large amount of power in Phase locked loop (PLL) based devices, decreasing the number of stages by increasing the division order is efficient for the power reduction of the frequency divider.Out with new set value by using xor gate in circuit through which low power consumption is introduced into frequency divider circuit and technique synchronized with divider circuit, which enhance whole circuit performance in 45 nm technology. Out with power gating technique synchronies in circuit through which low power consumption and controlled leakage has been introduced into frequency divider circuit[11-13].

II.PROPOSED SYSTEM

Block digram

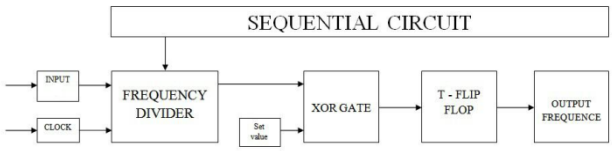

Fig 1:block diagram of Frequency divider circuit with set value sequential circuit

Frequency Divider

Cmos based divider topology is based upon the D type Flip-Flop. Require only one clock phase and having nine transistors, due to small number of transistor and small delay of D to 'out' the operational frequencies can chosen to high ranges.

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Tspc dividers presents a low power low voltage CMOS frequency divider using power gating technique, that's why it reduces the overall power consumption of circuit and increases the efficiency of circuit. This demonstrate various parameters and shows reduced leakage power (0.45×10^{-12}), Delay (6.26psec) and noise margin (11.53) of the circuit to analyze its performance in 45nm technology with power gating technology. The simulation results were done with cadence tool virtuoso environment at room temperature 27ºC with various supply voltage ranges (0.7V to 1.2V)

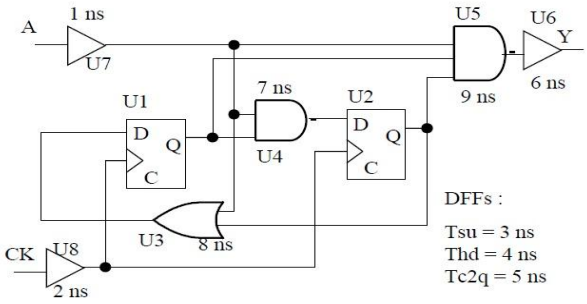

Fig 2: CIRCUIT DIAGRAM OF FREQUENCY DIVIDER

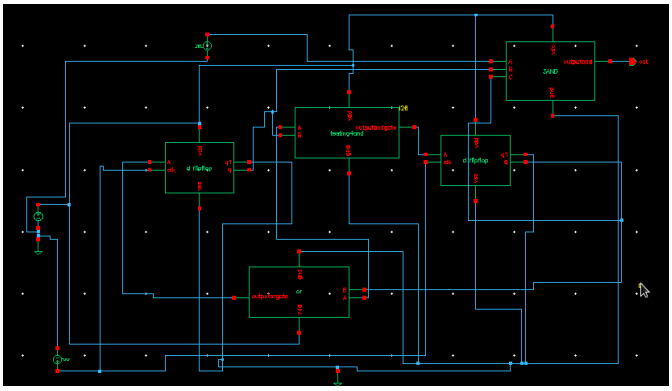

Fig 3: circuit of frequency divider using 45nm technology

cmos based divider are suitable structural design for divider as compared to static dividers when working over high frequency. Conversely tp requires input clock having nearly rail to rail voltage hang, this makes an order to achieve high frequency operations. Operation of Tp D-type Flip-flop is also follow and consists two working nodes evaluation mode,Hold mode. When clk is at high the D type Flip-flop works as evaluation mode if node a is at high the transistor mn1,mn2 are turned on. Node n0 will be pulled low and output 2 becomes high. If node n0 is low the transistor mn1 is turned off & node n1 which previously is pre-charged remains high. Thus the state of outB becomes low. Therefore node n0 transparent to node output out B becomes evaluation mode. When clk is at low D type Flip-flop work in hold mode namely precharged mode. Node n1 is pre-charged to high through, transistors mn2 & mn3 are off the value of outB is held. Fig explains the working of divide by two circuits which have clk input as output of previous stage and output being feedback to D as input. As the value of node 1 is inverted to value of input D when data is at node, it is transmitted to outB in evaluation mode. The data is at outB and becomes inverted to value of input D. when output node of outB is feedback to the node D outB will toggle to its own state after two clock of cycles.

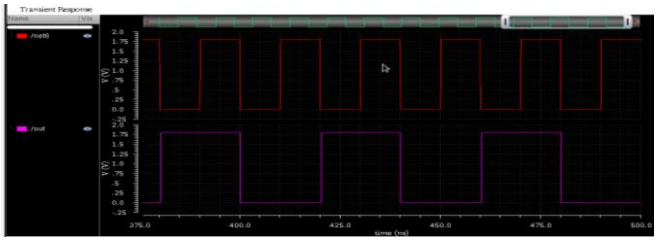

Fig 4: Graph representing transient response of FREQUENCY DIVIDER in 45nm TECHNOLOGY

Design of pass transistor OR gate

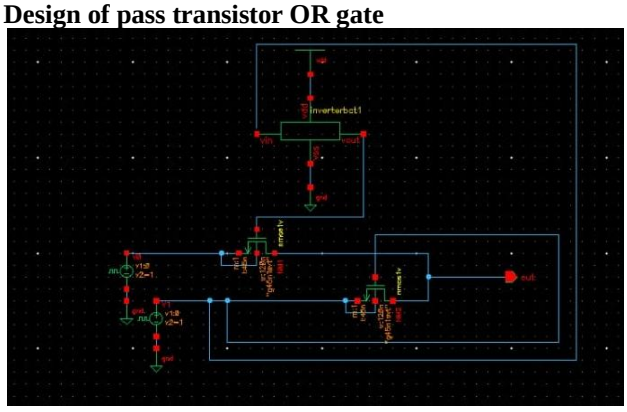

Fig 5: circuit diagram of pass transistorlogic of OR gate using 45nm technology

The sizes of the OR gate transistors are selected for proper values for 45 nm technology and theresults are simulated using Spectre. The schematics of the proposed pass transistor OR gate is as shown in Figure5. The schematic is made using Virtuoso Schematic Editor (VSE). The pass transistor OR gate consists of 1 PMOSs connected in series which are then in series with the one connected NMOSs. As illustrated in the figure 5 are given the same input signal A while PM_1 and NM_1 are given input B.

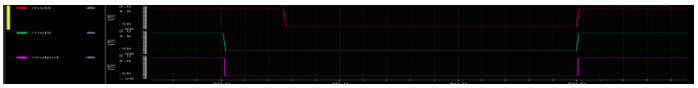

Fig6:Graph representing transient response of in XOR GATE 45nm TECHNOLOGY

The transient response showing the simulation results is shown in Figure 6. The waveforms are obtained for different two inputs combinations. When Vdd = 1.8V and inputs A=1, B=1 i.e. when both the inputs are HIGH PM_1 are OFF while NM_1 are ON thus connecting theoutput node directly to the ground and hence output waveform thus obtained is LOW. For any other combinations of inputs the output waveform is HIGH . As in case of OR gate, the cell is validated for DRC violations and is also verified for LVS using tools

Design of pass transistor AND gate

The sizes of the ANDgate transistors are selected for proper values for 45 nm technology and theresults are simulated using Spectre. The schematics of the proposed pass transistor AND gate is as shown in Figure7. The schematic is made using Virtuoso Schematic Editor (VSE). The pass transistor and gate consists of 1 PMOSs connected in series which are then in series with the one connected NMOSs. As illustrated in the figure7 are given the same input signal A while PM_1 and NM_1 are given input B.

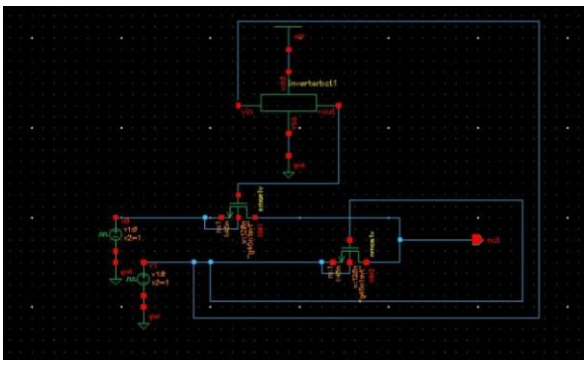

Fig 7: circuit diagram of pass transistor logic of AND gate using 45nm technology

The transient response showing the simulation results is shown in Figure 8. The waveforms are obtained for different two inputs combinations. When Vdd = 1.8V and inputs A=1, B=1 i.e. when both the inputs are HIGH PM_1 are OFF while NM_1 are ON thus connecting theoutput node directly to the ground and hence output waveform thus obtained is LOW. For any other combinations of inputs the output waveform is HIGH. As in case of AND gate, the cell is validated for DRC violations and is also verified for LVS using
Tools

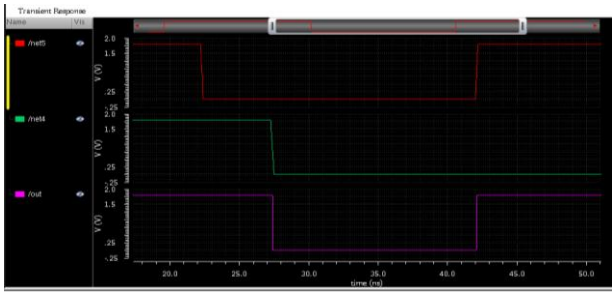

Fig 8: Graph representing transient response of in AND GATE 45nm TECHNOLOGY

D-Flip Flop

The D flip-flop is commonly used. This is also known as a "data" or "delay" flip-flop. W hen applied without a clock input on the D flip-flop or the falling edge of the clock signal, there will be no change in output. Keep the previous output value Q and inverts for Q'. If the clock signal is high (rising edge is more accurate) and D input is high, the output Q is high, the output Q' is low and where D input is low, the output Q will beremains

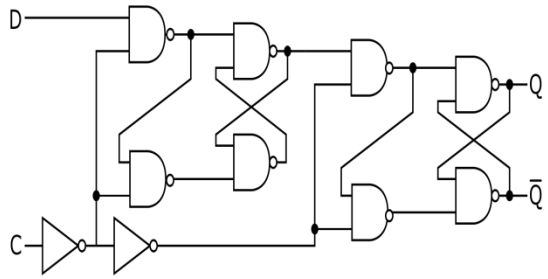

Fig 9.1 D-flipflopusinglogicalgates

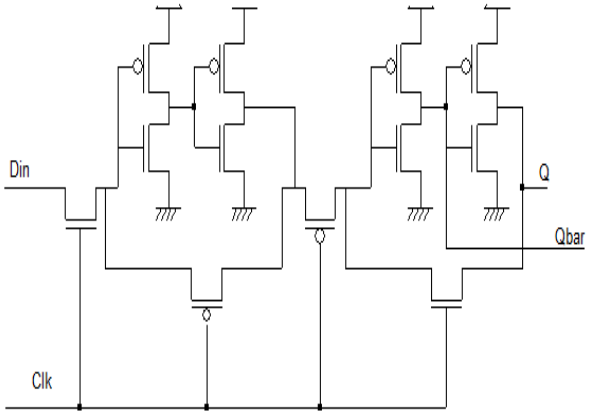

Fig 9.2D-flip flop using CMOS technology

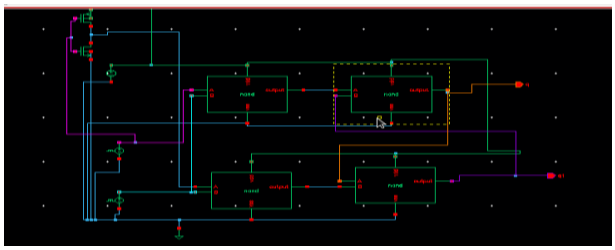

FIG 10:CIRCUIT DIAGRAM FOR D-FLIP FLOP USING 45nm TECHNOLOGY

Operation

If the clock is low, the signal to allow the master flip-flop is high. When the clock signal changes from low to high, master flip-flop data will store from input D. At the same time, the second flip-flop enable signal goes from low to high with clock signal due to double inversion. Data blocked flip-flop master during the rising edge was sent slave flip-flop.Fig 10.When the clock signal goes from high to low, exit master-slave flip-flop Flip failure as input and change their state. Master Memory Element supports the latest input values in the next rising edge.

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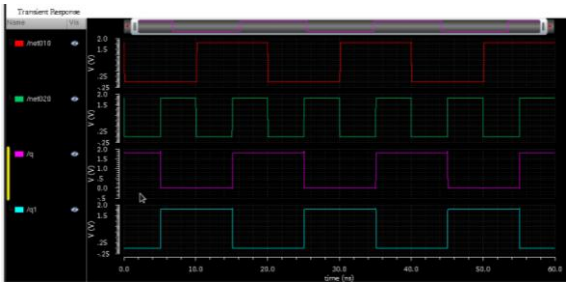


FIG 11: Graph representing transient response of D-flip flop in 45nm TECHNOLOGY

III. Design of pass transistor XOR gate

The sizes of the XOR gate transistors are selected for proper values for 45 nm technology XOR the results are simulated using Spectre. The schematics of the proposed and Gate is as shown in Figure12. The schematic is made using Virtuoso Schematic Editor (VSE). The pass transistor and gate consists of 2 PMOSs connected in series which are then in series with the one connected NMOSs. As illustrated in the figure12are given the same input signal A while PM_1 and NM_1 are given input B.

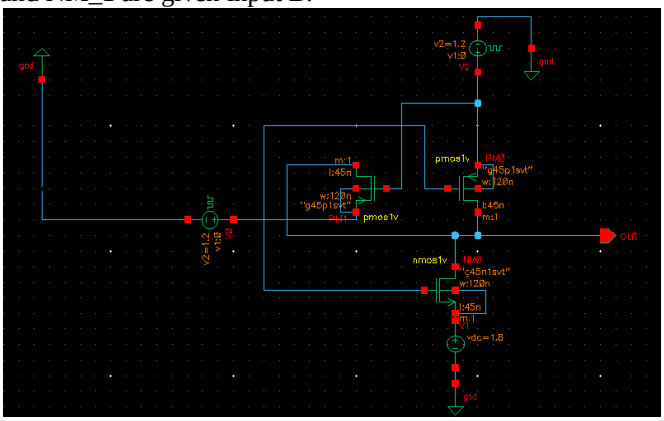


Fig 12: circuit diagram of pass transistor logic of XOR gate using 45nm technology

The transient response showing the simulation results is shown in Figure 13. The waveforms are obtained for different two inputs combinations. When Vdd = 1.8V and inputs A=1, B=1 i.e. when both the inputs are HIGH PM_1 are OFF while NM_1 are ON thus connecting theoutput node directly to the ground and hence output waveform thus obtained is LOW. For any other combinations of inputs the output waveform is HIGH . As in case of XOR gate, the cell is validated for DRC violations and is also verified for LVS using
Tools

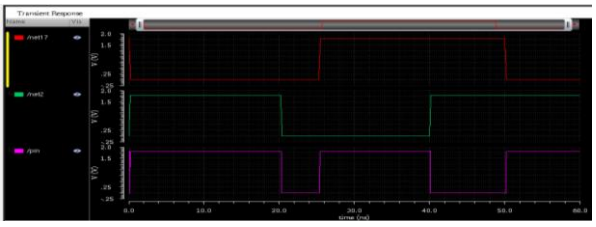


FIG 13:Graph representing transient response of in XOR GATE 45nm TECHNOLOGY

IV. Design of cmos logic T gate

Gate diffusion input is a modern technology, which provides implementation of digital circuit design to reduce area of digital circuits, power consumption and delay while advancement low complexity of logic design. In this Gate diffusion input (GDI) t-flip flop is intended according to the abstraction of t flip flop in which fewer numbers of transistors are acclimated as compared to conventional t flip flop and as well it uses lesser power and lesser delay. Simulation results on 45nm technology, which show that the proposed T-flip flop has, the less circuit design area and prorogation delay of 67.35% and consumption power is 57.43% in a power supply of 1 V GDI, CMOS, high speed, low power t-flip flop.

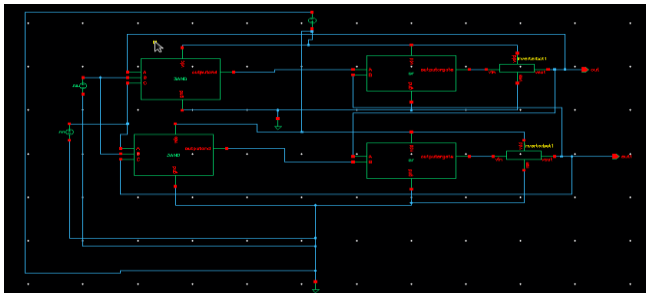
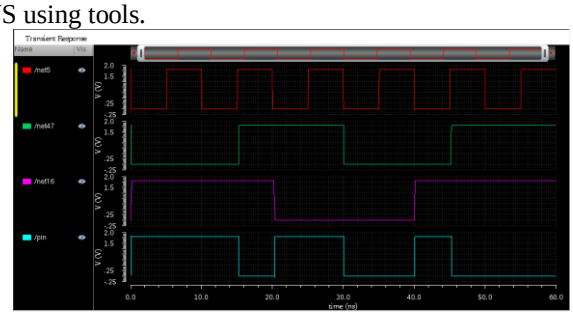


FIG 14: CIRCUIT DIAGRAM FOR T-FLIP FLOP USING 45nm TECHNOLOGY.

The transient response showing the simulation results is shown in Figure 15. The waveforms are obtained for different two inputs combinations. When Vdd = 1.8V and inputs A=1, B=1 i.e. when both the inputs are HIGH PM_1 are OFF while NM_1 are ON thus connecting theoutput node directly to the ground and hence output waveform thus obtained is LOW. For any other combinations of inputs the output waveform is HIGH . As in case of XOR gate, the cell is validated for DRC violations and is also verified for LVS using tools.



`FIG 15: Graph representing transient response of T-flip flop in 45nm TECHNOLOGY

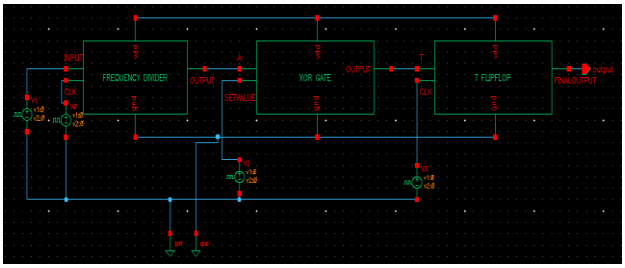


FIG 16: Circuit diagram of Frequency divider circuit with set value sequential circuit

V.SIMULATION RESULT

The circuit work simulated in cadence for 45nm technology from the result table, we are getting effective and average reduction result in delay, leakage power and noise margin with power gating technique as compare to basic TSPC frequency divider design technique

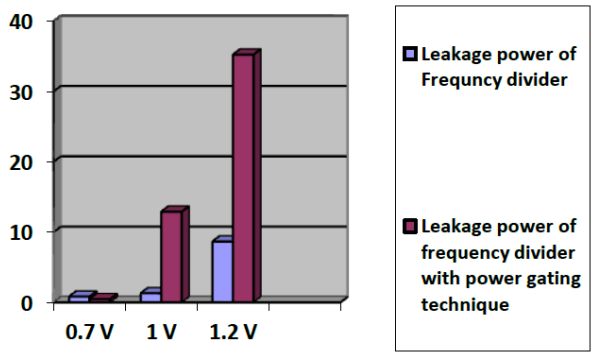
Leakage power

In frequency divider either the transistors are in off mode or in ON mode due to switching of opposite level leakage is introduced into devices. The power consumption in frequency divider consume a power off 1.66nw power gating technique power consumes is 5.16nw then, we finally getting the average result of frequency divider with power gating technique at 0.45pw so we achieved a power reduction of (0.45×10-12), show in table 1 more power reduction in comparison to power gating at 45nm technology, so from this we analyses a power reduction of 24% using power gating technique with frequency divider. It can also be observed through varied supply voltage as shown in comparison table 1 below

Pleackage = Ileakage .vdd (1)

Where, Ileakage=leakage current and Vdd = power supply.

Fig17 : Data analysis of frequency divider and frequency divider with power gating technique



Voltage	EXISTING SYSTEM		PROPOSED SYSTEM
	Leakage power of frequency divider	Leakage power of frequency divider with power gating technique	Leakage power of frequency divider with set values
0.7 V	0.81nW	0.4pW	0.32pW
1 V	1.2nW	6.88pW	0.35pW
1.2 V	8.64nW	22.6pW	045pW

Table1: comparison of leakage

The leakage power is calculated by this formula and we calculate the effective power in frequency divider with power gating technique (0.45×10-12) with supply voltage vdd= 0.7V The leakage power is calculated by this formula and we calculate the effective power in frequency divider with power gating technique (0.45×10-12) with supply voltage Vdd= 0.7V

Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of frequency divider generally varies as a function with amplitude of input a larger input will result in a smaller delay time. Delay time of the circuit is measured as the average of response time of gate for positive, negative output transition of sine wave. The comparative analysis of various circuit delay time is shown below. Delay will reduce when the voltage is increased, the main goal of using the frequency divider in our project, that we can set the threshold limits as per our requirement. In this we observe that power gating based frequency divider gives a better performance as compared to set value frequency divider, due to lower threshold voltage of frequency divider, we also observe that the signal rise and fall time lower provides fast signal propagation and less delay in 45nm technology

The Delay of the through during a signal transition is given as;

Delay = 0.69 Req X CL (2)

Where in above equation Req is the resistance that is implemented using the feed through cell and CL is the load capacitance.

Voltage	EXISTING SYSTEM		PROPOSED SYSTEM
	Delay of frequency divider	Delay of frequency divider with power gating technique	Delay of frequency divider with power gating technique
0.7 V	5.69 nsec	6.26 psec	3.1psec
1 V	9.23 nsec	36.95 psec	20.32psec
1.2 V	14.54 nsec	42.87 psec	30.45psec

Table2: comparison of delay

Propagation delay of frequency divider respectively (5.69 nsec) and with power gating technique have used delay is (6.26psec.).

Noise margin

The voltage difference between the graduate output level and the required input voltage level of a circuit is known as noise margin and we get the effective result with power gating technique as compare to conventional frequency divider, which is show below through the comparative analysis.

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VI. CONCLUSION

Proposed Frequency divider is modified by using transistors having less average power consumption with decreases in area, delay is also decreased by using only six PMOS as because delay is more concentrated to PMOS due to less mobility of holes compared to electrons, power gating based Frequency divider is created by using transistor and have better performance than the Frequency divider as there are fewer transistor counts by which area is reduced and delay is also reduced; the average power consumption of the proposed Frequency divider is less in comparison to the conventional Frequency divider, measured result correctly verified the principle of operation and characteristic of the low-power Frequency divider circuit. The circuit has been used for the design of low power.

REFERENCES

1. Hammad M. Cheema1, Reza Mahmoudi1, M.A.T. Sanduleanu2, Arthur van Roermund," A 44.5 GHz Differentially Tuned VCO in 65nm Bulk CMOS with 8% Tuning Range": 2018 IEEE
2. Honghui Deng Yongsheng Yin Goaming Du "phase Noise Analysis and Design of CMOS Differential Ring VCO". IEEE 2018.
3. ShyamAkashe, Deepak Kumar Sinha and Sanjay Sharma, "A low-leakage current power 45-nm CMOS SRAM", Indian Journal of Science and Technology, ISSN: 0974- 6846, Vol. 4 No. 4, April 2017
4. Y. Cao, T. Sato, D. Sylvester, M. Orshansky, C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," CICC, pp. 201-204, 2017
5. RavindranMohanavelu and PayamHeydari "A Novel Ultra High-Speed Flip-Flop-Based Frequency Divider Proceedings International Symposium on Circuits and Systems", pp 622-625, May 20116.
6. Koon-Lun Jackie Wong, Alexander Rylyakov, Chih- Kong Ken Yang "A Broadband 44-GHz Frequency Divider in 60-nm CMOS ''.Lee and B. Razavi, "A 40GHz Frequency Divider in 0.18µm CMOS Technology," Dig. Systm. VLSI Circuits, pp. 256-262, June 2016.
7. L. Romanò, S. Levantino, S. Pellerano, C. Samori, "A. Lacaita Low Jitter Design of a 0.35µm-CMOS Frequency Divider Operating up to 3GHz ESSCIRC 2016.
8. Chang, SFR, et al,''A dual-band RF transceiver for multistandard WLAN applications '',IEEE trans. Microwave Theory & tech., Vol.53, No.3,pp.1048- 1055,2016
9. BehzadRazavi, "design of analog CMOS integrated circuits". Book by Tata MC Graw –Hill Edition, 2015.
10. Keliushu,et al, ''A 2.4 GHz monolithic fractional N frequency synthesizer with robust phase-switching prescaler and loop capacitence multiplier, '' IEEE j. solid-state Circuits, Vol.38, No.6 pp.866-874, jun.,2015.
11. Dr.AntoBennet, M, SankarBabu G, Suresh R, Mohammed Sulaiman S, Sheriff M, Janakiraman G ,Natarajan S, "Design & Testing of Tcam Faults Using T_H Algorithm", Middle-East Journal of Scientific Research 23(08): 1921-1929, August 2015.
12. Dr.AntoBennet, M "Power Optimization Techniques for sequential elements using pulse triggered flipflops", International Journal of Computer & Modern Technology , Issue 01 ,Volume01 ,pp 29-40, June 2015.
13. Dr.AntoBennet, M,Manimaraboopathy M,P. MaragathavalliP,Dinesh Kumar T R, "Low Complexity Multiplier For Gf(2m) Based All One Polynomial", Middle-East Journal of Scientific Research 21 (11): 2064-2071, October 2014.
14. Rajesh, M., and J. M. Gnanasekar. "Path Observation Based Physical Routing Protocol for Wireless Ad Hoc Networks." Wireless Personal Communications 97.1 (2017): 1267-1289.
15. Rajesh, M., and J. M. Gnanasekar. "Sector Routing Protocol (SRP) in Ad-hoc Networks." Control Network and Complex Systems 5.7 (2015): 1-4.
16. Rajesh, M. "A Review on Excellence Analysis of Relationship Spur Advance in Wireless Ad Hoc Networks." International Journal of Pure and Applied Mathematics 118.9 (2018): 407-412.
17. Rajesh, M., et al. "SENSITIVE DATA SECURITY IN CLOUD COMPUTING AID OF DIFFERENT ENCRYPTION TECHNIQUES." Journal of Advanced Research in Dynamical and Control Systems 18.
18. Rajesh, M. "A signature based information security system for vitality proficient information accumulation in wireless sensor systems." International Journal of Pure and Applied Mathematics 118.9 (2018): 367-387.
19. Rajesh, M., K. Balasubramaniaswamy, and S. Aravindh. "MEBCK from Web using NLP Techniques." Computer Engineering and Intelligent Systems 6.8: 24-26.