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AVLS-based 32/33 Pre-scaler for frequency dividers

B.S. Premananda *, N. Sahithi, Sanya Mittal

Department of ETE, RV College of Engineering, Bengaluru, India

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ABSTRACT

Pre-scalers are widely used in phase-locked loops (PLL) which are vital components in communication systems. The Dual Modulus Pre-Scaler (DMPS) has dual division capability, to divide the clock by N/N+1 cycles, which can be controlled by the designer based on the control circuitry. Pre-scaler circuits are used to divide the received signal to obtain integer multiples of the received signal. This paper proposes a power efficient 32/33 pre-scaler for high-frequency operation. DMPS is composed of a series of D Flip-flops (D-FF) and logic gates along with feedback connection between the different stages. Clock skew is of major concern in the D-FFs, which can be reduced by realizing D-FFs using true single-phase clock (TSPC) logic. Furthermore, the incorporation of an Adaptive Voltage Level Source (AVLS) circuit decreases the power consumption of the circuits. By integrating the AVLS circuit to divide-by-32/33 DMPS, low power consumption is achieved. At different operating frequencies, both divide-by-32 and -33 modes of the proposed 32/33 DMPS with AVLS were analyzed. In comparison to the reference pre-scaler circuit, the proposed pre-scaler consumes 35.65% less power at 1GHz. CMOS 180nm technology in Cadence Virtuoso is used to realize circuits and Cadence Spectre is used to simulate circuits.

1. Introduction

A communication system that uses less power, performs better and has less jitter is considered to be extremely efficient. Phase-locked loops (PLL) are crucial components of communication systems. PLL synchronizes signals, tracks the input frequency, and generates a frequency that is multiple of the given frequency. When PLL is implemented using the conventional approach, consumes more power, and this power consumption increases as operating frequency increases. This problem must be resolved by implementing each component independently using techniques such as transistor sizing, decreasing transistor number, and connecting the bulk [1]. Individual circuits must be designed to consume less power and should be integrated to achieve higher power efficiency. In a PLL or a frequency synthesizer, the DMPS consumes maximum power as it remains on for the whole clock period and is connected in the feedback loop of a PLL. Since PLLs operate at very high frequencies of operation, thereby power consumption becomes a major constraint.

A dual-modulus N/N+1 ($N = 2^n$) pre-scaler divides frequency fed by N or N+1 while a divide-by-N counter divides frequency given by N [2]. Flip-flops (FF) and logic gates are used to construct the pre-scaler. FFs and logic gates' power consumption must be minimized to minimize pre-scaler power consumption. D-FF can be realized using transmission gates, pass transistors, basic gates, or TSPC logic [3]. The problem associated with realizing D-FF using pass transistors or basic gates is high area. TSPC-based logic is ideal for realizing D-FF in terms of area and power usage [4] and does not have clock skew problems. In TSPC, synchronization is accomplished by using a single-phase clock. TSPC has the advantage of consuming less area and eliminating clock skew problems and achieving higher frequencies. TSPC logic can be used to create designs with low-phase noise. TSPC logic has easy and compact clock distribution and logic design flexibility. Power reduction can further be improved by the incorporation of different low-power techniques. Adaptive Voltage level (AVL) is one of the low-power techniques used to reduce total power consumption. AVL is classified into two categories [1]. They are Adaptive voltage level source (AVLS) and Adaptive voltage level ground (AVLG).

When more than one clock frequency is required for different circuit subsystems in a system, pre-scalers become essential components [2]. The problem faced by pre-scalers is higher power consumption [5]. The objective of this work is to address this problem by designing a low-power divide-by-32/33 pre-scaler. After reviewing various low-power approaches, the AVLS technique was found to be more efficient with an increase in transistor count (by three). In the proposed design, the AVLS circuit is incorporated with the DMPS circuit to reduce power consumption. The designed circuits are simulated in various

* Corresponding author.
E-mail address: premanandabs@gmail.com (B.S. Premananda).

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frequencies to analyze the power. The designed circuits showed reduced power consumption in both lower and higher frequencies.

The paper is organized as follows: Section 2 discusses the literature review where various designs of components of the DMPS are studied. Section 3 discusses the AVL technique and DMPS circuits implementation in Cadence Virtuoso. Section 4 includes tables and a discussion of the simulation results. Section 5 entails the conclusion and future scope.

2. Literature review

In the context of frequency dividers, the pre-scaler is a significant component [6]. The amount of power consumed by pre-scalers is significant, due to the higher input frequency [7]. This paper presents a low-power divide-by-32/33 pre-scaler for frequency dividers.

The design and performance study of a TSPC latch with five transistors, six transistors, eleven transistors, a 2/3 pre-scaler, and a divide-by-2 counter was done. A divide-by-2/3 pre-scaler was developed using a low-power technique and is analyzed in terms of area, and power. Power reduction is achieved by combining the AVLS circuit with the TSPC-based circuit. The AVLS-TSPC based divide-by-2/3 DMPS was examined at 10 MHz, with a 1.8V supply voltage in both modes. Compared to existing pre-scalers, the 2/3 pre-scaler in [1] performed better while using less power.

To achieve low power, pass transistor logic was employed rather than gate logic. TSPC DFF-based frequency divider's power usage and speed were calculated. Three transistors were used to replace AND and OR (AND/OR) logic in the TSPC-based divide-by-2/3 pre-scaler with low-power consumption [2]. The circuits are realized in CMOS 180nm technology, and a divide-by-32/33 DMPS is built utilizing a 2/3 pre-scaler. The architectural composition of a generic DMPS consists of a series of D-FFs with specific feedback connections as well as a control input (master input) that controls the divide-by-N/N+1 capability. Logic gates are used in the feedback path. Many DFF-based solutions have already been proposed to increase the dual-modulus pre-scaler's operating speed. These systems are impacted by large load capacitance, which lowers the maximum working frequency and increases power consumption [4]. As a result, sequential and dynamic circuit approaches or TSPC must be employed to decrease circuit complexity, power consumption, and enhance operating speed.

Two TSPC-based D-FF and two E-TSPC-based D-FF techniques were proposed in [3]. The size of the device and body biasing techniques can be employed to obtain an efficient circuit with low power. Flip-flops that are appropriate for a low-voltage and high-frequency circuit must be selected. The D-FFs which are examined are dual-edge triggered (DET), pulse-triggered, and differential [5]. Since the DET switches on both edges of the clock cycle and the pulse-triggered D-FF has a larger clock load, they are ineffective in pre-scaler circuit design. The divide-by-2/3 DMPS is realized using TSPC, Master-Slave (MS), ETSPC, and differential-type DFFs and is compared in terms of power consumption. A 2/3 pre-scaler is popular because of its quick speed when compared to other pre-scalers.

Low-power consumption is achieved by reducing the number of switching stages, as well as transistor sizing, and restricting the power to D-FF during the divide-by-2 operation. The modified 2/3 pre-scaler has been combined to obtain divide-by-32/33 DMPS. A low-power D-FF circuit design using the AVL approach was proposed [8].

The AVLG circuit raises the ground potential, and whereas the AVLS circuit raises the supply potential, reduces overall power dissipation. The main objective of the designer was to lower the power dissipation of a D-FF. Simulation results show that the AVLS technique greatly lowers the power consumption of the device. Adiabatic circuits reduce power, but they also take up a lot of space, and delay is also very important [9].

The frequency of operation, short circuit, and switching power of the E-TSPC based 2/3 pre-scaler was described. The circuitry was implemented in 180nm CMOS technology. A unique, extremely wide band 2/3 pre-scaler has been designed and implemented. When compared to current E-TSPC circuits, the 2/3 pre-scaler operates at 6.5 GHz and without switching, short circuit (SC) power usage in the initial stage of D-FF2, and SC power consumption of D-FF1 [10]. To assist designers in selecting the best 2/3 pre-scaler for their design requirements, the paper focused on determining the best 2/3 DMPS in terms of area and speed. The power usage and maximum operating frequency of pre-scalers for TSPC and E-TSPC have been examined [11].

A new improved Multi-Modulus Divider (MMD) is presented for high-frequency application. The low-power 2/3 pre-scaler constructed with TSPC logic is used in the proposed MMD architecture's 6-stage design. The MMD's extended range offers programmable divisions from 8 to 127 [12]. FinFET technology is widely used in industry. The approach for performing setup and hold time analysis for various master slave D-FF designs in 18nm FinFET technology is presented [13].

Wideband frequency synthesizers are implemented using pre-scalers, which occupy less area and power when designed using TSPC-based D-FF in contrast to other D-FF designs. The power consumption of the current architectures becomes a significant problem on a larger scale. To address this, TSPC logic along with the AVLS circuit can be used.

3. Design and implementation of DMPS

Low-power approaches are essential to decrease the power consumption of pre-scalers. To achieve a low power divide-by-32/33 DMPS, it is crucial to minimize the power utilization of every component. Low-power approaches decrease circuit power only with a small area increase. There are various techniques to reduce power consumption as discussed in the literature review. Adiabatic logic, AVL, Gated leakage transistor (GALEOR), Leakage control transistor (LECTOR), stack, and clock gating are some of the techniques to reduce power consumption [14].

3.1. Adaptive voltage level

AVL is a technique for minimizing a circuit's power consumption. AVL can be classified into two categories namely AVLS and AVLG. AVLG raises the ground potential whereas AVLS raises the supply potential. In AVLG one n-MOS and two p-MOS transistors are in parallel. p-MOS bulk is connected to the ground and n-MOS is connected to the clock. AVLS consists of two n-MOS and one p-MOS transistor [14]. The n-MOSFETs are connected to the power supply, whereas the p-MOS transistor is connected to a clock that serves as an input. The n-MOS transistors are turned ON, but the p-MOS transistor switches between states in accordance with the clock. Minimizing leakage flowing through the p-MOS transistor decreases power usage. AVLS reduces power consumption compared to AVLG [1].

The implementation is carried out in the bottom-up approach where the elements of divide-by-32/33 pre-scaler such as D-FF, and logic gates such as NAND, and NOR are first designed and then integrated to obtain the required 32/33 pre-scaler circuit. CMOS 180nm technology in Cadence Virtuoso is used to implement circuits. Simulation of circuits is performed in Cadence Spectre. The next section explains in detail about design and implementation of the D-FF, 2/3 pre-scaler, and 32/33 pre-scaler.

3.2. Implementation of TSPC-based D-FF

The basic building blocks of sequential logic are FFs, which consist of two stable states and are designed to store data. The FFs are edge triggered and clocked which means output is changed w.r.t. input when the clock changes its state. The D-FF can be realized using basic gates (master-slave), transmission gates, pass transistors, and TSPC-based logic. TSPC-based D-FF requires eleven transistors. TSPC-based D-FFs require less area [15,16]. The issue of clock skew is resolved through TSPC, and they occupy less area and consume less power. A schematic of the 11T TSPC-based D-FF is depicted in Fig. 1. Five p-MOS and six

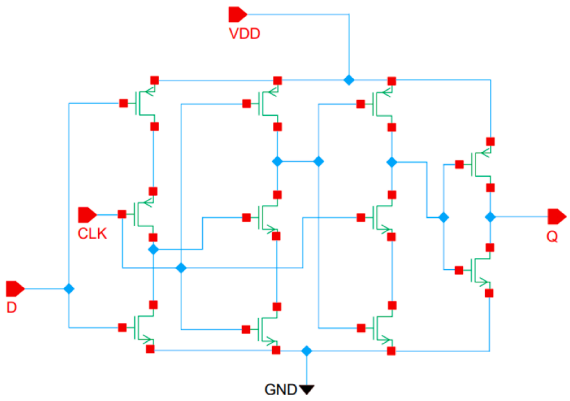

Fig. 1. TSPC-based D-FF circuit.

n-MOS transistors constitute a D-FF. To lower supply node potential, a proposed TSPC-based D-FF with AVLS technique (AT) is constructed by combining AVLS to D-FF is illustrated in Fig. 2. Proposed TSPC-based D-FF with AT requires three extra transistors compared to TSPC-based D-FF but there is a significant power reduction.

3.3. Implementation of TSPC-based divide-by-2/3 DMPS

Pre-scaler is a crucial component in PLL design in terms of power utilization because it is active throughout the entire working period [17]. DMPS are circuits that divide a given frequency by N or N+1 [8]. Based on the control given, 2/3 DMPS divides the given frequency by 2 or 3. TSPC-based 2/3 DMPS using D-FF and logic gates. When the control is high, the output is divided by 2 and when the control is low, the pre-scaler functions in the divide-by-3. The realization of AND and OR gates require twelve transistors which can be reduced by replacing logic gates with PTL. The divide-by-2/3 DMPS using pass transistor logic (PTL) requires fewer transistors compared to conventional 2/3 DMPS as illustrated in Table 1.

The proposed divide-by-2/3 pre-scaler is shown in Fig. 3. The AVLS circuit is incorporated with the pre-scaler circuit. One p-MOS and n-MOS transistor are used to realize the AND logic operation using PTL. Three transistors are used to implement the control. The MOSFET p-MOS1 is always active and equivalent to logic Q when the control is low. A strong signal drives the DFF2 since the drains of n-MOS1 and p-MOS2 transistors are connected to D-FF2. Pre-scaler functions in divide-by-3 mode. The input of n-MOS1 and p-MOS2 transistors is dependent on the inverted output of DFF2 when the control is high since MOSFET p-MOS1 is always off. DFF2 alone performs divide-by-2 mode.

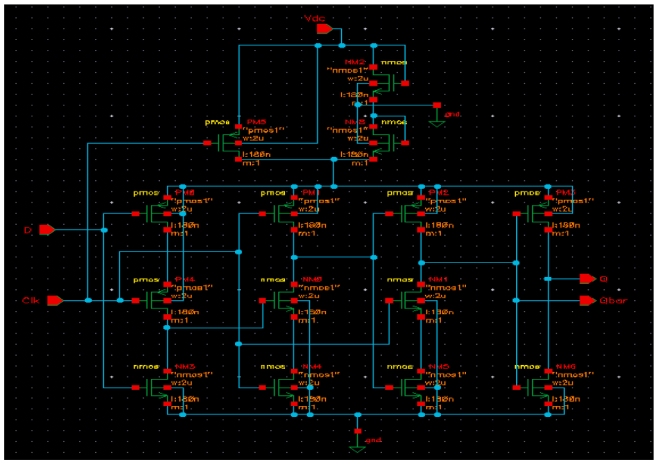

Fig. 2. Proposed TSPC-based D-FF with AVLS circuit.

Table 1
Area comparision of dividei-by-2/3 DMPS circuit.

Divide-by-2/3 DMPS Circuits	Transistor Count
TSPC-based D-FF and logic gates [2]	34
TSPC-based D-FF and PTL [2]	25
Proposed 2/3 DMPS with AVLS	28

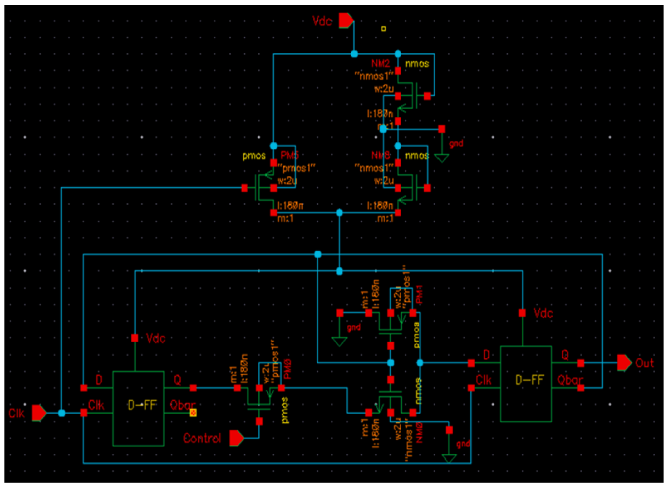

Fig. 3. Proposed divide-by-2/3 DMPS with AVLS circuit.

3.4. Implementation of TSPC-based divide-by-32/33 DMPS

The divide-by-32/33 DMPS is realized after implementing each block, such as the D-FF, NAND, and NOR gates. Using the cell-view option in Cadence Virtuoso, the previously mentioned circuits are converted into blocks. This is done to ensure that all the components can be connected without the hassle and improves the regularity of the design. The divide-by-32/33 DMPS circuit operates in two modes: divide-by-32 and divide-by-33 [18]. When the control is at logic high, it operates as a divide-by-32 unit, while the 2/3 pre-scaler within the design works as a divide-by-2 counter. When the control is at logic low, the 32/33 pre-scaler functions in divide-by-33.

Fig. 4 shows the proposed 32/33 DMPS with AVLS. In the case of a logic high control signal, the output of NOR2 is logic low, whereas NAND2's output is always forced to be logic '1', regardless of any data present on the inverted output of D-FF3. The 32/33 pre-scaler operates in divide-by-32 mode as a result. D-FF1 is completely off for 32 input clock cycles since the control is logic high. To decrease the power consumption of reference 32/33 pre-scaler a new 32/33 DMPS architecture is proposed.

The proposed circuit is an integration of divide-by-32/33 DMPS and AVLS. AVLS circuit is composed of two n-MOS and one p-MOSFETs connected in parallel. The gate terminal of n-MOSFET is connected to 1.8 V. The terminal of p-MOSFET receives a clock that serves as an input to the circuit. Supply node potential is reduced by AVLS. The proposed circuit increases the transistor count by three.

4. Results and discussion

The TSPC-based D-FF, divide-by-2/3 DMPS, and divide-by-32/33 DMPS circuits were realized in CMOS 180nm technology using Cadence's Virtuoso and simulated and analyzed the power using Cadence Spectre. The circuits are analyzed for a range of frequencies. The simulation of the circuits is performed with a supply voltage of 1.8V. The power consumption of these circuits is examined in this section along with the results inferred for the same.

The power analysis of the reference and proposed TSPC-based D-FF

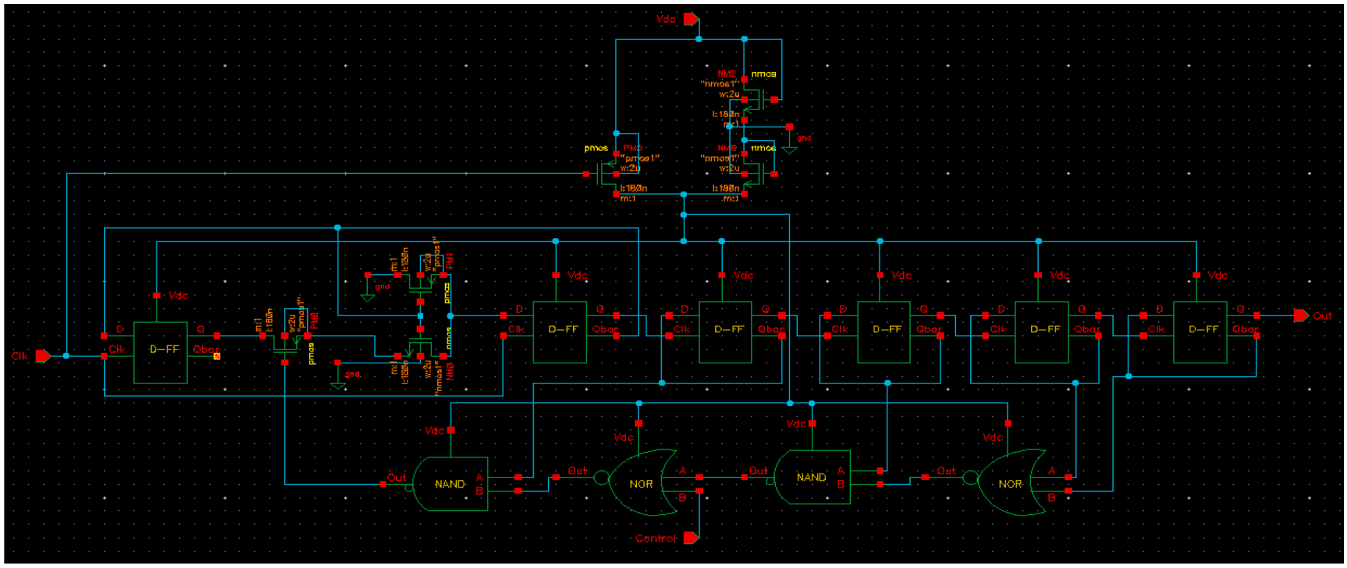

Fig. 4. Proposed divide-by-32/33 DMPS with AVLS circuit.

circuits are depicted in Fig. 5. The values infer that the proposed TSPC-based D-FF with AVLS consumes 44.48μW of power at 1GHz in contrast to the TSPC-based D-FF [2] which consumes 51.29μW, there is 13.28% reduction in power consumption. The D-FF along with logic gates is used to realize 2/3 DMPS and 32/33 DMPS circuits.

TSPC-based D-FF used in divide-by-2/3 DMPS is more compact, and the clock skew problem is also eliminated. Depending on the control, the input signal's frequency is divided by a factor of 2 or 3 in 2/3 pre-scaler. The divide-by-2/3 DMPS circuit is simulated at different frequencies (1MHz to 1 GHz) and analyzed the power consumption of the DMPS circuits. The power analyzed at a frequency of 1 GHz is illustrated in Fig. 6 to show the comparison between the reference and the proposed DMPS circuit. The divide-by-32/33 DMPS is designed by integrating realized 2/3 DMPS and logic gates (NAND and NOR gates) as shown in Fig. 4. Power analysis for both modes of 32/33 DMPS is performed at different frequencies.

Power analysis in divide-by-33 mode for multiple frequencies is performed and power consumed values are plotted in Fig. 7 for divide-by-32/33 DMPS circuits. From Fig. 7, it is evident that the proposed DMPS with an AVLS circuit incorporated decreases the overall power consumption. For instance, at 750 MHz, there is a reduction of power by 28.88%. The proposed 32/33 DMPS consumes less power at all frequencies in both modes of operation.

The power consumption of divide-by-32/33 DMPS circuits at 1 GHz operating frequency for both the modes is shown in Fig. 8. The power

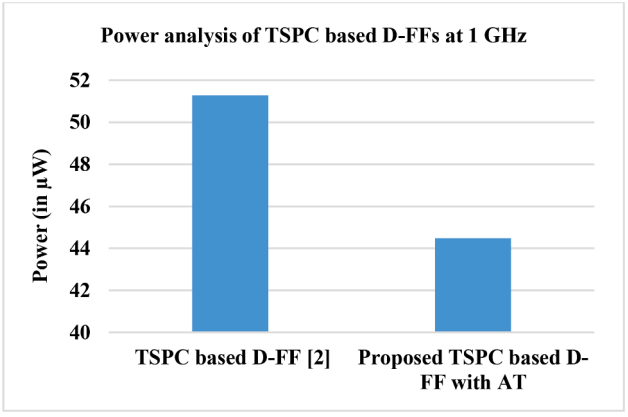

Fig. 5. Power analysis of TSPC-based D-FF.

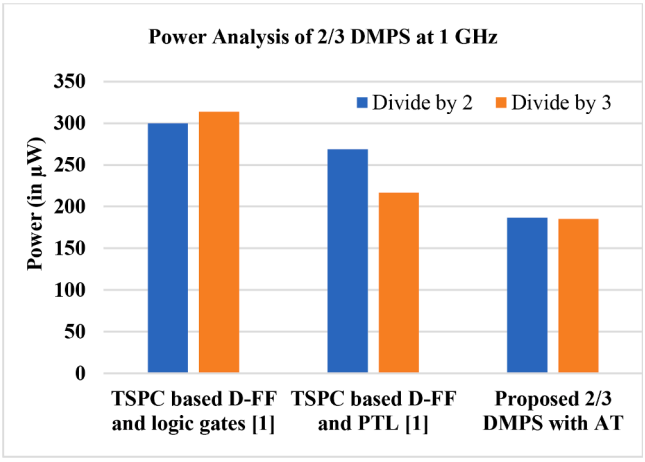

Fig. 6. Power analysis of TSPC based divide-by-2/3 DMPS circuits.

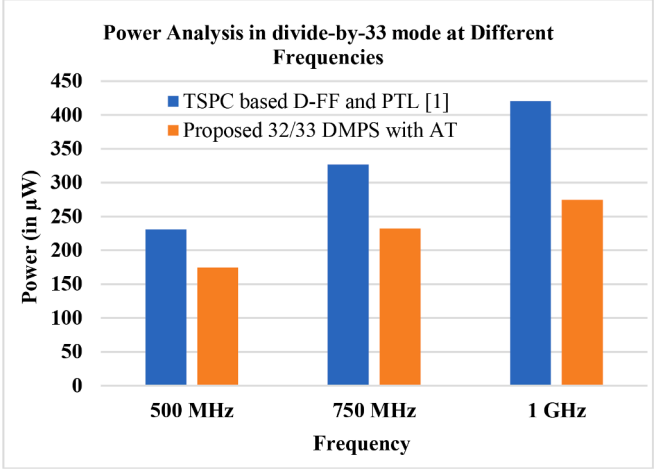

Fig. 7. Power analysis of divide-by-32/33 DMPS circuits in divide-by-33 mode at different frequencies.

consumption in both modes (divide-by-32 and divide-by-33) of

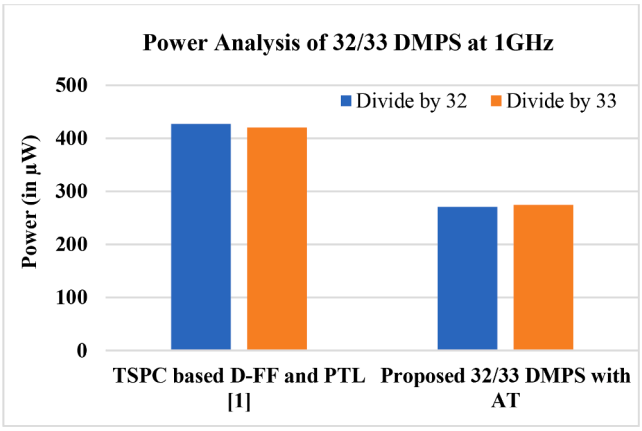

Fig. 8. Power analysis of divide-by-32/33 DMPS circuits.

operation at one higher frequency (1GHz) is plotted in Fig. 8, although the DMPS circuits power consumption is verified in other frequencies. In the proposed DMPS circuit, divide-by-32 mode consumes 36.55% lesser power whereas in divide-by-33 mode power reduction of 34.72% is observed with a trade-off in a marginal increase in transistor count (by 3 transistors) due to the addition of AVLS circuit. The area of the DMPS circuit can be optimized by realizing the logic gates (NAND and NOR) used in feedback (Fig. 4) of DMPS circuits using pass transistor logic.

5. Conclusion

In this work, the AVLS circuit is incorporated to reduce the power consumption of D flip-flops and pre-scaler circuits. The proposed divide-by-32/33 DMPS with an AVLS circuit incorporated also operates at a higher frequency (GHz). The proposed 32/33 DMPS circuit with AVLS circuit incorporation at 1 GHz, operating in divide-by-32/33 mode requires an average power of 272.7µW whereas DMPS in [2] consumes 423.75µW. There is a 35.65% reduction in power with a marginal increase in the area by 3.52%. Though the proposed DMPS with AVLS circuit increases transistor count by 3, there is a significant reduction in power consumption. Further DMPS circuits can be designed by using other variants of TSPC circuits which require lesser transistors while incorporating other low-power techniques.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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Dr. Premananda B.S. is associated with Rashtreeya Vidyalaya College of Engineering, Bengaluru, India. He is working as an associate professor in the Department of Electronics and Telecommunication Engineering and a senior IEEE member. His main areas of interest are in the field of Very-Large-Scale Integration (VLSI) Designs in ASIC/FPGA, Quantum-dot Cellular Automata (QCA), low-power and compact VLSI circuits, speech enhancement, signal processing, and communication. He has reviewed several papers for international journals and conferences and chaired the session at international conferences. He has published several research articles in international journals and conferences and guides many projects in his area of research.

N. Sahithi is pursuing her undergraduate course in Telecommunications Engineering at RV College of Engineering, Bengaluru, Karnataka, India. Her fields of interest are Digital design, CMOS, and low-power design.

Sanya Mittal is pursuing her undergraduate course in Telecommunications Engineering at RV College of Engineering, Bengaluru, Karnataka, India. Her fields of interest are Digital design, low-power VLSI designs, and CMOS.