(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

THIRD SEMESTER [BCA] JANUARY 2024

Paper Code: BCA-203 **Subject: Computer Organization and Architecture**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q.No.1 which is compulsory. Select one question from each unit.

Q1 Attempt the following (**any five**) **[5x5=25]**

a) What are logic gates? Draw the schematic diagram of XOR gate. Give its truth table.

b) Draw a MUX using NAND gates which selects from four inputs A0 t A3 and two select inputs S0 and S1.

c) What is the role of stack pointer in computer organization?

d) What is ROM? How PROM, EPROM and EEPROM differ from each other?

e) Design and explain Ring counter.

f) Explain the edge triggered D flip-flop.

UNIT-I

Q2 a) What are Universal gates? Explain how basic gates can be realize using NAND and NOR gates. **[6.5]**

b) State and prove Associative and Distributive theorems. **[6]**

Q3 a) Draw a full subtractor circuit using NAND gate. **[6.5]**

b) Minimise the following Boolean function using K-map. **[6]**
F(A, B, C, D) = Σ (3, 4, 5,7,9, 13, 14, 15)

UNIT-II

Q4 a) Realize JK flip-flop using SR flip flop. **[6.5]**

b) Differentiate between flip-flop and latches. **[6]**

Q5 a) Describe the operation of PISO shift register with the help of block diagram. **[6.5]**

b) Differentiate Combinational and Sequential circuits? **[6]**

UNIT-III

Q6 a) What is instruction cycle? Draw detailed flowchart of the instruction cycle. **[6.5]**

b) What are CPU buses and Why they are important? **[6]**

Q7 a) Explain the different types of addressing modes in basic computer. **[6.5]**

b) What is a register in a CPU and How Does it Work? **[6]**

UNIT-IV

Q8 a) Write difference between Programmed Input /Output and Interrupt Driven Input/output. **[6.5]**

b) How DMA controller communicates and transfers data between peripheral devices and RAM. **[6]**

P.T.O.

BCA-203
P1

Q9 a) Draw and explain the memory hierarchy structure and mark the arrow from low to high (speed) and high to low (Cost). **[6.5]**

b) What is associative memory? Explain its working with the help of diagram. **[6]**

****