EE301
Analog Circuit Project

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OBJECTIVE:

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

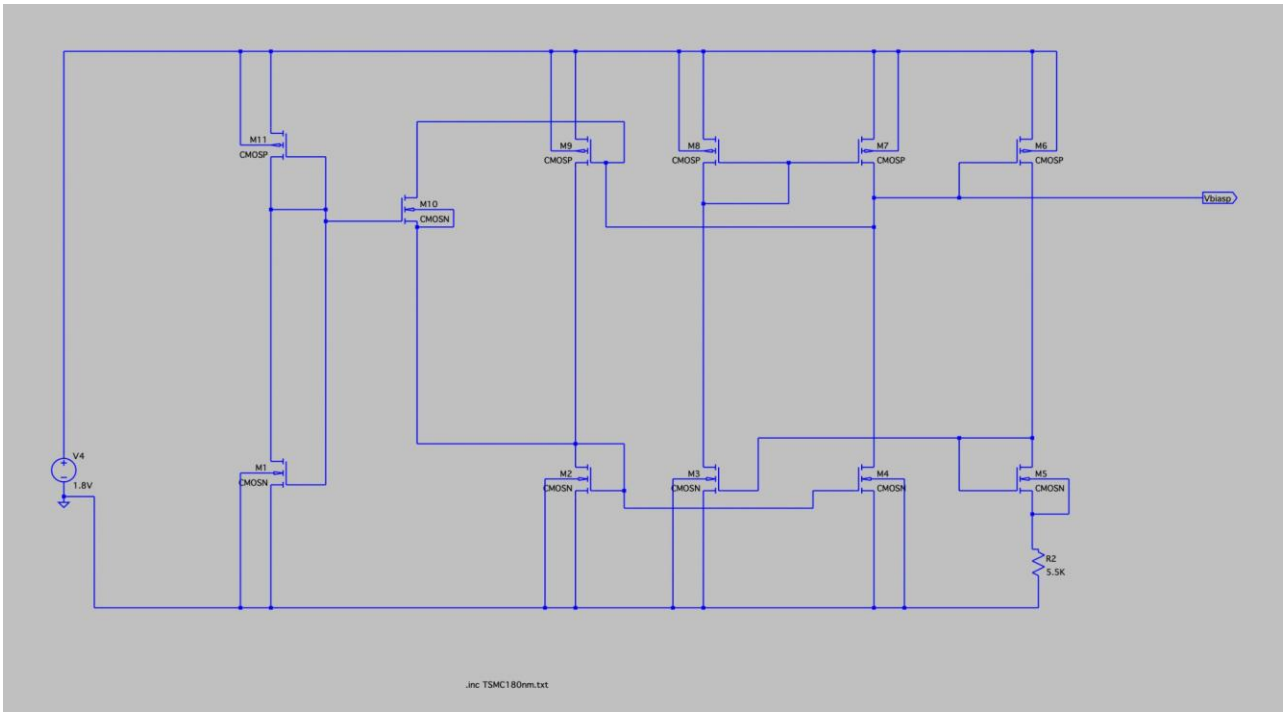
The target specifications for designing the cascode amplifier are as follows:

- VDD = 1.8 V
- AV = 20 V/V
- Power dissipation (PD) < 5 mW
- Load Capacitance (CL) = 1 pF
- Unity Gain Bandwidth(UGB) > 500 KHz.

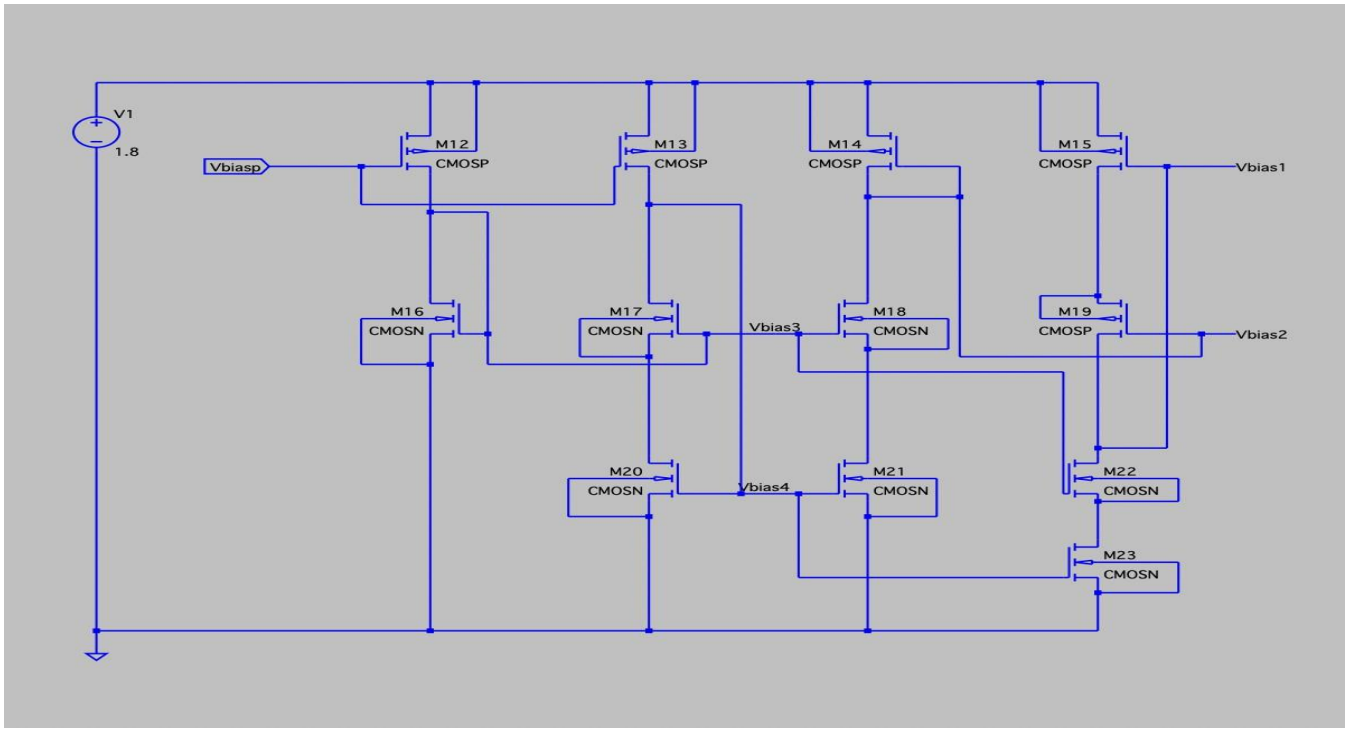
Circuits:[180nm]

Schematic:

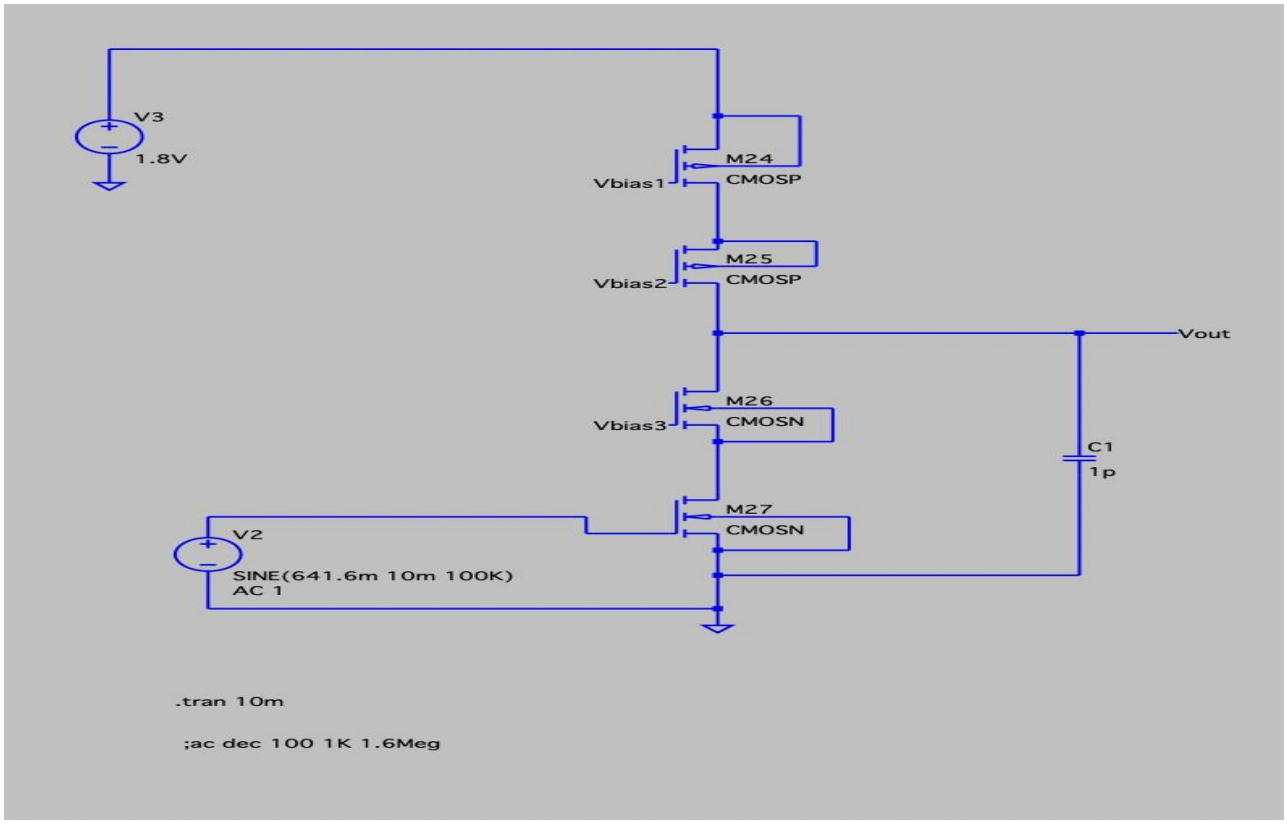
Beta Multiplier



Cascode Current mirror

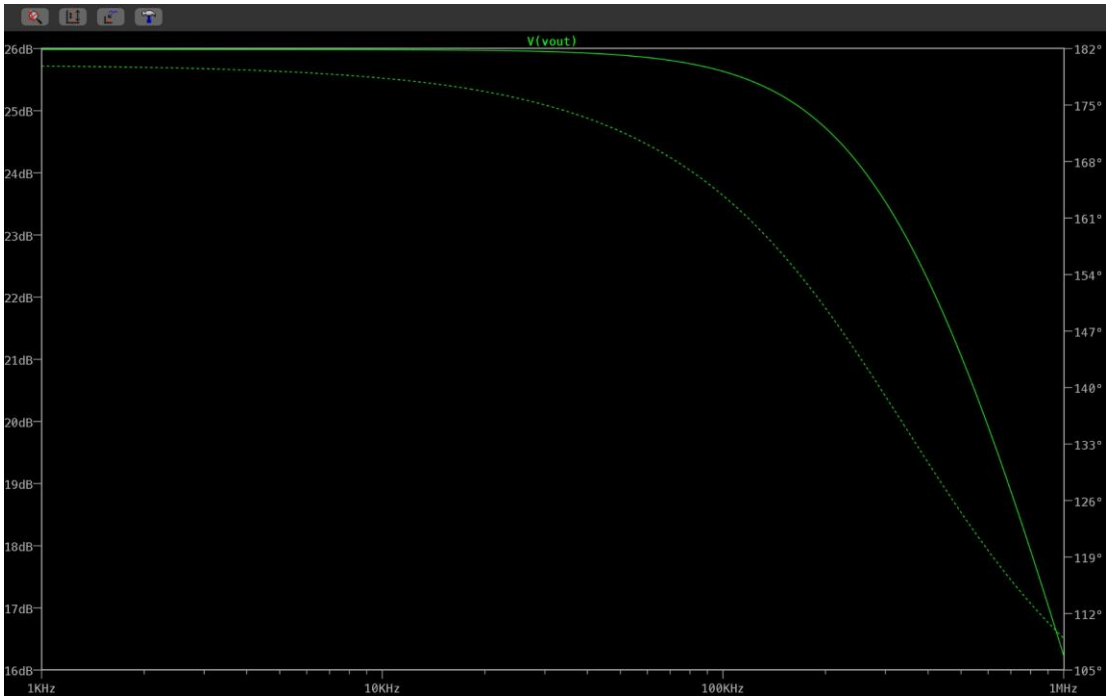


Cascode Amplifier

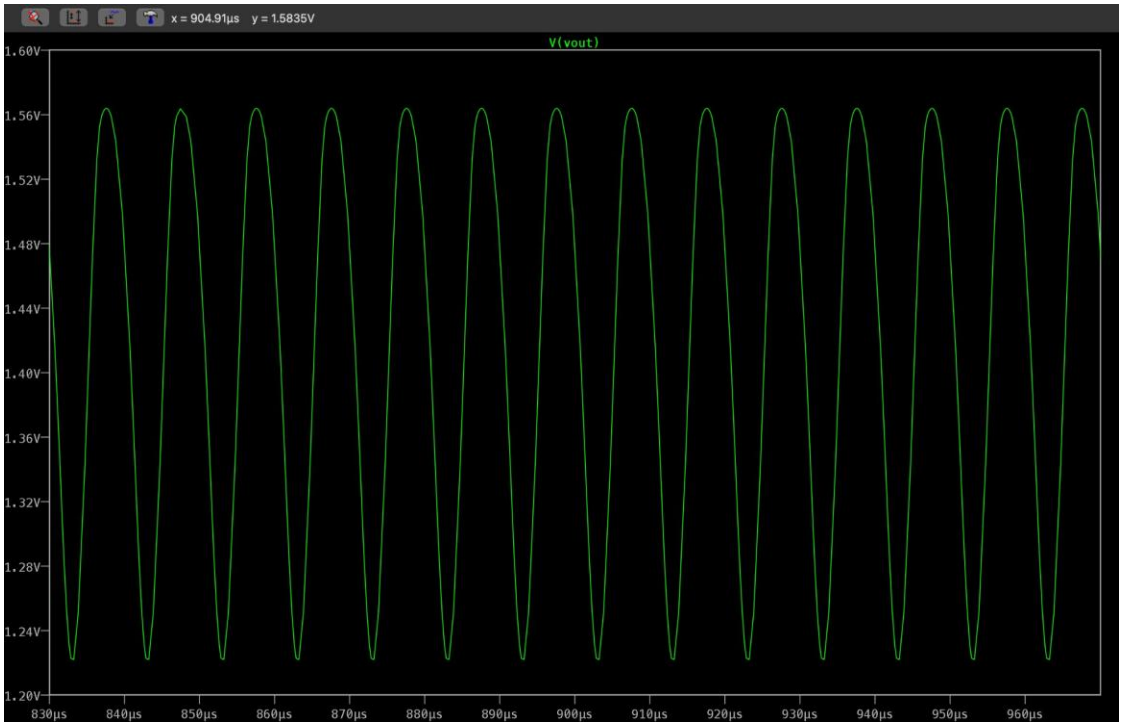


Simulations and Graph:

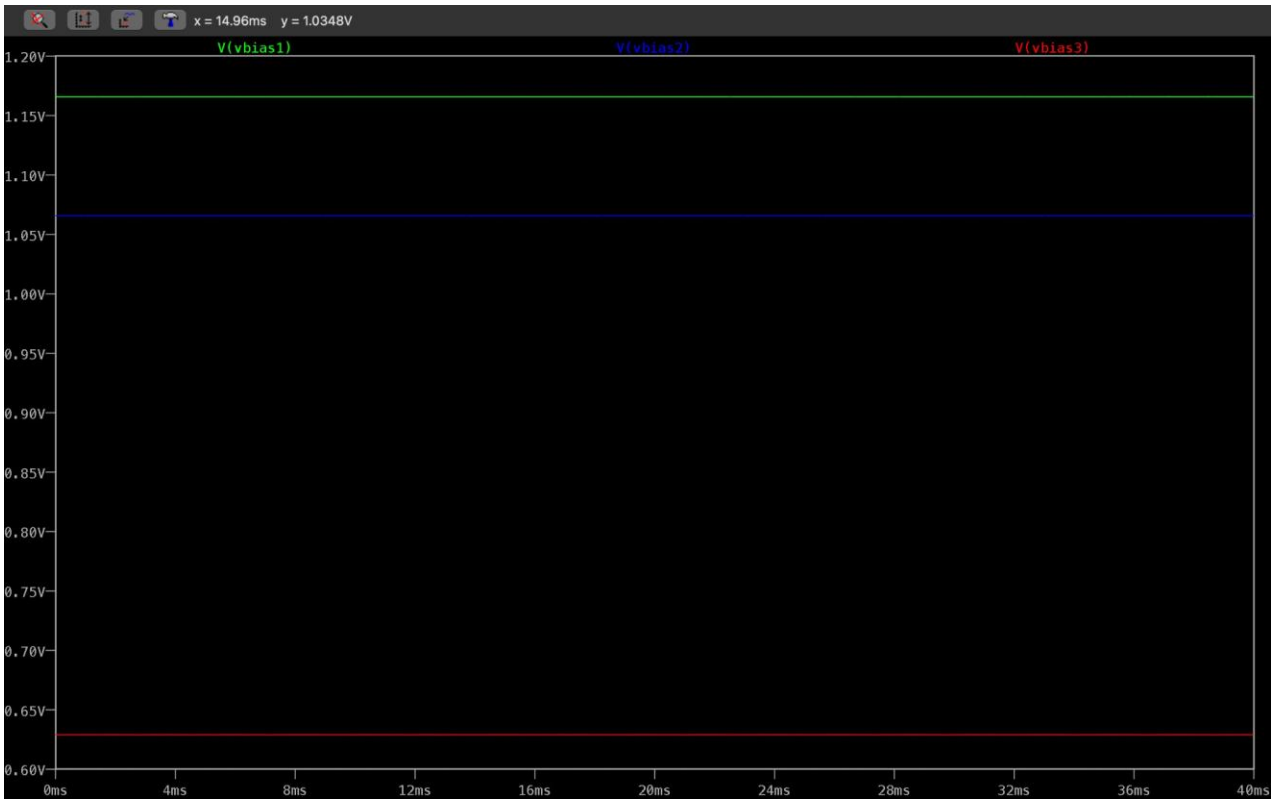
Bode Plot:



Vout:



Vbias1,Vbias2,Vbias3:



Beta Multiplier: This circuit is commonly used to generate a stable reference current that remains relatively unaffected by temperature variations and supply voltage. Here, it produces a bias voltage, Vbias, which is then supplied as an input to the Cascode Current Mirror.

Cascode Current Mirror: By using Vbias as an input, the Cascode Current Mirror can more accurately replicate the reference current. The cascode structure enhances output resistance and minimizes the effects of channel length modulation, making it well-suited for precise current mirroring

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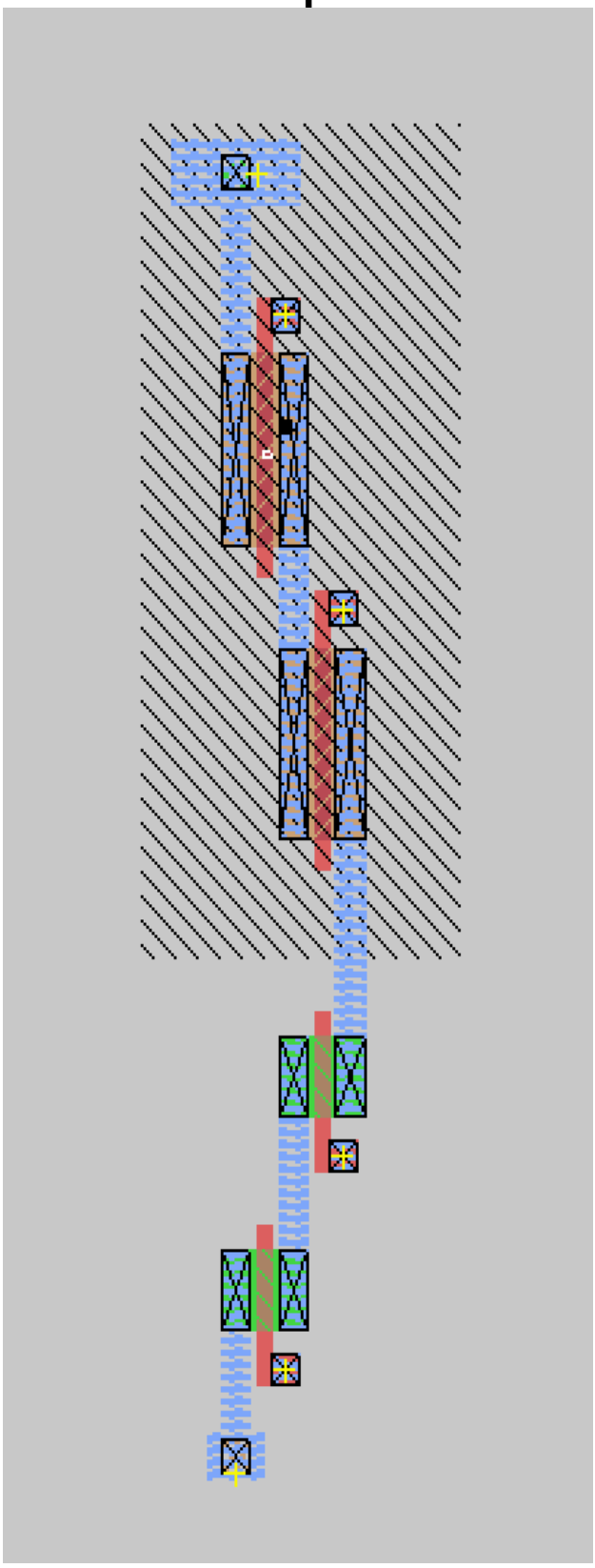
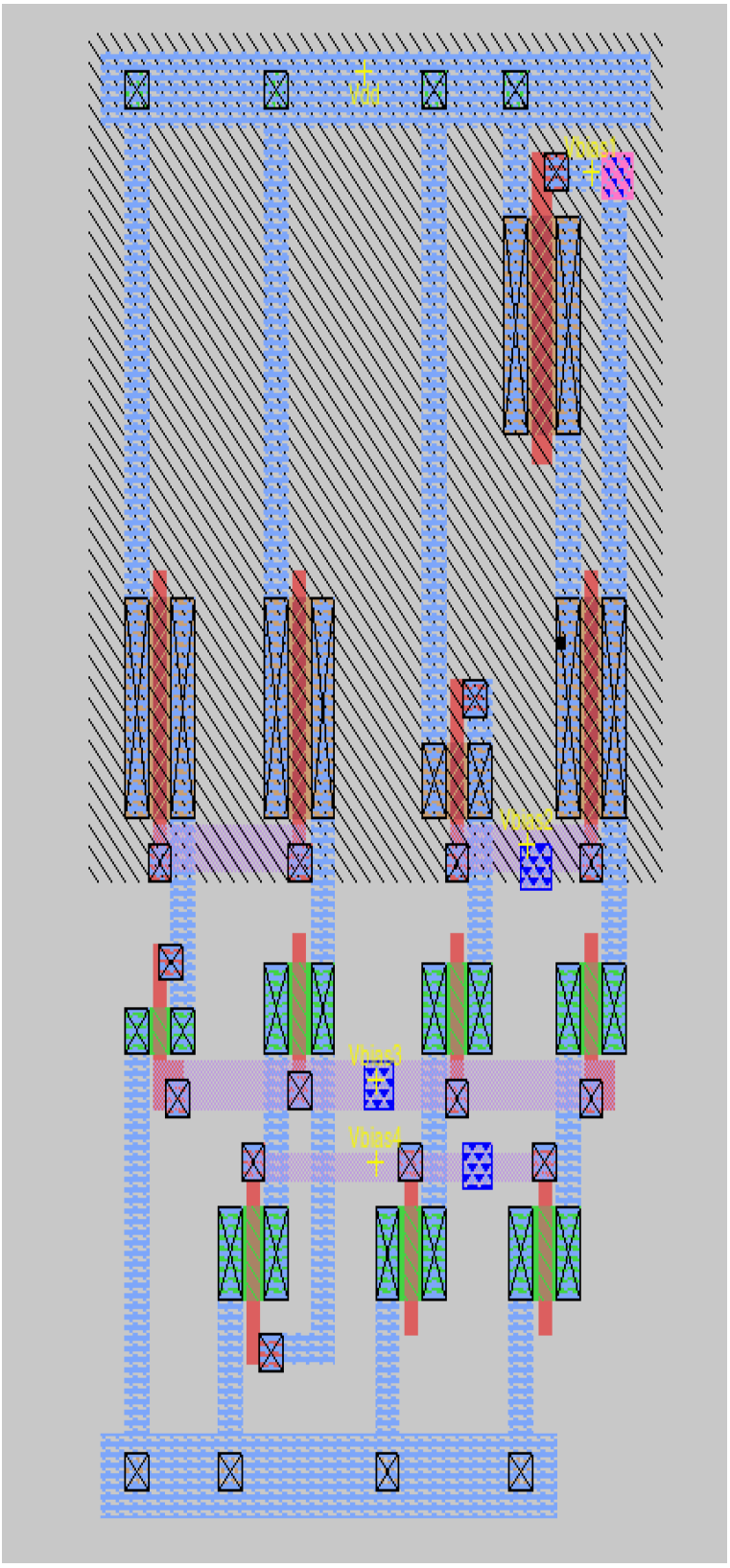
Cascode Amplifier: This amplifier relies on three bias voltages—Vbias1,Vbias2,Vbias3—to stabilize the operating points of the transistors within the cascode stages, improving gain and output impedance. Properly calculated W/L ratios for the transistors, likely based on desired gain and matching criteria, are essential for maintaining the amplifier's linearity and overall performance.

Magic Layout

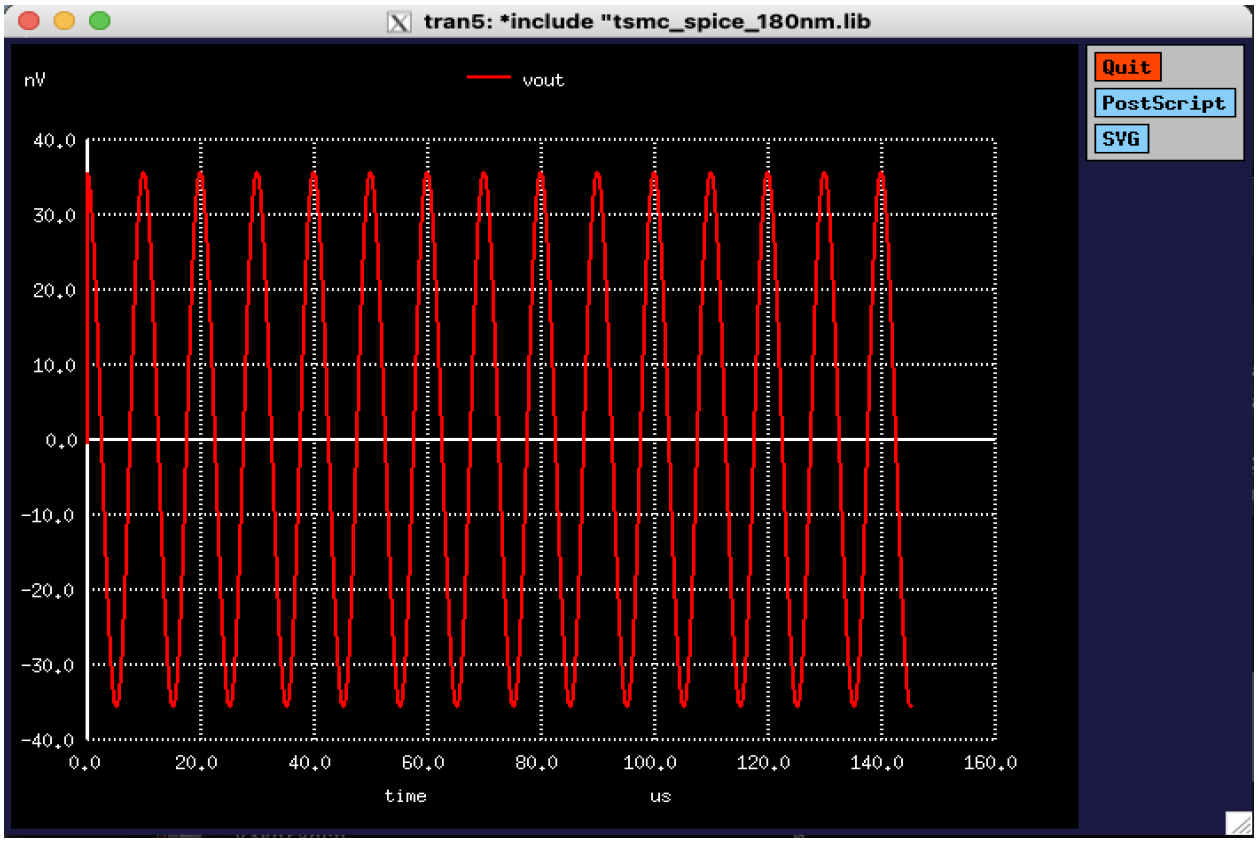
Cascode Amplifier



Cascode Current Mirror



Ngspice of cascode amplifier (180nm)




```
Warning: Pd = 2.7e-12 is less than W.
Warning: Ps = 2.7e-12 is less than W.

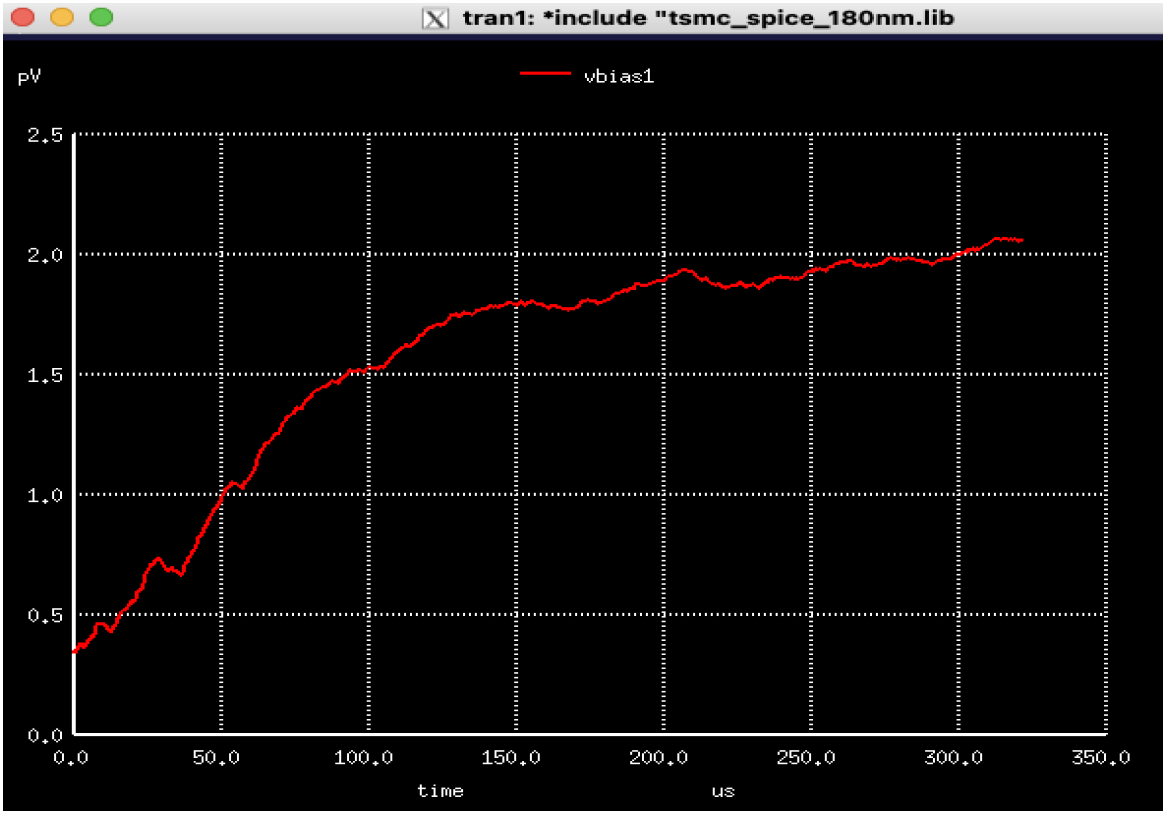
Checking parameters for BSIM 3.2 model pfet
Warning: Pd = 5.22e-12 is less than W.
Warning: Ps = 5.22e-12 is less than W.

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vbias1                                    1.57
vdd                                 -1.69946e-12
vout                                 -1.6995e-12
vbias3                                    0.63
vin                                     0.6416
vbias2                                    1.06
v4#branch                                    0
v3#branch                                    0
v2#branch                                    0
v1#branch                                    0

Reference value :  3.51609e-04
```

Ngspice of current mirror(180nm)

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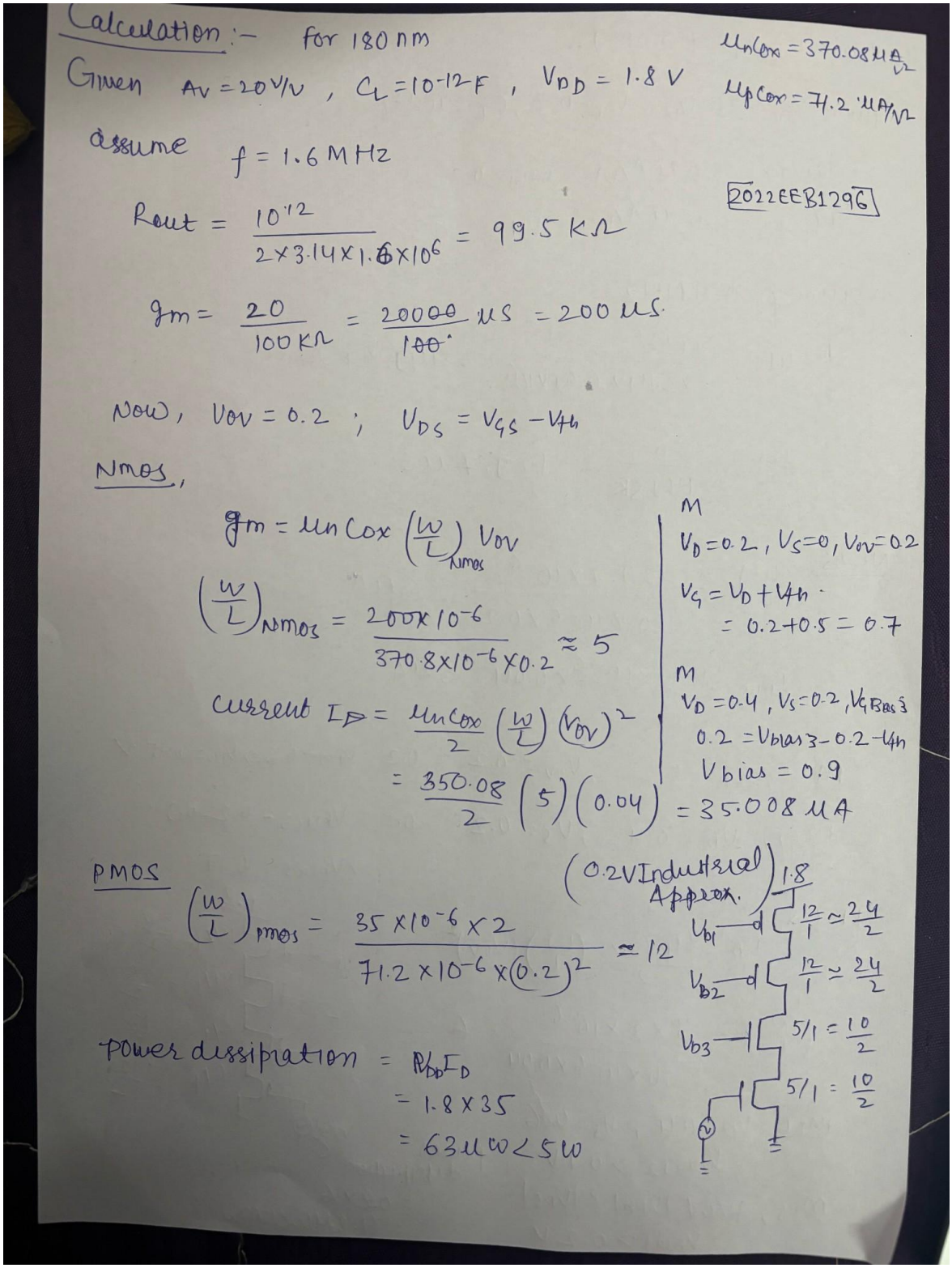
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                 7.30263e-12
vbias1                              3.45358e-13
```

Observation and Calculation:



Calculation :- for 180 nm

$\mu_n C_{ox} = 370.08 \mu A/V^2$

$\mu_p C_{ox} = 71.2 \mu A/V^2$

Given $A_V = 20 V/V$, $C_L = 10^{-12} F$, $V_{DD} = 1.8 V$

assume $f = 1.6 MHz$

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$$R_{out} = \frac{10^{12}}{2 \times 3.14 \times 1.6 \times 10^6} = 99.5 K\Omega$$

$$g_m = \frac{20}{100 K\Omega} = \frac{20000}{100} \mu S = 200 \mu S$$

Now, $V_{OV} = 0.2$; $V_{DS} = V_{GS} - V_{th}$

Nmos,

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_{Nmos} V_{OV}$$

$$\left(\frac{W}{L}\right)_{Nmos} = \frac{200 \times 10^{-6}}{370.8 \times 10^{-6} \times 0.2} \approx 5$$

current $I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{OV})^2$

$= \frac{350.08}{2} (5)(0.04) = 35.008 \mu A$

M

$V_D = 0.2$, $V_S = 0$, $V_{OV} = 0.2$

$V_G = V_D + V_{th}$

$= 0.2 + 0.5 = 0.7$

M

$V_D = 0.4$, $V_S = 0.2$, V_{GBias}

$0.2 = V_{bias3} - 0.2 - V_{th}$

$V_{bias} = 0.9$

PMOS

$$\left(\frac{W}{L}\right)_{pmos} = \frac{35 \times 10^{-6} \times 2}{71.2 \times 10^{-6} \times (0.2)^2} \approx 12$$

(0.2V Industrial Approx.)

1.8

V_{b1} — $12/1 \simeq 24/2$

V_{b2} — $12/1 \simeq 24/2$

V_{b3} — $5/1 = 10/2$

$5/1 = 10/2$

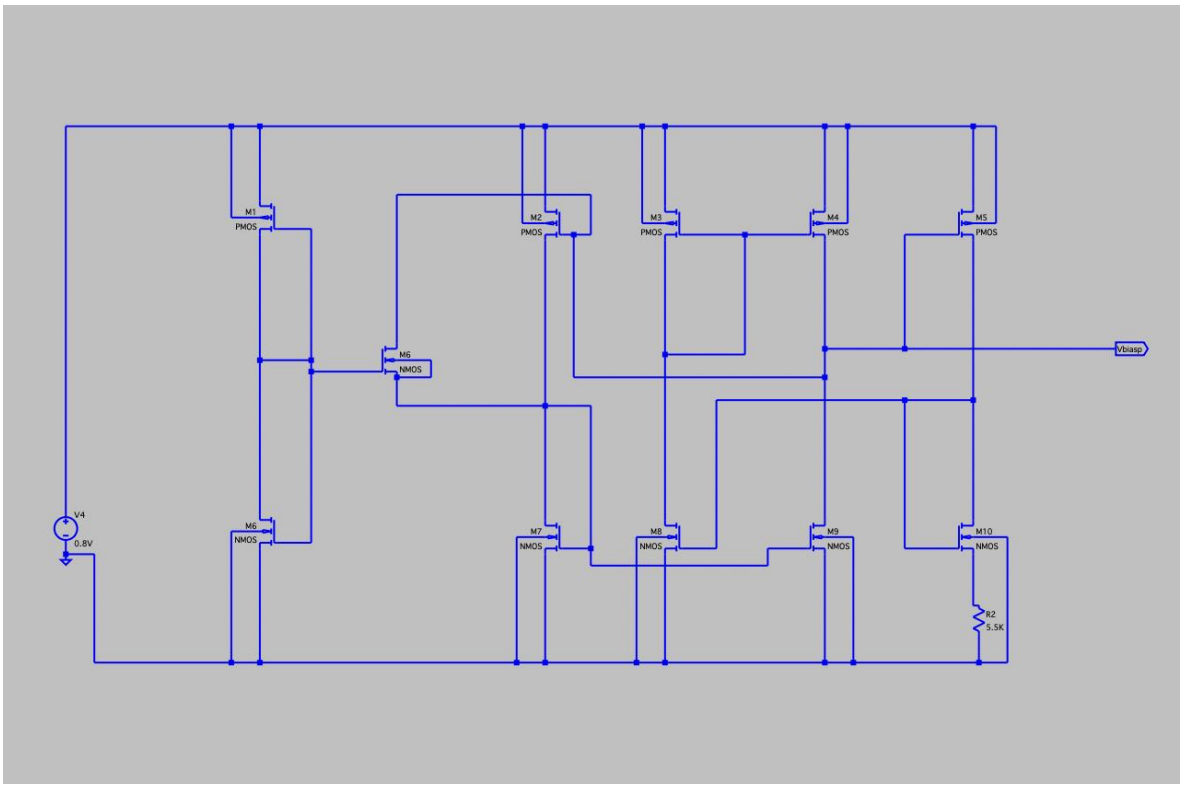
power dissipation $= P_{DD} I_D$

$= 1.8 \times 35$

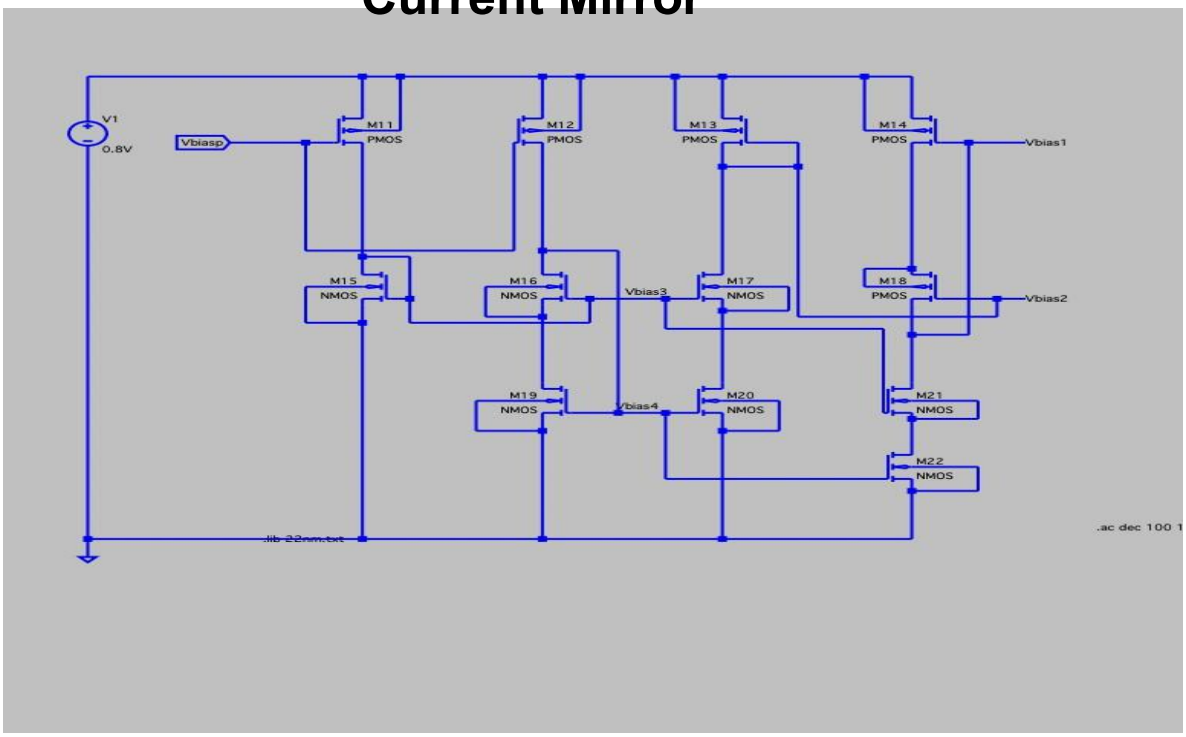
$= 63 \mu W < 5 W$

22nm Technology(Schematic)

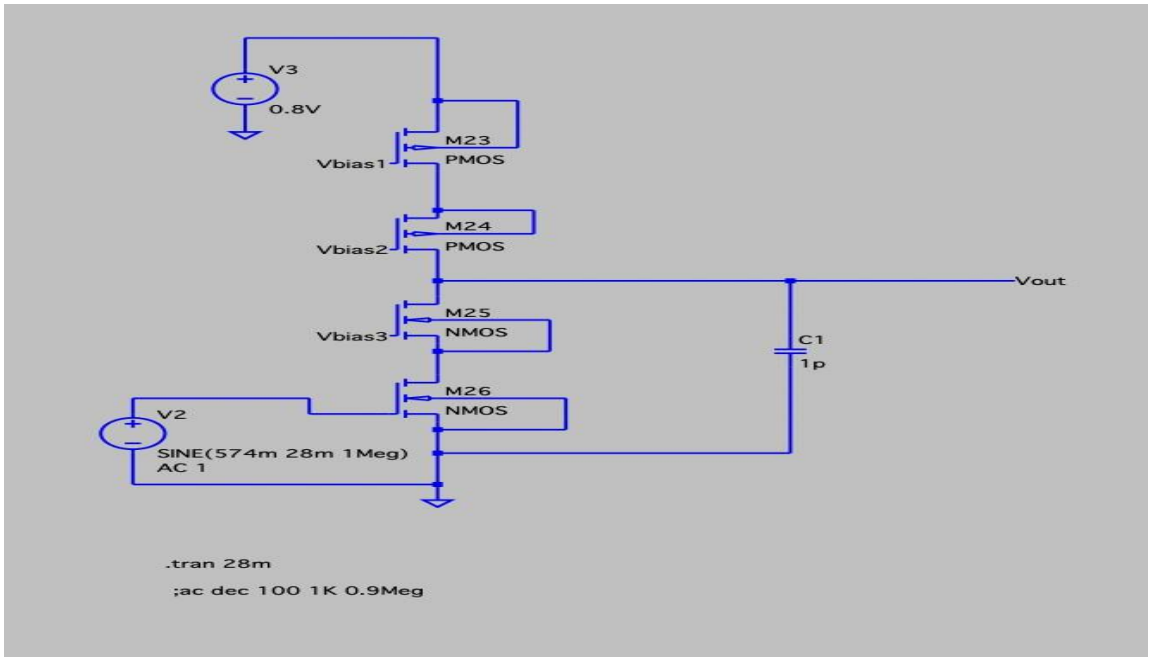
Beta Multiplier



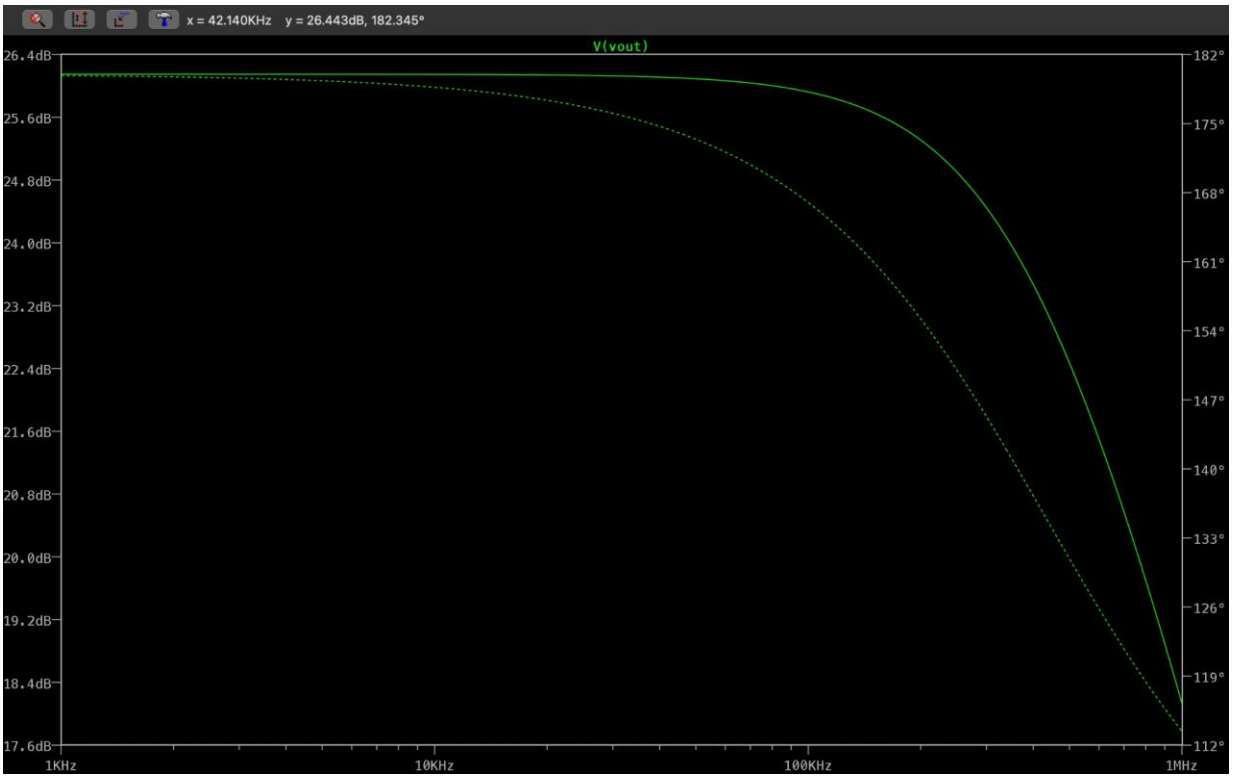
Current Mirror



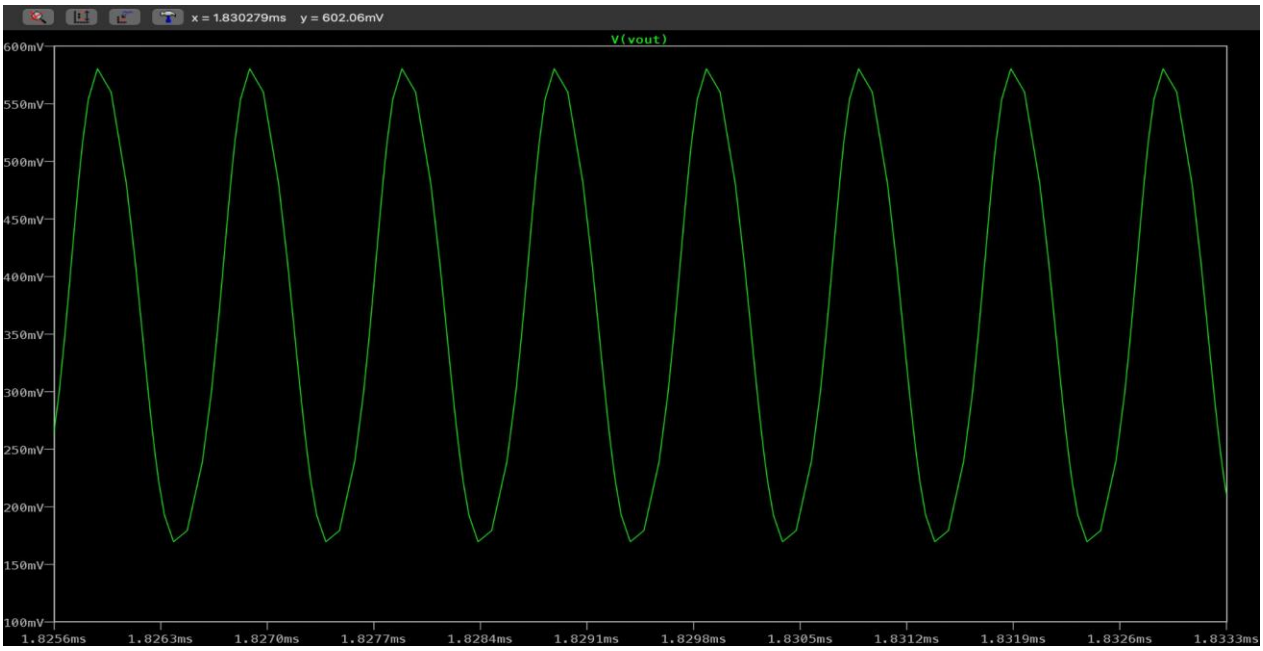
Cascode Amplifier



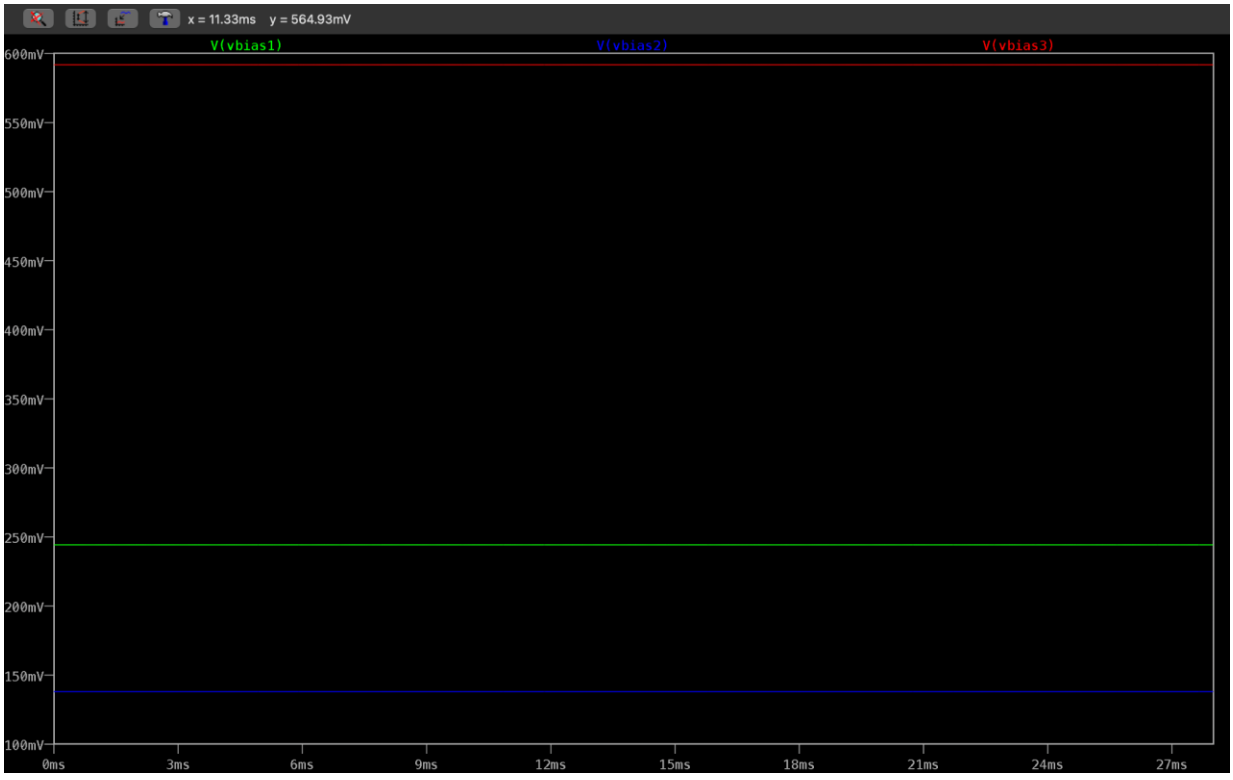
Bode plot:



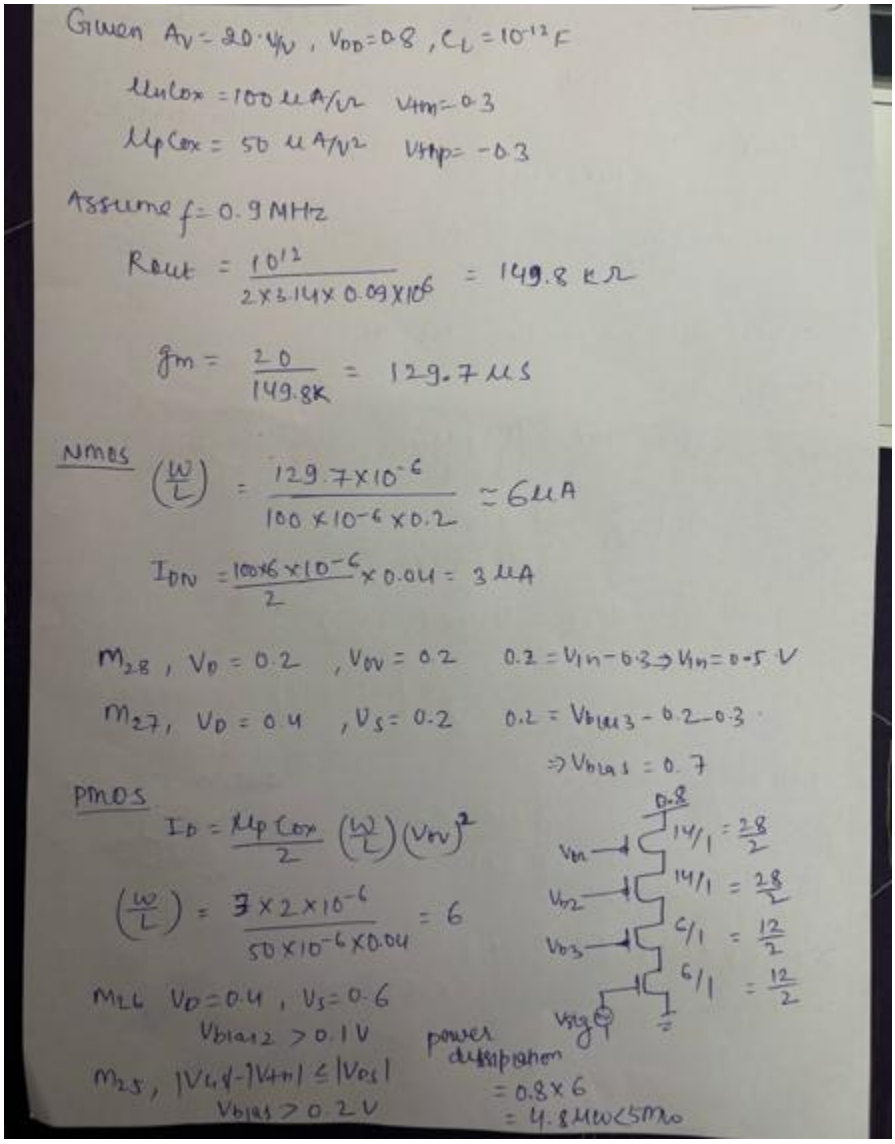
Vout:



Vbias 1 Vbias 2 Vbias 3 :



Observation and Calculations for 22nm :



Given $A_V = 20$ V/V, $V_{DD} = 0.8$, $C_L = 10^{-12}$ F

$\mu_n C_{ox} = 100\ \mu A/V^2$ $V_{thn} = 0.3$

$\mu_p C_{ox} = 50\ \mu A/V^2$ $V_{thp} = -0.3$

Assume $f = 0.9$ MHz

$$R_{out} = \frac{10^{12}}{2 \times 3.14 \times 0.09 \times 10^6} = 149.8\ K\Omega$$

$$g_m = \frac{20}{149.8K} = 129.7\ \mu S$$

NMOS

$$\left(\frac{W}{L}\right) = \frac{129.7 \times 10^{-6}}{100 \times 10^{-6} \times 0.2} \simeq 6\ \mu A$$

$$I_{DN} = \frac{100 \times 6 \times 10^{-6}}{2} \times 0.04 = 3\ \mu A$$

M_{28}, $V_D = 0.2$, $V_{OV} = 0.2$ $0.2 = V_{in} - 0.3 \Rightarrow V_{in} = 0.5$ V

M_{27}, $V_D = 0.4$, $V_S = 0.2$ $0.2 = V_{bias3} - 0.2 - 0.3$

$\Rightarrow V_{bias} = 0.7$

PMOS

$$I_D = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)(V_{ov})^2$$

$$\left(\frac{W}{L}\right) = \frac{3 \times 2 \times 10^{-6}}{50 \times 10^{-6} \times 0.04} = 6$$

M_{LL} $V_D = 0.4$, $V_S = 0.6$

$V_{bias2} > 0.1$ V

M_{25}, $|V_{tp}| - |V_{thn}| \leq |V_{DS}|$

$V_{bias} > 0.2$ V

power dissipation

$= 0.8 \times 6$

$= 4.8\ \mu W < 5\ \mu W$

Differences Between 180nm and 22nm Technology:

- Bias Voltages and Current: 22nm technology is better suited for applications requiring high densities since it runs at lower bias voltages and current levels than 180nm technology. This results in lower power consumption and a lesser danger of electrical overstress.
- Unity Gain Bandwidth (UGB): Compared to 180nm, 22nm technology offers a greater cutoff frequency and unity gain bandwidth.
- Transistor Density and Size: 22nm transistors are almost eight times smaller than 180nm transistors, which enables denser configurations and maybe better performance. But the smaller size makes the design more complicated, which might raise the cost of development.
- Power Consumption: 22nm technology is a good option for low-power applications, like portable and battery-powered devices, because its smaller transistors minimize leakage currents and demand lower operating voltages.

Applications and Suitability:

- 180nm Technology: Frequently utilized in analog, power, and mixed-signal applications where very high density and ultra-low power consumption are not essential.
- 22nm Technology: Preferred for digital circuits, high-speed processors, and applications that prioritize low power usage, high speed, and greater integration levels.

Conclusion:

Using LTSpice, the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier circuits were simulated in both 180nm and 22nm technologies for this project. The simulation findings met the intended performance benchmarks and were in good agreement with theoretical predictions. Magic was used to build layouts of the Cascode Current Mirror and Cascode Amplifier for 180nm technology. 180 nm and 22 nm were compared using LTSpice simulations and Magic layouts.

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