COMP3911 Suggested Exercises #1b

These suggested exercises are not to be handed in for marking, but should be used as a study aid. Solutions will be posted on the course website later in the term.

1) For the attached map of main memory and paging disk, create a page table for process P1. Then use this page table to show what happens when P1 attempts to access each of the following virtual addresses. (Do each case separately, *ie*.; do not assume changes caused by a) are there for b), c),...) The target architecture uses pure demand paging with a page size of 2048bytes, which implies a 11 bit page offset.

a) Read virtual address 0x2804
b) Modify virtual address 0x2244
c) Modify virtual address 0x1911
d) Read virtual address 0x1403
e) Modify virtual address 0x4f00
f) Read virtual address 0x5010

2) Given a TLB access time of 2 cycles and a memory (RAM) access time of 40 cycles, describe the fraction of time a TLB access takes, relative to the standard access if the TLB hit rate is:

a) 0.8
b) 0.95
c) 0.2
d) 0.05

3) How slow must the TLB be before no improvement is seen, if the TLB hit rate is 0.25 and a hardware memory access takes 25 cycles?

4) The following page reference strings were collected by a hardware monitor for a program running on an Acme computer system. (The Acme system is known to support a pure demand paging virtual memory subsystem.)

i) 0x7 0x6 0x7 0x8 0x9 0x7 ^ 0x8 0x7 0x8 0xa 0x8 ^ 0x8 0xa 0xb 0xb 0xc ^ 0x8 0x8 0xc 0xa 0xc ^ 0xa 0x7

ii) 0x1 0x1 0x1 0x1 0x1 ^ 0x1 0x1 0x2 0x3 0x4 ^ 0x5 0x2 0x3 0x4 0x5 ^ 0x2 0x3 0x4 0x5 0x2 ^ 0x3 0x4 0x5 0x2 0x3 ^ 0x4 0x5

iii) 0x1 0x2 0x3 0x4 0x5 0x6 0x1 0x2 ^ 0x3 0x4 0x5 0x6 0x8 0x9 0xa ^ 0x8 0x9 0xa 0x8 0x9 0xa 0x1 ^ 0x2 0x3 0x4 0x5 0x6

The tildes (^) indicate where the operating system cleared the Use bit on all frames in memory.

For a fixed page frame allocation of 3, simulate each of the following page replacement algorithms and count the number of page faults that occurs:

- FIFO
- LRU
- LFU
- Belady's optimal replacement
- Use Bit (falling back to FIFO)

5) What are the tradeoffs between using a small vs large page size in paged virtual memory systems?

6) If a machine that supports paged virtual memory is observed to be doing a lot of swapping, what change(s) should be made to the machine, in order to improve performance and why?

7) As the system manager of a web server, you have measured the following via "vmstat 5" and "uptime" running for an hour on three different occasions.

Average %idle CPU:	55	40	68
Load Average for hr:	0.85	1.6	0.45

(Remember that the "load average" is the average length of the CPU Run queue, which is the number of runable processes and that the CPU is idle when there are no runable processes.)

a) Does it look like an M/M/1 queue model would be appropriate for this server?

b) Customer service predicts a doubling in web traffic on the site after an updated web site is introduced next month and, in response to this, the boss suggests an upgrade on the server to the latest-generation CPU, which is 20% faster than the current one. What would your response to this suggestion be?

Page Table

	V	RO	D	U	Page Frame	Disk Addr
0x0						
0x1						
0x2						
0x3						
0x4						
0x5						
0x6						
0x7						
0x8						
0x9						
0xA						
0xB						
0xC						
0xD						
0xE						
0xF						

Main Memory

0x00	**P0-1 (RO)**	**P1-6**
0x02	**P5-4**	**P5-0**
0x04		**P1-5**
0x06	**P0-4**	**P5-F**
0x08	**P0-C**	**P2-1**
0x0A	**P5-1**	**PA-A**
0x0C	**P0-A**	**P1-3 (RO)**
0x0E	**PA-0**	**P0-8**
0x10	**P1-4**	**P1-E**
0x12	**P2-2**	**P4-2**
0x14	**P0-6**	**P2-0**
0x16	**P2-3**	**P0-2 (RO)**

Paging Disk