Soontech Annals

LC06: Stateless 10 Bit Double Dabble

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Tags: logic-and-computation, converter

Features

- Stateless, uses quasi-based logic
- Hopperspeed throughput

Applications

- Converting binary codes to decimal

General Description

The LC06 device converts binary to binary coded decimal (binary -¿ decimal) using the combinational double dabble algorithm. 17 gt per level. Input can be clocked 8gt.

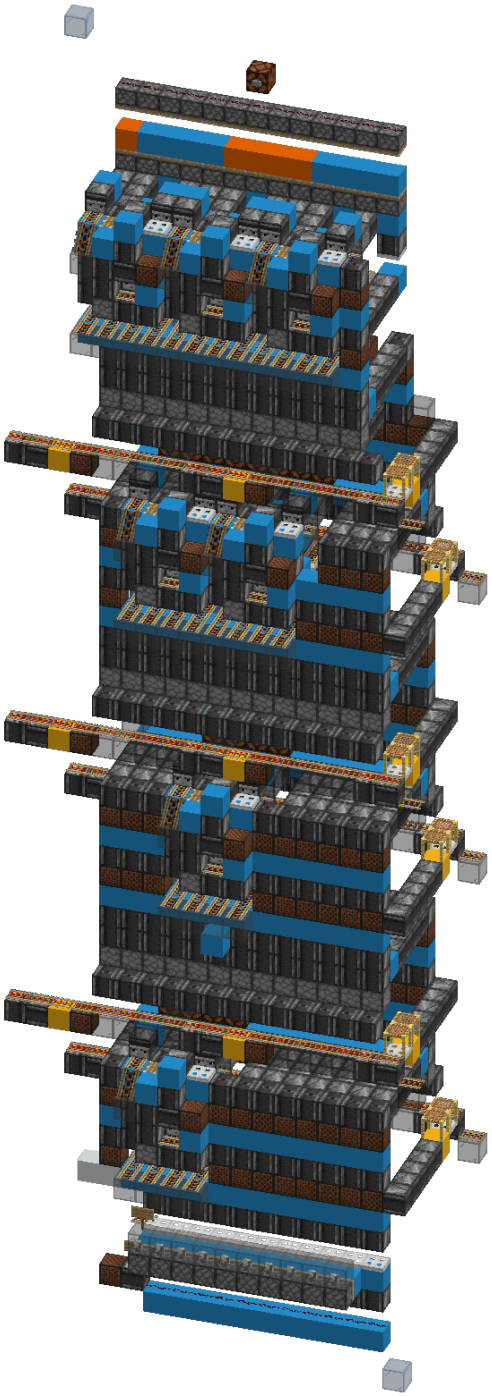

Figure 1: 10 Bit Double Dabble

Device Specifications

Table 1: Inputs

Name	Range	Description
Clock signal	Pulse	Executes converion algorithm with each pulse.
Binary input	10-bits	10 bit binary input to convert

Table 2: Outputs

Name	Range	Description
BCD Output	13-bits	Outputs in binary coded decimal

Table 3: Device Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Throughput	8	-	-	gt	Normal Usage
Latency	119	-	-	gt	From input to dropper activation.
MC Version	1.16	1.17.1	-	MCV	Latest version at time of writing: 1.19.3
Dimensions	11 x 60 x 19			Blocks	

Testing Data

Table 4: Executed Tests

Test	Result
Throughput test	Device was able to function with 8gt clocked input.

Download Information

Table 5: Download Information

Identifier	MC	File	Description
LC06	1.17.1	LC06_stateless_10bit_double_dabble.litematic	Schematic of device.