Soontech Annals

LC08: Precision Timings SIPO Register

By: Andrews54757
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Features

- Expandable, QC based "stateless" logic
- High precision timings support. Can discriminate order of signals sent in the same tick.

Applications

- Crackpot encoding mapping algorithm

General Description

The LC08 Precision Timings Serial Input Parallel Output (SIPO) Register seperates input signals by order of input. The device is capable of discriminating between signals sent in the same tick. The device is expandable, and can be used to decode crackpot encoding schemes.

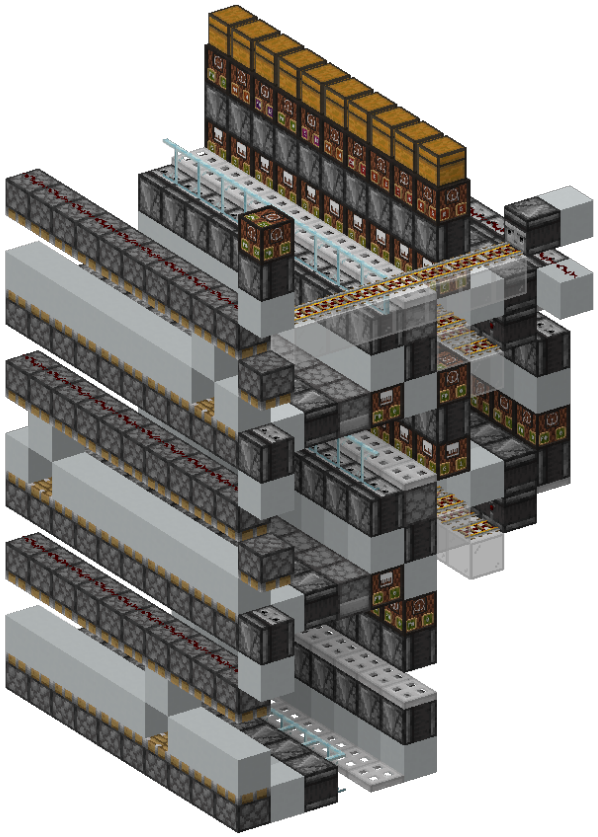

Figure 1: Precision Timings SIPO Register

Device Specifications

Table 1: Inputs

Name	Range	Description
Serial Input	Pulse	Noteblocks at the top
Reset	Pulse	Resets register

Table 2: Outputs

Name	Range	Description
Parallel Output	Pulse	Outputs at the bottom

Table 3: Device Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
MC Version	1.16	1.19.3	-	MCV	Latest version at time of writing: 1.20.4
Dimensions		16 x 22 x 14		Blocks	

Testing Data

Table 4: Executed Tests

Test	Result
SIPO test	Device was able to seperate signal order sent in same game tick.

Download Information

Table 5: Download Information

Identifier	MC	File	Description
LC08	1.19.3	LC08_Precision_Timings_SIPO_Register.litematic	Schematic of device.