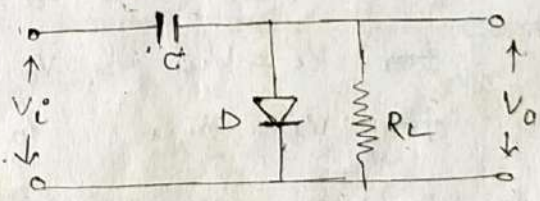
# Clamper circuit —

The clamper circuit (also known as a d.c. restorer) changes the d.c. voltage level of an input, but does not affect the shape of the waveform. The capacitor, diode and resistance are the three basic elements of the clamper circuit. Depending upon whether the positive d.c. or negative d.c. shift is introduced in the output waveform, the clampers are classified as,

a) Negative clampers (b) positive clampers

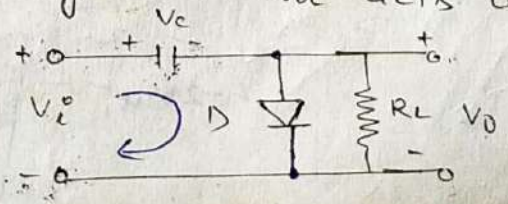
## Negative clamper —

A simple negative clamper which adds a negative level to the a.c. output, is shown below.




It consists of a capacitor C, the ideal diode D and the load resistance $R_L$. The time constt $\tau = RC$ is supposed to be very large by selecting large values of R and C.

During the first quarter of positive half cycle of $V_i$, the capacitor gets charged through forward biased diode D upto the maximum value $V_m$ of the input signal $V_i$. The capacitor charging is almost instantaneous which is possible by selecting proper values of $R_L$ & C. Capacitor once charged to $V_m$ acts as a battery.



Thus when D is ON, the output voltage $V_o = 0$.
As input voltage decreases after attaining its maximum value $V_m$ the capacitor remains charged to $V_m$ and diode D becomes reverse biased. Due to large RC time constant the capacitor holds its entire charge and capacitor voltage remains as $V_C = V_m$, output voltage $V_o = V_i - V_C = V_i - V_m$

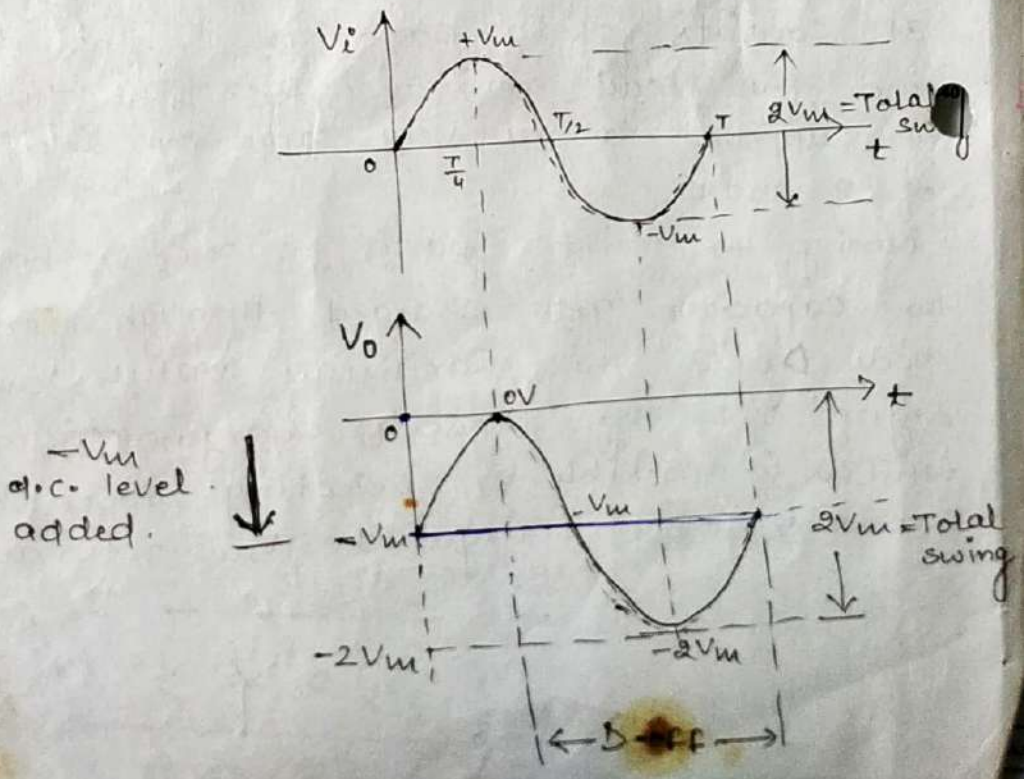
* In other words it is said as adding a negative d.c. level equal to $-V_m$ to the output.

In the negative half cycle the diode remains reverse biased. The capacitor start discharging through the load resistor $R_L$. As the time constant $R_L C$ is very large, it can be approximated that the capacitor holds all its charge, and remains charged to $V_m$ during this period also.

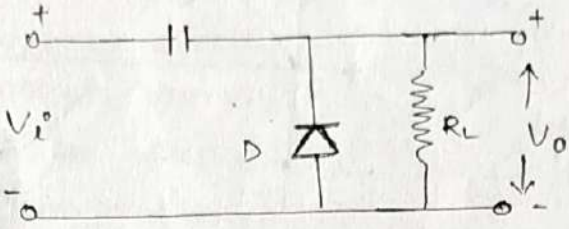
for $V_i = 0$, $V_o = -V_m$

for $V_i = V_m$, $V_o = 0$

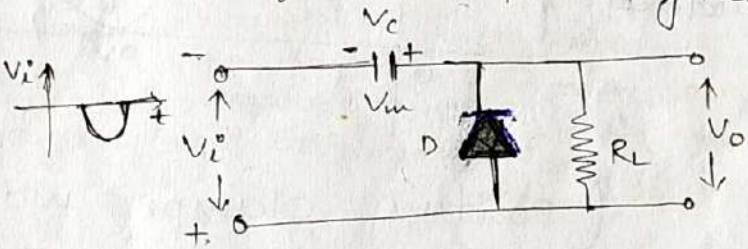
for $V_i = -V_m$, $V_o = -2V_m$



## Positive clamper —




During the negative half cycle of the input voltage $V_i$, the diode D gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value $V_m$ of the input signal $V_i$,




Under steady state conditions we can write

$$V_o = V_i + V_m$$

When $V_i = V_m$, $V_o = 2V_m$

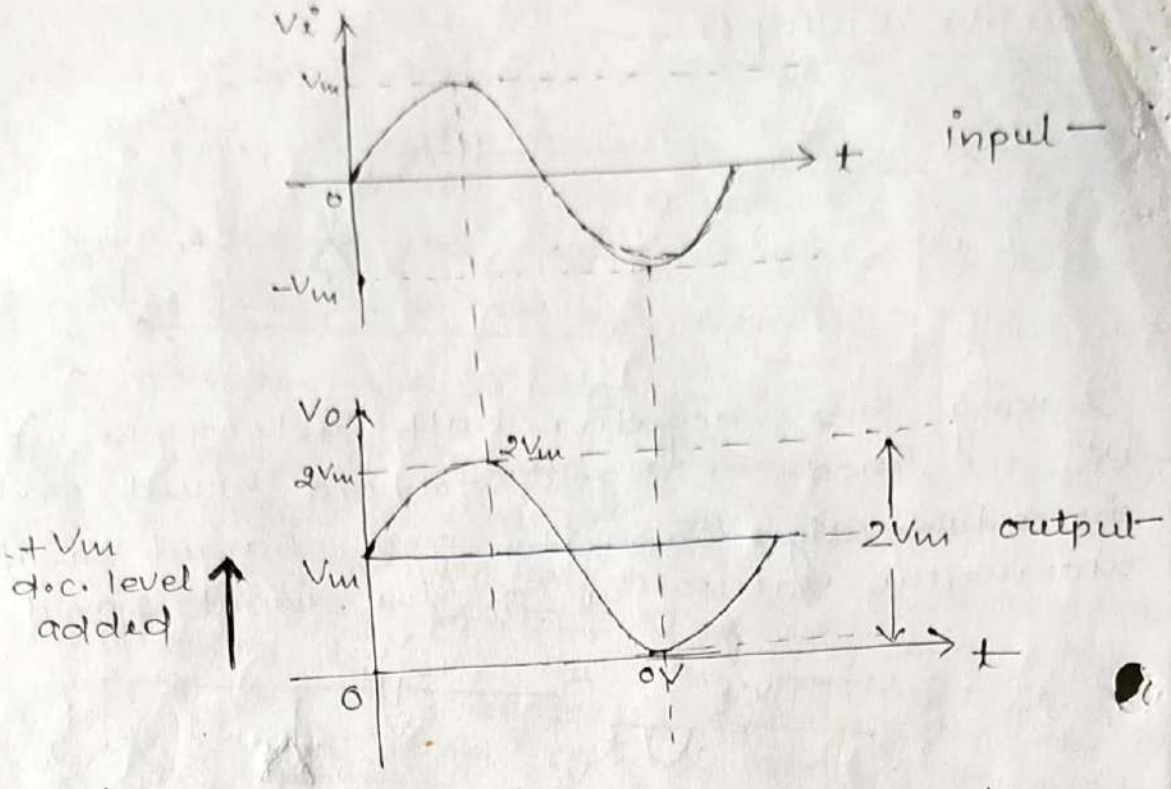
In the positive half cycle, the diode D is reverse biased. The capacitor starts discharging through $R_L$. The capacitor holds its entire charge all the times.

for $V_i = 0$ $V_o = V_m$

for $V_i = V_m$ $V_o = 2V_m$

for $V_i = -V_m$ $V_o = 0$

The input and output waveforms are shown below.



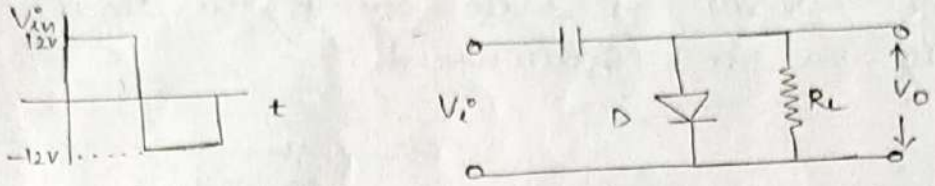

(positive clamper waveform)

* It can be remembered that the total output swing is always equal to the total input swing.

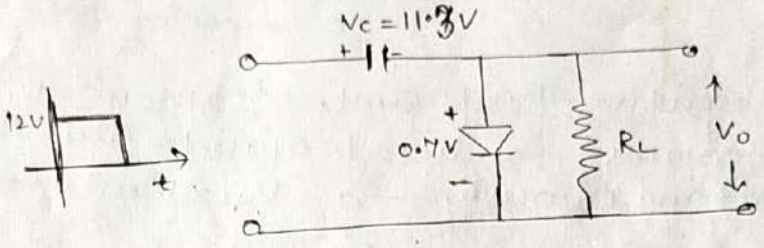
* The function of $R_1$ is to gradually discharge the capacitor over the several cycles of input waveform, so that it can be charged to a new voltage level if the input changes.

* The difference between clipping and clamping ckt is now apparent. While the clipper clips off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak to a desired d.c. level.

P.1 — Sketch the output voltage waveform for the ckt. given below, assuming large time constt and silicon diode ($V_\gamma = 0.7V$).




Soln → For positive half cycle of the input, the equivalent ckt. with polarities and potentials are

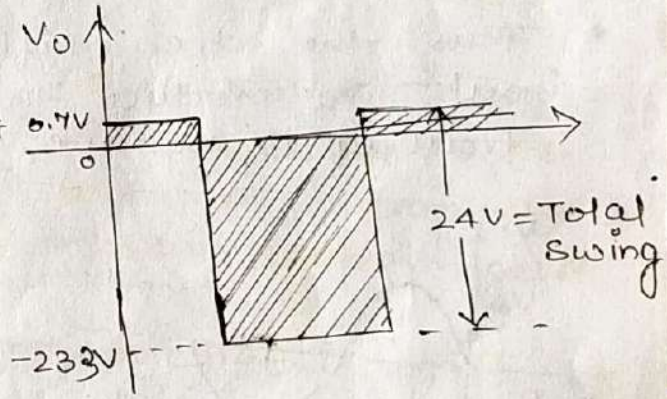



$V_o = V_{in} - V_c = V_{in} - 11.3\ V$

Thus when $V_{in} = 12V$, $V_o = 0.7\ V$

and when $V_{in} = -12V$, $V_o = -23.3\ V$

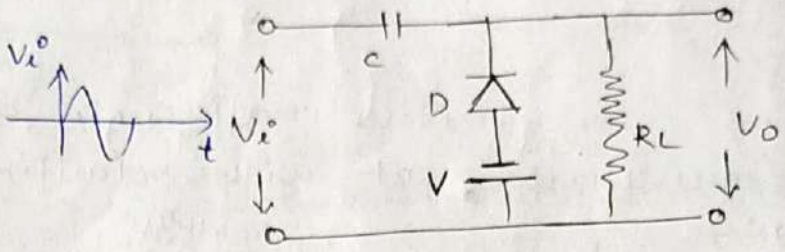
The output voltage waveform is shown below



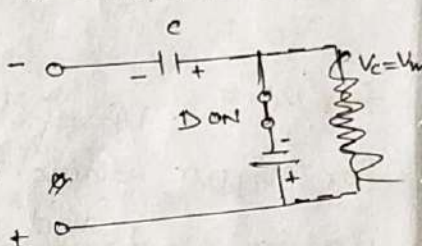

Thus the circuit adds a d.c. level of -11.3V to the input.

## Addition of battery in clamper :—

The shape of the output can be controlled by adding additional voltage supply in series with the diode with the polarity as per requirement.




In the negative half cycle. When $V_i < V$, the diode becomes forward biased. The capacitor gets charged instantaneously to $V_m - V$ as shown below




Thereafter capacitor retains its charge all the time and its voltage remains at $V_c = V_m - V$

Applying KVL to the circuit—

$$+V_c - V_o + V_i = 0$$

or $$V_o = V_i + V_c = V_i + (V_m - V) \quad \text{--- (1)}$$

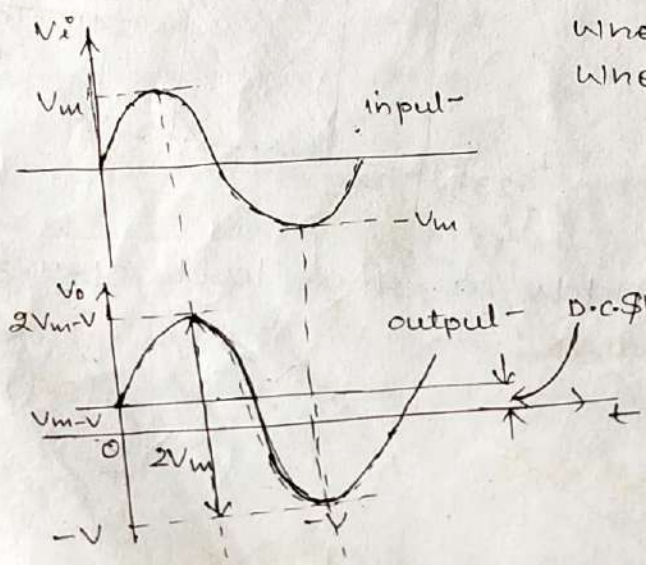
* Thus the d.c. shift of $V_m - V$ gets added to the input to produce the output.

from eqn (1) we have

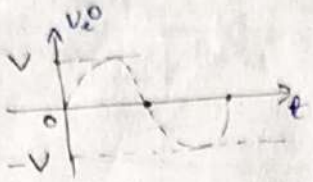
when $V_i = +V_m$, $V_o = 2V_m - V$

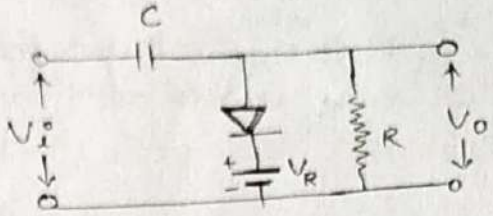
when $V_i = 0$, $V_o = V_m - V$

when $V_i = -V_m$, $V_o = -V$



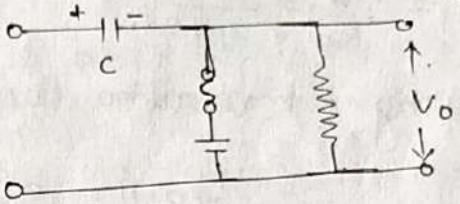
Ex: Draw the output waveform for the ckt shown below.




$RC \geq 10T$

Soln: Assuming ideal diode, during the positive half cycle of input, when $V_i > V_R$, the diode is forward biased and C gets charged to $(V_i - V_R)$ as shown



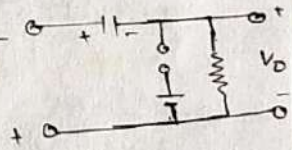

$V_o = V_i - V_C = V_R$

for $V_i = V$ , $V_o = V_R$

for $V_i = 0$ , $V_o = -V_C = -(V - V_R)$

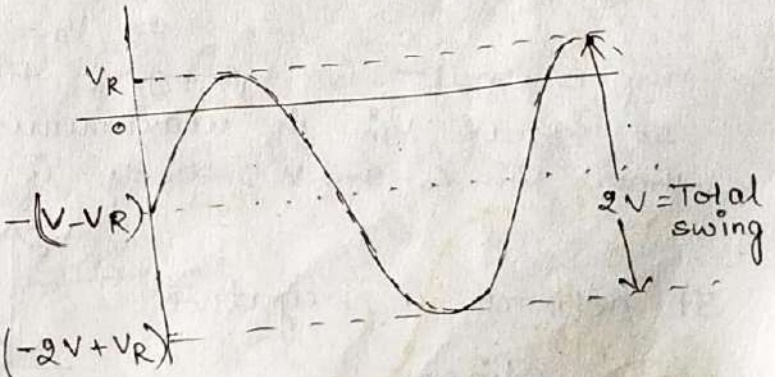
During negative half cycle, the capacitor hardly discharges through R as $RC \gg 10T$. Thus it remains charged at $(V - V_R)$ with same polarity. And

$V_o = -V_i - (V - V_R)$

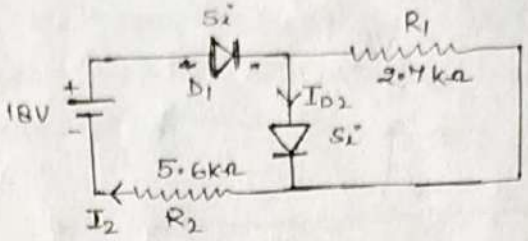



for $V_i = -V$ , $V_o = -2V + V_R$

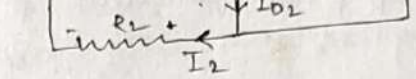
for $V_i = 0$ $V_o = -(V - V_R)$



P-2. Determine the currents $I_1$, $I_2$ and $I_{D_2}$ for the network shown below.




Due to 18V supply, both $D_1$ and $D_2$ are forward biased and conducting. The drops across $D_1$ and $D_2$ are 0.7




$$V_A = 0.7$$

$$I_1 = \frac{V_A}{R_1} = \frac{0.7}{2.7 \times 10^3} = 0.259 \text{ mA}$$

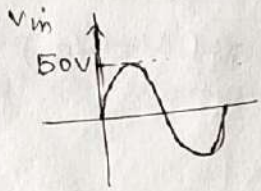
Applying KVL to loop.

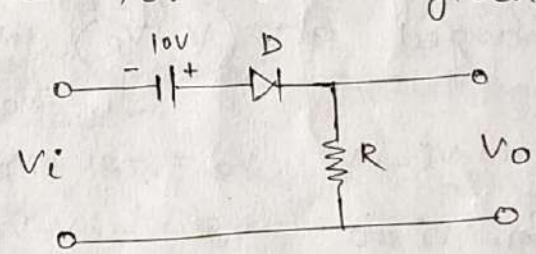
$$-0.7 - 0.7 - I_2(5.6 \times 10^3) + 18 = 0$$

$$\text{or} \quad I_2 = 2.96 \text{ mA}$$

$$I_{D_2} = I_2 - I_1 = 2.701 \text{ mA}$$

P-3 — Sketch the output for the ckt. given bel



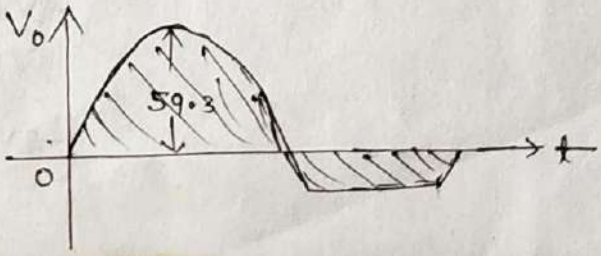

Due to battery diode is forward biased So $V_O = V_{in} + 10 - 0.$

$$\text{or} \quad V_O = V_{in} + 9.3V$$

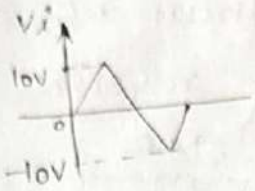
The output is $V_{in} + 9.3V$ till the $V_{in}$ reduces to $-9.3V$ so when $V_{in}$ in maximum $V_O = 50 + 9.3 = 59.3V$

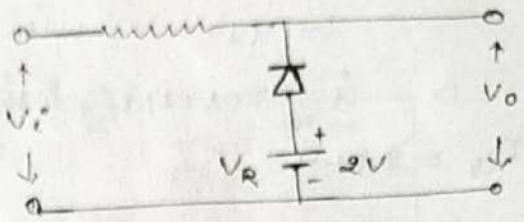
When $V_{in} < -9.3\,V$, diode is reverse biased, $V_O = 0$ for $V_i >$

It acts as a negative clipper

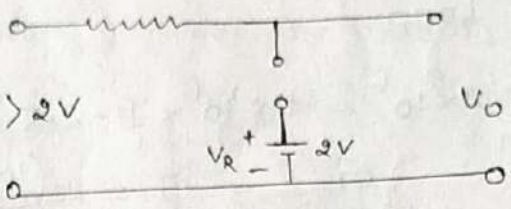


-4- Determine $V_o$ for the network shown below.

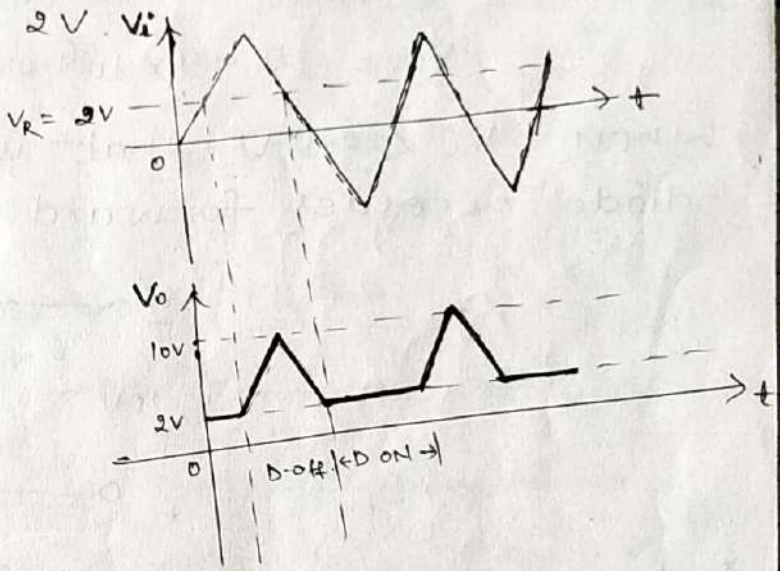


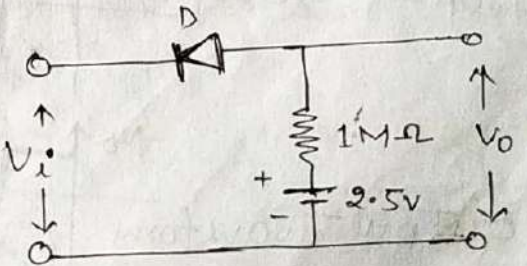

When $V_i > 2V$, the diode is reverse biased, $V_o = V_i$




for $V_i \leq 2V$, $V_o = 2V$

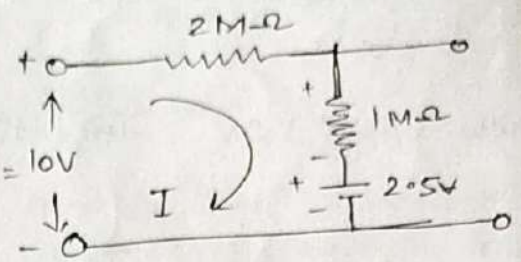



P. 5 — A symmetrical 5KHz square wave varying between +10V and -10V is impressed upon the clipping ckt. shown below. Assuming $R_f = 0\Omega$, $R_r = 2M\Omega$ and $V_\gamma = 0V$. Sketch the steady state output waveform.



Soln.:

When $V_i$ is greater than 2.5V, the diode D is reverse biased with reverse resistance $R_r = 2\,M\Omega$.



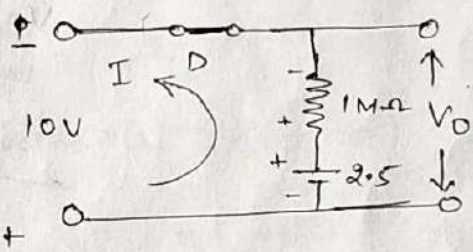

Applying KVL to the loop

$$-I \times 2\times10^6 - 1\times10^6 \times I - 2.5 + V_i = 0 \qquad (\text{as } V_i = 10\,V)$$

or $$I = \frac{(10-2.5)}{3\times10^6} = 2.5\,\mu A$$

$$V_o = I \times 1\times10^6 + 2.5 = 5V$$

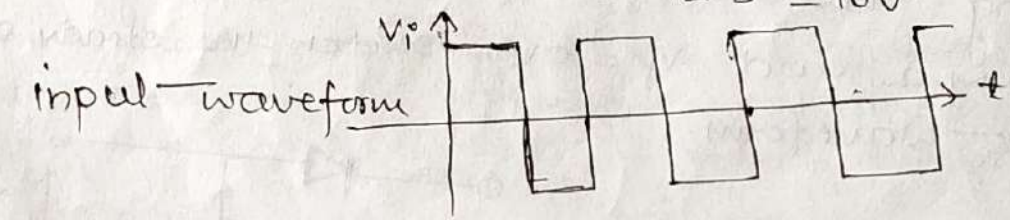
When $V_i < 2.5\,V$ that is equal to $-10\,V$, the diode becomes forward biased



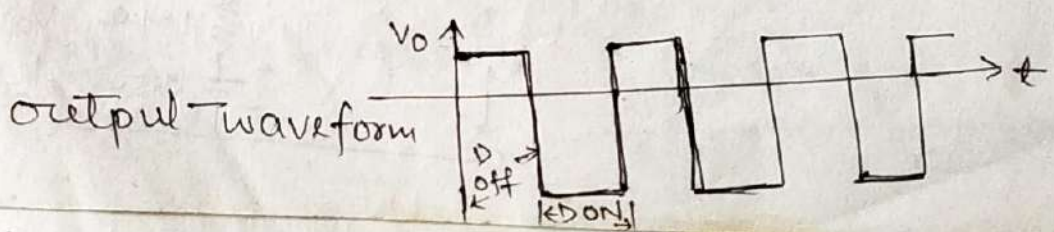

Applying KVL $\quad -I \times 1\times10^6 + V_i + 2.5 = 0$

or $$I = \frac{10+2.5}{1\times10^6} = 12.5\,\mu A$$

$$V_o = 2.5 - I \times 1\times10^6 = 2.5 - 12.5 = -10V$$

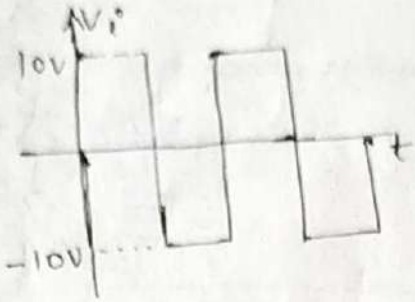


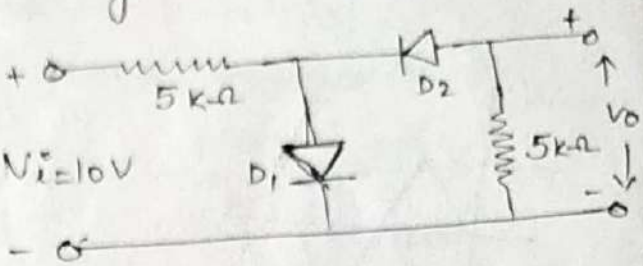

input waveform




output waveform

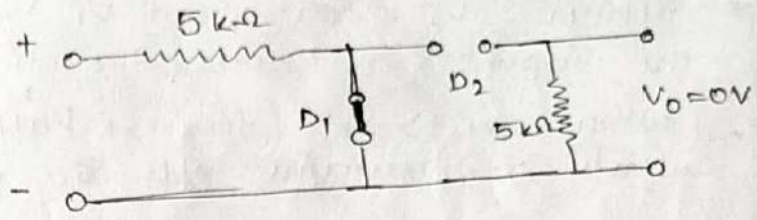
2.6 — Sketch the output voltage $V_o$ for the ckt shown below, assuming ideal diodes used.



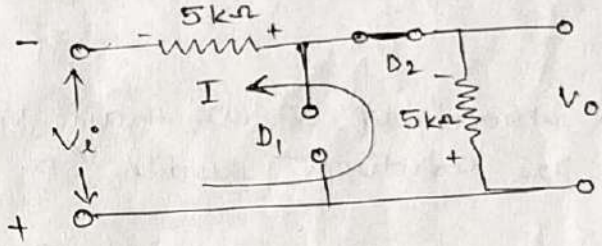

Soln. for positive half cycle, diode $D_1$ is forward biased and diode $D_2$ is reversed biased. Hence

$V_o = 0V$



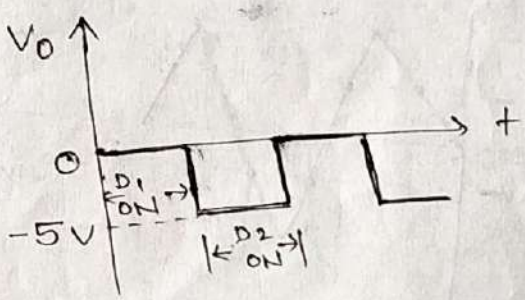

When $V_i = -10V$, the diode $D_2$ is forward biased and $D_1$ is reversed biased. Applying KVL to the loop

$$I = \frac{V_i}{(5+5)\times 10^3} = \frac{10}{10\times 10^3} = 1mA$$

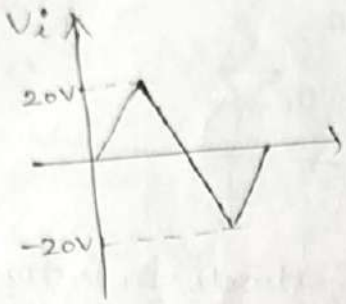


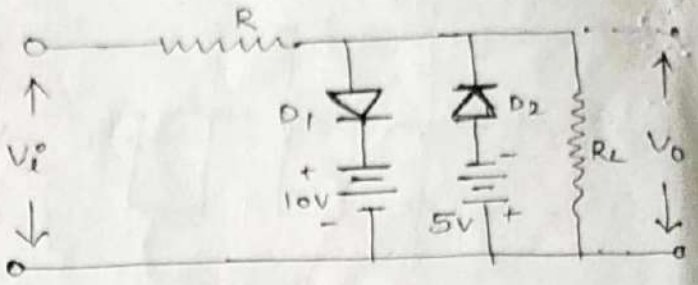

$\therefore V_o = -5\times 10^3 \times 1mA = -5V$

output-wave form

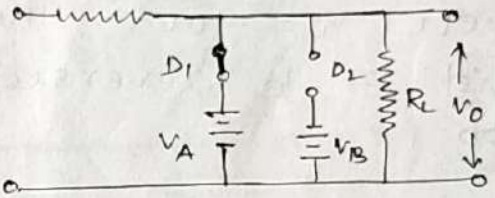


P-7 — Draw the output waveform for the circuit shown below.

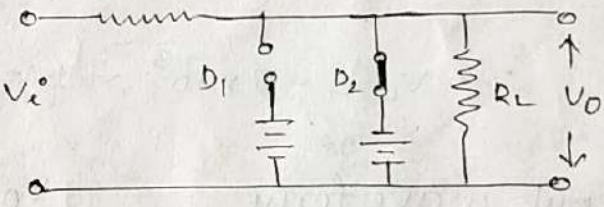


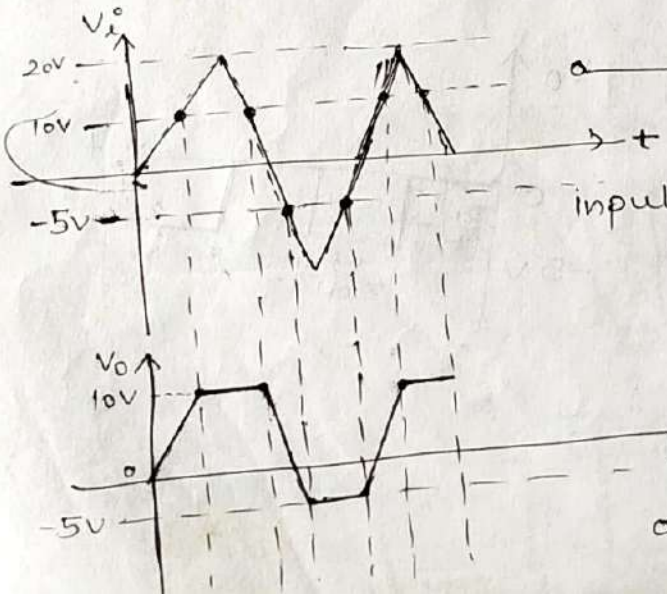




* When $V_i < 10V$ and $V_i > -5V$, the output follows the input as both the diodes remain reverse biased
* When $V_i > V_A$ (for +ve half cycle) the diode $D_1$ conducts while $D_2$ remains off. So $V_O = V_A = 10V$




* When $V_i$ is less than $V_B$ (for -ve half cycle), the diode $D_2$ conducts while $D_1$ remains off. Thus $V_O = V_B = -5V$



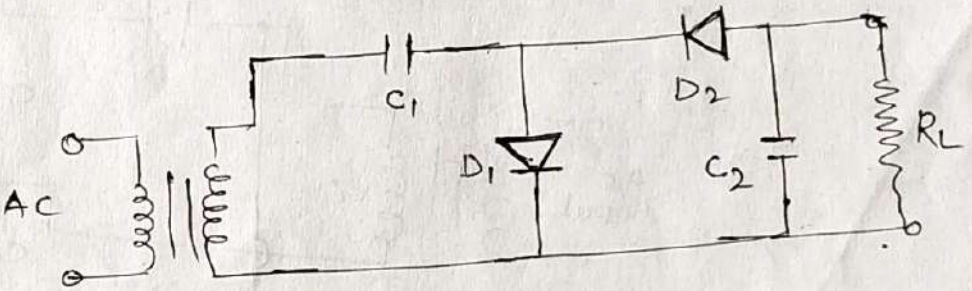



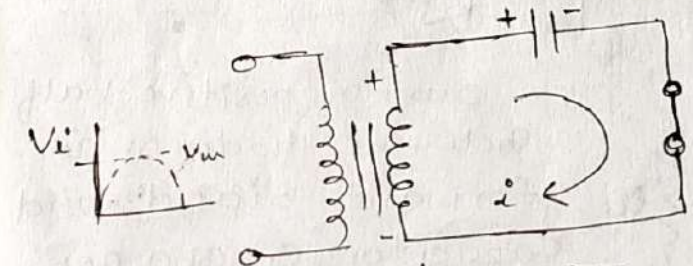
## Voltage Multipliers.

A voltage multiplier is a rectifier circuit that gives a d.c. output voltage approximately equal to a multiple of the peak input a.c. voltage. The voltage multipiers provide an inexpensive method of obtaining high voltages required to accelerate the electron beam in Cathode ray tubes. They are also used in electronic voltmeters to convert the ac being measured to a proportional d.c. voltage which can be indicated by the d.c. meter. The advantage of the circuit is that it can produce a high output voltage avoiding the use of bulkier transformer. The various voltage multiplier circuits are

(a) voltage doubler (b) voltage tripler (c) voltage quadrupler

### (a) Half wave voltage doubler.



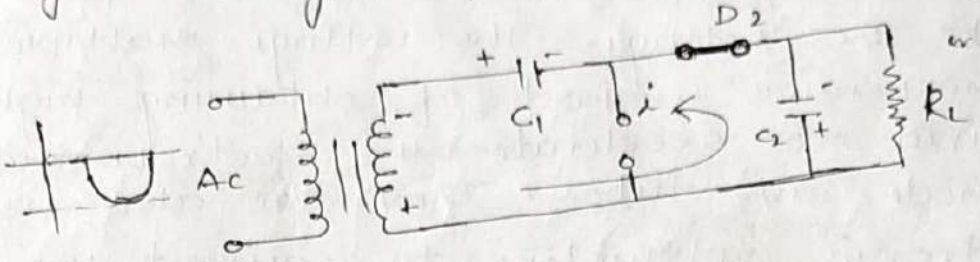




During positive half cycle of $V_i$, $D_1$ will be forward biased and the diode $D_2$ will be reverse biased. The capacitor $C_1$ get charged equal to $V_m$. As $D_2$ is reverse biased, next part of the ckt remains disconnected.

for negative half cycle of the input the diode $D_1$ will be reversed biased and the diode $D_2$ will be forward biased. So the capacitor $C_2$ will get charged equal to $2V_m$.

$-V_m - V_{C_1} + V_{C_2} = 0$

$\Rightarrow V_{C_2} = 2V_m$

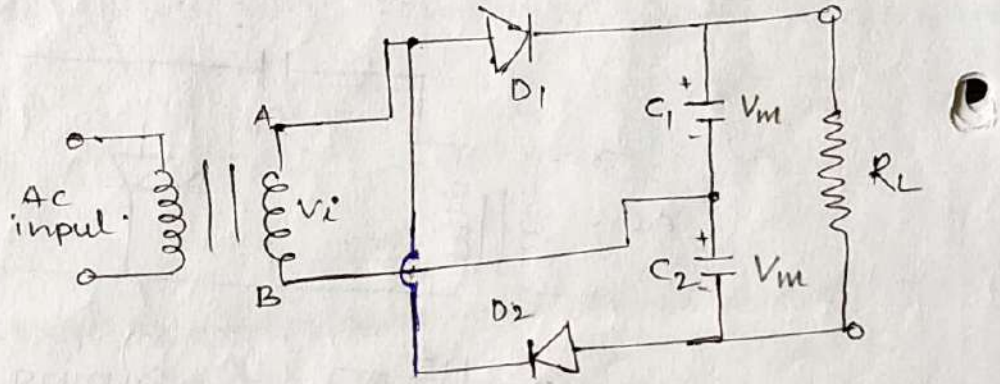


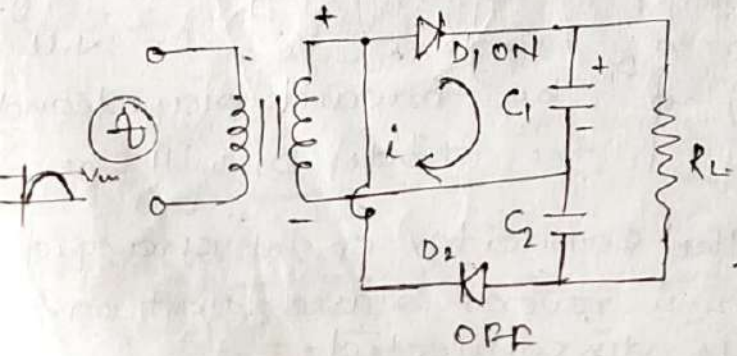

The capacitor $C_2$ charges equal to $2V_m$ as the voltage $V_m$ on $C_1$ adds to the input voltage. The capacitor $C_1$ retains its voltage $V_m$ all the time, once charged.

$$V_{C_2} = V_m + V_{C_1} = V_m + V_m = 2V_m$$

As capacitor charges in alternate half cycle the circuit is called half wave doubler.

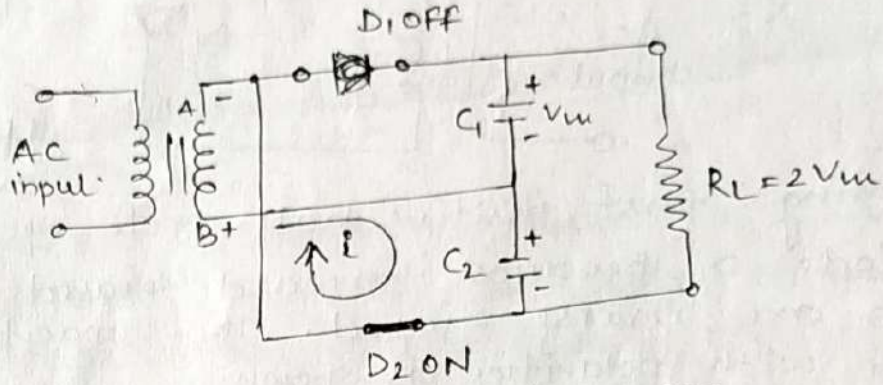
## Full wave doubler circuit —




During positive half cycle the diode $D_1$ is forward biased and capacitor $C_1$ charges equal to $V_m$

In the negative half cycle, the diode $D_2$ is forward biased while the diode $D_1$ is reverse biased. The capacitor $C_2$ gets charged equal to $V_m$ with the polarity as shown.



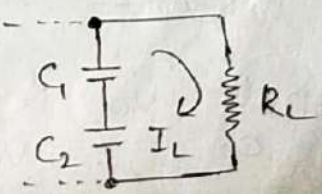

The voltage rating of the ~~transistor~~ capacitors $C_1$ and $C_2$ is $V_m$ while the PIV rating of the diodes $D_1$ and $D_2$ is $2V_m$.

The output is taken across 2 capacitors in series is $V_o = V_{C_1} + V_{C_2} = V_m + V_m = 2V_m$

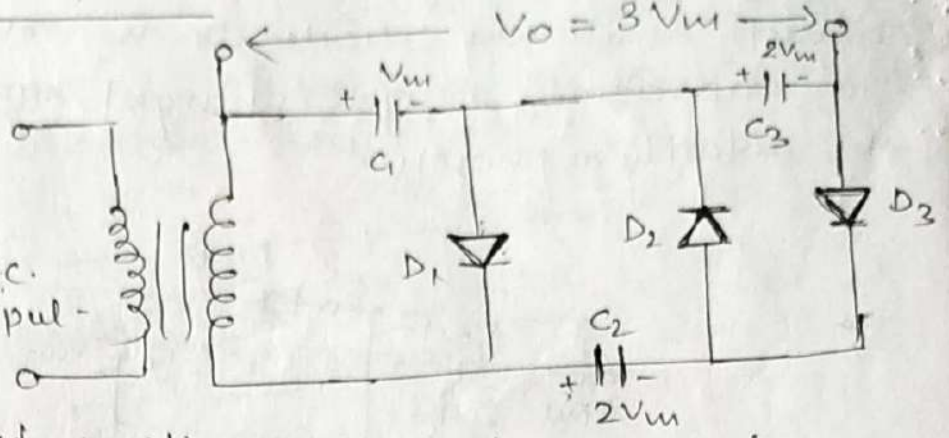
Why regulation is poor $\longrightarrow$ When load is connected, capacitors start discharging through the load and capacitor voltages start discharging.

Equivalent capacitance $= \frac{C_1 C_2}{C_1 + C_2}$

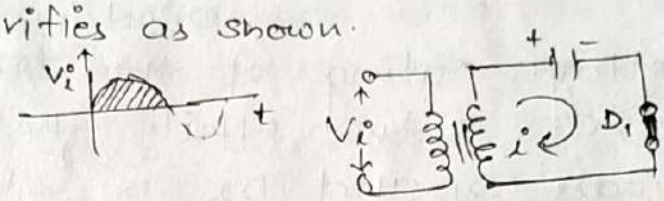
This value is less than individual value of $C_1$ and $C_2$. The ripple factor is inversely proportional to the value of filtering capacitor. Thus ripple factor increases which indicates that ripple content in the output increases as filtering action is poor.



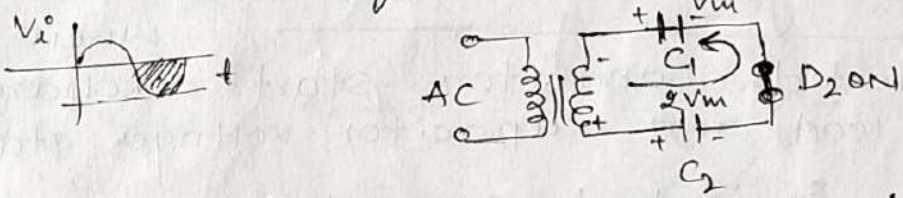
# Voltage Tripler



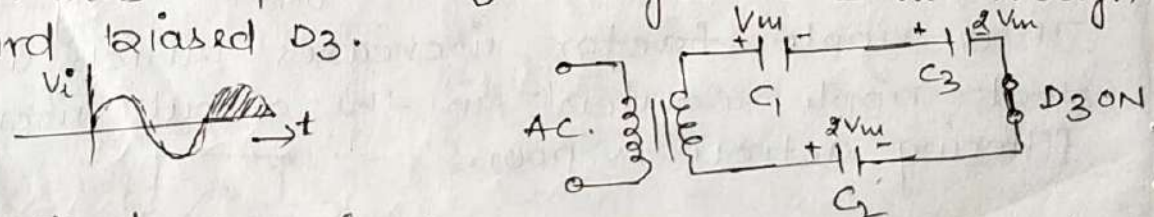

During first positive half cycle of the input, the diode $D_1$ becomes forward biased while $D_2$ and $D_3$ are reverse biased. The capacitor $C_1$ charges to $V_m$ with polarities as shown.




During negative half cycle of the input, the diode $D_2$ is forward biased. The capacitor $C_1$ holds its entire charge and voltage remains at $V_m$. Hence the capacitor $C_2$ charges to $2V_m$.

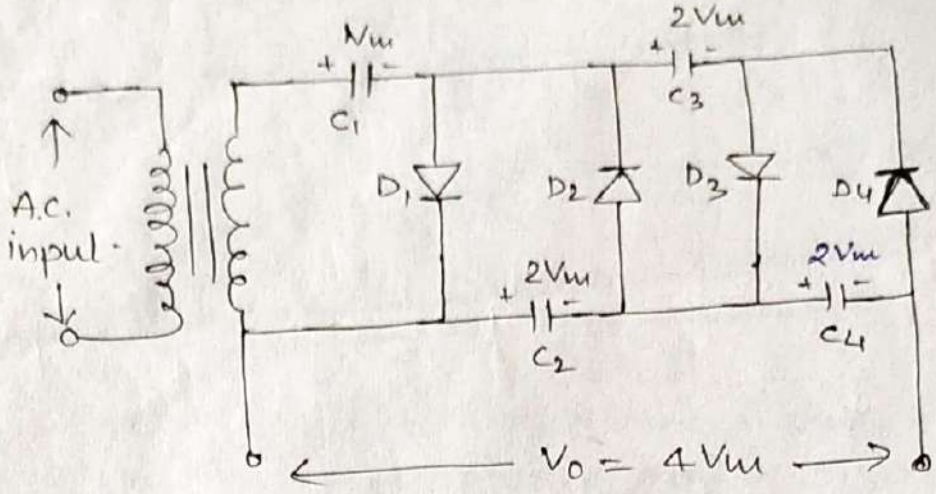



for the next positive half cycle of the input the diode $D_3$ is forward biased as $C_2$ remains its charge and voltage to $2V_m$ while $C_1$ retains its voltage to $V_m$. The diode $D_1$ and $D_2$ are reverse biased. Thus capacitor $C_3$ charges to $2V_m$ through forward biased $D_3$.




The output $V_o$ is taken across the capacitors $C_1$ and $C_3$ $\therefore V_o = V_{C_1} + V_{C_3} = V_m + 2V_m = 3V_m$

## Voltage Quadrupler —




* The multipliers are used in applications like television receivers and cathode ray tube anode voltage.

* The ripple also increases according to the increased load current. The voltage regulation becomes more poor and poor. Hence these ckts are useful in very low current applications only.