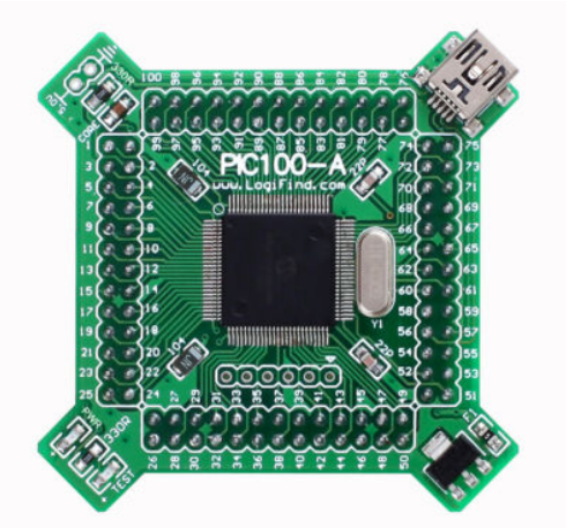
PIC24FJ128GC010



- Analog
  - 12 bit ADC
    - Upto 50 channels pipeline
    - Conversion rate = **10Msps**
    - Conversion available in sleep and idle
  - 16 bit Sigma-Delta ADC
    - Programmable data rate
    - 2 differential channels
  - 10 bit DAC
    - 2 channels
    - 1 Msps
  - 2 General Purpose Operational Amplifiers: Bandwidth = 2.5 MHz
  - 3 Comparator
- Low current consumption
  - WDT: 270nA
  - RTCC: 350nA @ 32 kHz
  - Deep sleep: **75 nA**

Device	Memory		Pins	Analog Peripherals						Digital Peripherals							LCD Controller (pixels)	USB OTG	Deep Sleep w/V_{BAT}
	Program Flash (bytes)	Data RAM (bytes)		12-Bit HS A/D (ch)	16-Bit ΣΔ A/D (diff ch)	10-Bit DAC	Op Amps	Comparators	CTMU (ch)	Input Capture	Output Compare/PWM	I^2C	SPI	UART w/IrDA®	EPMP/PSP	16-Bit Timers			
PIC24FJ128GC010	128K	8K	100	50	2	2	2	3	50	9	9	2	2	4	Y	5	472	Y	Y

- Peripheral
  - Supply voltage = (2, 3.6)V
  - **5.5V** tolerant input pins
  - High Current on I/O pins = 18 mA
  - 2 voltage regulators = 1.8 V and 1.2 V
  - Configurable open drain output on digital pins
  - **USB V2.0** Speed = (1.5Mbps, 12Mbps)
  - Serial communication
    - **2 SPI** modules
    - **4 UART** modules
    - **2 I2C** modules
  - CPU
    - Harvard Architecture
    - Upto 16 MIPS
    - C compiler instruction set