FPGA Based Digital Camera

Ryan Henderson

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Digital Imaging

- Real time video capture
- CMOS Image Sensor
- FPGA
- External Memory
- PC or Monitor Display
- Image Sensor Evaluation Kit

Presentation Overview

- External Hardware
  - Image Sensor
  - XSA-100
- Host PC Software
  - Save Pictures as JPG / BMP
  - Control Image Sensor
- FPGA Design
  - Parallel Port
  - Master Control
  - Memory Control
  - SDRAM
  - I2C
  - Image Sensor Data Reader

External Hardware

FPGA Based Digital Camera

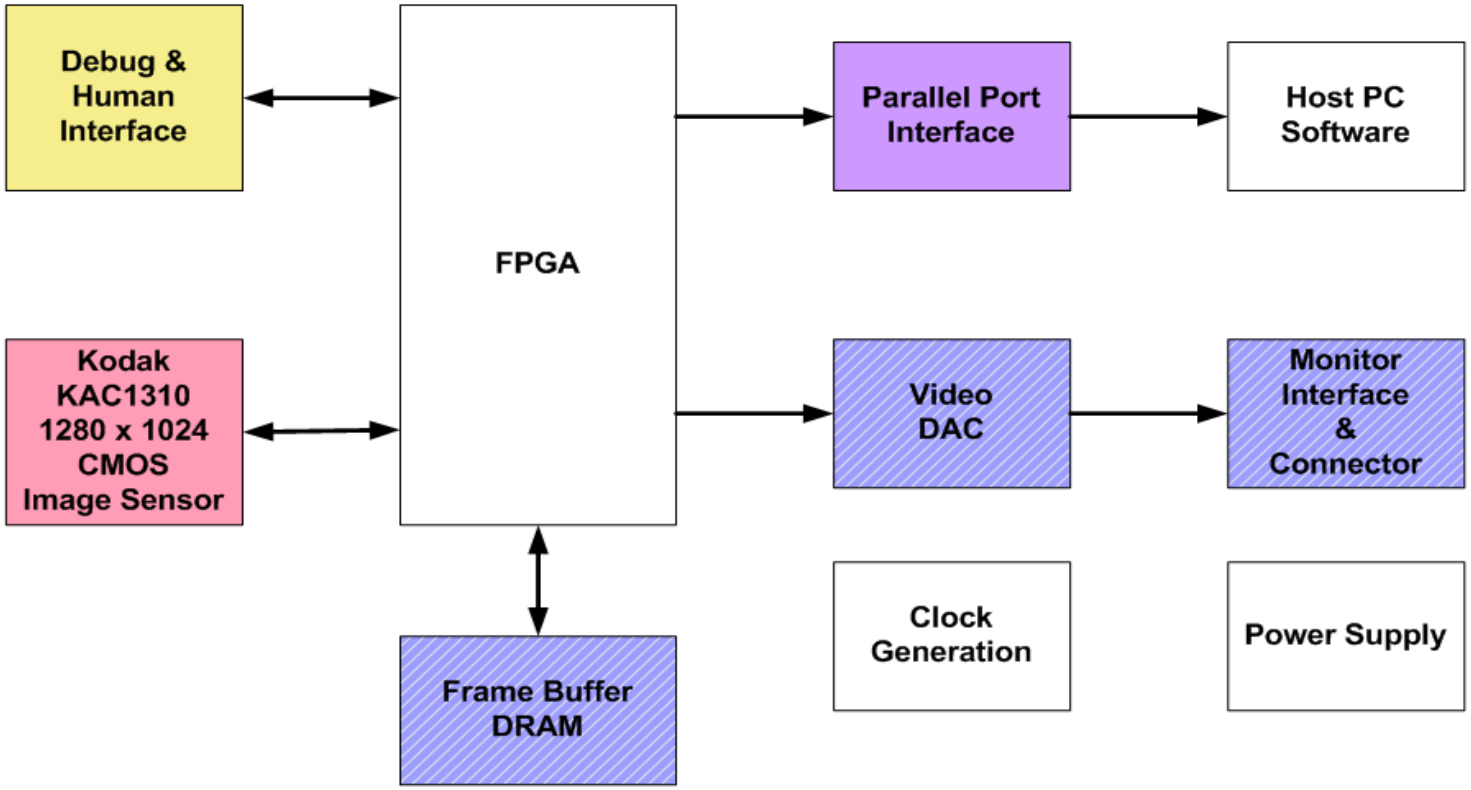

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Image Sensor

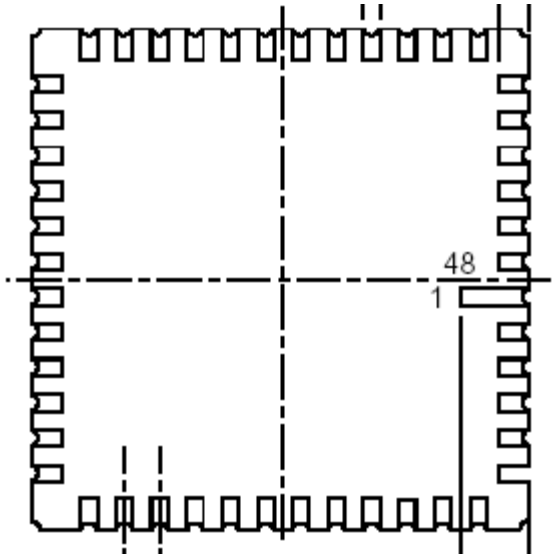
- Motorola ImageMOS ™ MCM20027
- Kodak Digital Science ™ KAC – 1310

Image Sensor Features

- 1280 x 1024 Pixels Resolution
- Continuous / Single Shutter Modes
- 10-bit, RSD ADC Analog to Digital Converter
- 48-pin Ceramic LCC Package
- Digitally Programmable via I2C Interface
- 10/15 fps full SXGA at 13/20Mhz Master Clock Rate
- Bayer-RGB Color Filter Array
- 3.3V Analog and 3.3V Digital at 250mW Operation
- Camera on a Chip

Feature Notes

- 1280 x 1024 x 10bits x 15fps = 196 608 000 Mbps
- Sub sample and window of interest (WOI)
- Surface mount Leadless Chip Carrier



Plastronics Socket

- Zero insertion force
- Strange bottom pin out
- Required adaptor to .1” hole spacing
- Only socket available under $250

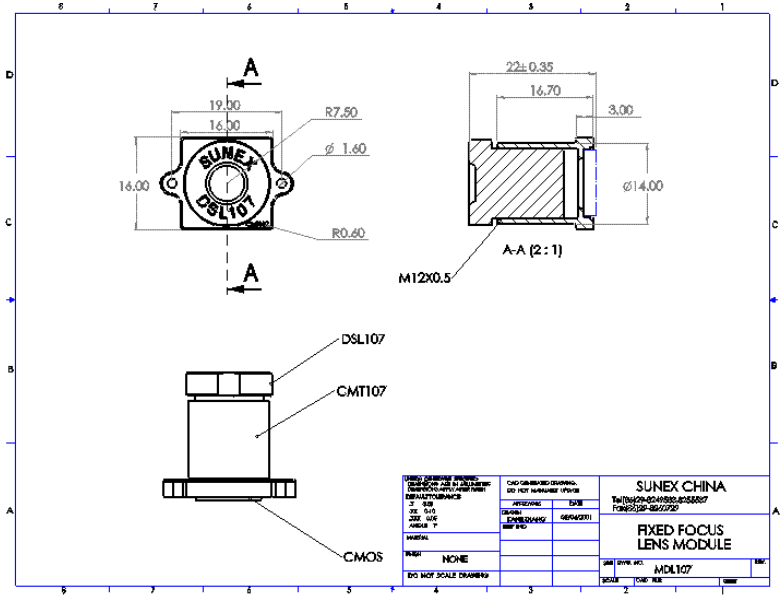
leadless chip carrier

LCC

Drilling adaptor with CNC Mill

Sunex Lens

- Blurry image without lens
- Matches
  - F stop
  - Focal Length
  - Center of Sensor
- Plastic



Bayer RBG Color Microlenses

- Twice as many green pixels
- Combine set of 4 to get RGB value

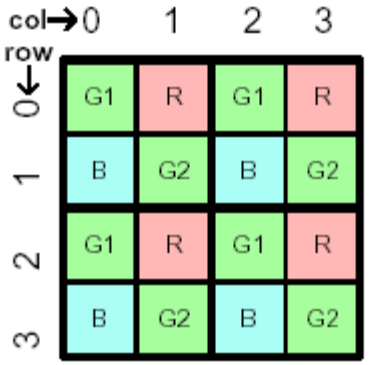


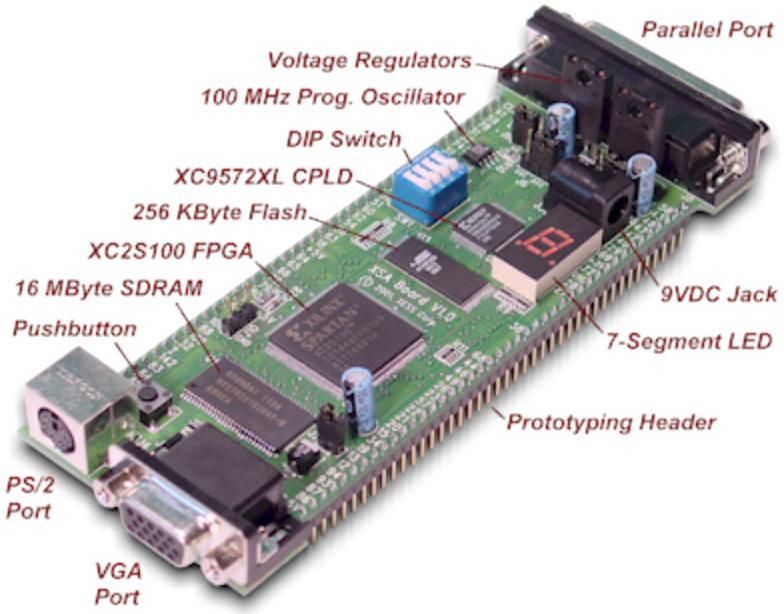
Figure 6 - Optional Bayer RGB Pattern CFA

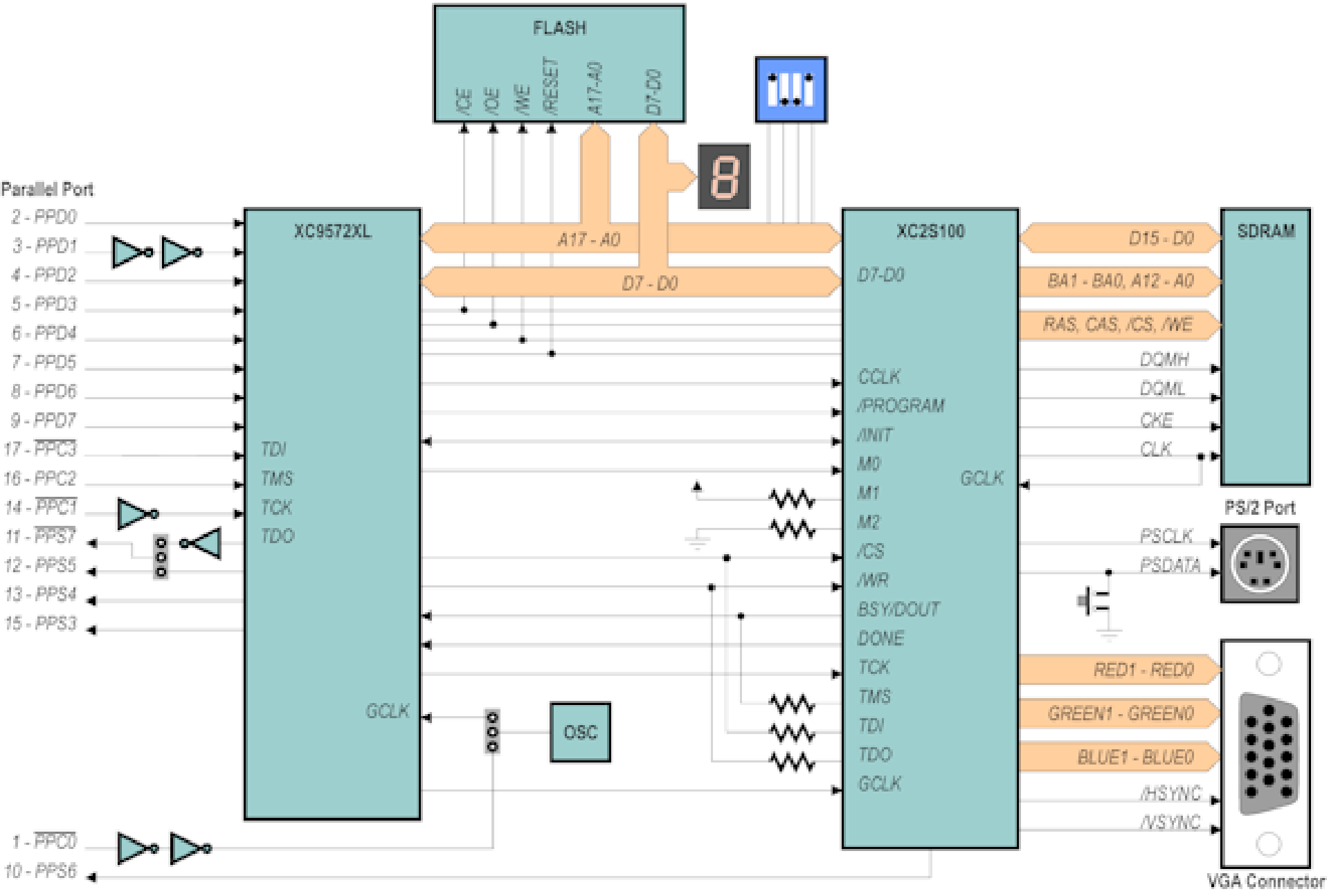
Control Registers

- 41 8-bit Registers
- Analog adjustment
  - Exposure, white balance etc
- Digital functions / sensor interface
  - Zoom, pan, sub-sample
- Column offsets for WOI

FPGA Development Board

- Xess XSA-100
- Spartan 2
- 16Mb SDRAM
- 100MHz Osc.
- Parallel Port
- 84 Pin Prototype Header




FLASH
/CE
/OE
/WE
/RESET
A17-A0
D7-D0
8
Parallel Port
2 - PPD0
3 - PPD1
4 - PPD2
5 - PPD3
6 - PPD4
7 - PPD5
8 - PPD6
9 - PPD7
17 - PPC3
16 - PPC2
14 - PPC1
11 - PPS7
12 - PPS5
13 - PPS4
15 - PPS3
1 - PPC0
10 - PPS6
XC9572XL
TDI
TMS
TCK
TDO
GCLK
A17 - A0
D7 - D0
OSC
XC2S100
D7-D0
CCLK
/PROGRAM
/INIT
M0
M1
M2
/CS
/WR
BSY/DOUT
DONE
TCK
TMS
TDI
TDO
GCLK
GCLK
D15 - D0
BA1 - BA0, A12 - A0
RAS, CAS, /CS, /WE
DQMH
DQML
CKE
CLK
SDRAM
PS/2 Port
PSCLK
PSDATA
RED1 - RED0
GREEN1 - GREEN0
BLUE1 - BLUE0
/HSYNC
/VSYNC
VGA Connector

XC2S100 Spartan 2

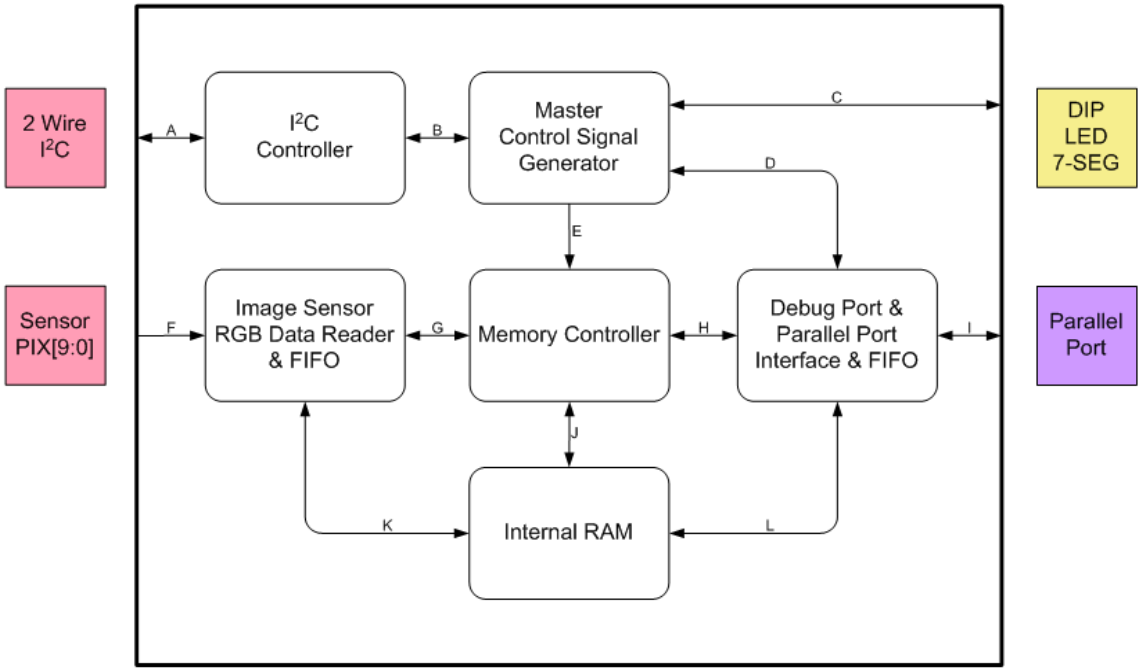
- 100k System Gates
- 40k Bits Block SelectRAM+
- 38k Distributed RAM
- 4 Global Clocks
- 4 Delay Locked Loops
- 2.5V, 3.3V or 5V I/O
- Altera Flex 10K70
  - 4x Slower
  - 18k total RAM

SDRAM

- Hynix HY57V281620A
- 4 Banks x 2M x 16bits
- PC133 CAS 2
- External PCB Clock Feedback
- Prebuilt Xess VHDL Interface

FPGA Design

Planned Top Level



Sub components and their interfaces

Parallel Port Module

- Connects through PLD to PC parallel port
- 6 Download data lines d6 – d0
  - Line d7 controls reconfiguration of Spartan
- 4 Upload Lines
- Data Strobe controlled by PC
- Receives commands from PC to:
  - Set / Read registers in image sensor
  - Upload from RAM
- 17,000 Gates

Do nothing, or

Parallel Port Upload

- XSA-100 limitation, only upload using status pins
- Debounced strobe signal
- DDR upload 4 bits / clock edge
- ~150K bytes/sec
- Asynchronous Coregen FIFO
  - 16 bits 50MHz in
  - 4 bits ~75kHz out
- Counter determines memory addresses

Parallel Port Download

- Commands and addresses received
- Latched and sent to Master Control Signal Generator

Master Control Signal Generator

- State machine
- Branches to receive commands from PC
- Controls Memory Controller
  - Sends start address, end address for upload
- Relay data between PC and image sensor through I2C interface

Memory Controller

- Arbitration between different components that access the memory
- Interleaved memory read and write operations
- Connected to internal RAM or SDRAM controller

SDRAM Controller

- Sample VHDL code from XESS
  - 100ns Access
  - No Burst Mode
  - Incorrectly set Mode Register
- If then else state machine implementation
- Example of DLL use
- Modify to fit project needs
- 16, 000 Gates

SDRAM Controller Problems

- Errors in code
- Would synthesize in Leonardo but fail Xilinx place and route
- Had to move I/O buffer instantiations to top level

I2C

- CoolRunner XPLA3 I2C bus controller implementation from Xilinx
- App note XAPP333
- Microcontroller interface
  - Write / Read from registers using bus cycles
  - Similar to Wishbone common interface from Open Cores
- Includes test benches
- 2000 Gates I2C plus 4000 Gates my controller

I2C Block Diagram

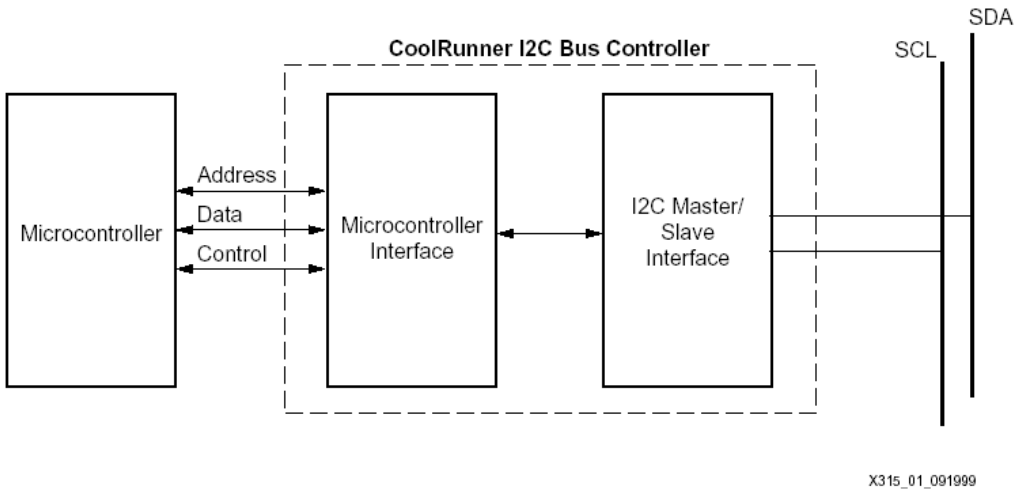
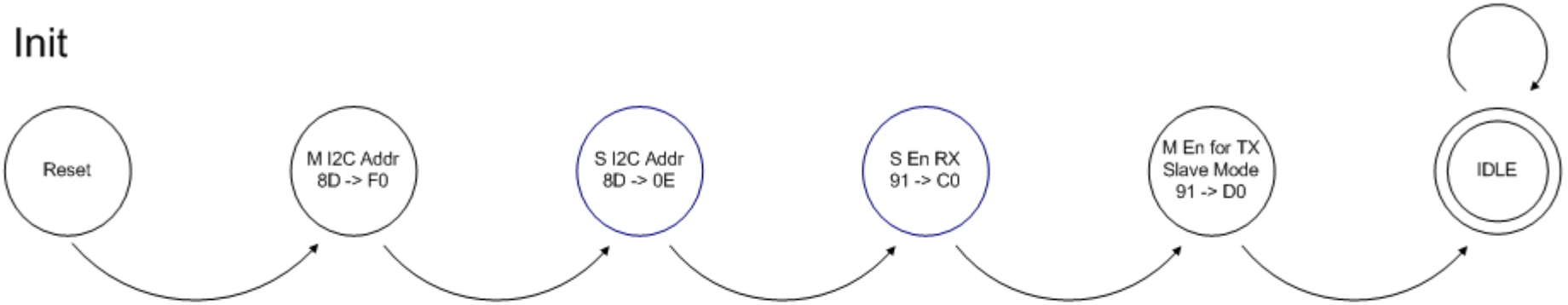


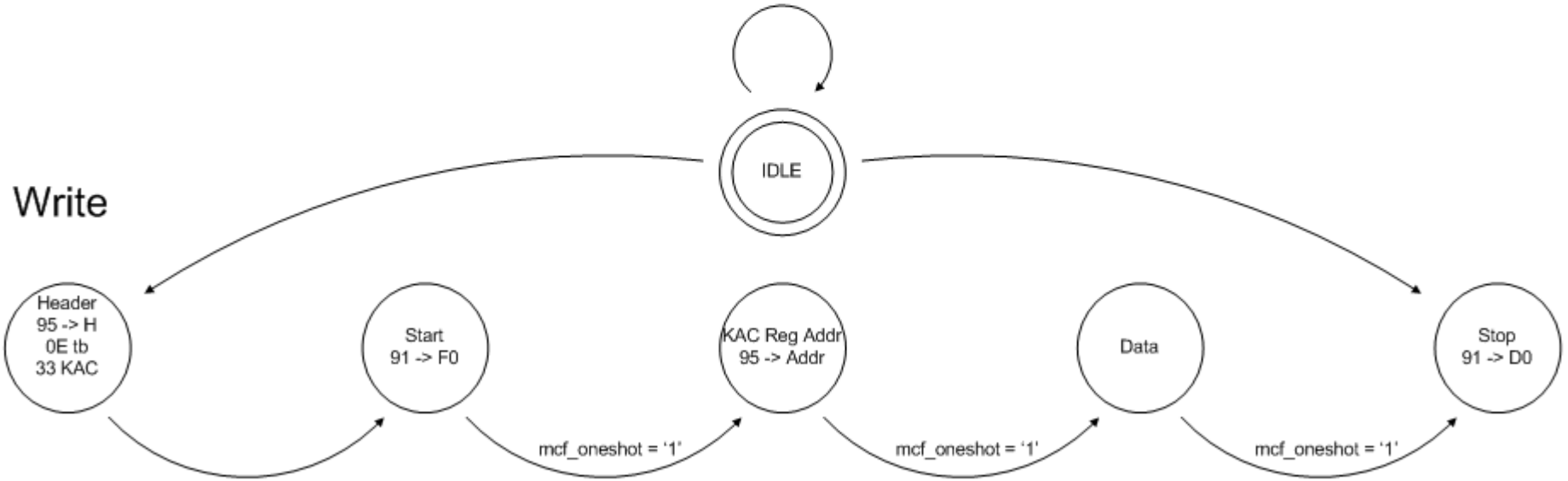
Figure 1: **CoolRunner I²C Bus Controller**

I2C State Sequence

Init



Write



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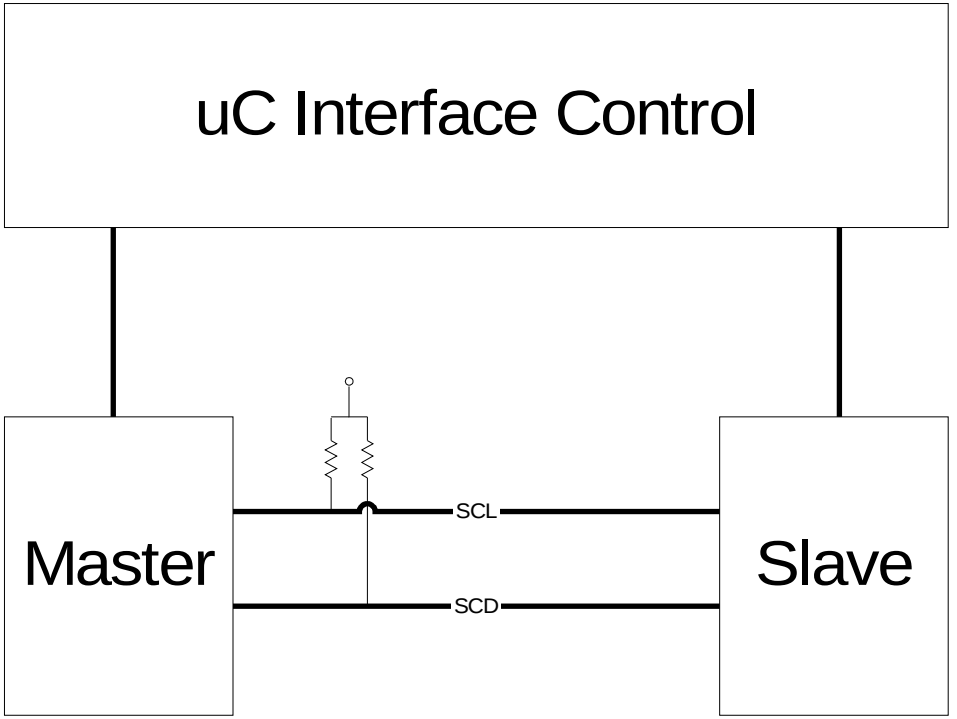
I2C Test Bench

- Bi-directional bus requires slave response to test master
- Slave simulates KAC during functional verification



I2C Interface Flow

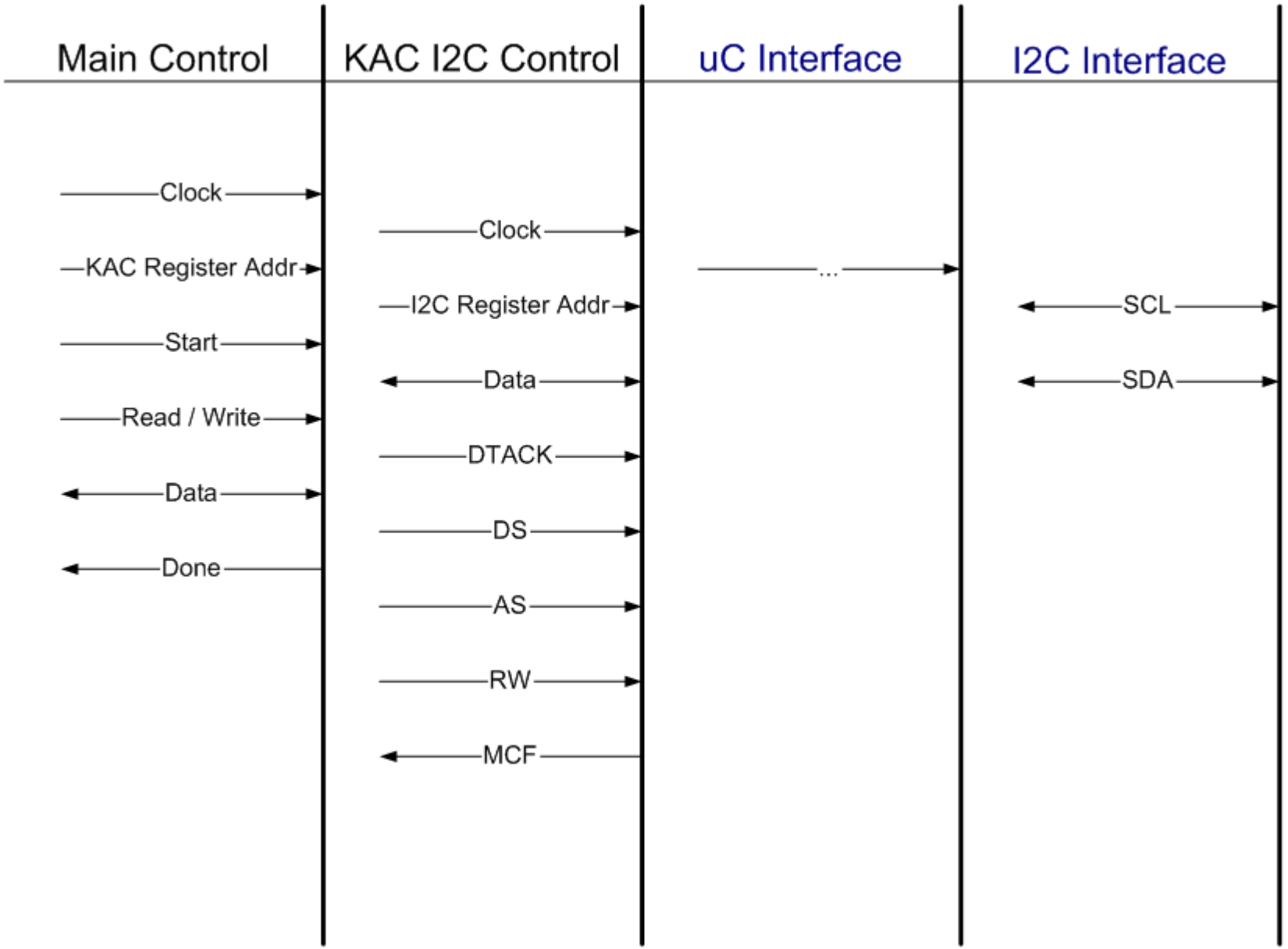


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Image Sensor Data Reader

- Transfer data from image sensor to FPGA
- 5 bits / Pixel
- 1 pixel / 12MHz clock
- FIFO between Image sensor and memory
- Handle timing for image sensor signals
- Convert Bayer pattern to RGB values
  - Buffer pairs of lines
- 20,000 Gates with FIFO and Buffers

Host PC Software

- Control parallel port transfers
- Save uploaded pixel data as JPG or BMP
- Read and write image sensor register values
- GUI spring term
  - Implement live video

Conclusion

External Hardware Summary

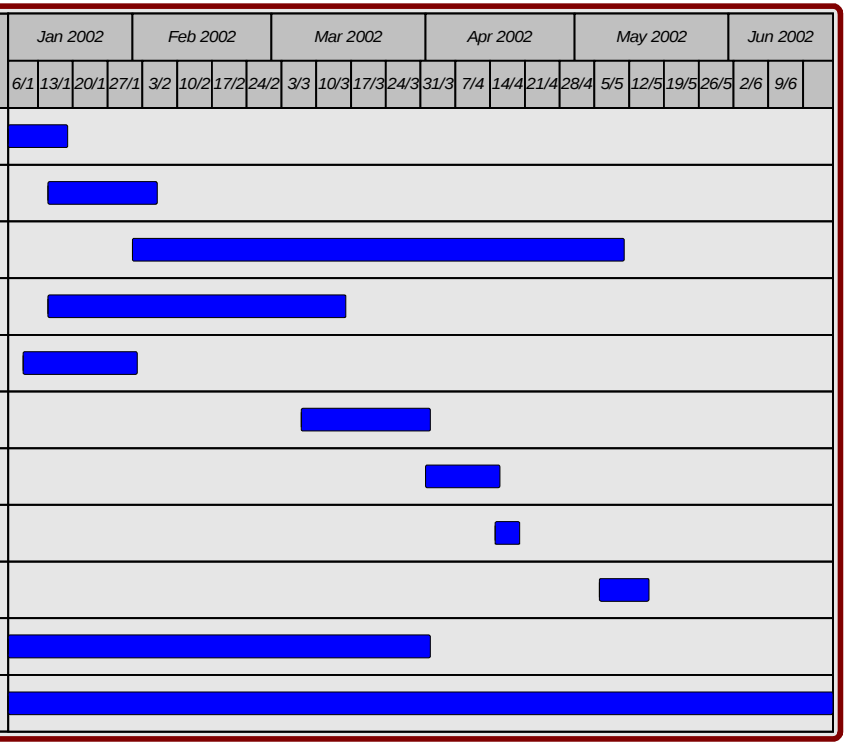
- 1280x1024 Kodak CMOS Image Sensor
- XESS XSA-100 FPGA Board
  - 100k Gate Spartan 2
  - 16M bytes SDRAM
  - Parallel Port

FPGA Design Summary

- Parallel port
- SDRAM controller
- Memory read write arbitrator
- I2C
- RGB data conversion
- 80, 000 Gates total

Schedule

ID	Task Name	Start	Finish	Duration
1	Develop Design Flow	1/7/2002	1/18/2002	10d
2	Parallel Port Connection	1/15/2002	2/5/2002	16d
3	Master Control Signal Generator	2/1/2002	5/10/2002	71d
4	Memory Controller	1/15/2002	3/15/2002	44d
5	SDRAM Interface	1/10/2002	2/1/2002	17d
6	I2C	3/7/2002	4/1/2002	18d
7	Image Sensor RGB Data Reader	4/1/2002	4/15/2002	11d
8	Signal Processor	4/15/2002	4/19/2002	5d
9	Monitor Interface	5/6/2002	5/15/2002	8d
10	Build Image Sensor Board	1/7/2002	4/1/2002	61d
11	Project Documentation	1/7/2002	9/6/2002	175d



Sources

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- Motorola e-www.motorola.com
- Kodak www.kodak.com/US/en/digital/ccd/sensorsMain.shtml
- Plastronics www.locknest.com
- Comp.arch.fpga