intel

APPLICATION NOTE

AP-72

# Application of Intel's 5V EPROM Family for Microprocessor Systems

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## INTRODUCTION

This Application Note discusses how the Intel family of 5 volt EPROMs can be used with microprocessor systems. The pinout evolution and philosophy are explored in detail, which leads directly to system architecture. Particular emphiisis will be placed on the pitfalls of bus contention and the microprocessor/memory interface. Finally, an actual printed circuit board layout is presented.

## PINOUT EVOLUTION

As EPROM technology has evolved, there are often periods of confusion over EPROM pinouts. In particular, there are normally two or three densities of EPROMs which have attained widespread usage. As we have seen, after the 2716 16K EPROM was introduced, a new standard pinout emerged and "triumphed" over an earlier "three-voltage standard." The reason this pinout change occurred was the savings associated with the Intel single supply device. At the same time, users often use the highest available density ROM so they combine modular firmware and minimize device count. Of course, many users never do go to the ROM stage with their equipment, preferring to minimize inventory levels and utilize standard designs that can be customized for final equipment configurations, but they always want the capability to do so if desired.

In addition, over the past few years, the development of microprocesscrs has been intimately entwined with EPROMs.

The 1702A and its ROM counterpart, the 1302, were completely adequate to support the requirements of the 4004 series of microprocessors. In order to support the 5 volt, 3MHz 8085A and 5MHz 8086, it is desirable to use a compatible device such as the Intel 5 volt 2716, whose 450ns access time is compatible with the microprocessor requirements. Some high performance versions of these processors may require selected versions of the 2716 (such as the 2716-1 with $t_{CE} = 350ns$, or the 2716-2 with $t_{CE} = 390ns$) depending on the actual system configuration.

Summarizing these events since the introduction of the Intel 1702A, which was the first EPROM, we can postulate the following hypothesis: the flexibility offered by the EPROM is enhanced by the existence of greater density devices with compatible pinouts. EPROMs must evolve along with rricroprocessor developrnents—so memory performance does not limit system performance.

The devices which are discussed in this Application Note represent an extension of the 5 volt compatible family to 32K bit and 64K bit densities, while improving performance as discussed above. It also follows that the pinout for the 32K devices must be derived from the 2716 in order to maintain socket compatibility. This 16K to 32K pinout evolution is shown in Figure 1.

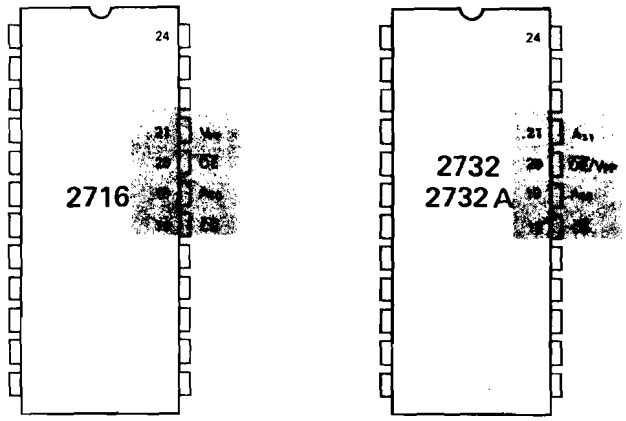



**Figure 1. 2716,2732 and 2732A Offer Common Pinout**

## SYSTEM ARCHITECTURE

As higher performance microprocessors have become available, the architecture of microprocessor systems has been evolving, again placing demands on memory. For many years, system designers have been plagued with the problem of bus contention when connecting multiple memories to a common data bus. There have been various schemes for avoiding the problem, but device manufacturers have been unable to design internal circuits that would guarantee that one memory device would be "off" the bus before another device was selected. With small memories (512x8 and 1Kx8), using the 1702, it had been traditional to connect all the system address lines together and utilize the difference between $t_{ACC}$ and $t_{CO}$ to perform a decode to select the correct device (as shown in Figure 2).

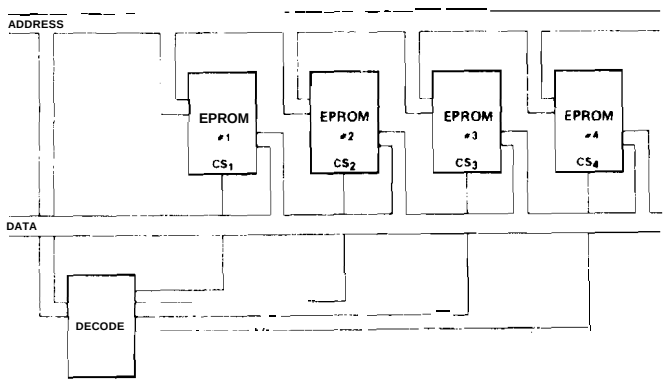



**Figure 2. Single Control Line Architecture**

With the 1702A, the chip select to output delay was only 100ns shorter than the address access time; or to state it another way, the $t_{ACC}$ time was 1000ns while the $t_{CO}$ time was 900ns. The 1702A $t_{ACC}$ performance of 1000ns was suitable for the 4004 series microprocessors, but the 8080 processor required that the corresponding numbers be reduced to $t_{ACC}$ = 450ns and $t_{CO}$ = 120ns. This allowed a substantial improvement in performance over the 4004 series of microprocessors, but placed a substantial burden on the memory. The 2708 was developed to be compatible with the 8080 both in access time and power supply requirements. A portion of each 8080 machine cycle time had to be devoted to the architecture of the system decoding scheme used. This devoted portion of the machine cycle included the time required for the system controller (8224) to perform its function before the actual decode process could begin.

Let's pause here and examine the actual decode scheme that was used so we can understand how the control functions that a memory device requires are related to system architecture.

The 2708 can be used to illustrate the problem of having a single control line. The 2708 has only one read control function, chip select ($\overline{CS}$), which is very fast ($t_{CO}$ = 120ns) with respect to the overall access time ($t_{ACC}$ = 450ns) of the 2708. It is this time difference (330ns) that is used to perform the decode function, as illustrated in Figure 3. The scheme works well and does not limit system performance, but it does lead to the possibility of bus contention.

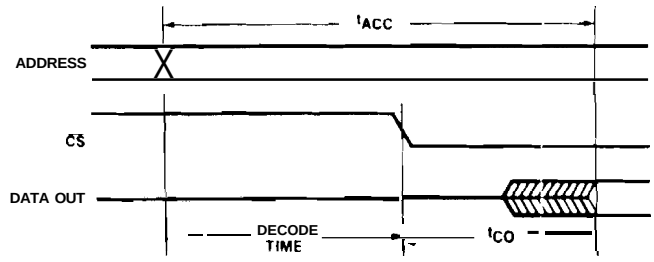



**Figure 3. Single Line Control Architecture**

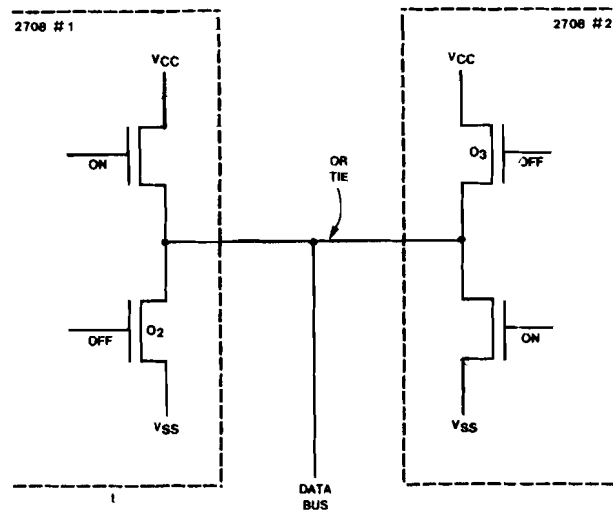



**Figure 4. Results of Improper Timing when OR Tying Multiple Memories**

## BUS CONTENTION

There are actually two problems with the scheme described in the previous section. First, if one device in a multiple memory system has a relatively long deselect time. and a relatively fast decoder is used, it would be possible to have another device selected at the same time. If the two devices thus selected were reading opposite data; that is, device number one reading a HIGH and device number two reading a LOW, the output transistors of the two memory devices would effectively produce a short circuit, as Figure 4 illustrates. In this case, the current path is from $V_{CC}$ on device number one to GND on device number two. This current is limited only by the "on" impedance of the MOS output transistors and can reach levels in excess of 200mA per device. If the MOS transistors have a lot of "extra" margin, the current is usually not destructive; however, an instantaneous load of 400mA can produce "glitches" on the $V_{CC}$ supply — glitches large enough to cause standard TTL devices to drop bits or otherwise malfunction, thus causing incorrect address decode or generation.

The second problem with a single control line scheme is more subtle. As previously mentioned, there is only one control function available on the 2708 and any decoding scheme must use it out of necessity. In addition, any inadvertent changes in the state of the high order address lines that are inputs to the decoder will cause a change in the device that is selected. The result is the same as before — bus contention, only from a different source. The deselected device cannot get "off" the bus before the selected one is "on" the bus as the addresses rapidly change state. One approach to solving this prcblem would be to design (and specify as a maximum) devises with $t_{DF}$ time less than $t_{CO}$ time, thereby assuring that if one device is selected while another is simultaneously being deselected, there would be some small (20ns) margin. Even with this solution, the user would not be protected from devices which have very fast $t_{CO}$ times ($t_{CO}$ is specified as a maximum).

The only sure solution appears to be the use of an external bus driver/transceiver that has an independent enable function. Then that function, not the "device selecting function," or addresses, could control the flow of data "on" and "off" the bus, and any contention problems would be confined to a particular card or area of a large card. In fact, many systems are implemented that way — the use of bus drivers is not at all uncommon in large systems where the drive requirements of long, highly capacitive interconnecting lines must be taken into consideration — it also may be the reason why more system designers were not aware of the bus contention problem

until they took a previously large (multicard) system and, using an advanced microprocessor and higher density memory devices. combined them all on one card, thereby eliminating .he requirement for the bus drivers, but experiencing the problem of bus contention as described above.

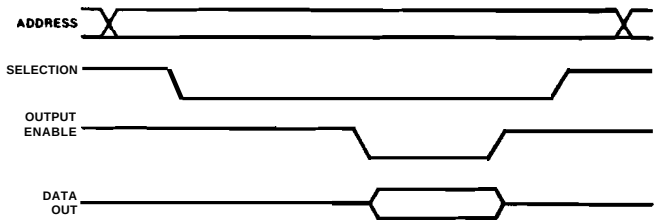



**Figure 5. Two Control Line Architecture**

## THE MICROPROCESSOR/MEMORY INTERFACE

From the foregoing discussion, it becomes clear that some new concept!;, both with regard to architecture and performance are required. A new generation of two control line EPROM devices is called for with general requirements as listed below:

1. A power control function that allows the device to enter a low-power standby mode when deselected. This function can be used as the primary device selecting function, independent of the output control.
2. Capability to control the data "on" and "off" the system bus, independent of the device selecting function identified above.
3. Access time compatible with the high performance microprocessors that are currently available.

Now let's examine the system architecture that is required to implement the two line control and prevent bus contention. This is shown in the form of a timing diagram (Figure 5). As before, addresses are used to generate the unique device selecting function, but a separate and independent Output Enable (OE) control is now used to gate data "on" and "off" the system data bus. With this scheme, bus contention is ccmpletely eliminated as the processor determines the time during which data must be present on the bus and then releases the bus by way of the Output Enable line, thus freeing the bus for use by other devices, either memories or peripheral devices. This type of architecture can be easily accomplished if the memory devices have two control functions, and the system is implemented according to the block diagram shown in Figure 6. It differs from the previous block diagram (shown in Figure 2) in that the control bus, which is connected to all memory Output Enable pins, provides separate and independent control over the data bus. In this way, the microprocessor is always in control of the system; while in the previous system, the microprocessor passed control to the particular memory device and then waited for data to become available. Ar other way to look at it is, with a single control line the system is always asynchronous with respect to microprocessor/memory communications. By using two control lines, the memory is synchronized to the processor.

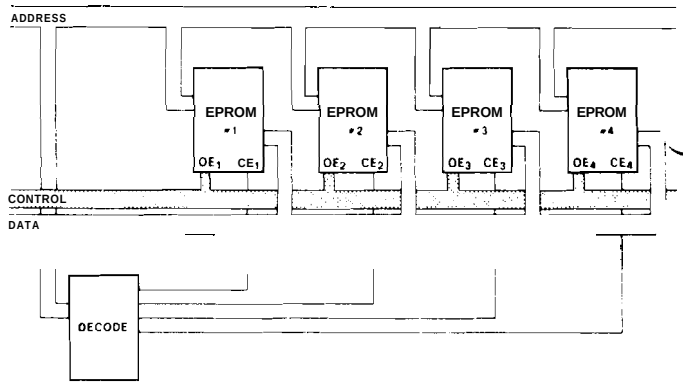



**Figure 6. Two Control Line Architecture**

## TERMINOLOGY

Some of the terminology applied to the functions of the Intel 5 volt compatible family may be confusing or unfamiliar to many EPROM users, so the various terms are defined here. Actually, the nomenclature was developed by various standards groups and is reiterated here to avoid confusion as we begin a detailed discussion of the devices themselves.

First of all, Chip Enable (CE) must be defined, as it is the primary device selection pin. By agreed standards, that function which substantially affects power dissipation is called CE. Any memory device that has a CE function has both an active and standby power level associated with it.

Output Enable (OE) is the signal that controls the output. The fundamental purpose of OE is to provide a completely separate means of controlling the output buffer of the memory device, thereby eliminating bus contention.

Chip Select (CS) is a signal that gets logically ANDed with addresses. In a completely static device, CS must remain stable throughout the entire device cycle, and its function is equivalent to Output Enable (OE).

## THE NEW INTEL FAMILY

Figure 7 shows the new Intel 5 volt compatible family of EPROMs. In order to take advantage of the modular compatibility offered by the family, the functional compatibility of device pins 18, 19 and 21 must be understood. (Shaded area in Figure 7.)

First, we must examine the compatibility of the two oldest EPROM members of the 5 volt family—the 8K (2758) and the 16K (2716).

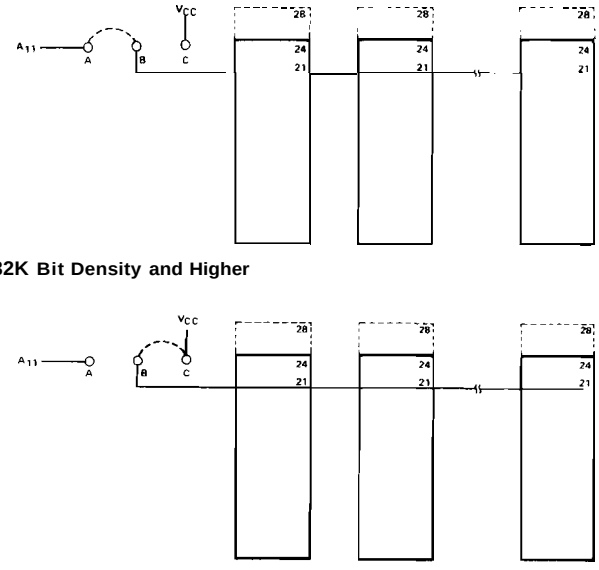
Pin 21 ($V_{PP}$) is normally connected to $V_{CC}$ for read only applications of both devices, and pin 19 is either at GND ($V_{IL}$) for the 8K 2758 or connected to $A_{10}$ for the 16K 2716. Further details on either of these devices can be found in Section 2 of the 1980 Intel Data Catalog.

The 32K (4K x 8) devices will now be discussed. Pin 18 is $\overline{CE}$. Pin 19 is $A_{10}$, while pin 20 is $\overline{OE}$. As was pointed out before, Output Enable is the function which allows independent control of the data "on" and "off" the output bus. As Figure 7 indicates, $V_{PP}$ (the programming voltage for the 2732 EPROM) is now multiplexed with $\overline{OE}$ on pin 20. Pin 21 becomes $A_{11}$, which is the additional address bit that is required as the density increases from 16K to 32K.

Pin 21 is the only pin that requires any special consideration when designing a system to accept the 16K, 32K, or the 64K device. With the 8K and the 16K devices, pin 21 must be connected to $V_{CC}$, while with the 32K and higher density devices, it must be connected to $A_{11}$. This is easily accomplished by making sure the printed circuit trace links all pin 21's together as though they were an address line and allowing for a jumper that will connect pin 21 to either $V_{CC}$ or $A_{11}$ at the edge of the array (this technique can be seen in the "Printed Circuit Board Design" section and in Figure 8). Connecting the pin 21's together in this manner is acceptable as the read current requirement for $V_{PP}$ is 4mA maximum per device—low enough to be handled by a signal trace, but too high for an address driver to provide directly.

The highest density member of the family is a 64K EPROM which is also shown in Figure 7. In order to maintain compatibility and future upgrade capability it is packaged in a standard 28-pin package.

It may seem as though the 28 pin package is not compatible with the rest of the family, but referring again to Figure 7, note that the lower 24 pins are identical to the 24 pin 8K, 16K and 32K devices. To allow for compatibility within the family, printed circuit boards may be laid out to accommodate 28 pin sites. A jumper must be included to accommodate pin 21 as shown in Figure 8. This compatibility can also be seen graphically in Figures 9 and 10. The upper portion of the figure shows how 24 pin devices are used in the 28 pin sites. The two control lines ($\overline{CE}$ and $\overline{OE}$) remain unchanged as discussed earlier, and $A_{12}$, the next address bit required for a 64K bit device, is connected to pin 2 of the 28 pin site. The lower portion of the figure illustrates the use of 28 pin devices. Address bit $A_{12}$ is already connected to the right pin, and pins 1, 27 and 28 are connected to $V_{CC}$ through a card edge jumper. Pin 1 must be connected to $V_{CC}$ as Vpp is a 5V power supply when the 2764 is not being programmed.




32K Bit Density and Higher

8K and 16K Density Devices

**Figure 8. Pin 21 Connections for Various Density Devices**

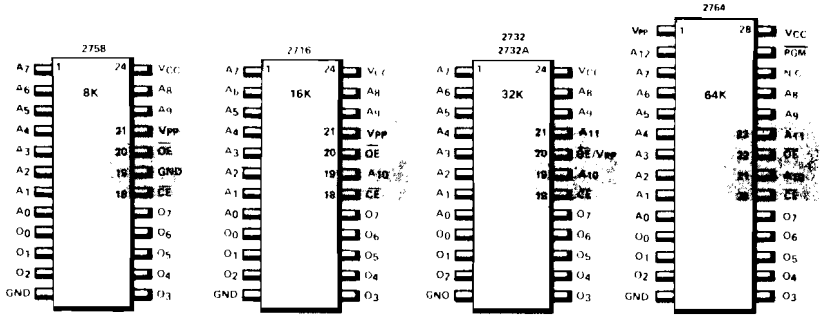
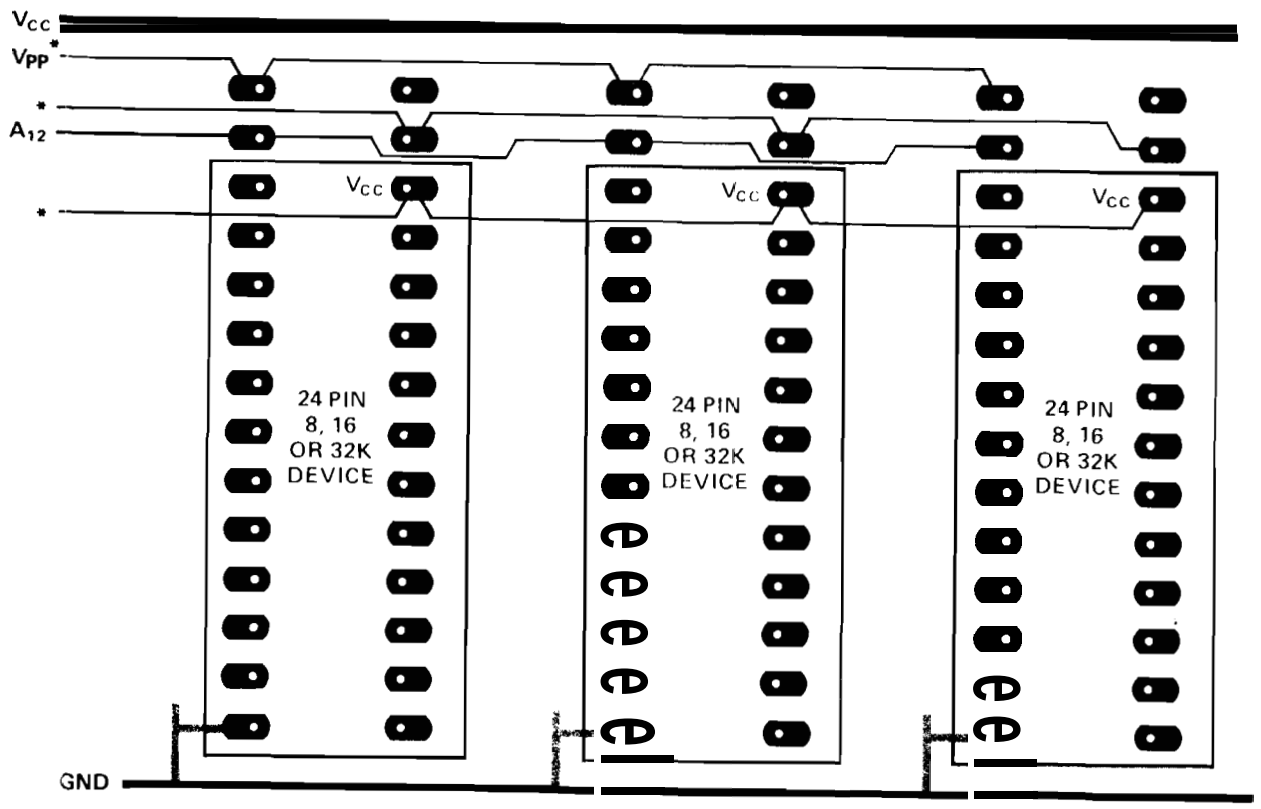
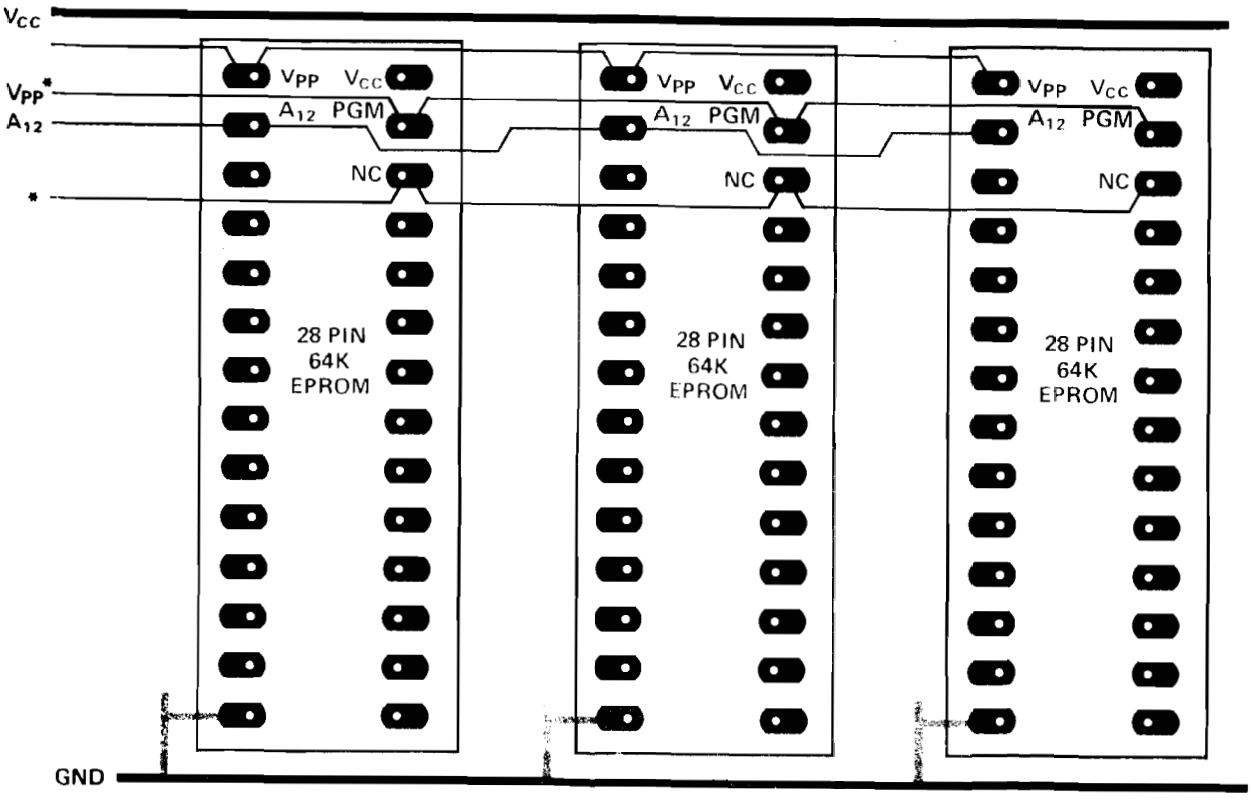



**Figure 7. 5 Volt EPROM/E² Compatible Family**




**24 Pin Devices and 28 Pin Sites**




**28 Pin Devices and 28 Pin Sites**

Figure 9.

*Card edge jumpers for future device compatibility

To summarize, the selection of a 28 pin package for 64K devices has several benefits of importance to present and future system designs:

1. Two line control philosophy (separate $\overline{CE}$ and $\overline{OE}$ functions) is preserved at the 64K bit level.
2. 64K EPROM compatibility is allowed for by maintaining a pin for the $V_{PP}$ function.

With the jumper provision for pin 21 included on the card as described above, any member of the family can be plugged into the same socket—16K, 32K, 64K or 128K bytes—without any card modification or redesign. In addition, future devices of higher density will fit in the same pinout.

## PRINTED CIRCUIT BOARD DESIGN

The $I_{CC}$ waveform for the 2732 is shown in Figure 10. The supply current, $I_{CC}$, has three segments that are of concern to the system designer—the standby level, active level and the transient peaks that are produced on the rising and falling edges of Chip Enable. The transient currents must be suppressed by properly selected decoupling capacitors. High quality, high frequency ceramic capacitors of small physical size with low inherent inductance should be used. In addition, bulk decoupling must be provided, usually near where the power supply is connected to the array. The purpose of the bulk decoupling is to overcome the voltage droop caused by the inductive effects of the PC board traces. Electrolytic or tantalum capacitors are suitable for bulk decoupling. The following capacitance values and locations are recommended for the 2716 and 2732:

1. A 0.1$\mu$F ceramic capacitor between $V_{CC}$ and GND at every other device.
2. A 4.7$\mu$F electrolytic capacitor between $V_{CC}$ and GND for each eight devices.

A printed circuit board layout for a total array of 16 devices is shown in Figure 11. This printed circuit layout incorporates a power supply distribution system such that the power supply and ground traces on the PC board are gridded both vertically and horizontally at each memory device; this technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors. Provisions are included for all address inputs, output enable inputs, data outputs and decoded chip enable inputs. The 0.1$\mu$F capacitors referred to above are included for every other device (indicated by the legend C2) while the bulk decoupling capacitor is shown at the upper left-hand corner (indicated by the legend C1). The layout consists of four rows of four 28-pin device sites each and embodies all of the concepts explained above. Note that pins 28, 27 and 26 are all connected to $V_{CC}$. The single jumper provision discussed in the previous section is also included at the upper lefthand corner of the array (indicated by A, B, and C). Pad B is connected to pin 21 of all devices in the array; pad A should be connected to the $A_{11}$ address driver and pad C is connected to $V_{CC}$. For use with 32K bit or larger devices, a jumper must be installed between pads A and B; for use with the 2716 (16K) or the 2758 (8K), the jumper must be installed between pads B and C.

A full size (2x) artwork film is included on the last page of this Application Note. The entire array, or segments of it can be photographed and used directly as part of a system board.

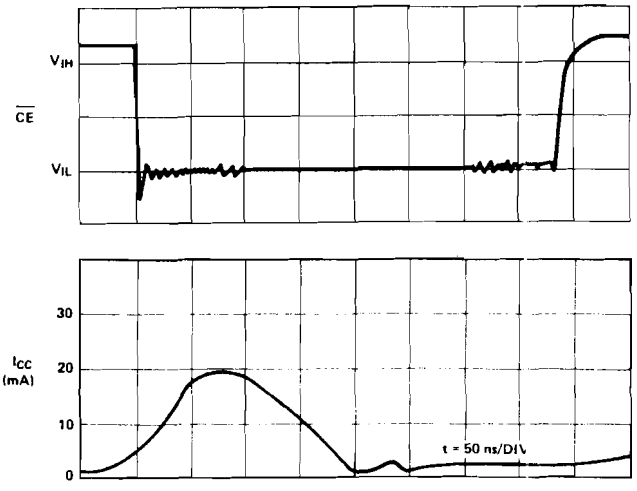



**Figure 10. Typical $I_{CC}$ Current vs. Time—2732**

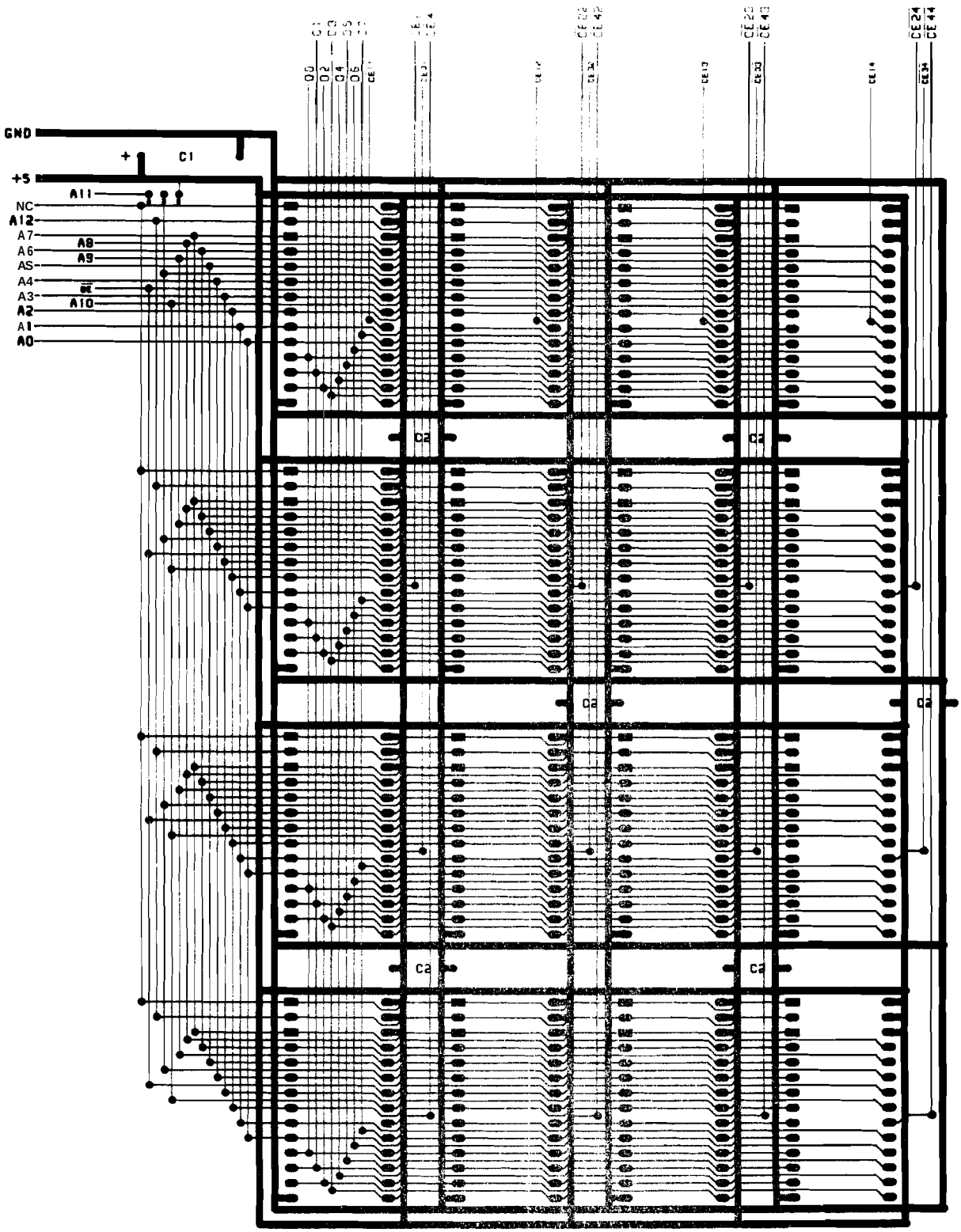



**Figure 11.** Printed Circuit Board Layout for 16 Devices