Core Area Calculations

Name of Block	Category	Gate/FF Count	Area (um2)	Comments
On-chip SRAM	Reg. w/ Reset	776	1,862,400	tree storage: max nodes = equal frequencies for all 128 chars (128 leaves, so 128*2 - 1 total nodes, which means probably (128*2 - 1) * (1 + 2) (due to char (8bit) and frequency (16bit)), in addition, unencoded message must be stored to be encoded later
Controller Next-State Logic	Combinational	24	18,000	# of states + # of inputs to get to each state
Controller State Register	Reg. w/ Reset	4	9,600	11 states = 4 FF
Controller Output Logic	Combinational	5	3,750	# of states with outputs
Accumulator Counter Next Count Logic	Combinational	4	3,000	bits * 2 (1 bit is a full adder, 2 gates)
Accumulator Counter Count Register	Reg. w/ Reset	2	4,800	2-bit
Accumulator Counter Output Logic	Combinational	2	1,500	
Size Counter Next Count Logic	Combinational	32	24,000	bits * 2
Size Counter Count Register	Reg. w/ Reset	16	38,400	16-bit
Size Counter Output Logic	Combinational	16	12,000	
Read Buffer Logic	Combinational	1007	755,250	for a 2^n:1 mux, there are (n + 2^n + 1) gates. muxes added first. assume adder is 5 gates/bit
Read Buffer Register	Reg. w/ Reset	4352	10,444,800	
Tree Constructor Next-State Logic	Combinational	16	12,000	# of conditional input (if/else) * 4 + next state assignments
Tree Constructor State Register	Reg. w/ Reset	4	9,600	10 states = 4 bits
Tree Constructor Other Register	Reg. w/ Reset	4248	10,195,200	10 states = 4 bits
Tree Constructor Output Logic	Combinational	31	23,250	# outputs + # of conditional statements (4 per if/else)
Tree Encoder Next-State Logic	Combinational	130	97,500	# of conditional input (if/else) * 4 + next state assignments
Tree Encoder State Register	Reg. w/ Reset	6	14,400	33 states = 6 bits
Tree Encoder Other Register	Reg. w/ Reset	146	350,400	
Tree Encoder Output Logic	Combinational	137	102,750	# outputs + # of conditional statements (4 per if/else)
Total Core Area			23,982,600	

Chip Area Calculations (units in um or um2)

Number of I/O Pads:	-		
I/O Pad Dimensions:	-	by	-
I/O Based Padframe Dimensions:	-	by	-
Core Dimensions	4,897	by	4,897
Core Based Padframe Dimensions:	4,897	by	4,897
Final Padframe Dimensions:	4,897	by	4,897
Final Chip Area:	23,982,600		