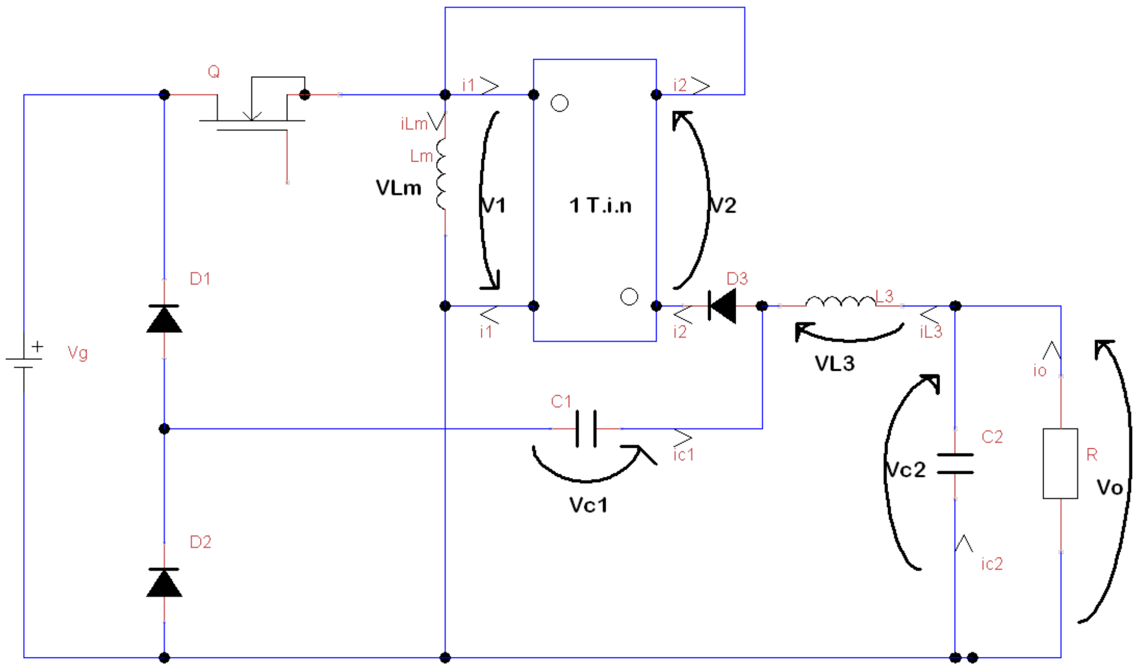
Power Electronics Project

Project 1 – PE

Sorescu Denis-Valentin, 1.2

Toth Razvan-Catalin, 1.2

Slejiuc Robert-Andrei, 1.2



Design values known:

- Vg(min) ÷ Vg(max)
- Vo, ΔVo, f_s
- Po(min) ÷ Po(max)

Transformer equations:

$$\begin{cases} v_1 = \frac{v_2}{n} \\ i_1 + n_{i_2} = 0\ , \end{cases}$$

In which we derive: $n = \frac{N_2}{N_1}$;

<u>1.</u> Justify why the direction of capacitor voltages and inductor currents have been chosen as such, and how do they result positive.

$i_{L_3} = i_{D_3} + i_{C_1}$;

In DC we know that : $i_{L_3} = i_{D_3} > 0$;

$v_{C_2} = -v_{L_m} - v_2 + v_{D_3} - v_{L_3}$;

For DC: $V_{L_m} = V_{L_3} = 0 => V_2 = 0 => V_{C_2} = V_{D_3} > 0$;

$v_{C_1} = v_{D_2} + v_{C_2} + v_{L_3}$, so we can see that $V_{C_1} = V_{D_2} + V_{C_2} > 0$;

$i_{L_m} = i_Q - i_1$, in which we derive that $i_1 = -ni_2$, but $i_2 = i_{D_3}$ =>

=> $i_{L_m} = i_Q + ni_{D_3}$ => $i_{L_m} = i_Q + ni_{D_3} > 0$;

<u>2.</u> Justification for the conduction state of the diodes.

We can assume that in the first state(ON state), Q and D_1 are conducting, and $D_2\ with\ D_3$ are off.

ON state: -Q & D_1(conducting);

-D_2&D_3(off);

$i_{D_3} = 0 => i_2 = 0 => i_1 = -ni_2 = 0;$

$i_q = i_{L_m} + i_1 - i_2 = i_{L_m} > 0;$

$i_{D_1} = i_{D_2} - i_{C_1} = -i_{C_1} = -(-i_{L_3}) = i_{L_3} > 0;$

$v_{D_2} = V_g > 0;$

$v_{D_3} = v_2 + v_{C_1} = v_{C_1} + v_{L_m} = v_{C_1} + nV_g > 0;$

We assume that in the second topological state(OFF state), Q and D_1 are off, and obviously D_2 si D_3 are turned on and are conducting themselves.

OFF state: -Q&D_1(off);

-D_2&D_3(conducting);

$$i_{D_2} = i_{C_1} = i_2 - i_{L_3} = -\frac{i_1}{n} - i_{L_3} = \frac{i_{L_m}}{n+1} - i_{L_3} > 0;$$

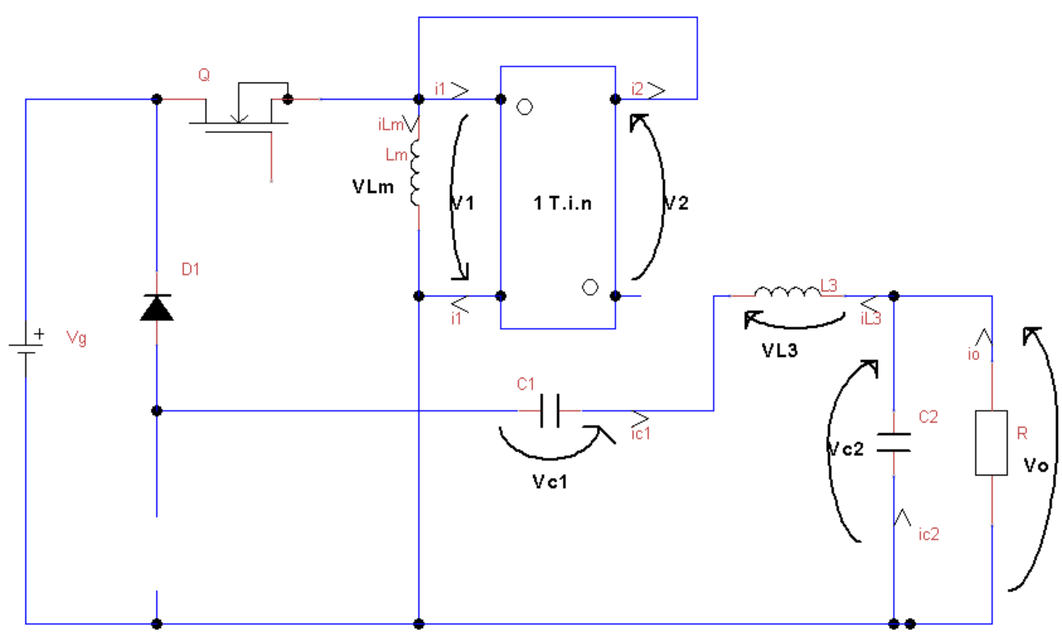
$$i_{D_3} = i_{L_3} + i_{D_2} = \frac{i_{L_m}}{n+1} > 0;$$

$$v_{D_1} = V_g > 0;$$

$$v_Q = V_g - v_{L_m} = V_g - \left(-v_2 - v_{C_1}\right) = V_g + \frac{v_{C_1}}{n+1} > 0;$$

3.

ON state:



Equations resulted:

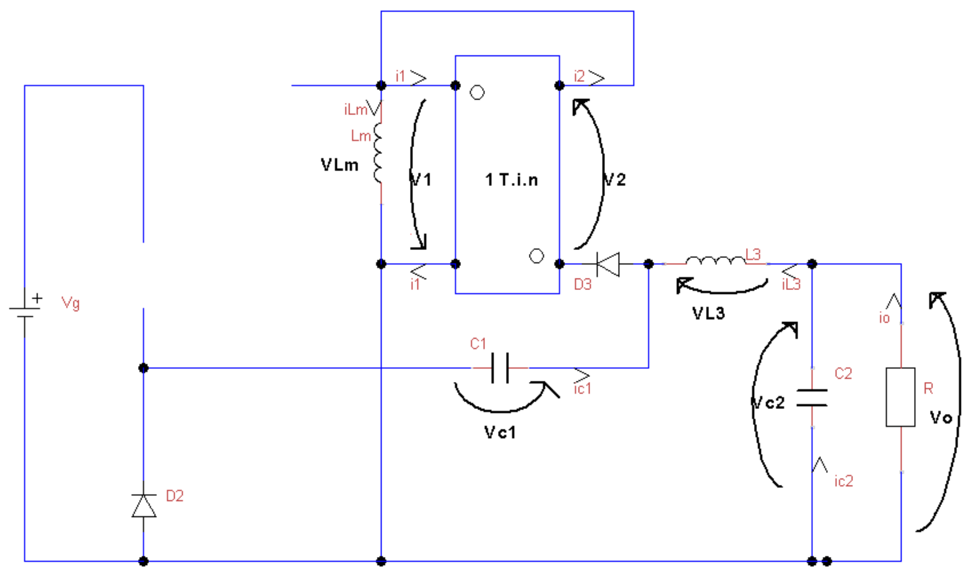
$$v_{L_{3ON}} = v_{C_1} - v_{C_2} - V_g;$$

$$v_{L_{mON}} = V_g;$$

$$i_{C_{1ON}} = -i_{L_3};$$

$$i_{C_{2ON}} = i_{L_3} - \frac{v_{C_2}}{R};$$

OFF state:



Equations resulted:

$$v_{L_{3OFF}} = -v_{C_2} + v_{C_1};$$

$$v_{L_{mOFF}} = -\frac{v_{C_1}}{n+1};$$

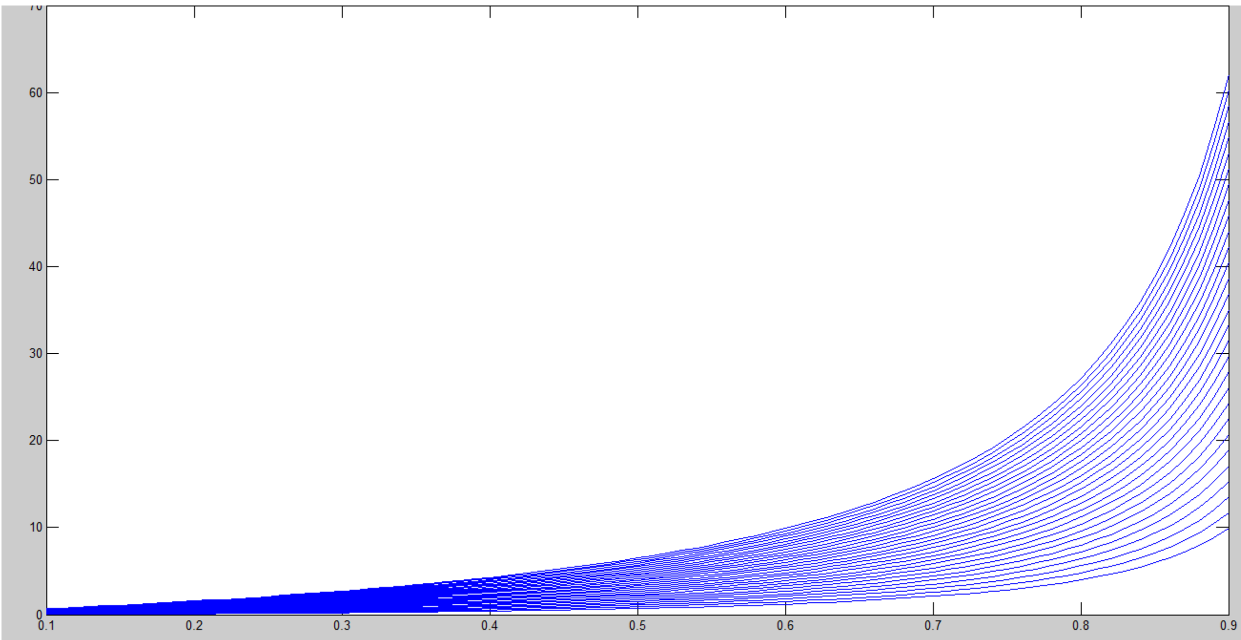
$$i_{C_{1OFF}} = \frac{i_{Lm}}{n+1} - i_{L_3};$$

$$i_{C_{2OFF}} = i_{L_3} - \frac{v_{C_2}}{R};$$

Ideal static conversion ratio – final formula :

$$M_{IDEAL} = \frac{D}{1-D}(n+D);$$

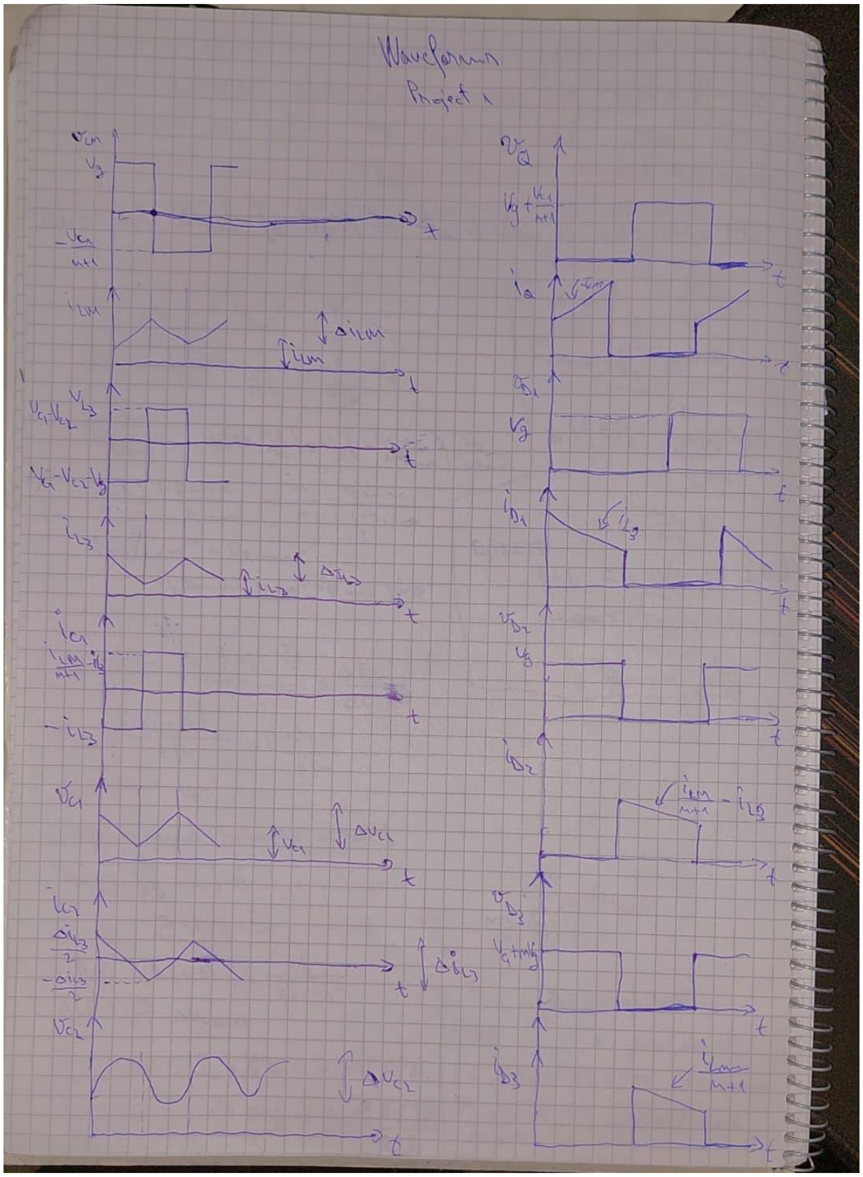
4. Static conversion ratio representation against the duty cycle with turns ratio as a parameter.



From the resulted graph, we can see that we have a buck-boost converter type.

At low duty cycles(under 0.25), we have a static conversion ratio which is underlimited, and as the duty cycle rises, the converter continues to ramp up in power.

5. Waveforms



6. Ripple calculation in terms of dc supply voltage, dc output voltage, output power converter and switching freq.

$$v_{L_{m_{ON}}} = L_m \frac{\Delta_{i_{L_m}}}{DT_s} => \Delta_{i_{L_m}} = \frac{v_{L_{m_{ON}}} \; DT_s}{L_m} => \; \Delta_{i_{L_m}} = \frac{DV_g}{L_m f_s};$$

$$v_{L_{3_{OFF}}} = L_3 \frac{\Delta_{i_{L_3}}}{(1-D)T_s} => \Delta_{i_{L_3}} = \frac{(1-D)(v_{C_1} - v_{C_2})}{L_3 f_s} => \Delta_{i_{L_3}} = \frac{D(1-D)V_g}{L_3 f_s};$$

$$\left| i_{C_{1_{ON}}} \right| = C_1 \frac{\Delta_{V_{C_1}}}{DT_s} => \Delta_{V_{C_1}} = \frac{i_{L_3} \; D}{C_1 f_s} => \Delta_{V_{C_1}} = \frac{D^2 (n + D) V_g}{(1 - D) \; R \; C_1 \; f_s};$$

For the formula of $\Delta_{V_{C_2}}$ we need to consider load for $\Delta_{V_{C_1}} = \frac{\Delta_Q}{C_2}$, where we deduce that

$$\Delta_Q = \frac{1}{2} \frac{T_s}{2} \frac{\Delta_{i_{L_3}}}{2} => \Delta_{V_{C_2}} = \frac{D(1 - D)V_g}{8 \; C_2 \; L_3 \; f_s{}^2};$$

7. Semiconductor voltage and current stresses formulas resulted based on V_o, P_o, V_g, and n.

We get : $\frac{D}{1-D}(n+D)=\frac{V_o}{V_g} => D=f\left(V_o, V_g, n\right)$;

$$P_o=\frac{{V_o}^2}{R} => R=\frac{{V_o}^2}{P_o};$$

Approximate for calculus ($v_{C_1} \sim V_{C_1}, v_{C_2} \sim V_{C_2}$):

$V_{Q_{mean}}=(1-D)\left(V_g+\frac{V_{C_1}}{n+1}\right)$;

$V_{D_{1mean}}=(1-D)V_g$;

$V_{D_{2mean}}=DV_g$;

$V_{D_{3mean}}=D\left(V_{C_1}+nV_g\right)$;

RMS values:

$1-D \rightarrow \sqrt{1-D}$;

$D \rightarrow \sqrt{D}$;

Identical otherwise.

8. Conditions for CCM operations, canonical form.

For D1;

$$\boldsymbol{i_{D_1} \geq 0 \leftrightarrow i_{D_{1_{min}}} \geq 0 => i_{L_3} - \frac{\Delta_{i_{L_3}}}{2} \geq 0};$$

$$\boldsymbol{\frac{D(D+n)}{1-D}\frac{V_g}{R} \geq \frac{D(1-D)V_g}{2\,L_3\,f_s} => \frac{2\,L_3\,f_s}{R} \geq \frac{D(1-D)^2}{D(D+n)} => \frac{2\,L_3\,f_s}{R} \geq \frac{(1-D)^2}{(D+n)}};$$

For D2;

$$\boldsymbol{i_{D_2} \geq 0 \leftrightarrow i_{D_{2_{min}}} \geq 0 => \frac{\Delta_{i_{L_m}}}{n+1} - i_{L_3} - \frac{\Delta_{i_{L_m}}}{2(n+1)} + \frac{\Delta_{i_{L_3}}}{2} \geq 0};$$

$$\boldsymbol{\frac{D\,Vg(D\;+\;n)}{R(D\;-\;1)} - \frac{DVg}{2Lm\,fs\,(n\;+\;1)} - \frac{D\,Vg(D\;-\;1)}{2\;L3\;fs} + \frac{D\,Vg\;(D\;+\;n)}{R\;(D\;-\;1)^2}};$$

For D3;

$$\boldsymbol{i_{D_3} \geq 0 \leftrightarrow i_{D_{3_{min}}} \geq 0 => \frac{i_{L_m}}{n+1} - \frac{\Delta_{i_{L_m}}}{2(n+1)} \geq 0};$$

$$\boldsymbol{\frac{D(D+n)V_g}{R(1-D)^2} \geq \frac{DV_g}{2\,L_m\,f_s(n+1)} => \frac{2\,L_m\,f_s}{R} \geq \frac{(1-D)^2}{(n+1)(D+n)}};$$

9. *Initial relationships for inductors and capacitor design, with Matlab final numerical results.*

Vg_min=15; Vg_max=18; Vo=25; Po_min=25; Po_max=50; dvo=0.25; fs=100e3;

```
L1 =

   1.1718e-04


L2 =

   3.0612e-05


L3 =

   1.7708e-04


C1 =

   1.6580e-05


C2 =

   1.2500e-06

>>
```

Choose D_{max} in case of V_{min} and get rid of n; Calculate D_{min} for V_{max};
$D_{min} < D < D_{max}$;

10. *Power stage simulation for ideal converter(Table).*

Vg=18; R=25; D=0.5637; n=0.5111; L3=180e-6; C1=16.5e-6; C2=1.25e-6; Lm=120e-6; fs=100e3;

Program used	MATLAB	CASPOC
IQ_mean	1.9520	1.960
IQ_rms	2.5999	2.613
ID1_mean	0.5636	0.5657
ID1_rms	0.7507	0.7543
ID2_mean	0.5636	0.5634
ID2_rms	0.8533	0.8681
ID3_mean	0.9998	0.9996
ID3_rms	1.5137	1.519
VQ_mean	18	18
V_DS	41.256	
V_D3	44,342	44,34V
V_out_mean	25	25.016
V_out_rms	25	25.010

11. **Main parameters of the devices, semiconductors and the loss parameters.**

Transistor: N-MOSFET; unipolar; 500V; 4A; 29,2W; TO220FP;

The 3 Diodes: rectifier Schottky; THT; 60V; 2A; DO15; Package from : Ammo Pack;

Condensator C1: electrolytic; reduced impedance; THT; 18uF; 63VDC;

Condensator C2 out: electrolytic; THT; 1,5uF; 50VDC; Ø4x7mm; Pitch: 1,5mm;

The diodes have been chosen uniformly as the same type for them to have consistent diode forward turn-on time (commutation).

12. $\mathbf{D_{max}}$ **and** $\mathbf{D_{min}}$ **resulted from Matlab.**

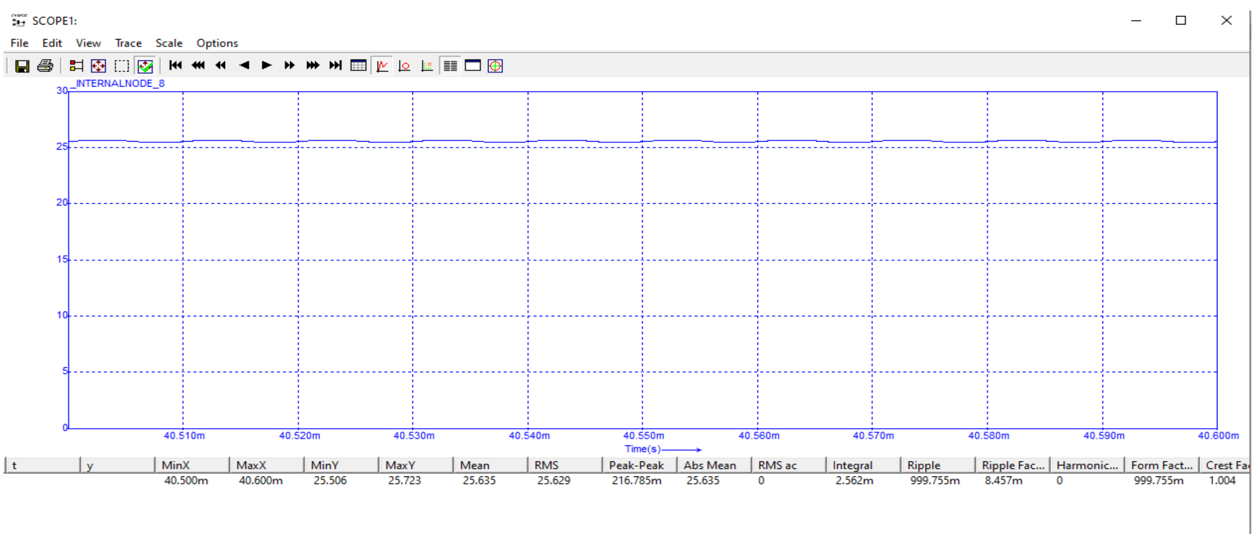
$D_{max} = 0.6414;$

$D_{min} = 0.6008;$

13. Operating point arbitrarily chosen and Output Ripple Voltage

We chose the operating point $V_{max} = 18V$, for which it corresponds to the following minimum duty cycle chosen at point 10 $D_{min} = 0.6008;$

Output voltage ripples are in the allowed limits, as seen in the photo provided (Peak-Peak for reference value).



$Ripple_{V_{out}} = 216.785mV;$