University of Tehran
College of Engineering
School of Electrical and Computer Engineering

Communication Circuits

Computer Assignment 2

Soroush Mesforush Mashhad

SN:810198472

Khordad 02

Contents

Abstract

In this project we shall get familiar with the functionality of a **Phased Locked Loop(PLL)**.

We use the **Voltage Controlled Oscillator(VCO)** designed in the first project and then we go on to design the other needed circuits such as the **Divider Circuit**,**Differential to Single Ended(D2S)** and the **Charge Pump(CP)** circuit.

In the end we create the **Phased Locked Loop (PLL)** by connecting the different circuit symbols accordingly.

1 Question 1

The schematic of the **Voltage Controlled Oscillator (VCO)** we designed is as follows.

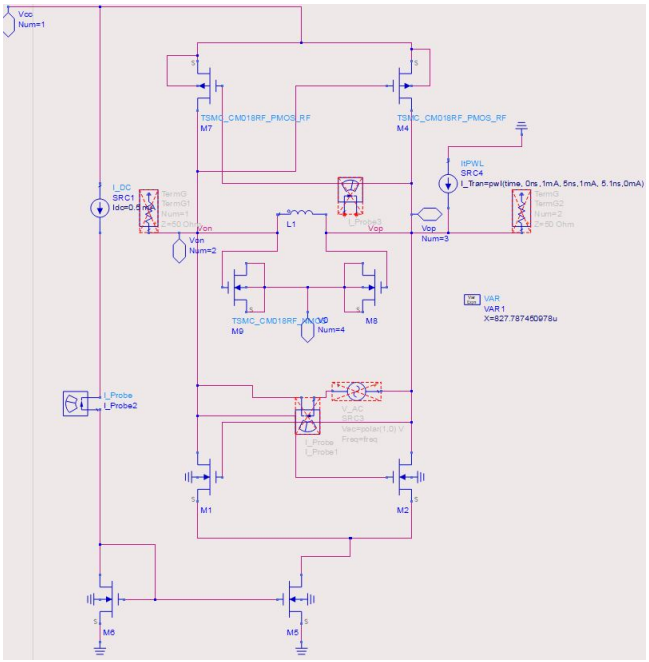


Figure 1: Voltage Controlled Oscillator

Now we shall test it just to be sure. To do so I have created the symbol of this circuit in a new schematic and tested it accordingly.

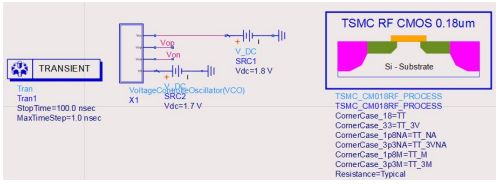


Figure 2: Voltage Controlled Oscillator Symbol and test

The results are as follows.

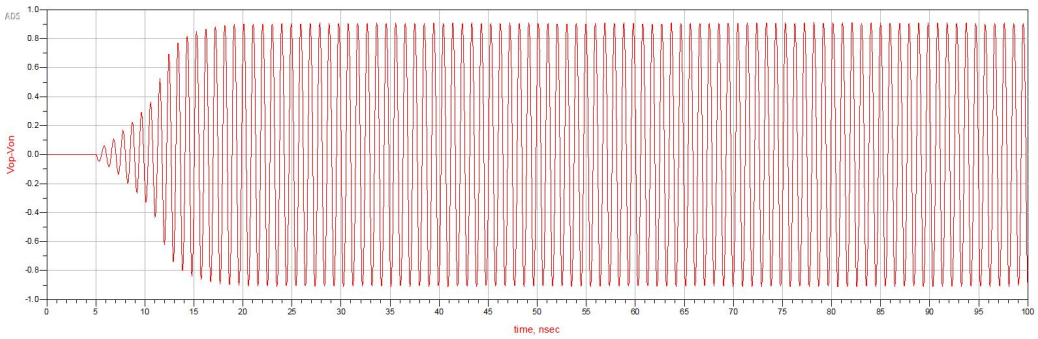


Figure 3: Voltage Controlled Oscillator Symbol and test

2 Question 2

We know that a**Differential to Single Ended** circuit is used to change the differential output of the **Voltage Controlled Oscillator (VCO)** to a one ended output. In reality this circuit is an Opamp with a current mirror, we have drawn the circuit and it is depicted below.

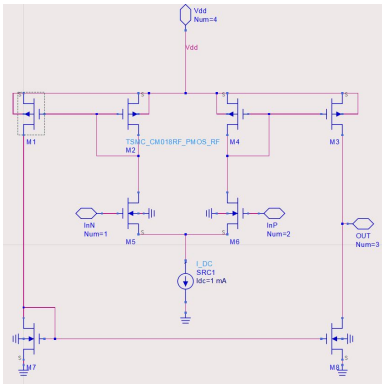


Figure 4: Differential to Single Ended

As instructed by Dr.Kamarei, for this circuit to work we need the gain of of the transistors of the differential part to be more than the other transistors, hence we need to change the $\frac{W}{L}$ ratio, we take $L = 0.18\mu m$ to be static and go on to change W accordingly, to do so we change the parameters of the **NMOS** and **PMOS** transistors.

To perform simulation, we draw the circuit in its entirity and go on to test it part by part.

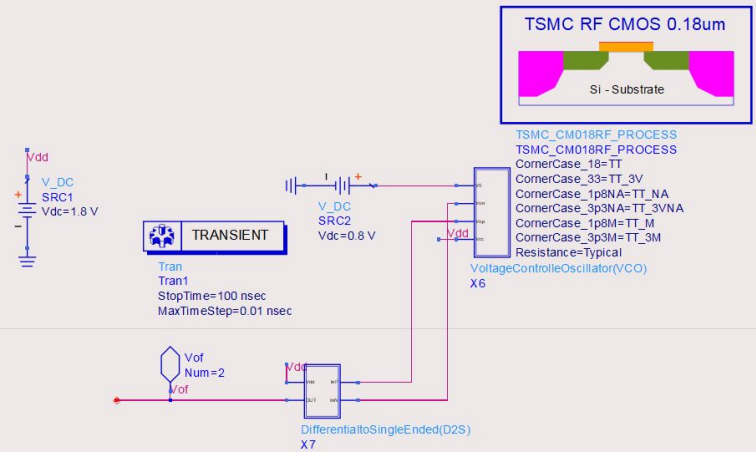


Figure 5: Differential to Single Ended

The output is as follows.

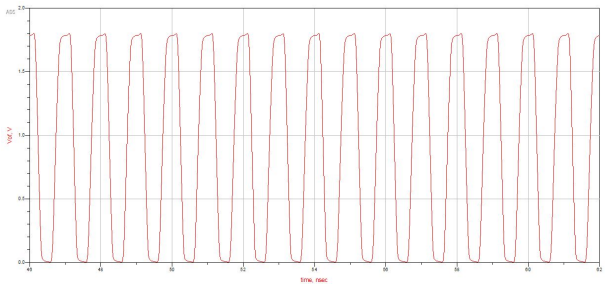


Figure 6: Differential to Single Ended output

As we can see it is somewhat close to a rectangular pulse and satisfies our needs in this question.

3 Question 3

Here we shall design the divider circuit as instructed in the project description.

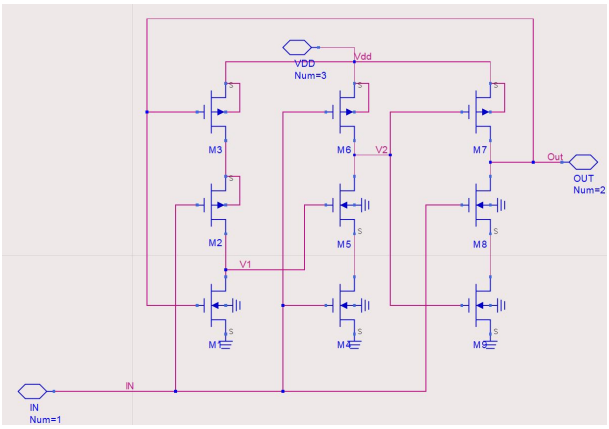


Figure 7: Divider Circuit

Now we go on to simulate it as follows.

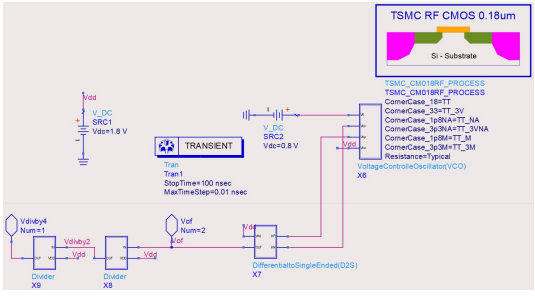


Figure 8: Divider Testing

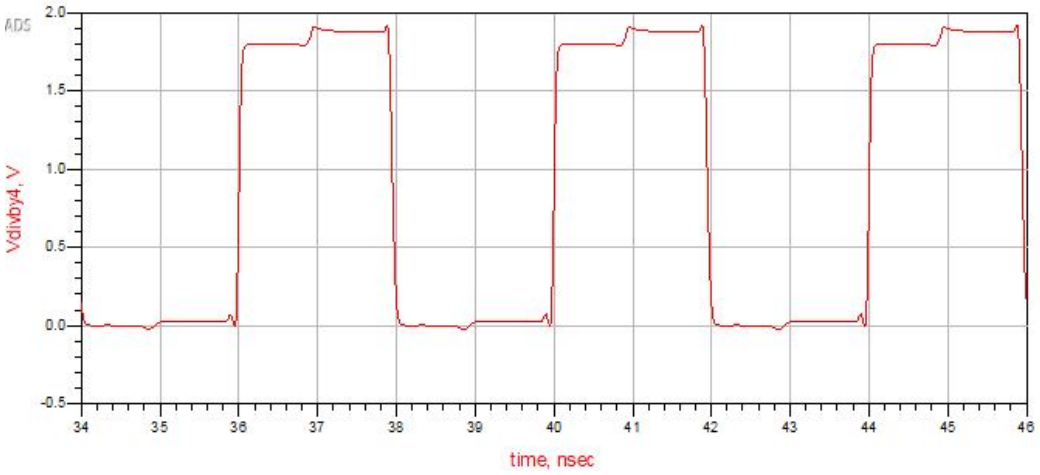


Figure 9: Divider Test

As we can see the divider is working beautifully, just to make sure we shall include the following plot.

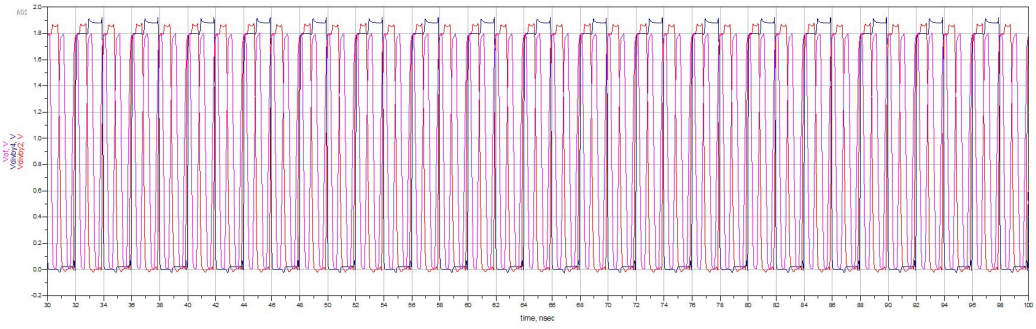


Figure 10: Divider Verification

4 Question 4

4.1 Phase Frequency Detector(PFD)

Here we shall design the **Phase Frequency Detector (PFD)**, to do so we firstly inspect the original circuit carefully.

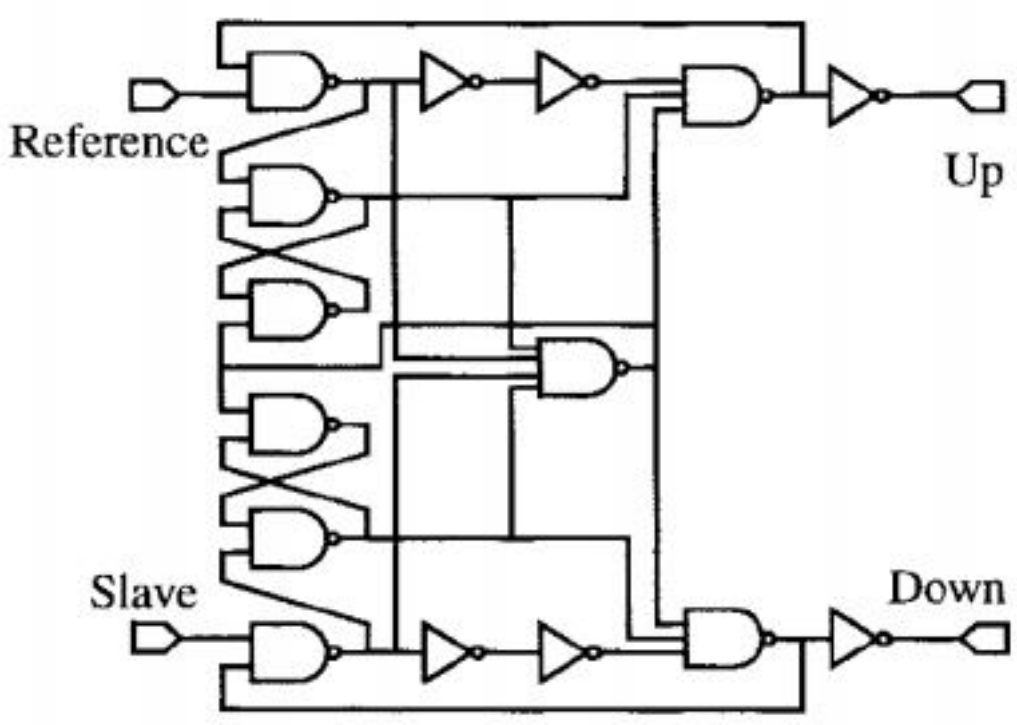
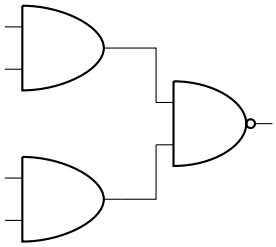


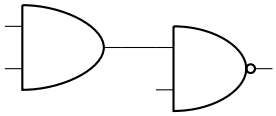
Figure 11: Phase Frequency Detector (PFD) Circuit

We don't have 3 and 4 input **NAND** gates, we shall construct them with what we learned from the **Digital Logic Design** course.

4.1.1 Three Input NAND gate implementation



4.1.2 Four Input NAND gate implementation



Using the above implementations, we design the circuit as follows.[1]

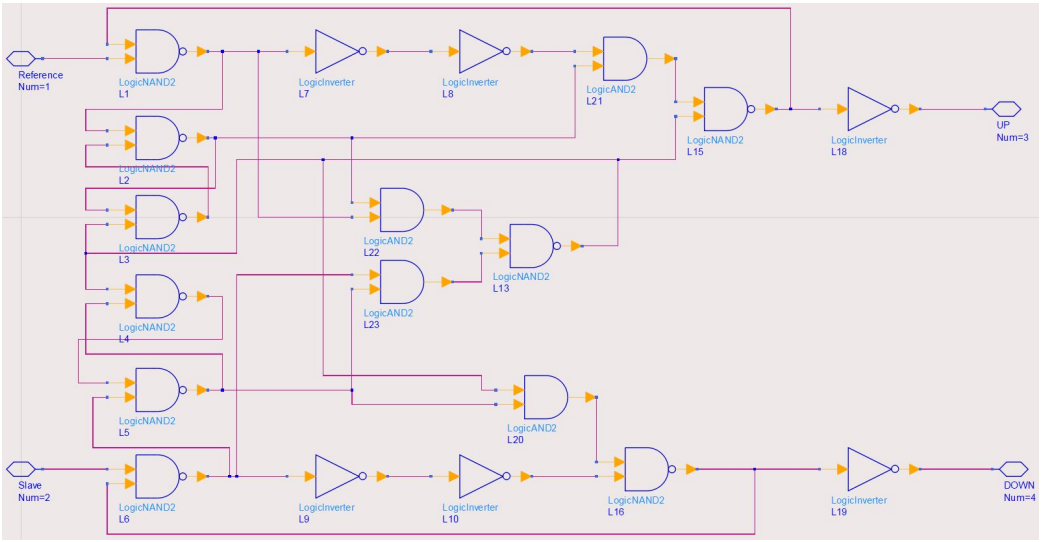


Figure 12: Phase Frequency Detector (PFD)

[1] As Mr. Kazazi implied we have used the built in PFD in the next parts.

As a second approach, we constructed the needed NAND gates and inverters with transistors, the schematics are as follows.

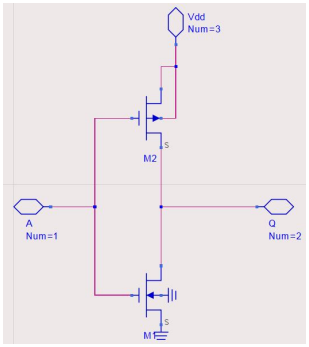


Figure 13: Inverter Transistor level

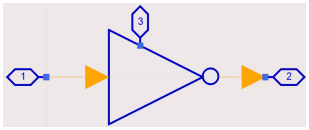


Figure 14: Inverter Transistor level symbol

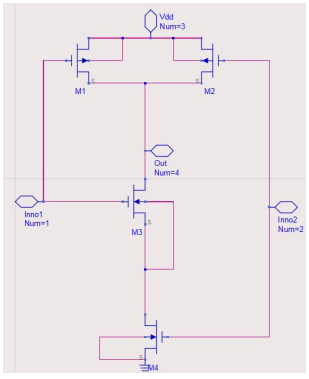


Figure 15: NAND 2 input Transistor level

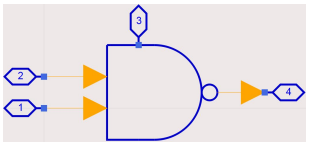


Figure 16: NAND 2 input Transistor level symbol

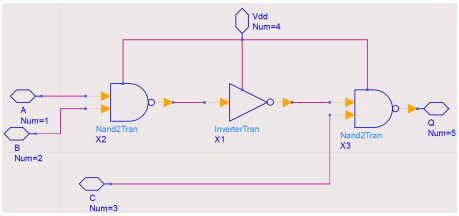


Figure 17: NAND 3 input Transistor level

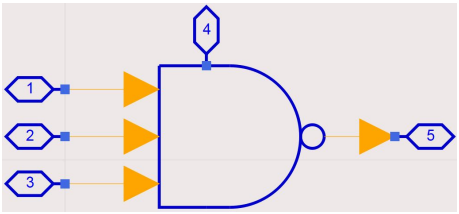


Figure 18: NAND 3 input Transistor level symbol

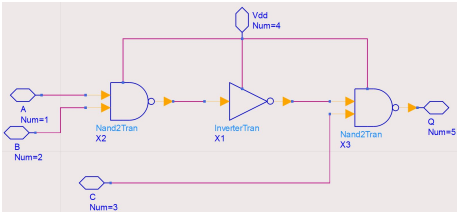


Figure 19: NAND 3 input Transistor level

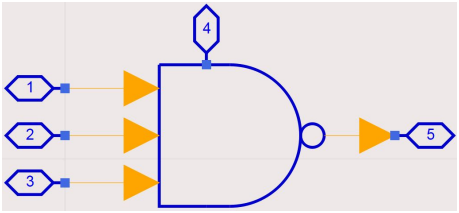


Figure 20: NAND 3 input Transistor level symbol

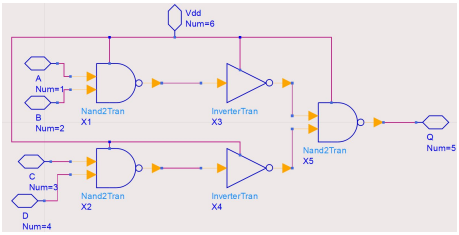


Figure 21: NAND 4 input Transistor level

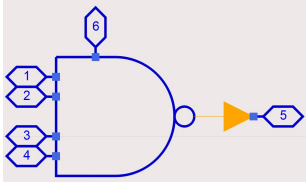


Figure 22: NAND 4 input Transistor level symbol

In the end the **PFD** is as follows.

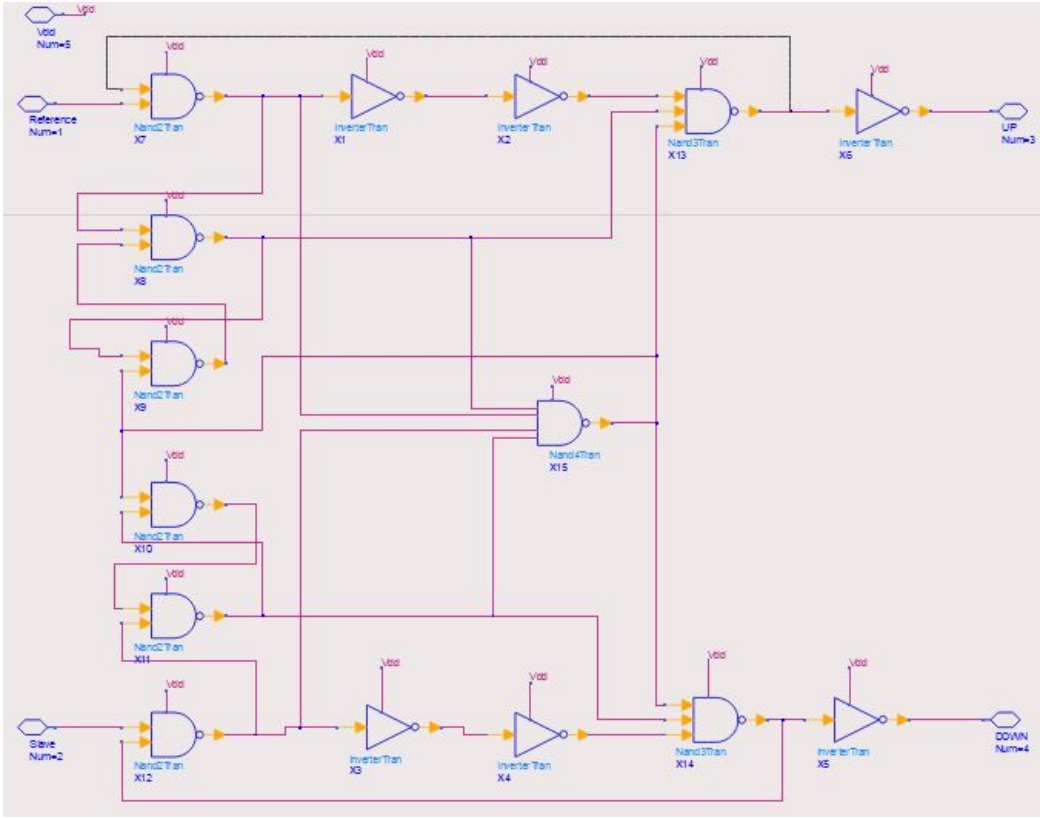


Figure 23: Phase Frequency Detector (PFD)

In the end we've used the built in **PFD** to get better results.

4.2 Charge Pump(CP)

After this, we go on to design the **Charge Pump (CP)** accordingly. First of all we inspect the circuit carefully.

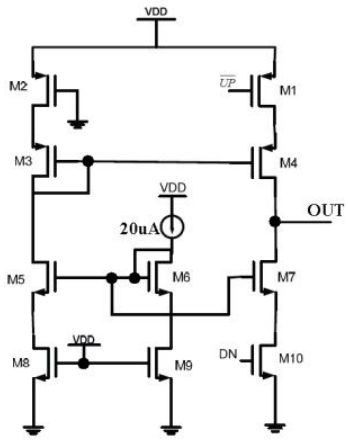


Figure 24: Charge Pump (CP)

After this we design the circuit in ADS as follows.

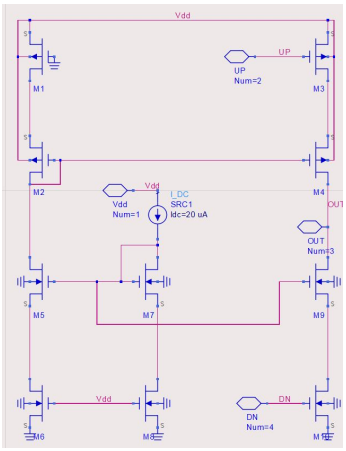


Figure 25: Charge Pump (CP)

5 Question 5

Here we shall test the design in its entirity, the design is as follows.

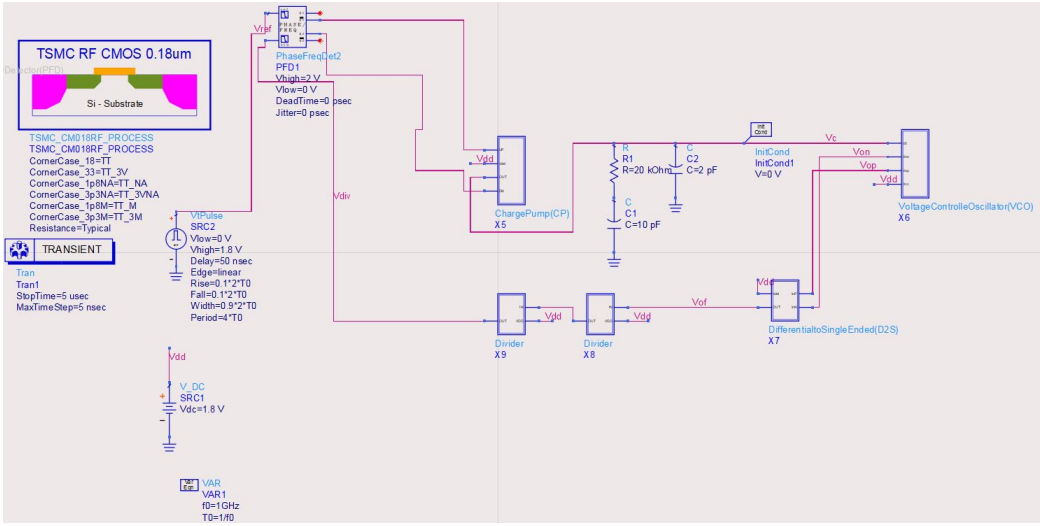


Figure 26: Phase Locked Loop (PLL)

We will include the outputs for all of the voltages for different frequencies.

5.1 $F = 950MHz$

We can see that the **Phase Locked Loop** works perfectly and it locks in this frequency.

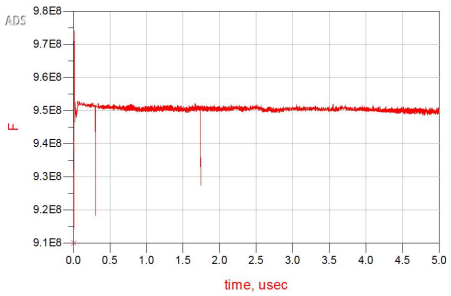


Figure 27: Phase Locked Loop functionality at $F = 950MHz$

5.2 $F = 1000MHz$

We can see that the **Phase Locked Loop** works perfectly and it locks in this frequency.

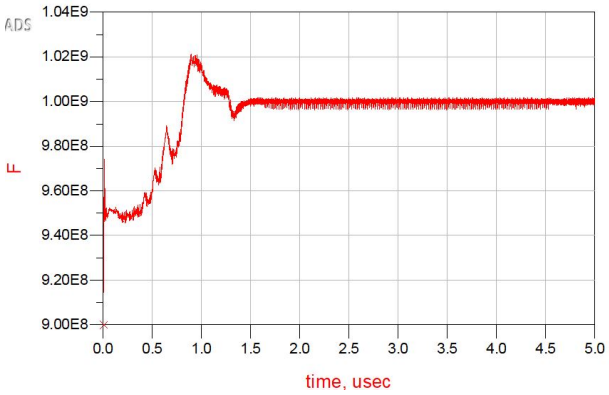


Figure 28: Phase Locked Loop functionality at $F = 1000MHz$

5.3 $F = 1050MHz$

We can see that the **Phase Locked Loop** works perfectly and it locks in this frequency.

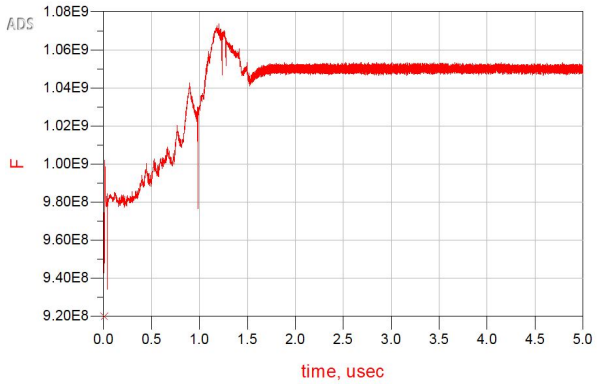


Figure 29: Phase Locked Loop functionality at $F = 1050MHz$

6 Bonus 1

In this section we shall implement the circuit exactly as depicted below.

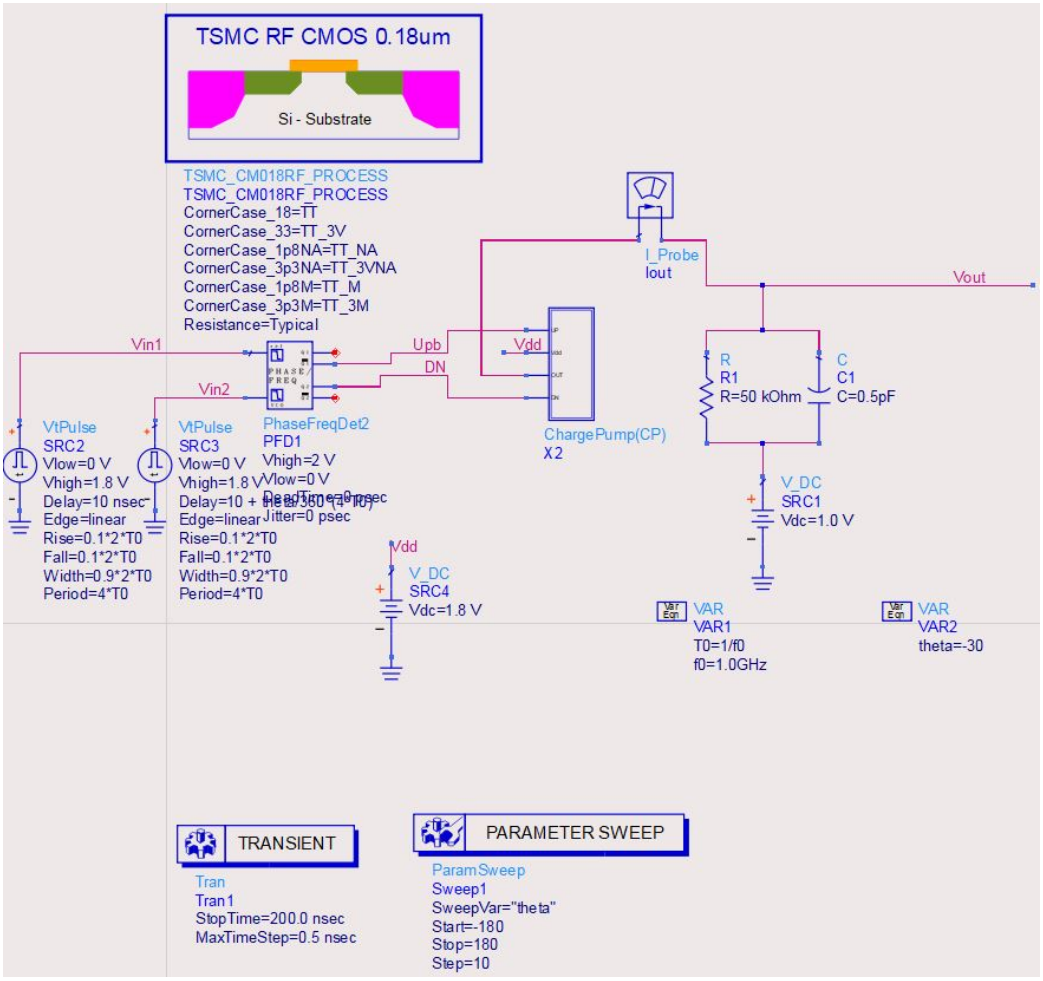


Figure 30: Bonus Circuit 1

As instructed by the course TA, we must plot the maximum amount of the probe current. The results are shown in a linear and scatter plot as follows.

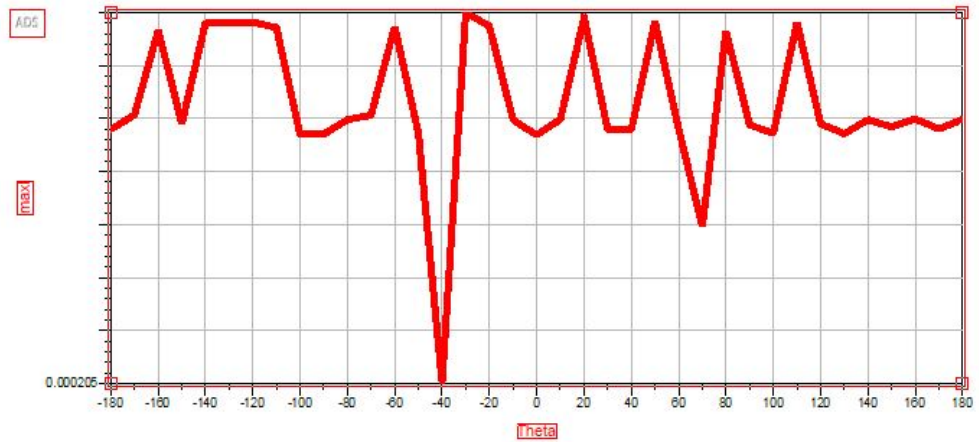


Figure 31: Maximum Probe current linear plot

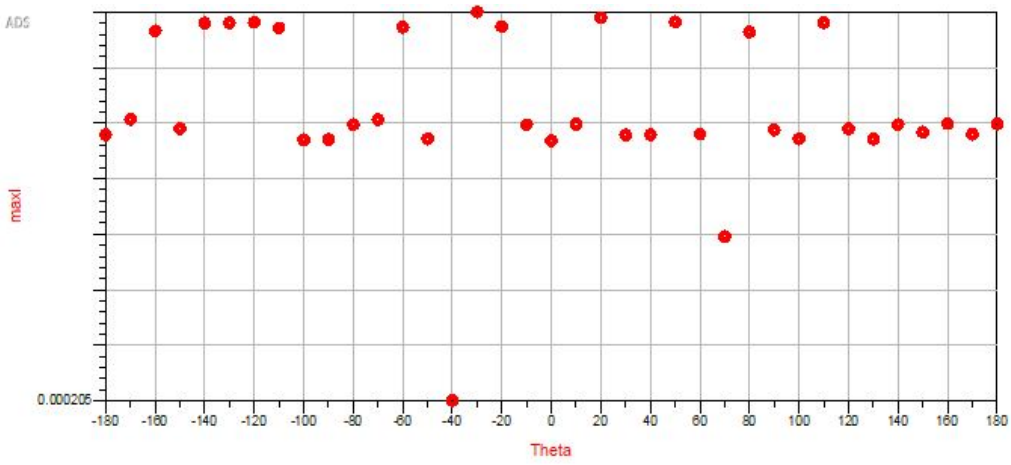


Figure 32: Maximum Probe current scatter plot

7 Bonus 2

In this section we shall implement the circuit exactly as depicted below.

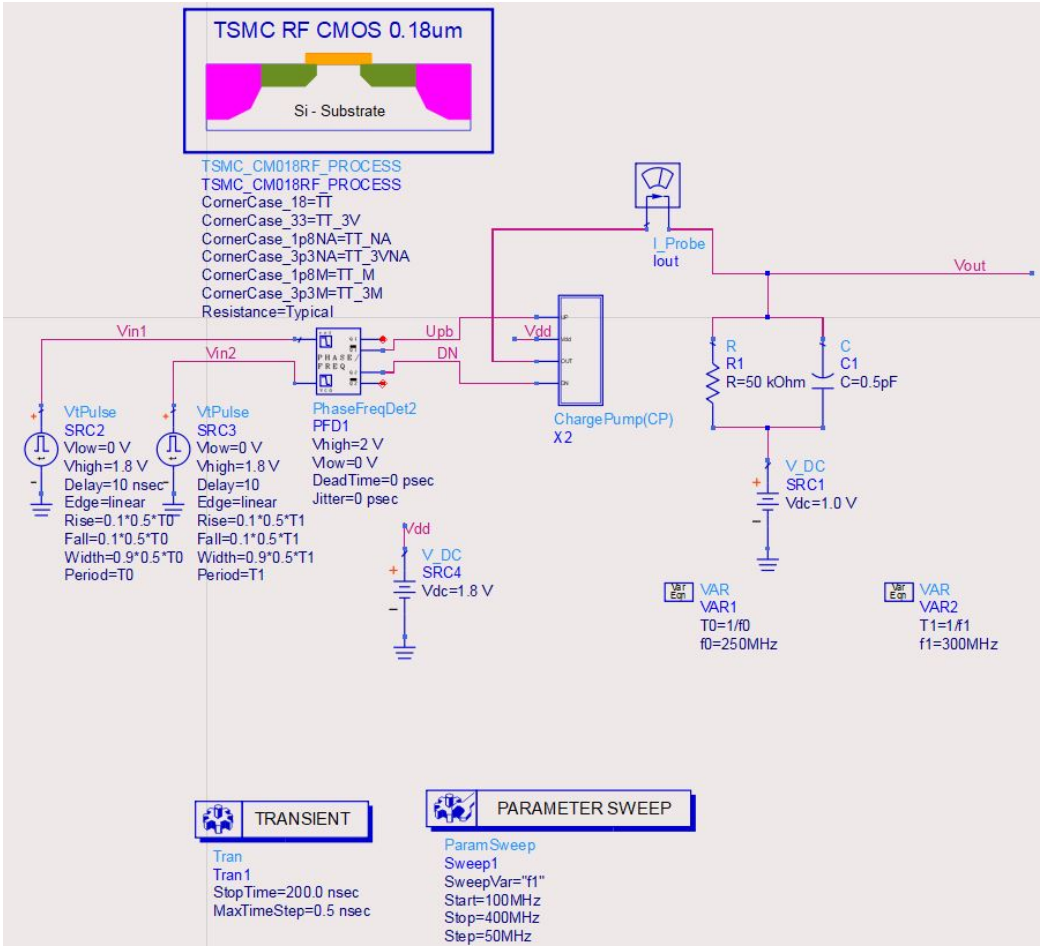


Figure 33: Bonus Circuit 2

As instructed by the course TA, we must plot the maximum amount of the probe current. The results are shown in a linear and scatter plot as follows.

Figure 34: Maximum Probe current linear plot

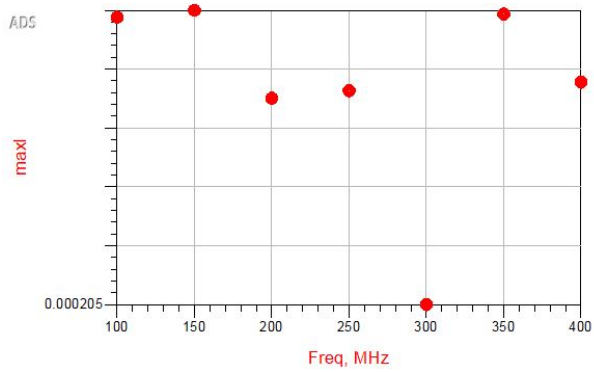


Figure 35: Maximum Probe current scatter plot

Bonus 3

As instructed, we have created symbol blocks for each part of the **Phase Locked Loop** for brevity.

References

[1] Omid Shoaei, *Electronics III, Lecture Notes, Spring 01*

[2] Zainalabedin Navabi, *Digital Logic Design, Lecture Notes, Spring 99*