UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 12, Week 16

Design of a Processing Element

Name:	**Date:**
Username:	

Approximate Taylor expansion for *cosh()* is shown below. In this problem you are to design a sequential circuit that computes an approximation of *cosh()* using the first *n* (1<*n*<16) terms of its Taylor expansion. The circuit has an approximation input that determines when to stop adding new terms to the final result.

$$\cosh(x) \cong \sum_{k=0}^{n} \frac{x^{2k}}{(2k)!}$$

The algorithm shown here can be used to approximate *cosh()*. The module issues *ready* to indicate that it is ready to accept new data to process. To start the process, a positive pulse is issued on *start*. The output *ready* becomes 0 when *start* becomes 1. After this, the module accepts a 16-bit fixed point value on its *inBus* for the *x* input, followed by the approximation value, *apx*, that appears on *inBus* on the next immediate clock.

```
e = 1;
a = 1;
for (k = 1; k < 16; k=k+2)
{
    a = a * x;
    a = a * x;
    a = a * (1/k)
    a = a * (1/(k+1))
    e = e + a;
}
```

After these two values are received, computation begins. Iterations continue until either the term being added to the result is less that the *apx* value, or the maximum iterations has reached. When done, the result becomes available on output *y* and *ready* is issued.

Assume $0 \leq x < 1$. All numbers are represented in 16-bit fixed point format. In addition, a 16-bit fixed point adder and a 16-bit fixed point array multiplier are available for you to use as datapath components. Moreover, values for $1/k$, for $1 \leq k \leq 16$, have been computed, and are stored in a combinational lookup table. The table has four address lines and a 16-bit data output.

- **a.** Show the complete datapath of *cosh()*, including the components and necessary internal control signals.
- **b.** Draw a state diagram that shows the behavior of your controller. In each state show control signals that are issued.
- **c.** Write Verilog description of the controller circuit.
- **d.** Show wiring between the datapath and the controller.