UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 11, Week 15

RTL Design

Name:	**Date:**
Username:	

1. A circuit for finding the largest data in a block of memory is to be designed. The data to be handled is in the form of 8-bit signed numbers. After a complete positive pulse appears on *go*, the circuit reads the 8-bit start address and count of the number of bytes from its *beginAddr* and *countData* input busses. The circuit starts reading data from the memory and looks for the largest data. When *countData* number of bytes have been read, the largest data will appear on the circuit *largestValue* 8-bit output. Along with this data, *done* becomes 1 and stays 1 until another *go* is issued. Reading from the memory: Our circuit has a *dataBus* and an *addressBus* for communicating with the memory. To read a data byte from the memory, our circuit issues the *readMem* signal and at the same time puts the proper address on the *addressBus*. At this time (within one clock period), the memory puts the data on the *dataBus*, and our circuit picks up data from *dataBus* and removes its *readMem* output. The circuit has a *reset* input that resets the machine in its starting state.

   a. Show the complete datapath of this circuit. Show control signals coming to the datapath.
   b. Show the controller state diagram. Show all signals issued by this controller.
   c. Show datapath and controller wiring.