UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 10, Week 14

RTL Components and a Simple RTL Design

Name:	**Date:**
Username:	

1. Using NAND gates, multiplexers, decoders (as needed), and edge-triggered D flip-flops, design an 8-bit shift register module with the functionality described in the table below.

S1	S0	Mode
0	0	Shift Right
0	1	Left Shift
1	0	Swap right most 4 bits with left-most 4 bits
1	1	Synchronous parallel load

2. Show block diagram of an 8-bit up-counter with parallel load, count-up, asynchronous reset, and carry-in inputs. The counter outputs are carry-out and eight parallel count outputs.

3. Using the counter of Problem 2 show the complete design of a waveform generator with a clock input and a wave output. A pulse of one clock duration is generated on the wave output for every 59, 191, and 99 clock pulses in this sequence. Provide an initialization mechanism that starts the sequence with 59. Show complete wiring of the counter that produces the waveform.

4. An expensive fast adder (carry lookahead) is to be used for adding 64-bit data A, B, and C. To save silicon area, only one such adder is to be used. The inputs appear on *inputBus* in three consecutive clock edges after a 1 is seen on the control input *dataArriving*. The output must appear on the 64-bit circuit output *resultBus* , along with *carryOut* after the adding is complete. When the result is ready, a one-clock duration pulse appears on the *resultReady* output simultaneous with the correct output.
   a. Show the complete datapath for this adder circuit.
   b. Show a state diagram for the control unit of this circuit.