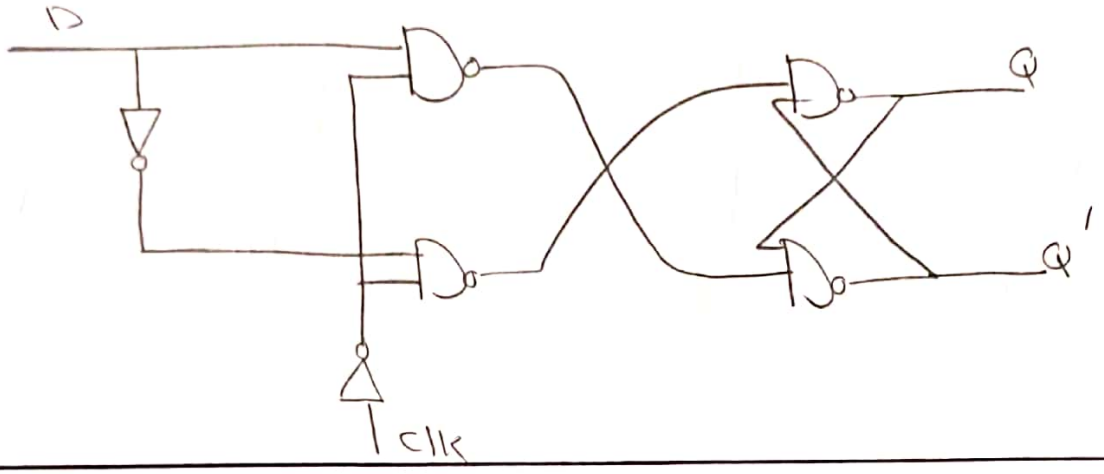
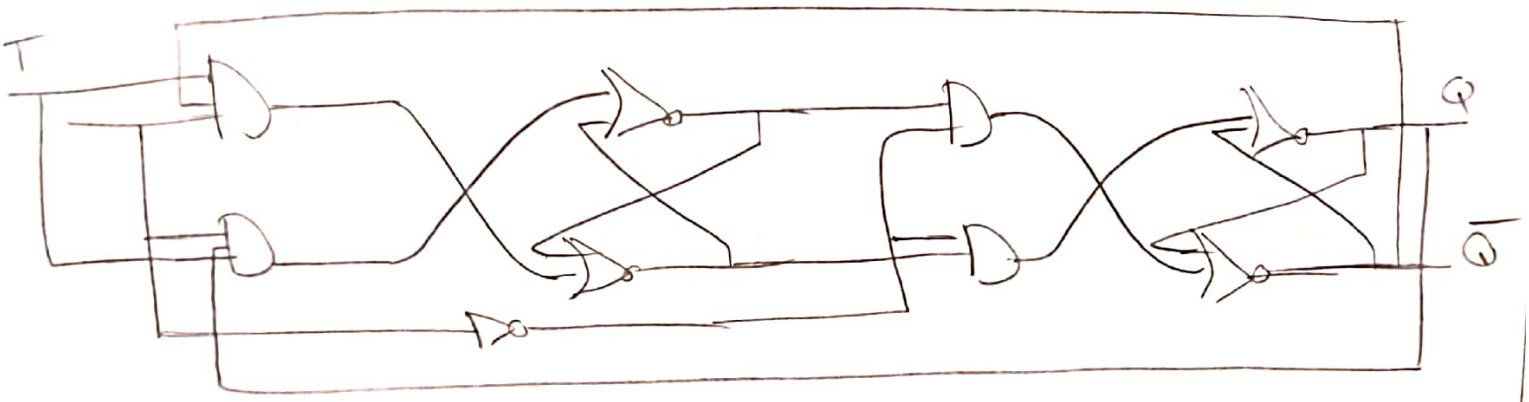
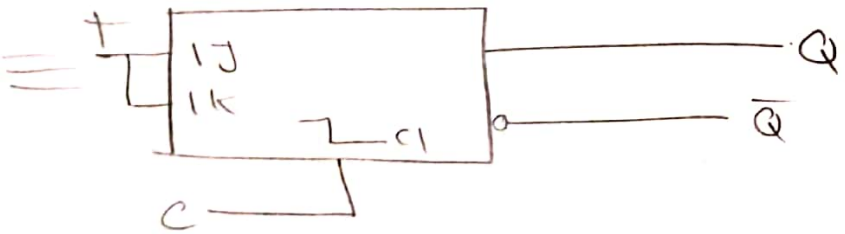
1- we modify the D-latch discussed in class tomake it work when our clk is zero.



clk	D	Q^+
0	0	1
0	1	0
1	—	Q

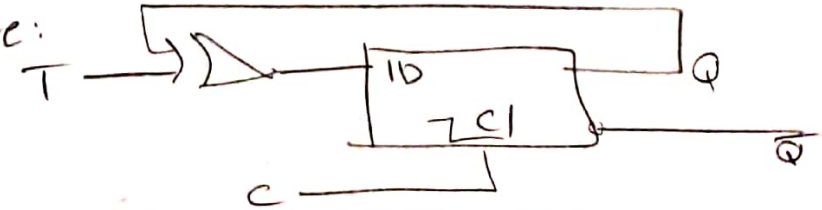
2- our flow route is to create a JK flip flop from a D flip flop then connect J, K together.



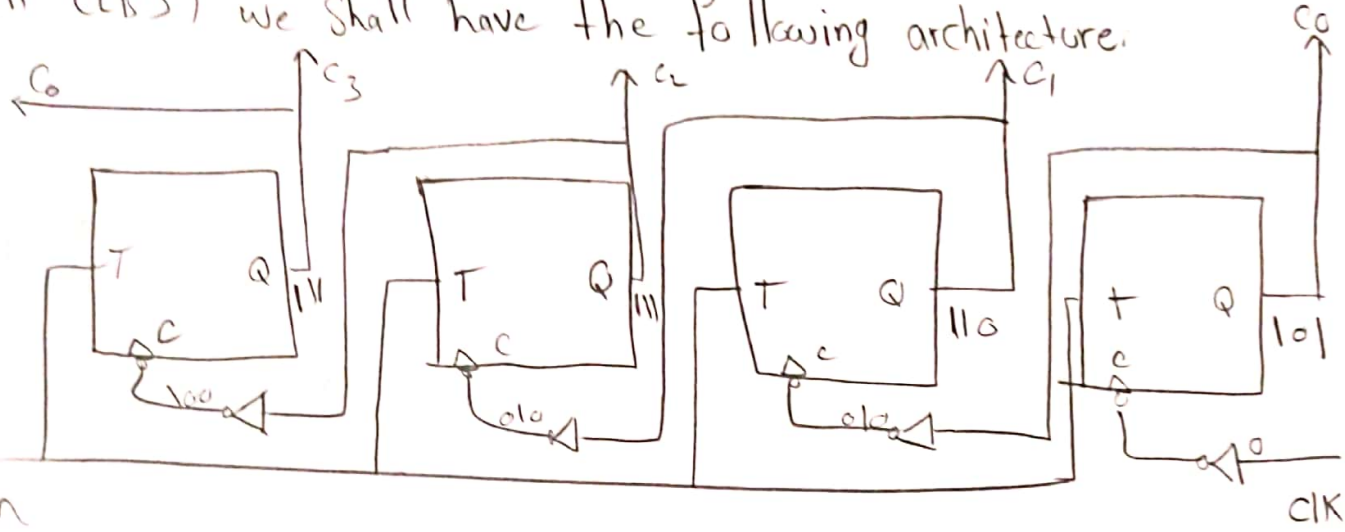


So as shown above we have created a T-flip flop.

To exclusively use D-type we have:



4- In this design, by putting an inverter on the CLK inputs (all CLK's) we shall have the following architecture.



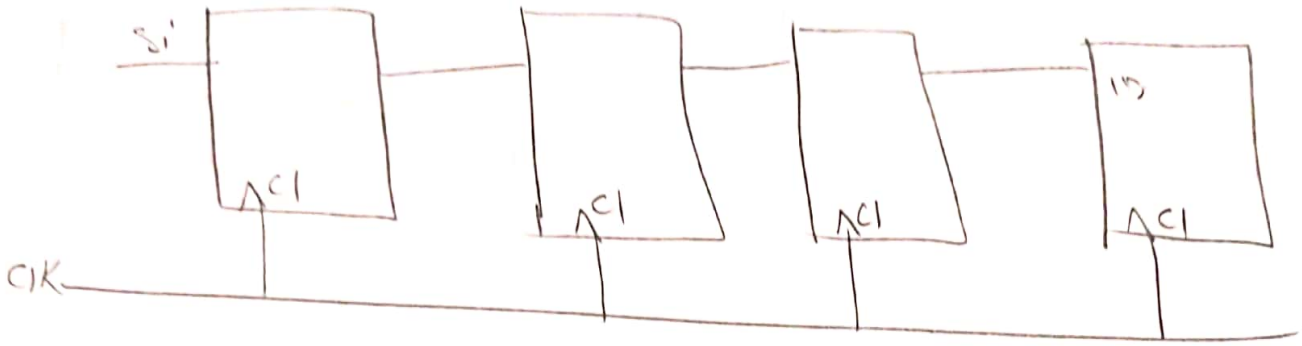
This design shall count backwards, say we start from 0000 the structure shall perform a rollover and go to 1111, then we shall reduce until we reach 0000 again. we set the en to 1 hence everytime we tick the clock the rightmost bit shall be complimented I have added the flow for a few transitions to the shape to make it more clear. (starting from all Q's being 0),

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	1	1	1	1
1	1	1	1	1	1	1	0
1	1	1	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	0	0	1	0	1	1
⋮				⋮			
1	1	1	1	0	0	0	0

→ Backwards Counting

Last, we consider that the T-flip flops are functional only when the clks go from 1 to 0 (negedge).

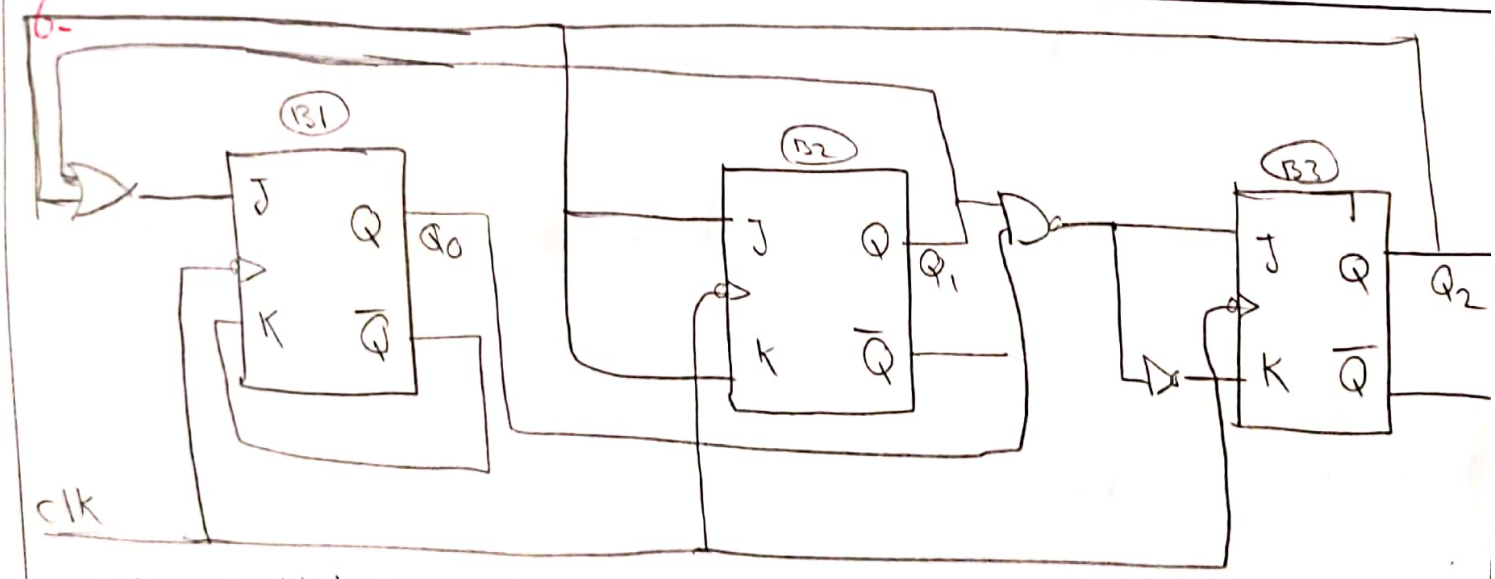
5- From Lecture 26. we recall the form of the shift register.



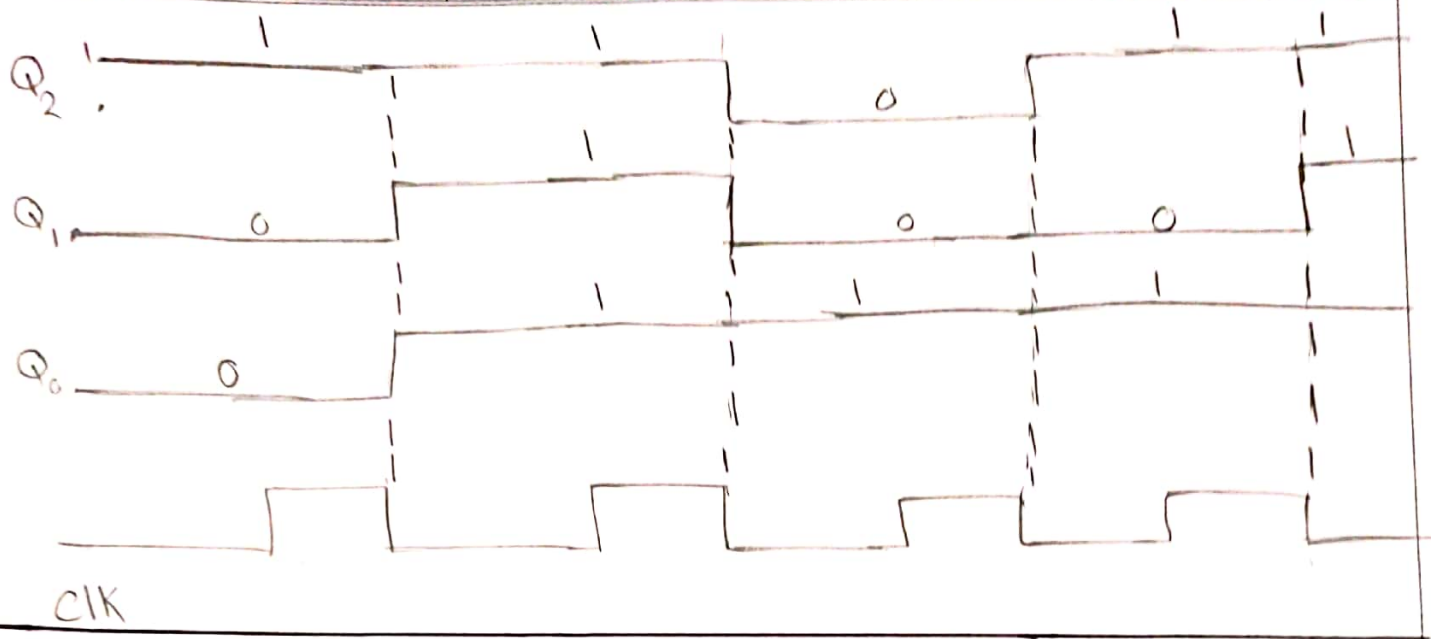
In a shift register Q_i drives D_{i-1}, So if the starting contents are 0100 and Si is 1 we have

0100 $\xrightarrow{clk1}$ 1010 $\xrightarrow{clk2}$ 1101 $\xrightarrow{clk3}$ 1110 $\xrightarrow{clk4}$ 1111 $\xrightarrow{clk5}$ 1111 ⟶ gets stuck on 1111

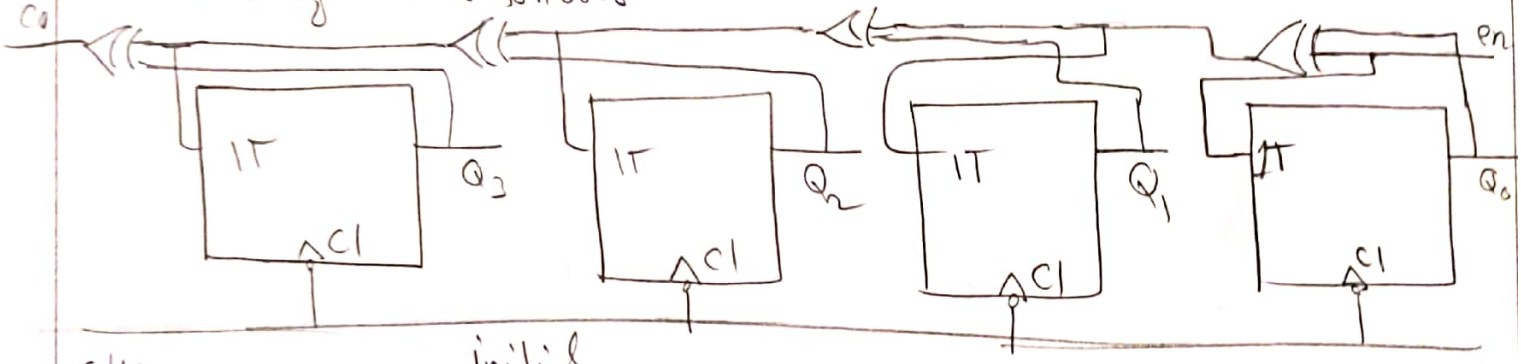
6-



the initial values are 100 — So $Q_2 = 1$ $Q_1 = 0$ and $Q_0 = 0$, Now we shall display the changes Accordingly in a waveform.



3- the design is as follows



initial

$Q_3Q_2Q_1Q_0 \rightarrow 0000$ $\quad 01 \rightarrow clk=1,\ Q_0=0$ ✓

in this case all of the T's become and we have the following flow: $0000 \rightarrow 0001 \rightarrow 0011 \rightarrow 0111 \rightarrow 1111$

the same flow will happen with any other input sequences;

$1010 \rightarrow 1011 \rightarrow 1001 \rightarrow 1101 \rightarrow 0101$