UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 8, Week 12

Counters, Shift-registers

Name:	**Date:**
Username:	

1. Write SystemVerilog description for an 8-bit up counter with a falling-edge clock, asynchronous active-low reset, active-high count-enable, active-high load-enable, carry-in, carry-out, 8-bit parallel inout, and an active high output-enable input.

2. In a schematic diagram, show how four of the counters of Problem 1 can be cascaded to generate a 32-bit counter.

3. Write SystemVerilog description for an 8-bit right-shift shift-register with a falling-edge clock, asynchronous active-low reset, active-high shift-enable, active-high load-enable, serial-in, serial-out, 8-bit parallel input, and an 8-bit shift output.

4. In a schematic diagram, show how four of the shift-registers of Part 3 can be cascaded to generate a 32-bit shift register.

5. The synchronous counter discussed in class used T flip-flops with AND gates to build a synchronous up-counter. Use XOR gates instead of the AND gates in a similar fashion to that done in class to build a new counter. What does this counter do? Write the count sequence with carry-in of 0 and carry-in of 1.

6. Available to you, there is an 8-bit up-counter with rising-edge clock, asynchronous reset, count-enable, load-enable, carry-in, carry-out, 8-bit parallel input, and an 8-bit parallel output. Use this counter to build a circuit that alternates between dividing the clock frequency by 50, 150, and 250. Provide an initialization input that sets the counter in the divide by 60 mode.

7. Write SystemVerilog description for a 4-bit up counter with a rising-edge clock, asynchronous active-high reset, active-high count-enable, active-high load-enable, carry-in, carry-out, 4-bit parallel input, and an 4-bit parallel-output. Synthesize this with Yosys and analyze the results of synthesis.