UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 7

***Latches and Flip-flops***

| **Name:** | **Date:** |
|---|---|
| **Username:** | |

1. Show design of a D-latch that works with negative clock pulses. Start with cross-coupled NAND gates.

2. Starting with a D type flip-flop, show the design of a T flip-flop.

3. In a synchronous T flip-flop-based counter the T input of each bit is formed by ANDing all previous bits together. Use XOR gates instead of the AND gates and show the count sequence for a 4-bit counter. Start with 01 on the inputs of the right-most XOR and assume initial 0000 in all flip-flops.

4. In an asynchronous T flip-flop-based counter the clock input of each bit is connected to the output of the previous bit (lower order bit), and the count input is connected to the clock input of bit 0. This way, when the clock makes a 1 to 0 transition, the counter counts up in the binary count sequence. Modify this counter structure by placing inverters on all clock inputs of the T flip-flops. Show the count sequence for a 4-bit counter.

5. A shift-register is formed by the output of a flip-flop driving the input of the next. Show the design of a 4-bit shift-register in which $Q_i$ drives $D_{i-1}$. The $D_3$ input becomes the serial input (*si*) of the shift register. If the starting contents of the shift register is 0100, and the *si* input remains at 1, what happens to the four outputs of the shift register in the next 5 clock pulses.

6. Draw a timing diagram (four complete clock cycles) for $Q_0$, $Q_1$ and $Q_2$. Assume that initial values of the flip-flops are 100. Note that flip-flops are falling edge trigger.