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Digital Systems 1

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Computer Assignment 2

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Abstract

In this assignment our goal is to design a 4-bit barrel shifter using 4-to-1 multiplexers designed in the previous assignment,then inspired by the 4-to-1 MUX we design a 16-to-1 MUX and then by getting inspiration from the 4-bit barrel shifter,we design a 16-to-1 barrel shifter.

1 Project generated files

A full view of the generated and used SystemVerilog files in my project can be seen below:

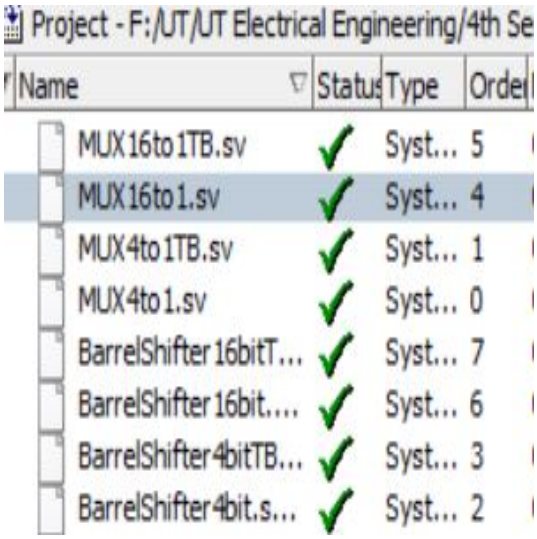

Figure 1: Generated and Compiled .sv files

2 Questions

2.1 Q1

2.1.1 Hand-Simulation

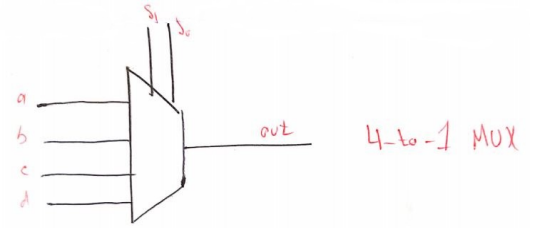

Figure 2: Hand Simulation

As requested we have used the delays of the previous project(41ns worst case to 1(111011 to 111001) and 44ns worst case to 0(011001 to 011011)),hence we shall have 41ns when the MUX's output is 1 and 44ns when the MUX's output is 0.

2.1.2 Verilog Code & Testbench

```
`timescale 1ns/1ns
module MUX4to1(input a,b,c,d,input[1:0] s,output w);
  wire [0:3] J;
  assign J={a,b,c,d};
  assign #(41,44) w=J[s];
endmodule
```

```
`timescale 1ns/1ns
module MUX4to1TB();
  logic aa=0,bb=0,cc=0,dd=0,ss0=0,ss1=0;
  logic [1:0] ss;
  assign ss={ss1,ss0};
  wire ww;
  MUX4to1 UUT(aa,bb,cc,dd,ss,ww);
  initial begin
  #50 aa=1;
  #50 aa=0;
  #50 ss0=1;
  #50 bb=1;
  #50 bb=0;
  #50 ss1=1;
  #50 dd=1;
  #50 $stop;
  end
endmodule
```

Figure 3: Verilog Code & Testbench

2.1.3 Waveform

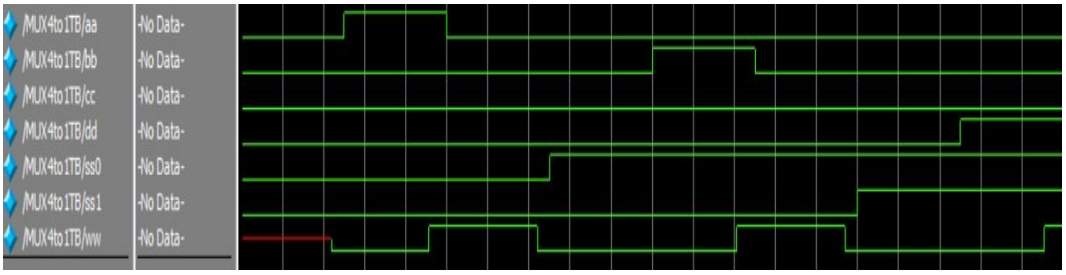

Figure 4: 4-to-1 MUX Waveform

2.2 Q2

2.2.1 Hand-Simulation

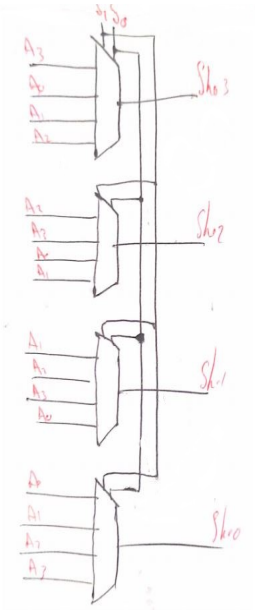

Figure 5: Hand Simulation

The 4-bit barrel shifter is in fact made out of 4 4-to-1 multiplexers,hence the delay of each shifted output is the delay of the said multiplexer for example if we want to transition from 1110 to 0111,(by changing the select from 00 to 01) the first bit must transition from 1 to 0 which shall take 44ns and the last bit must go from 0 to 1 which takes 41ns,so the delay of each shifted output depends on the transition of the MUX.

2.2.2 Verilog Code & Testbench

```
`timescale 1ns/1ns
module BarrelShifter4bit(input [3:0] a ,input[1:0] s,output [3:0] sh);
  MUX4to1 MUX1 (.a(a[3]),.b(a[0]),.c(a[1]),.d(a[2]),.s(s),.w(sh[3]));
  MUX4to1 MUX2 (.a(a[2]),.b(a[3]),.c(a[0]),.d(a[1]),.s(s),.w(sh[2]));
  MUX4to1 MUX3 (.a(a[1]),.b(a[2]),.c(a[3]),.d(a[0]),.s(s),.w(sh[1]));
  MUX4to1 MUX4 (.a(a[0]),.b(a[1]),.c(a[2]),.d(a[3]),.s(s),.w(sh[0]));
endmodule
```

```
`timescale 1ns/1ns
module BarrelShifter4bitTB();
  logic [3:0] aa=4'b1110;
  logic [1:0] ss=2'b00;
  wire [3:0] sh;
  integer i=0;
  BarrelShifter4bit UUT(aa,ss,sh);
  initial begin
  #100
  while(i<3) begin
  #100 ss=ss+1;
  i=i+1;
  end
  #100 $stop;
  end
endmodule
```

Figure 6: Verilog Code & Testbench

2.2.3 Waveform

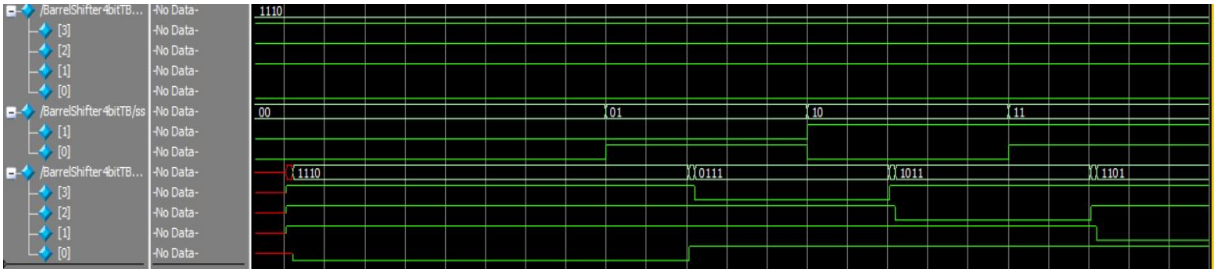

Figure 7: 4-bit Barrel Shifter Waveform

2.3 Q3

2.3.1 Hand-Simulation

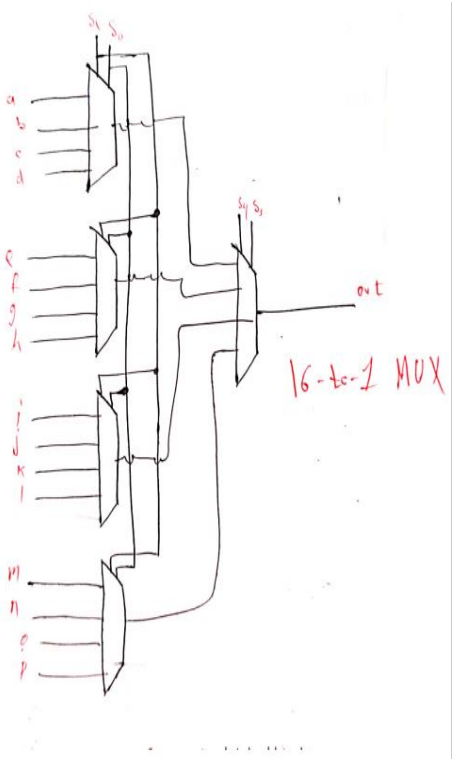

Figure 8: Hand Simulation

This MUX is made of 4 parallel 4-to-1 MUX's in series with 1 4-to-1 MUX,hence when we have 1 on the output the delay should be twice the worst case to 1 delay which is 82ns and to get 0 on the output we have twice the worst case to 0 delay which shall be 88ns,the waveform shown in the next page confirms this page.

2.3.2 Verilog Code & Testbench

```
`timescale 1ns/1ns
module MUX16to1(input [0:15] J ,input[3:0] s,output w);
      wire out1,out2,out3,out4;
      MUX4to1 MUX1 (.a(J[0]),.b(J[1]),.c(J[2]),.d(J[3]),.s({s[1],s[0]}),.w(out1));
      MUX4to1 MUX2 (.a(J[4]),.b(J[5]),.c(J[6]),.d(J[7]),.s({s[1],s[0]}),.w(out2));
      MUX4to1 MUX3 (.a(J[8]),.b(J[9]),.c(J[10]),.d(J[11]),.s({s[1],s[0]}),.w(out3));
      MUX4to1 MUX4 (.a(J[12]),.b(J[13]),.c(J[14]),.d(J[15]),.s({s[1],s[0]}),.w(out4));
      MUX4to1 MUX5 (.a(out1),.b(out2),.c(out3),.d(out4),.s({s[3],s[2]}),.w(w));
endmodule
```

```
`timescale 1ns/1ns
module MUX16to1TB();
  logic [0:15] jj=16'b0101010101010101;
  logic [3:0] ss=4'b0000;
  integer i=0;
  wire ww;
  MUX16to1 UUT(jj,ss,ww);
  initial begin
  #100 ss=0;
  while(i<15) begin
  #200 ss=ss+1;
  i=i+1;
  end
  #100 $stop;
  end
endmodule
```

Figure 9: Verilog Code & Testbench

2.3.3 Waveform

Figure 10: 16-to-1 MUX Waveform

2.4 Q4

2.4.1 Hand-Simulation

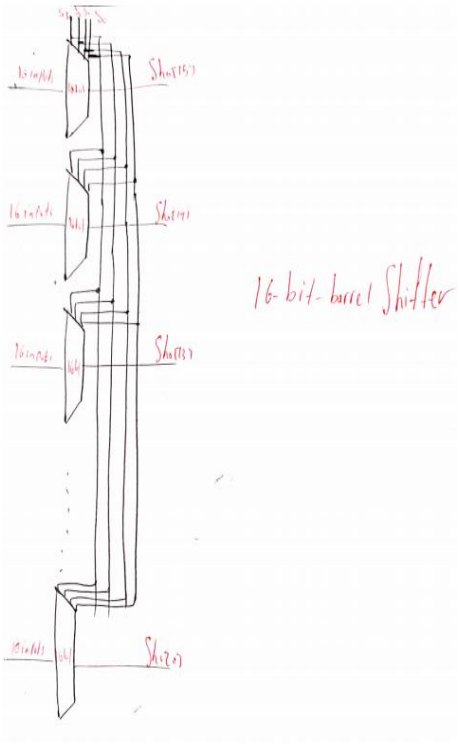

Figure 11: Hand Simulation

The 16-bit barrel shifter is in fact made out of 16 16-to-1 multiplexers,hence the delay of each shifted output is the delay of the said multiplexer for example if we want to transition from 111111111111110 to 0111111111111111,(by changing the select from 0000 to 0001) the first bit must transition from 1 to 0 which shall take 88ns and the last bit must go from 0 to 1 which takes 82ns,so the delay of each shifted output depends on the transition of the MUX.

2.4.2 Verilog Code & Testbench

```
`timescale 1ns/1ns
module BarrelShifter16bit(input [15:0] a ,input[3:0] s,output [15:0] sh );
  MUX16to1 MUX1 (.J({a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14]}),.s(s),.w(sh[15])),
           MUX2 (.J({a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13]}),.s(s),.w(sh[14])),
           MUX3 (.J({a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12]}),.s(s),.w(sh[13])),
           MUX4 (.J({a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11]}),.s(s),.w(sh[12])),
           MUX5 (.J({a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10]}),.s(s),.w(sh[11])),
           MUX6 (.J({a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9]}),.s(s),.w(sh[10])),
           MUX7 (.J({a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8]}),.s(s),.w(sh[9])),
           MUX8 (.J({a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7]}),.s(s),.w(sh[8])),
           MUX9 (.J({a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5],a[6]}),.s(s),.w(sh[7])),
           MUX10 (.J({a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4],a[5]}),.s(s),.w(sh[6])),
           MUX11 (.J({a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3],a[4]}),.s(s),.w(sh[5])),
           MUX12 (.J({a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2],a[3]}),.s(s),.w(sh[4])),
           MUX13 (.J({a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1],a[2]}),.s(s),.w(sh[3])),
           MUX14 (.J({a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0],a[1]}),.s(s),.w(sh[2])),
           MUX15 (.J({a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15],a[0]}),.s(s),.w(sh[1])),
           MUX16 (.J({a[0],a[1],a[2],a[3],a[4],a[5],a[6],a[7],a[8],a[9],a[10],a[11],a[12],a[13],a[14],a[15]}),.s(s),.w(sh[0]));
endmodule
```

```
`timescale 1ns/1ns
module BarrelShifter16bitTB();
  logic [15:0] aa=16'b1111111111111
  logic [3:0] ss=4'b0000;
  integer i=0;
  logic [15:0] ww;
  BarrelShifter16bit UUT(aa,ss,ww)
  initial begin
  while(i<15) begin
  #300 ss=ss+1;
  i=i+1;
  end
  #100 $stop;
  end
endmodule
```

Figure 12: Verilog Code & Testbench

2.4.3 Waveform

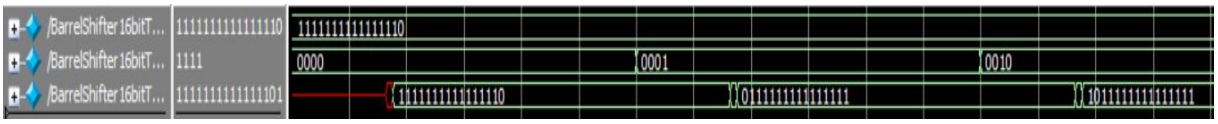

Figure 13: 16-bit Barrel Shifter Waveform