UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Spring 1399-1400

Homework 9, Week 13

Counters, Shift-registers

Name:	**Date:**
Username:	

1. Show gate level design of a Moore machine detecting the sequence 11101. Show all steps of the work until reaching gates and D flip-flops. Provide an asynchronous reset.

2. Write SystemVerilog description of a Mealy machine detecting 01010.

3. Show one-hot implementation of a Mealy detector detecting the 01010 sequence. Provide a synchronous reset.

4. Show gate level implementation of a Mealy machine detecting 0110 sequence on its J input. Use T type flip-flops.

5. Show gate level design of a Moore machine that detects 101 and 110 on its J input. If in three consecutive clock periods either sequence is detected the output becomes 1 and remains 1 for exactly one clock cycle. Assign binary numbers for the states of the machine (binary encoding) and use D flip-flops in your final implementation.

6. Input A[1:0] contains 2-bit binary numbers that appear synchronous with a clock input. Show the design of a circuit that continuously receives A, and calculates MOD-6 of sum of all numbers every received on A.

7. Write SystemVerilog description of a shift register with two control inputs I_0 and I_1. The shifter has a master clock-enable and a serial input and has the following functionalities:
    a. I_0,I_1 = 0,0: Shift right one place, using *sin*;
    b. I_0,I_1 = 0,1: Shift right two places, using *sin*;
    c. I_0,I_1 = 1,0: Rotate right one place;
    d. I_0,I_1 = 1,1: Parallel load.

8. Write SystemVerilog description of a Mealy machine detecting 0101, and the Moore implementation of the same sequence.
    a. In a timing diagram show an input sequence that makes the outputs of the two circuits to be different.
    b. Using Yosys, synthesize the two circuits and compare the results.
    c. Optional: Perform post synthesis simulation of the netlist generated by Yosys.