1- 6539 $\xrightarrow{\text{Binary representation}}$ 1100110000111 ⟶ 13 bits for unsigned Binary representation.

6539 $\xrightarrow{\text{BCD}}$ 0110 0101 0011 1001 ⟶ 16 bits

2- Both of the 4-bit gray code and binary code are useful number system which are depicted below and can be converted to eachother in a manner which I shall explain shortly.

Binary Code:		Gray Code:	
0	0000	0	0000
1	0001	1	0001
2	0010	2	0011
3	0011	3	0010
4	0100	4	0110
5	0101	5	0111
6	0110	6	0101
7	0111	7	0100
8	1000	8	1100
9	1001	9	1101
10	1010	10	1111
11	1011	11	1110
12	1100	12	1010
13	1101	13	1011
14	1110	14	1001
15	1111	15	1000

Now we want to convert Binary to gray code, if we compare the most significant bit (MSB) of these two codes in all cases they are the same.

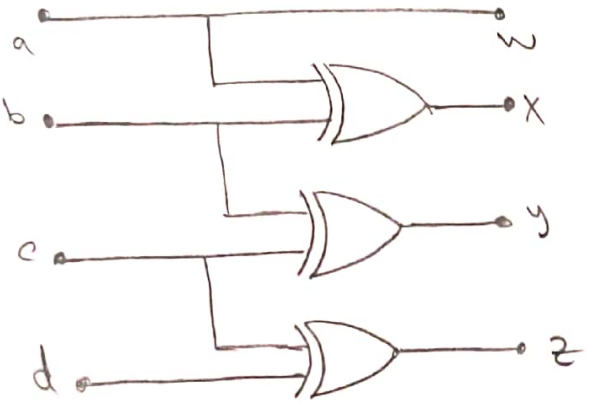
to find the other bits of the gray code from binary we do the following

To find the n^{th} bit of the gray code from binary we must perform XOR on the $(n-1)^{th}$ and n^{th} bit of the binary number and put it as the n^{th} bit of the gray code

example : 1011 (binary) → 01 XOR 1, 10 XOR 1, 11 XOR 0 → 1110 (gray code)

Gate implementation:

abcd (binary) → wxyz (gray)

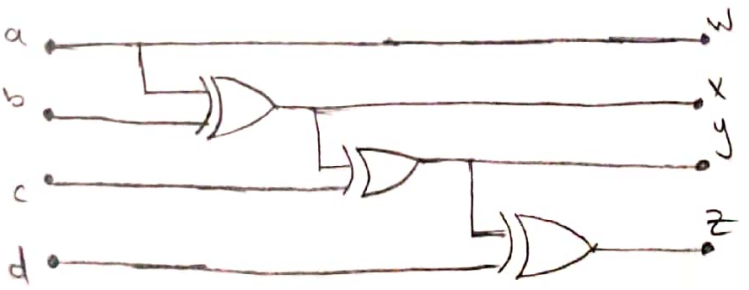


Now we shall convert gray code to binary.

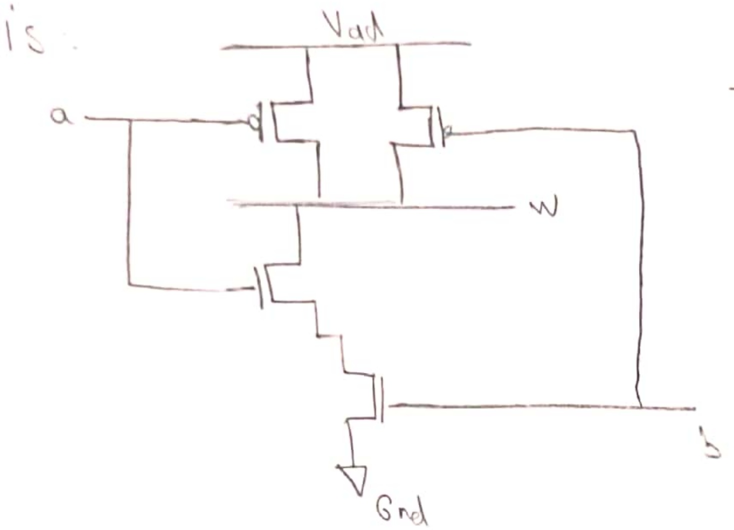
To do this, we note that the MSB for gray code and binary code are the same, for the n^{th} bit we check the gray code, if its n^{th} bit is 1, then the n^{th} bit for binary shall be the complement of the $(n-1)^{th}$ bit of the binary number and if the gray code's n^{th} bit is 0 the n^{th} bit of the binary number shall be its $(n-1)^{th}$ bit

Gate implementation:

abcd (gray) → wxyz (binary)



3. For inputs a and b and output w the boolean form of the NAND gate shall be: $w = \overline{a.b}$ and the CMOS implementation is:



Truth table:

a	b	w
1	1	0
1	0	1
0	1	1
0	0	1

nmos: # (3,5,7)

Pmos: # (4,6,8)

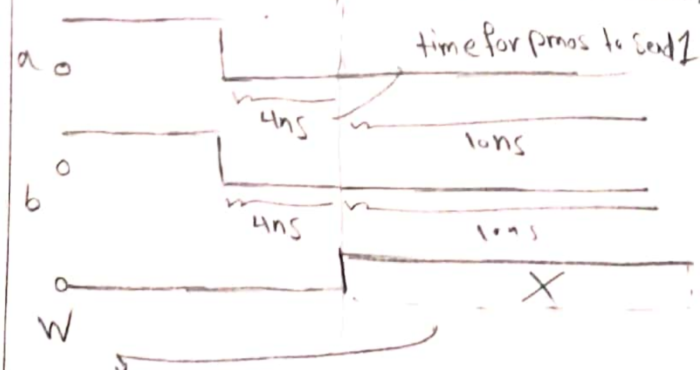
Worst Case Delay to 1: For us to have 1 on the output one of the pmos transistors should conduct, which means we need 4 nano seconds for it. both the nmos transistors should send Z so the worst case delay to 1 shall be: 7+7 = 14ns

Worst Case Delay to 0: To have 0 on the output we must get Z from at least one of the pmos transistors which takes a minimum of 8 nano seconds and both the nmos transistors must send 0 so the delay is 5+5 = 10ns

Worst Case to 1 Delay waveform:

a b w → a b w (can also be 0 1 / 1 0, no difference)

1 1 0 → 0 0 1



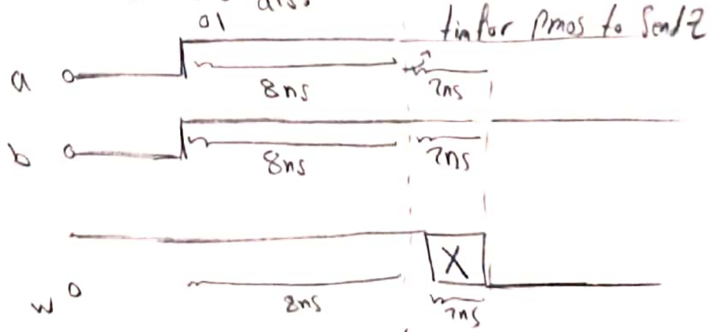
in this part the pmos is sending 1 and the nmos's don't send Z yet so we have X

Worst Case to 0 Delay waveform:

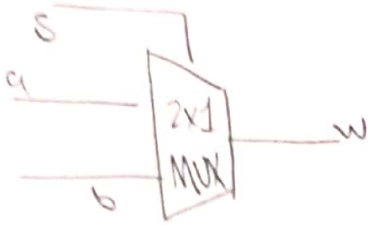
a b w → a b w

0 0 1 → 1 1 0

↳ can be 1 0 / 0 1 also.



4- Here I shall create a 2x1 MUX, for inputs a, b and S as the Select Value a simple Schematic and truth table is depicted below:



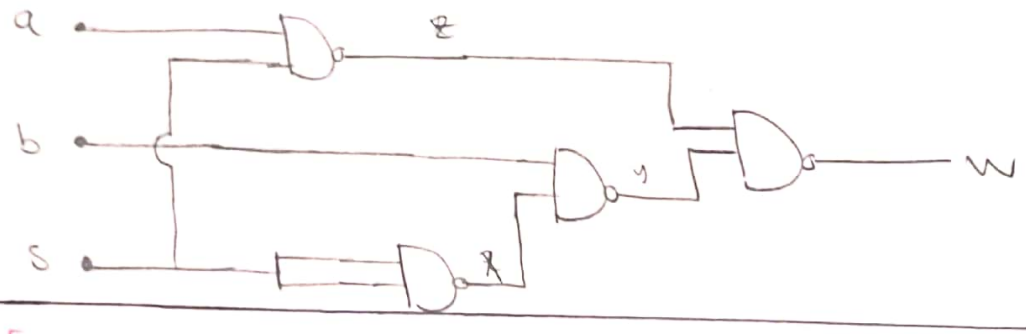
Truth table:

a	b	S	W
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

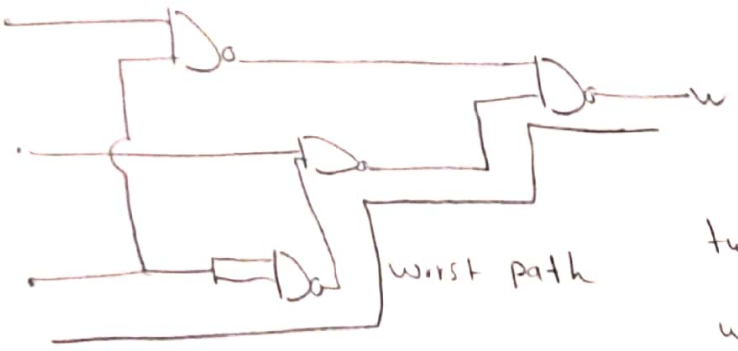
Boolean:

$W = \bar{S}.a + S.b$

NAND gate implementation of MUX:



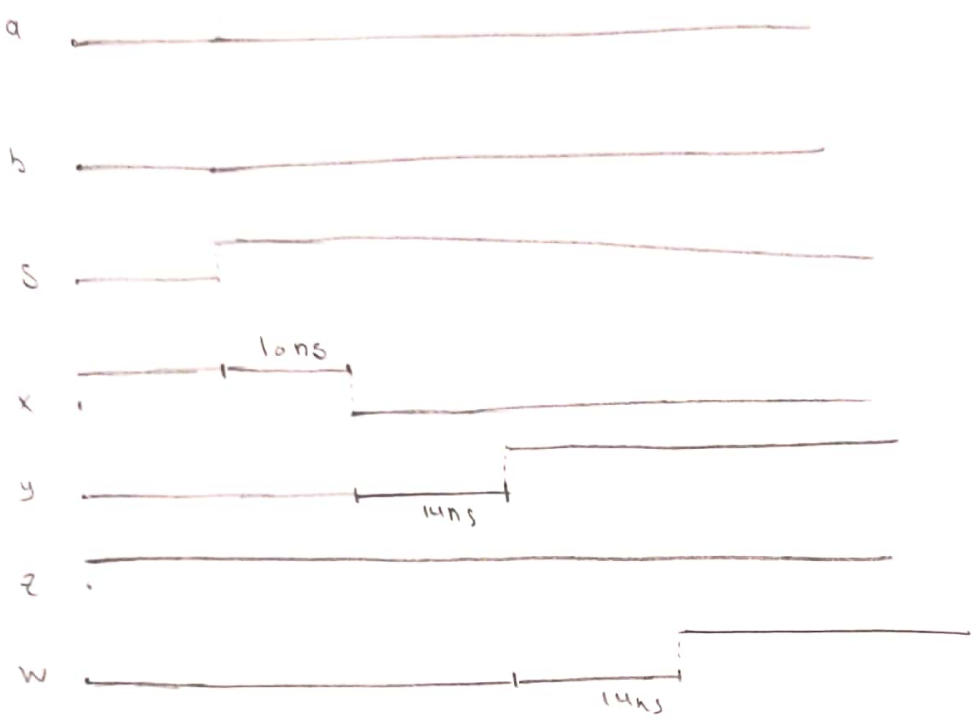
5- In question 3 the worst case to 1 for a nand gate was: 14ns and the worst case to 0 was: 10 ns here we shall use these delays. The worst path we can choose is depicted below



for all scenarios we worst thing that can happen is two worst case to 1 Delays and one worst case to 0, this is the worst case all in all which is: 111+14+10 = 38ns

To generate the waveform we have:

a	b	s	a.b.s
0	1	0	0
			1



Delay: 14+14+10 = 38ns

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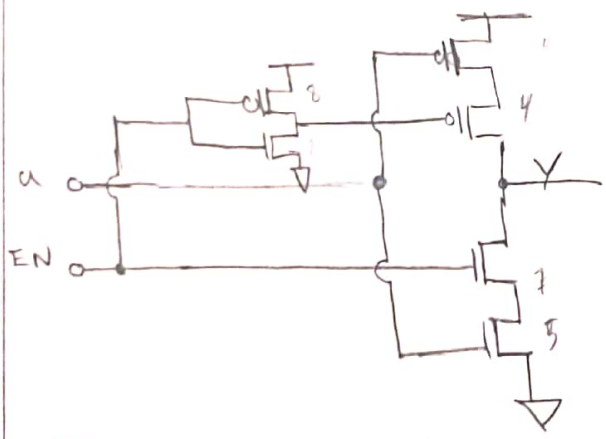
c- We draw the structure and its truth table accordingly:



truth table:

nmos: #(3,5,7)

pmos: #(4,6,8)

a	EN	Y
1	1	0
1	0	Z
0	1	1
0	0	Z

To 0: We must have Z from the upper part and 0 from the lower nmos transistors. if a=EN=1 the lower nmos's shall have 4ns delay, for the upper part we have 8ns delay for the pmos in the inverter and another 8ns for the pmos which is connected to the inverter, the

Upper pmos transistor shows the same manner, So: Delay = 16ns

To 1: For this to happen a=0, EN=1 in this case the lower part of the structure has a 14ns Delay, and the pmos of the inverter shall have an 8ns delay and the lower pmos connects in 4ns hence we have 8+4=12ns So: Delay = 14ns

To 2: The Delay for a=EN=0 is greater than the other form So I shall write this one only. In this case we shall have to 2 delays for the lower nmos transistors which is 14ns. for the inverter we have a 7ns nmos delay and for the following pmos we have 8ns delay So. Delay: 8+7 = 15ns

7- For the first we shall find the time needed to go from $0.9V_0$ to $0.1V_0$

$V = V_0 e^{\frac{-t}{RC}}$ $0.9V_0 = V_0 e^{-t_1/RC}$ (1) $0.1V_0 = V_0 e^{\frac{-t_2}{RC}}$ (2) $\frac{(1)}{(2)}$ ⟶

$9 = e^{\frac{\Delta t}{RC}}$ ln ⟶ $\frac{\Delta t}{RC} = \ln 9$ ⟶ $\Delta t = RC/\ln 2 \simeq 2.19\,RC$

For the second part a reasonable approximation could be $0.001V_0$ Similar to the last part we have: $1000 = e^{\frac{\Delta t}{RC}}$ ln ⟶ $\Delta t = RC/\ln(1000) \simeq 6.9\,RC$

To find Δt when going from V_0 to $0.5V_0$ we have (Similar to previous parts) $V_0 = V_0 e^{-t/RC}$ (1) $0.5V_0 = V_0 e^{\frac{-t}{RC}}$ (2) $\frac{(1)}{(2)}$ ⟶ $2 = e^{\frac{\Delta t}{RC}}$ ln ⟶ $\Delta t = RC/\ln 2 \simeq 0.69\,RC$