1. Description

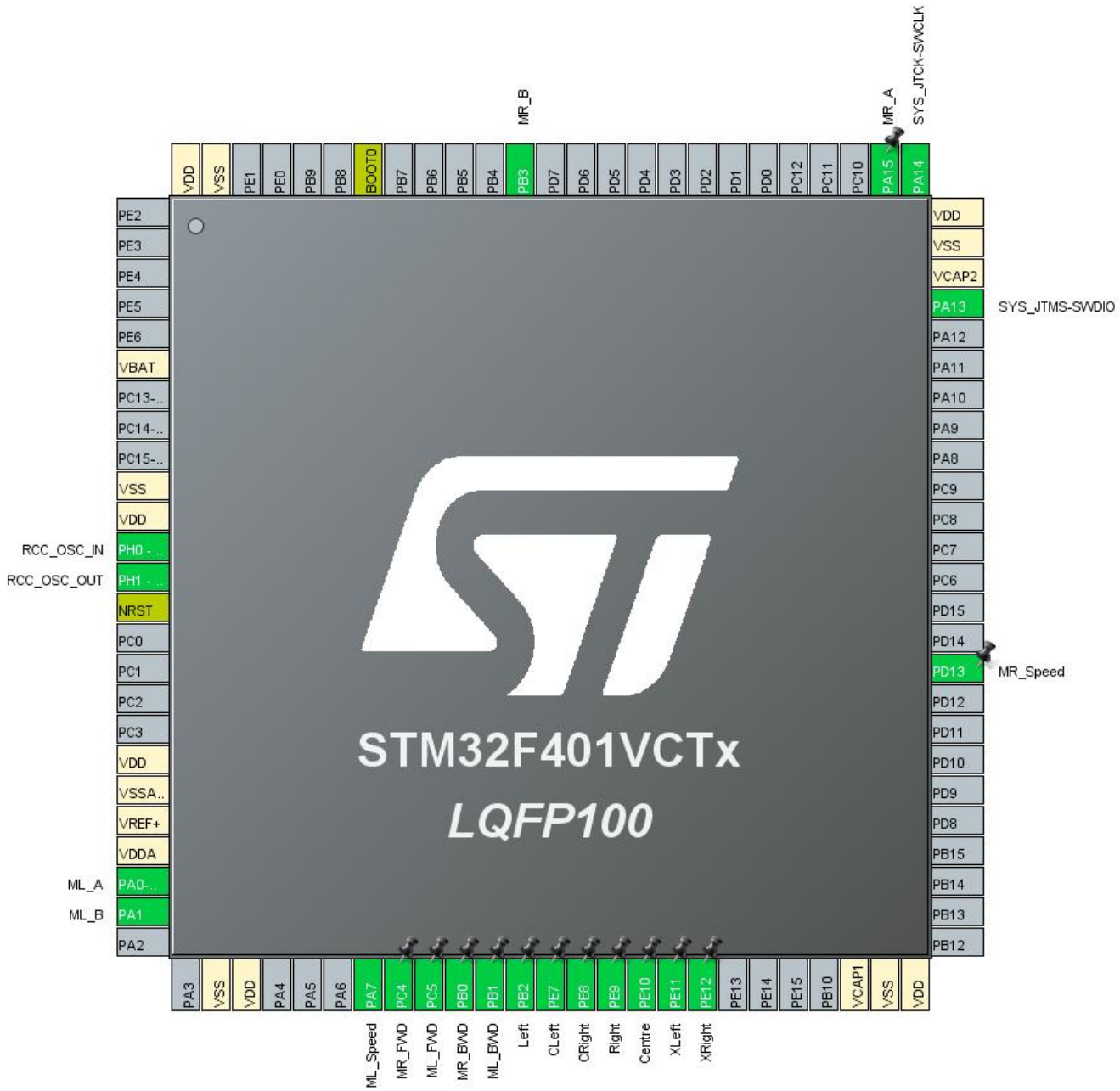
1.1. Project

Project Name	FST
Board Name	STM32F401C-DISCO
Generated with:	STM32CubeMX 5.5.0
Date	02/04/2020

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



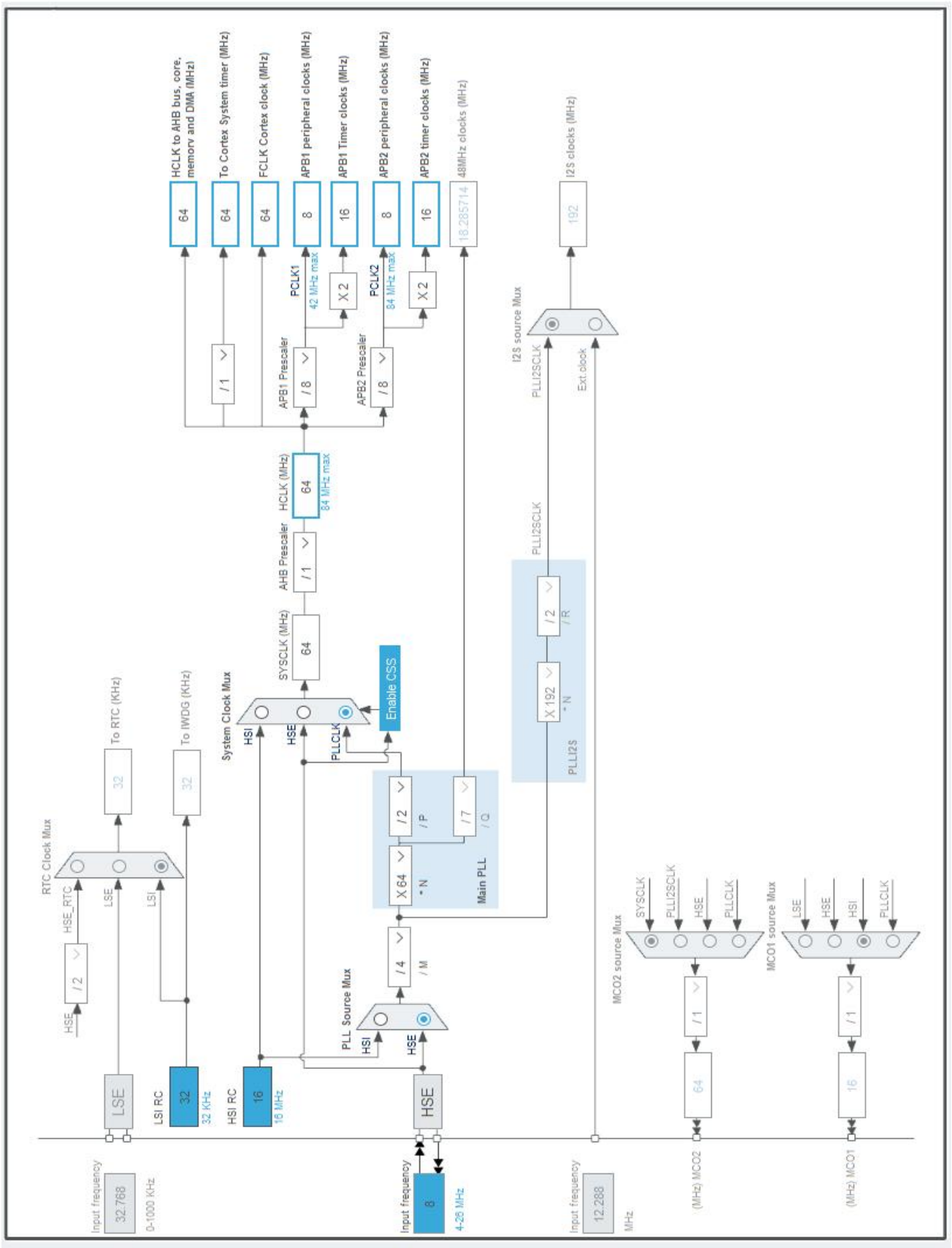
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0 - OSC_IN	I/O	RCC_OSC_IN	
13	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA/VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	ML_A
24	PA1	I/O	TIM5_CH2	ML_B
27	VSS	Power		
28	VDD	Power		
32	PA7	I/O	TIM3_CH2	ML_Speed
33	PC4 *	I/O	GPIO_Output	MR_FWD
34	PC5 *	I/O	GPIO_Output	ML_FWD
35	PB0 *	I/O	GPIO_Output	MR_BWD
36	PB1 *	I/O	GPIO_Output	ML_BWD
37	PB2 *	I/O	GPIO_Input	Left
38	PE7 *	I/O	GPIO_Input	CLeft
39	PE8 *	I/O	GPIO_Input	CRight
40	PE9 *	I/O	GPIO_Input	Right
41	PE10 *	I/O	GPIO_Input	Centre
42	PE11 *	I/O	GPIO_Input	XLeft
43	PE12 *	I/O	GPIO_Input	XRight
48	VCAP1	Power		
49	VSS	Power		
50	VDD	Power		
60	PD13	I/O	TIM4_CH2	MR_Speed
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	TIM2_CH1	MR_A

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
89	PB3	I/O	TIM2_CH2	MR_B
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	FST
Project Folder	C:\Users\souha\STM32CubeIDE\workspace_1.2.0\FST
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.2

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401VCTx
Datasheet	024738_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. GPIO

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 2

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. TIM1

Clock Source : Internal Clock

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**20 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

7.5. TIM2

Combined Channels: Encoder Mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.6. TIM3

Channel2: PWM Generation CH2

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.7. TIM4

Channel2: PWM Generation CH2

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM5

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MR_A
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MR_B
TIM3	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ML_Speed
TIM4	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MR_Speed
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ML_A
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ML_B
GPIO	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MR_FWD
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ML_FWD
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MR_BWD
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ML_BWD
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Left
	PE7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CLeft
	PE8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CRight
	PE9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Right
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Centre
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	XLeft
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	XRight

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report