

Design & Layout of Dynamic CMOS logic circuit

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Dynamic CMOS logic circuit

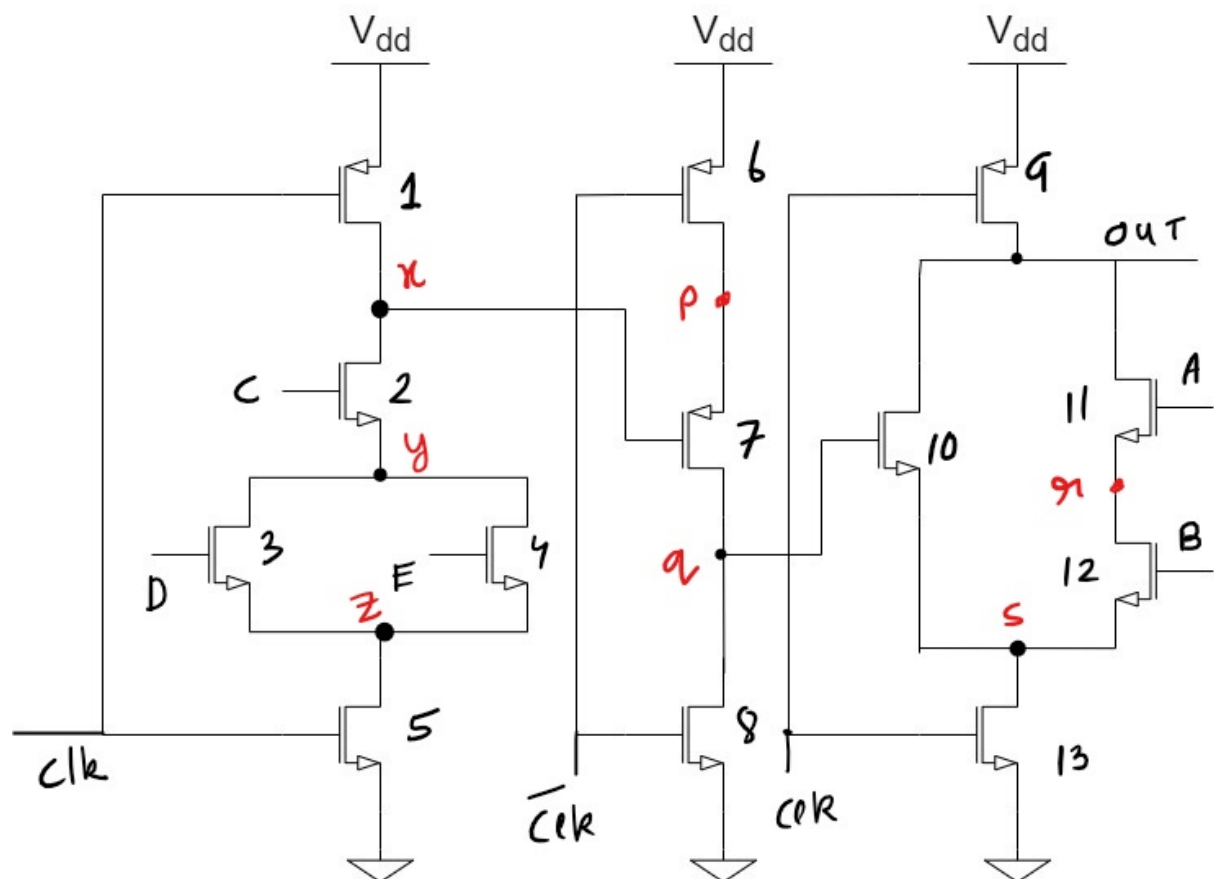
Given logic:

$$(AB + C(D + E))'$$

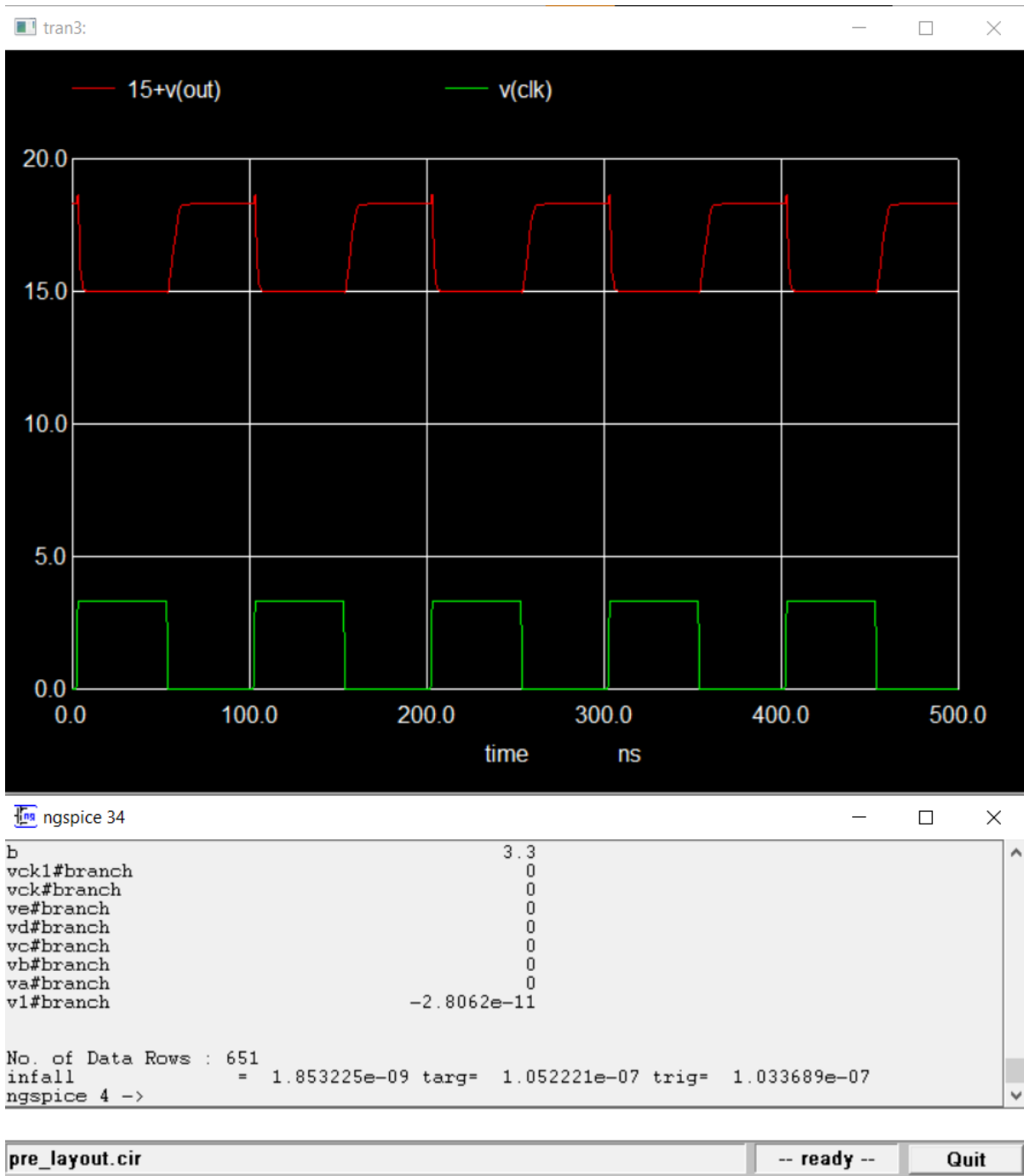
Dynamic style used :

Zipper Style

Circuit Diagram



PRE-LAYOUT SIMULATION

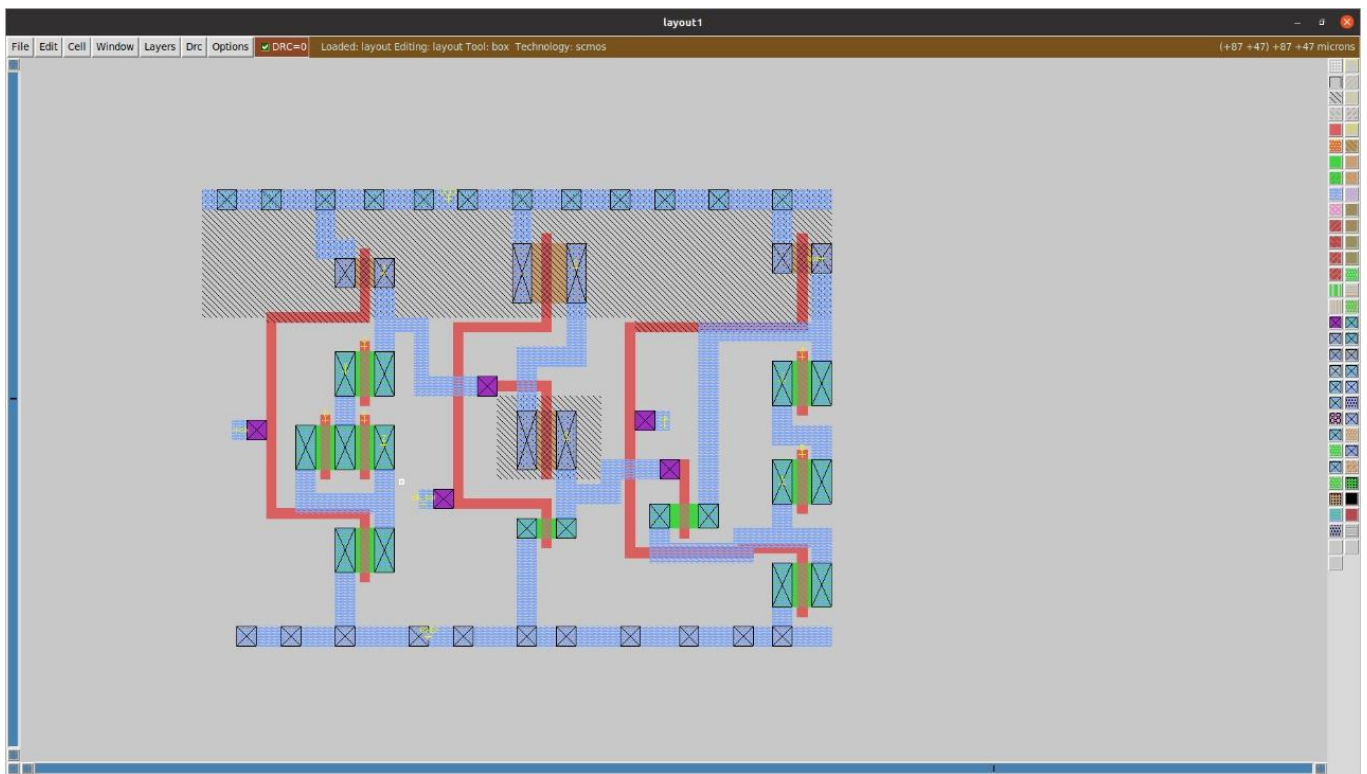


For Max frequency of operation, input vector chosen:

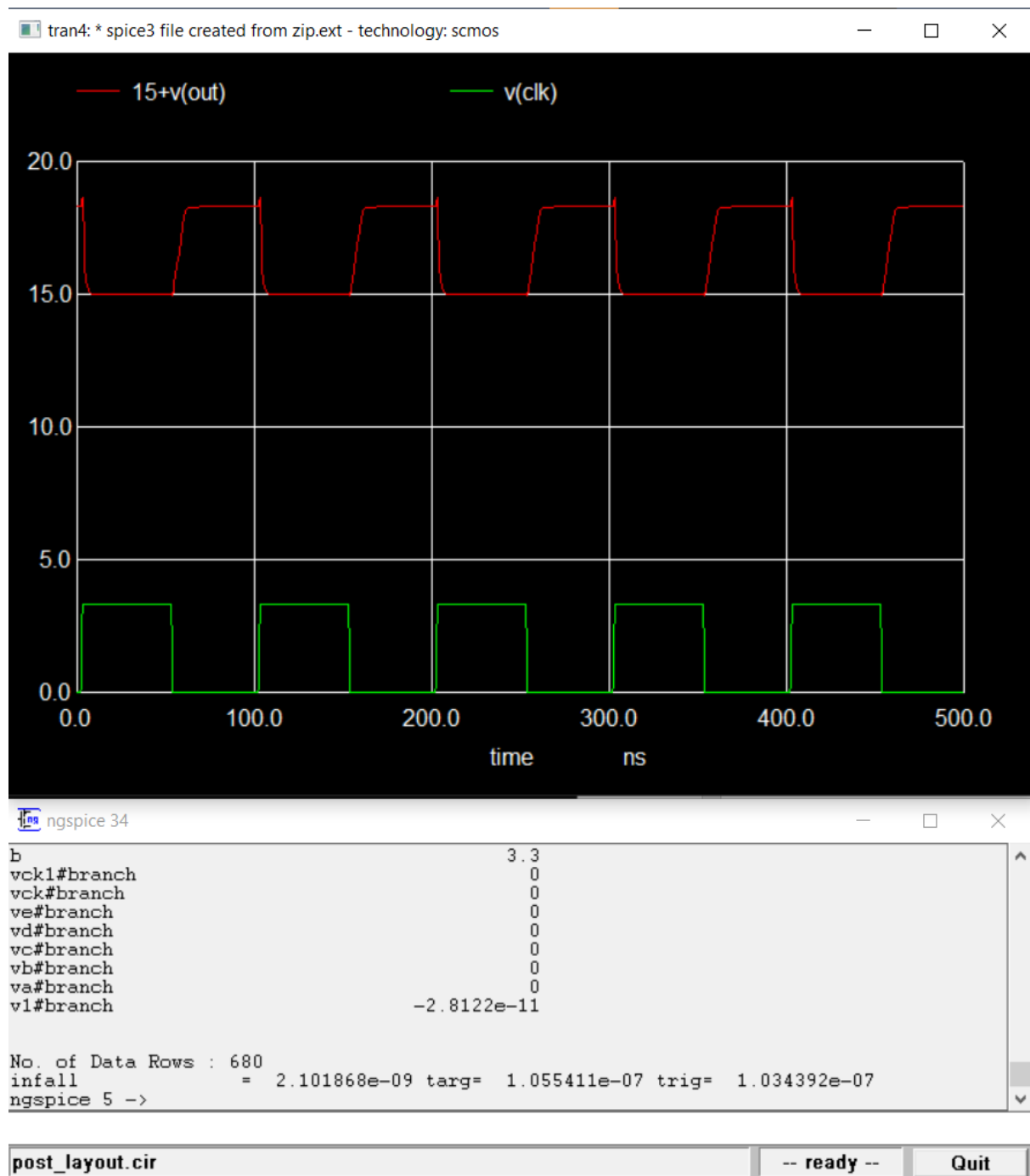
A=1,B=1 , C=0, D=x , E=x as this corresponds to the worst case condition.

Max Freq = $1/\text{infall} = 539.6 \text{ MHz}$

LAYOUT OF THE CIRCUIT



POST-LAYOUT SIMULATION



For Max frequency of operation, input vector chosen:

A=1,B=1 , C=0, D=x , E=x as this corresponds to the worst case condition.

Max Freq = $1/\text{infall} = 475.7826 \text{ MHz}$

Thus,

We can operate at a higher frequency for the pre-simulation case.