

A. Two-Pole Transfer Function

Often, the signal transfer, e.g. from input current i_{in} to an output current i_{out} , is governed by a two-pole transfer function like

$$G(s) = \frac{K}{(s - s_1)(s - s_2)} = K \frac{1}{s^2 + as + b} \quad . \quad (\text{A.1})$$

In analogy to an oscillator this equation can be rewritten as

$$G(s) = \frac{G_o \omega_r^2}{s^2 + s2\omega_r D + \omega_r^2} \quad . \quad (\text{A.2})$$

The transfer behavior is characterized by these parameters [79]:

- G_o dc value of $G(s)$, i.e., dc and low frequency gain, $G_o = G(s = 0)$
- ω_r resonance frequency
- D damping or damping coefficient, respectively

For damping coefficients above unity the poles of (A.2) are real values, for $D = 1$ a double real pole occurs. For values $D < 1$, both poles leave the real axis and become complex conjugated. In the frequency domain this results in a gain overshoot (at the resonance frequency ω_o) while in the time domain some amount of ringing can be observed.

Ringing and gain overshoot relate to system stability. In general, a system is stable if all poles of the transfer function have a negative real part. In circuit design often the poles are not available explicitly and the denominator is rather represented by a polynomial. In this case the coefficients of the polynomial are utilized to analyze and maintain the stability of this system. Among others, the Hurwitz stability criterion can be applied. For two-pole functions like (A.2) it requires the coefficients a and b of the second order polynomial to be positive. Hence,

$$\text{Re}\{s_1, s_2\} < 0 \quad \Longleftrightarrow \quad a, b > 0 \quad . \quad (\text{A.3})$$

Even though these conditions are met, ringing can still be too large. As a rule of thumb, in practical applications the damping coefficient should always be greater than 0.5 [79], i.e.,

$$D > \frac{1}{2} \quad . \quad (\text{A.4})$$

In order to achieve a fast response, the upper limit of the damping coefficient should be unity. In systems with feedback the stability is exclusively determined by the frequency response of the loop gain. As the loop gain increases it will be more difficult to maintain the condition of (A.4).

B. Step Response

A system can be described by its transfer function. In order to obtain the time domain response to a step signal at the input the residual method can be applied. With focus on current sensing a transfer function $G(s) = \frac{i_{out}}{i_{in}}$ will be assumed. With an input current step $i_{in}(s) = \frac{I_m}{s}$ of magnitude I_m the residual theorem [67] yields

$$\begin{aligned} i_{out}(t) &= \mathcal{L}^{-1} \{i_{out}(s)\} = I_m \sum_{s=0, s_i} \text{Res} \left[\frac{G(s)}{s} e^{st} \right] \\ &= I_m \left\{ G_o + \sum_{s=s_i} \text{Res} \left[\frac{G(s)}{s} e^{st} \right] \right\} \end{aligned} \quad (\text{B.1})$$

with the dc gain G_o according to (A.2). If the system is stable (refer to (A.3)) a final value

$$i_{out}(t \rightarrow \infty) = I_m G_o \quad (\text{B.2})$$

can be derived.

A pair of complex conjugated poles may occur in the form

$$\begin{aligned} s_1 &= \alpha + j\beta \\ s_2 &= \alpha - j\beta \end{aligned} \quad (\text{B.3})$$

Based on (B.1) and (B.3) the step response for various transfer functions, which are important in the field of current sensing, are derived below.

(a) One pole, no zero

$$\boxed{G(s) = K \frac{1}{(s - s_1)} = -\frac{G_o s_1}{(s - s_1)}} \quad (\text{B.4})$$

In this simple case the step response is given by

$$i_{out}(t) = I_m G_o (1 - e^{s_1 t}) \quad (\text{B.5})$$

From this equation the delay until i_{out} reaches a specified value I_{out} can be calculated in the form

$$t = \frac{1}{s_1} \ln \left(1 - \frac{I_{out}}{I_m G_o} \right) \quad . \quad (\text{B.6})$$

If the delay is referred to 63% of the final value $I_m G_o$ (see also (4.31)), the logarithmic term becomes (-1). Then the reciprocal value of the pole is a measure for the delay.

(b) One pole, one zero

$$G(s) = K \frac{(s - s_o)}{(s - s_1)} = -G_o \frac{s_1 (s - s_o)}{s_o (s - s_1)} \quad (\text{B.7})$$

Equation B.1 results in a step response

$$i_{out}(t) = G_o I_m \left\{ 1 + \left(\frac{s_1 - s_o}{s_o} \right) e^{s_1 t} \right\} \quad . \quad (\text{B.8})$$

From this equation the delay until i_{out} reaches a given value I_{out} can be calculated in the form

$$\begin{aligned} t &= \frac{1}{s_1} \ln \left\{ \left(1 - \frac{I_{out}}{I_m G_o} \right) \frac{s_o}{s_o - s_1} \right\} \\ &= \frac{1}{s_1} \left\{ \ln \left(1 - \frac{I_{out}}{I_m G_o} \right) - \ln \left(\frac{s_o - s_1}{s_o} \right) \right\} \quad . \end{aligned} \quad (\text{B.9})$$

The right hand expression of (B.9) consists of two logarithmic terms. If the delay is referred to 63% of the final value $I_m G_o$ (see also (4.31)), the first logarithmic term becomes (-1). If in addition the second term is approximated based on $\ln x \approx (x - 1)$, (B.9) simplifies to

$$t = -\frac{1}{s_1} \left(\frac{s_o - s_1}{s_o} \right) = -\frac{1}{s_1} + \frac{1}{s_o} \quad . \quad (\text{B.10})$$

Due to the zero the delay is reduced in comparison to a one-pole system without zero, (B.6).

(c) Two poles, no zero

$$G(s) = K \frac{1}{(s - s_1)(s - s_2)} = \frac{G_o s_1 s_2}{(s - s_1)(s - s_2)} \quad (\text{B.11})$$

From (B.1)

$$i_{out}(t) = G_o I_m \left\{ 1 + \frac{e^{s_1 t}}{\frac{s_1}{s_2} - 1} + \frac{e^{s_2 t}}{\frac{s_2}{s_1} - 1} \right\} \quad (\text{B.12})$$

can be found. For real poles s_1 and s_2 (B.12) sufficiently describes i_{out} in the time domain. Depending on the values one pole will be dominant.

In the presence of complex conjugated poles according to (B.3), the following expression can be derived:

$$\begin{aligned} i_{out}(t) &= I_m G_o \left\{ 1 + \frac{(\alpha - j\beta)e^{(\alpha + j\beta)t} - (\alpha + j\beta)e^{(\alpha - j\beta)t}}{(\alpha + j\beta) - (\alpha - j\beta)} \right\} \\ &= I_m G_o \left\{ 1 + e^{\alpha t} \left(\frac{\alpha}{\beta} \frac{1}{2j} (e^{j\beta t} - e^{-j\beta t}) - \frac{1}{2} (e^{j\beta t} + e^{-j\beta t}) \right) \right\} \\ &= I_m G_o \left\{ 1 + e^{\alpha t} \left(\frac{\alpha}{\beta} \sin \beta t - \cos \beta t \right) \right\} \end{aligned}$$

Comparing the coefficients of the denominator polynomial in (B.11) with the ones in (A.2),

$$(s - s_1)(s - s_2) = (s - \alpha - j\beta)(s - \alpha + j\beta) = s^2 + s2D\omega_r + \omega_r^2$$

results in

$$\begin{aligned} \alpha &= -D\omega_r, \\ \beta &= \omega_e = \sqrt{\omega_r^2(1 - D^2)}. \end{aligned}$$

where $\omega_e (= \beta)$ refers to the eigenfrequency. Hence,

$$i_{out}(t) = I_m G_o \left\{ 1 - e^{-D\omega_r t} \left(\frac{D\omega_r}{\omega_e} \sin \omega_e t + \cos \omega_e t \right) \right\}. \quad (\text{B.13})$$

Equation (B.13) allows to derive the step response without explicitly knowing the poles.

(d) Two poles, one zero

$$G(s) = K \frac{(s - s_o)}{(s - s_1)(s - s_2)} = - \frac{G_o s_1 s_2}{s_o} \frac{(s - s_o)}{(s - s_1)(s - s_2)} \quad (\text{B.14})$$

The residual theorem of (B.1) yields

$$i_{out}(t) = I_m G_o \left\{ 1 - \frac{1}{s_o(s_1 - s_2)} (s_2(s_1 - s_o)e^{s_1 t} - s_1(s_2 - s_o)e^{s_2 t}) \right\}. \quad (\text{B.15})$$

While this expression is adequate for real poles, it can be further resolved if conjugated complex poles occur:

$$i_{out}(t) = G_o I_m \left\{ 1 - e^{-D\omega_r t} \left(\frac{D\omega_r}{\omega_e} \left(1 + \frac{\omega_r}{Ds_o} \right) \sin \omega_e t + \cos \omega_e t \right) \right\}. \quad (\text{B.16})$$

Equation (B.16) differs from (B.13) by the highlighted factor.

C. Common-Mode Stability

Differential Type C and Type D current sensing circuits as described in Sects. 4.4.2 and 4.5.2 may become unstable due to finite common-mode gain of the feedback amplifier. As the stability conditions expressed by (4.62) and (4.88) are similar, this issue will be discussed with focus on Type D. For the implementation of Type D according to Fig. 4.32 common-mode stability requires

$$-A_{CM} = |A_{CM}| < \frac{1}{r_{in} q_m} \quad (\text{C.1})$$

where A_{CM} refers to the common-mode voltage gain of the fully-differential feedback amplifier. Figure C.1 illustrates the transient behavior of the output and bitline voltages if (C.1) is violated. Within a certain delay the output voltages v_{outp} , v_{outn} approach V_{DD} while the bitline voltage v_{BL} goes to a value near 0V. The actual differential part of the signals v_{outp} and v_{outn} is superimposed to a common-mode part (see also Fig. 4.33).

In order to satisfy (C.1) the absolute value of the common-mode gain A_{CM} has to be as low as possible. From the circuit model of Fig. C.2 for a simple differential stage the common-mode gain can be found to be

$$A_{CM} = - \frac{r_o}{2r_B + \frac{1}{g_{mn}} \left(1 + \frac{r_o + 2r_B}{r_{DS}} \right)} \quad (C.2)$$

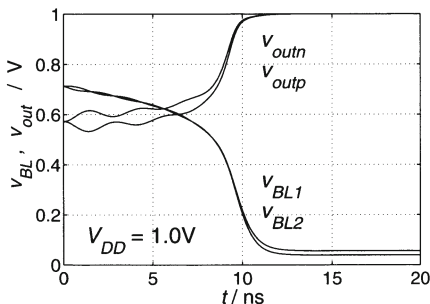


Fig. C.1. Simulated transient response of a Type D differential current sensing circuit in the presence of instability

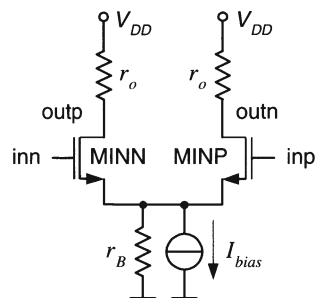


Fig. C.2. Circuit model of a simple differential amplifier

where g_{mn} and r_{DS} denote the transconductance and the output resistance of MINP and MINN. As these transistors operate in the saturation region, the denominator is dominated by r_B and the second term in the denominator can be neglected. Therefore, (C.2) can be simplified to

$$A_{CM} = -\frac{r_o}{2r_B} \quad (C.3)$$

which can often be found in the literature [66]. Figure C.2 results in a differential gain of

$$A_D = g_{mn} r_o \quad (C.4)$$

According to (C.1), it is essential to use feedback amplifier circuits with small common-mode gain. On the other hand, for good performance (sensing speed) the differential gain must not be too small. As a figure of merit the common-mode rejection ratio CMRR can be taken into account. Dividing (C.4) by (C.2) yields

$$\text{CMRR} = \left| \frac{A_D}{A_{CM}} \right| = 2g_{mn} r_B \quad (C.5)$$

To achieve a large CMRR the input transistors should have a large transconductance g_{mn} . In addition, a bias current source with a large output resistance r_B is of advantage. Since the current source is basically formed by a transistor, r_B represents its drain-source resistance. The resistance r_B can be further increased as shown in Fig. C.3a. In comparison to a simple differential amplifier Fig. C.3a comprises an additional cascode transistor MC that improves the bias current source formed by transistor MB. Due to the additional series transistor an implementation for low supply voltages becomes difficult. The circuit example of Fig. C.3b achieves differential operation by using

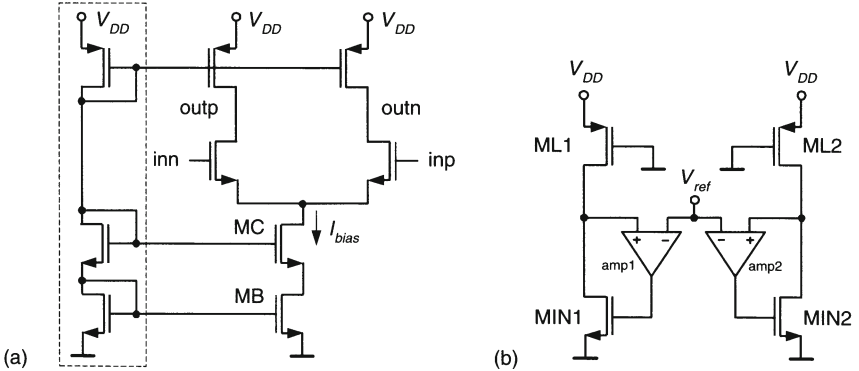


Fig. C.3. Circuits with reduced influence of the common-mode gain. (a) differential voltage amplifier with cascode transistor MC; (b) differential current sensing based on two single-ended circuits

two single-ended sensing circuits which do not suffer from common-mode instability. The use of two amplifiers increases layout area, power dissipation, and also the offset influence. In addition a reference voltage V_{ref} has to be generated. In this context it also has to be noted that sophisticated analog applications use common-mode feedback circuits to control the common-mode output voltage.

In SRAM designs most of the above circuit techniques are not suitable, because the area and power penalty and the biasing effort cannot be accepted. Consequently, there will still be a considerable common-mode gain. For a given common-mode gain A_{CM} , (C.1) requires small values of r_{in} and g_m . This is contrary to the conditions for high sensing speed. Due to the constraints regarding A_{CM} , r_{in} and g_m , common-mode stability is difficult to ensure.

On the other hand, from Fig. C.1 it can be observed that the time constant of the common-mode part is much larger than the sensing delay determined by the differential signal. Therefore an instable operation can be tolerated if the sensing takes place at the very beginning followed by an immediate deactivation of the sense amplifier. With respect to Fig. C.1 sensing can be finished below 1ns while a significant influence due to common-mode instability does not occur up to 5ns. This has to be analyzed further.

The transfer function of (4.85) consists of a common-mode and a differential part. Due to the linearity theorem of the Laplace transform [67] also the corresponding step response can be separated into a common-mode and a differential term, i_{CM} and i_D , respectively. Assuming a step magnitude I_m , this yields

$$\frac{i_{out}(t)}{I_m} = \frac{i_{CM}}{I_m} + \frac{i_D}{I_m} \quad (C.6)$$

where

$$\begin{aligned} \frac{i_{CM}}{I_m} &= \frac{1}{2} \frac{A_{CM} g_m r_{in}}{1 + A_{CM} g_m r_{in}} \left\{ 1 - e^{-\frac{t}{\tau_{in}} \left(\frac{1}{r_{in}} + A_{CM} g_m \right)} \right\} \\ \frac{i_D}{I_m} &= \frac{1}{2} \frac{A_D g_m r_{in}}{1 + A_D g_m r_{in}} \left\{ 1 - e^{-\frac{t}{\tau_{in}} \left(\frac{1}{r_{in}} + A_D g_m \right)} \right\} . \end{aligned}$$

It has to be noted that unlike the diffential part, the exponential term of the common-mode part will become positive if (C.1) is not satisfied causing a fast increase of $i_{CM}(t)$. For a correct circuit operation, the common-mode part i_{CM} must not exceed a certain fraction of the wanted signal i_D . In order to calculate the ratio $\frac{i_{CM}}{i_D}$ at a given time, it is convenient to focus on multiples q of the time constant of i_D , i.e.,

$$t = q \frac{1}{\frac{1}{\tau_{in}} \left(\frac{1}{r_{in}} + A_D g_m \right)} . \quad (C.7)$$

Accordingly, the current ratio becomes

$$\frac{i_{CM}}{i_D} = \frac{A_{CM}}{A_D} \frac{1 + A_D g_m r_{in}}{1 + A_{CM} g_m r_{in}} \frac{1 - e^{-q \frac{\frac{1}{r_{in}} + A_{CM} g_m}{\frac{1}{r_{in}} + A_D g_m}}}{1 - e^{-q}} \quad (C.8)$$

This ratio can be expressed as a function of $x = \frac{1}{g_m r_{in}}$, i.e.,

$$\frac{i_{CM}}{i_D} = \frac{A_{CM}}{A_D} \frac{x + A_D}{x + A_{CM}} \frac{1 - e^{-q \frac{x + A_{CM}}{x + A_D}}}{1 - e^{-q}} \quad (C.9)$$

At a given time (determined by q) this equation describes the ratio of the possibly instable common-mode signal i_{CM} to i_D . According to (C.1) the sensing circuit will be stable as long as $x > |A_{CM}|$. Figure C.4 shows a typical graph defined by (C.9) for different multiples q of the time constant of i_D . The intersection with the y-axis represents the worst case. Based on (C.9) it can be calculated by

$$\left. \frac{i_{CM}}{i_D} \right|_{x=0} = \frac{1 - e^{-q \frac{A_{CM}}{A_D}}}{1 - e^{-q}} \approx \frac{A_{CM}}{A_D} = \frac{1}{\text{CMRR}} \quad (C.10)$$

A small ratio $\frac{i_{CM}}{i_D}$ can mainly be achieved by a large common-mode rejection ratio CMRR of the feedback amplifier as it determines $\frac{A_{CM}}{A_D}$ (see (C.5)). The need for a small common-mode gain agrees to (C.1).

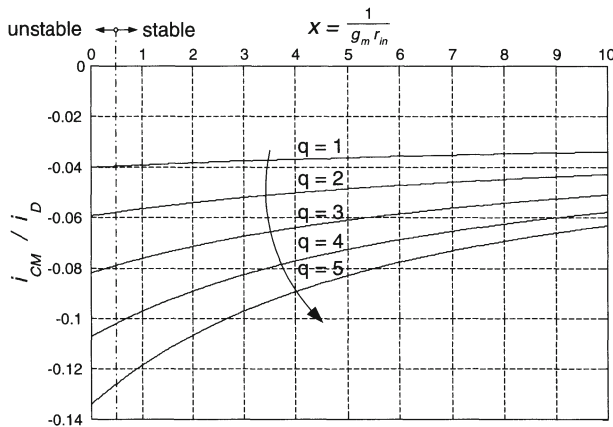


Fig. C.4. Common-mode rejection. The ratio $\frac{i_{CM}}{i_D}$ is plotted as a function of $\frac{1}{g_m r_{in}}$ at different times $t = q\tau$ with parameters $A_D = 20$, $A_{CM} = -0.5$. The maximum ratio $\left| \frac{i_{CM}}{i_D} \right|$ can be obtained from the intersection with the y-axis. This ratio increases with time and yields 4% at $q = 1$ and 13.4% at $q = 5$. Although the circuit is unstable for values below $x = -A_{CM} = 0.5$, even for $x = 0$ ($g_m \rightarrow \infty$, $r_{in} \rightarrow \infty$) a finite value of $\frac{i_{CM}}{i_D}$ can be obtained. For $q \rightarrow 0$ the ratio reaches the minimum $\left| \frac{i_{CM}}{i_D} \right| = 2.5\%$

The above investigation represents only an estimation as it does not consider the frequency dependence of common-mode and differential gain. If the frequency behavior is taken into account the time constants of both i_D and i_{CM} will increase. Even though the resulting equations will be very complex, it can be shown that the stability criterion of (C.1) holds. Moreover, while the limited bandwidth of the differential gain causes ringing of the signal i_D , ringing will not occur for the common-mode signal i_{CM} .

It can be concluded that also for common-mode instability a correct sensing operation can be achieved because the differential part of the output voltages v_{outp} , v_{outn} develops much faster than the common-mode part of these signals. The circuit will be initialized by precharge as described in Sect. 7.3.

D. Delay Versus Supply Voltage

Sense amplifiers have to be able to operate at various supply voltage levels depending on the product specification. Since sensing speed is the major advantage of current sense amplifiers it is interesting to investigate how the speed depends on V_{DD} in comparison to voltage sensing. For the design example in Chap. 7 the delay has been plotted in Fig. 7.5 as a function of V_{DD} . Obviously, in that case, current sensing is more sensitive to changes of the supply voltage than voltage sensing. It has to be analyzed if this increased sensitivity of current sensing is due to this particular design or if it represents an inherent property of the sensing circuit.

In Sect. 7.2 it has been discussed that the output voltage swing ΔV_{out} of the current sensing stage should reach a value pV_{DD} to ensure a correct decision of the voltage sense amplifier. This is based on the yield analysis of the voltage sense amplifier presented in Chap. 3 where Fig. 3.13 shows the relation between voltage swing and V_{DD} . The factor p is identical to the slope in that figure. For example, $p = 0.05$ can be extracted for a yield of 99.8%. If ΔV_{out} is substituted by pV_{DD} the delay expression of (4.38) becomes

$$t_c(V_{DD}) = \sqrt{\frac{C_{BL}}{kA_o\omega_o} \frac{pV_{DD}}{I_m}} = C_{BL} \sqrt{\frac{pV_{DD}}{I_m}} \underbrace{\sqrt{\frac{1}{C_{BL}kA_o\omega_o}}}_{d_c} . \quad (D.1)$$

Being an approximation (D.1) is valid for Type B, C and D. The second square root term d_c represents the difference to voltage sensing delay.

To allow for a comparison, the voltage sensing delay according to (2.10) can be rewritten to

$$t_v(V_{DD}) = C_{BL} \frac{pV_{DD}}{I_m} = C_{BL} \sqrt{\frac{pV_{DD}}{I_m}} \underbrace{\sqrt{\frac{pV_{DD}}{I_m}}}_{d_v} . \quad (D.2)$$

The delay difference between (D.1) and (D.2) is determined by the factors d_c and d_v . The magnitude I_m of the cell current and the feedback amplifier's gain-bandwidth product $A_o\omega_o$ depend on the supply voltage.

With focus on the differential amplifier of Fig. 7.2 $A_o\omega_o$ is basically proportional to the transconductance of the input transistor of amplifier divided

by the output load capacitance C_L . As this transconductance is a function of the bias current I_B the gain-bandwidth product is given by

$$A_o\omega_o = \frac{g_m}{C_L} = \frac{1}{C_L} \sqrt{2\beta I_B} \quad . \quad (\text{D.3})$$

In Fig. 7.2 the bias current is provided by transistor MB1. Since the biasing network forms a voltage divider, the gate potential V_G of MB1 will be a fraction of V_{DD} , i.e., $V_G = V_{DD}/n_c$ with $n_c > 1$. To first order, the factor n_c can be assumed to be constant. Therefore, the bias current of the feedback amplifier can be approximated by

$$I_B = \frac{\beta}{2} \left(\frac{V_{DD}}{n_c} - V_{th} \right)^2 \quad (\text{D.4})$$

and (D.3) becomes

$$A_o\omega_o = \frac{\beta}{C_L} \left(\frac{V_{DD}}{n_c} - V_{th} \right) \quad . \quad (\text{D.5})$$

For simplicity it is assumed that all transistors have the same transconductance parameter β . Equation (D.5) reveals a linear dependency on V_{DD} .

As C_{BL} and k are constants with respect to supply voltage, the delay factor d_c of (D.1) can be represented by a general approach

$$d_c = \sqrt{\frac{1}{c_1 V_{DD} + c_2}} \quad . \quad (\text{D.6})$$

Figure D.1a proofs the validity of the approximation of the term $C_{BL}kA_o\omega_o$ by a linear function $(c_1 V_{DD} + c_2)$.

The factor d_v of the bitline delay during voltage sensing contains the cell current $I_m = I_{cell}$ which has been plotted in Fig. 6.9 as a function of V_{DD} . In the relevant range of V_{DD} (above 0.8V), the current is nearly proportional to V_{DD} . Therefore, in general, d_v can be expressed by

$$d_v = \sqrt{\frac{V_{DD}}{c_3 V_{DD} + c_4}} \quad . \quad (\text{D.7})$$

Figure D.1a reveals a good matching between the term I_{cell}/p and its linear approximation $(c_3 V_{DD} + c_4)$. By using this linear approximation of the cell current a characteristic point is the intersection with the V_{DD} -axis. As can be seen in Fig. 6.9, this occurs at some value of V_{DD} near the threshold voltage of the transfer transistor of the memory cell (transistors MT1, MT2 in Fig. 2.2). Accordingly, the intersection refers to $V_{DD} = n_v V_{th}$ with a factor n_v similar to n_c for current sensing.

Based on d_c and d_v the sensitivity of both voltage and current sensing on changes of the supply voltage can be analyzed. For this reason the sensitivity function has to be derived which quantifies the relative deviation of d_c and, respectively, d_v on a relative change of V_{DD} . For current sensing this results in

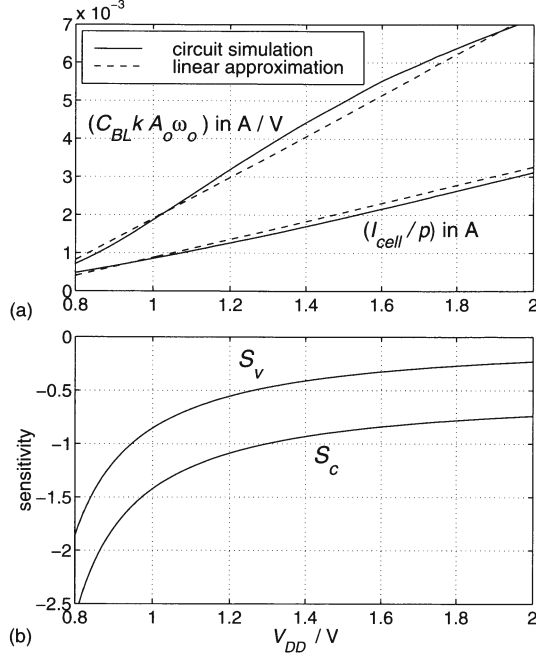


Fig. D.1. On the supply voltage dependence of the sensing delay. All curves correspond to the design example of Chap. 7 (Fig. 7.1). (a) Linearization of the terms $C_{BL} k A_o \omega_o$ and I_{cell}/p (obtained from simulation) by $(c_1 V_{DD} + c_2)$ and $(c_3 V_{DD} + c_4)$, respectively. Parameters are $c_1 = 5.4 \text{mA/V}^2$, $c_2 = -3.5 \text{mA/V}$, $c_3 = 2.4 \text{mA/V}$, $c_4 = -1.5 \text{mA}$, $p = 0.05$, $k = 0.4$, and $C_{BL} = 500 \text{fF}$. (b) Sensitivities S_c (current sensing) and S_v (voltage sensing) of the sensing delay to changes of the supply voltage plotted as a function of V_{DD} (parameters: $n_c = 2.1$, $n_v = 2.2$, $V_{th} = 0.3 \text{V}$)

$$S_c = \frac{\Delta d_c / d_c}{\Delta V_{DD} / V_{DD}} = \frac{\partial d_c}{\partial V_{DD}} \frac{V_{DD}}{d_c} = -\frac{1}{2} \frac{1}{1 + \frac{c_2}{c_1 V_{DD}}} \quad . \quad (\text{D.8})$$

From (D.1), (D.5) and (D.6) the ratio $\frac{c_2}{c_1} = -n_c V_{th}$ can be obtained and inserted into (D.8). This yields

$$S_c = -\frac{1}{2} \frac{1}{1 - \frac{n_c V_{th}}{V_{DD}}} \quad . \quad (\text{D.9})$$

Applying the same procedure to d_v gives

$$S_v = \frac{\Delta d_v / d_v}{\Delta V_{DD} / V_{DD}} = \frac{\partial d_v}{\partial V_{DD}} \frac{V_{DD}}{d_v} = \frac{1}{2} \frac{1}{1 - \frac{c_3}{c_4 V_{DD}}} \quad . \quad (\text{D.10})$$

The ratio of the coefficients c_3 , c_4 can be calculated from the intersection of I_{cell} with the V_{DD} -axis (Fig. 6.9), defined by

$$0 = \frac{I_{cell}(V_{DD} = n_v V_{th})}{p} = c_3 n_v V_{th} + c_4 \quad . \quad (\text{D.11})$$

As this yields $\frac{c_4}{c_3} = -n_v V_{th}$ the sensitivity becomes

$$S_v = \frac{1}{2} \frac{1}{1 - \frac{V_{DD}}{n_v V_{th}}} = -\frac{1}{2} \frac{\frac{n_v V_{th}}{V_{DD}}}{1 - \frac{n_v V_{th}}{V_{DD}}} \quad (D.12)$$

The difference between S_c and S_v explains the different increase of the sensing delay as V_{DD} is reduced. The factors n_c and n_v can be assumed to be equal, with 2.0 being a typical value. The threshold voltage V_{th} will be around 300mV. Hence, an estimation of the terms $n_c V_{th}$ and $n_v V_{th}$ results in 0.6V. As a consequence, the denominators of (D.9) and (D.12) will be identical while a significant difference is determined by the numerator. The latter remains unity for current sensing but it alters with V_{DD} for voltage sensing. With $n_v V_{th} \approx 0.6V$ the sensitivity S_v will be only 30% of S_c at $V_{DD} = 2.0V$. This agrees to Fig. D.1b where S_c and S_v are shown based on (D.9) and (D.12) for the design example of Chap. 7. If V_{DD} is reduced the absolute sensitivities increase. However, S_v will remain smaller. At $V_{DD} = 1.0V$ it can be estimated that S_v reaches 60% of S_c .

Assuming equal factors $n_c = n_v$ the difference between the sensitivities given in (D.9) and (D.12) becomes simply

$$|S_c - S_v| = \frac{1}{2} \quad (D.13)$$

This agrees well with the curves in Fig. D.1b. In consequence the current sensing delay will increase twice as much as the delay for voltage sensing if the supply voltage is reduced by the same amount. For example, if the supply voltage is reduced by half, from 2.0V to 1.0V, in Fig. 7.5 the current sensing delay rises from 166ps to 449ps. This corresponds to a delay increase by 170%. On the other hand, the voltage sensing delay increases by only 83.2% from 321ps to 588ps. However, despite the lower sensitivity, voltage sensing is still slower than current sensing.

As long as the current sensing delay is smaller than the delay of voltage sensing the larger sensitivity on V_{DD} may be tolerated in many applications. This points to an advantage of current sensing. Even though the tuning of the sensitivity S_c is limited, the desired current sensing delay can be adjusted within a wide range by means of design. Voltage sensing cannot be improved as it is defined by capacitive discharge of the bitline capacitance.

It can be concluded that the sensitivity of both sensing methods on variations of the supply voltage is characterized by just two parameters, the threshold voltage and a factor n_c or n_v , respectively. For a given technology the threshold voltage and the factor n_v are basically fixed. Only n_c can be adjusted by design since it refers to a fraction of V_{DD} generated by the voltage divider in the biasing network of the feedback amplifier (Fig. 7.2). However, in practical designs the range of n_c is limited. Therefore, the increased sensitivity of current sensing is an inherent property of the current sensing circuit caused by the feedback amplifier. It can be reduced by the use of improved feedback amplifiers at the cost of increased complexity.

E. Experimental Results: Current Sensing

Two test chips have been realized to confirm the theory covered in this book. The emphasis of this section is on the first chip with focus on current sensing. Measurements on voltage sensing from the second test chip are presented in Appendix F. Figure E.1 shows the microphotograph of the first chip, fabricated in a $0.18\mu\text{m}$ CMOS technology. The active area is $1024\mu\text{m} \times 85\mu\text{m}$. A $2\text{k} \times 6\text{-bit}$ SRAM macro forms the main part. It utilizes different current sense amplifiers, i.e., Type A to C, and Type D with and without multiplexer compensation. Figure E.2 shows more details. Separate circuits (Fig. E.3) have been included for analog measurements (step response, memory cell behavior, etc.). Several experimental results have been already presented in Chaps. 5 and 6. The following figures depict additional measurements at a supply voltage of 1.8V or, if noted, at 2.0V. Figures E.4 to E.8 show the step response of the different current sensing principles which have been implemented as single ended circuits. The input (bitline) capacitance is basically determined by the capacitance of the bonding pad and package pin, which can be estimated to be approximately 2.4pF. To investigate the influence of different bitline capacitances, external discrete capacitances (below 10pF) have been added. It has to be noted that the step response is also affected by parasitics (bond wire inductance, package capacitances). These values have been taken into account during circuit simulations [37] and the results are also shown (Fig. E.4 illustrates the influence of parasitics). The sensing delay from the wordline signal to the CMOS level output of the sense amplifier is plotted in Fig. E.9 and Fig. E.10 for Type A and C, respectively. The corresponding plot for Type D is presented in Fig. 5.18. The absolute delay is affected by parasitic capacitances which cause a delay offset.



Fig. E.1. Microphotograph of the experimental $2\text{k} \times 6\text{-bit}$ SRAM macro

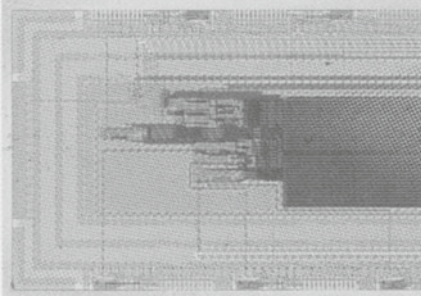


Fig. E.2. Detail photograph of the sense amplifiers on the SRAM

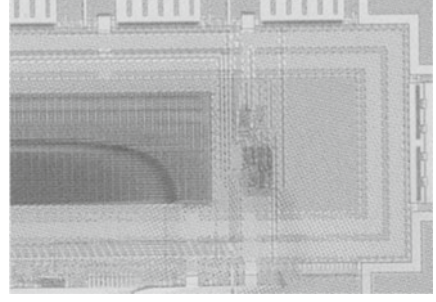


Fig. E.3. Detail photograph of the separate current sensing circuits

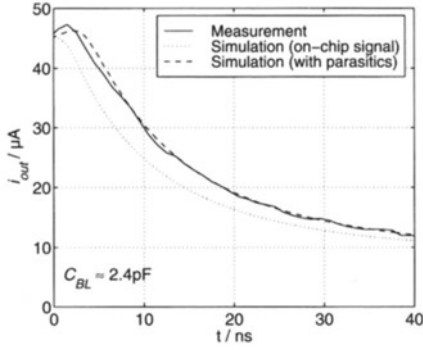


Fig. E.4. Measured and simulated step response of a Type A sensing circuit

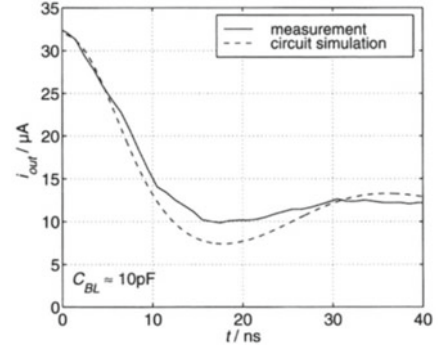


Fig. E.5. Measured and simulated step response of a Type B sensing circuit

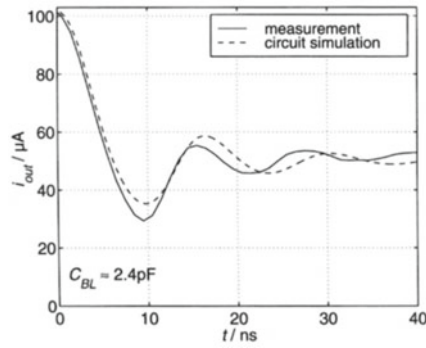


Fig. E.6. Measured and simulated step response of a Type C sensing circuit

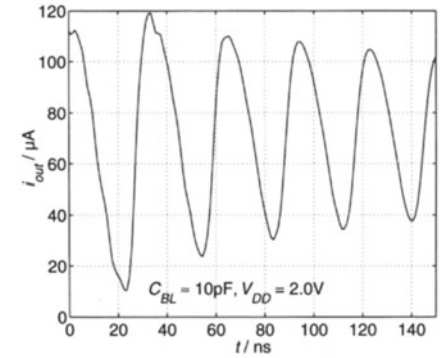


Fig. E.7. Step response of Type C operating close to a violation of the stability conditions derived in Sect. 4.4

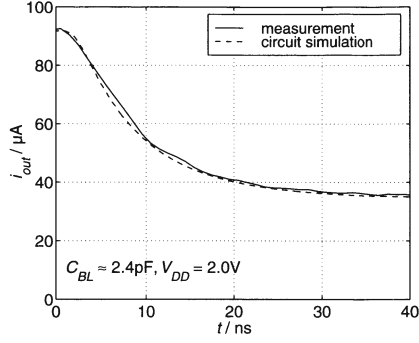


Fig. E.8. Measured and simulated step response of a Type D sensing circuit

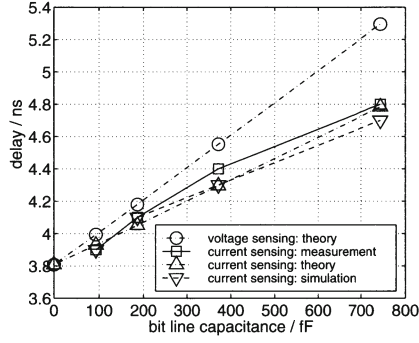


Fig. E.9. Sensing delay vs. bitline length of the SRAM macro using a Type A sense amplifier. Theoretical curves given by (4.4), (B.6) (current sensing) and (2.10) (voltage sensing) with $\Delta V_{BL} = \Delta V_{out} = 200\text{mV}$ have been included. Assuming the same delay offset the theoretical delays at $C_{BL} = 0$ have been set equal

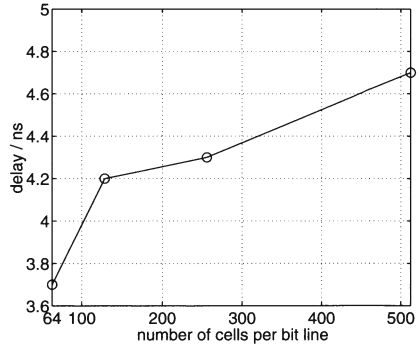


Fig. E.10. Sensing delay vs. bitline length of the SRAM macro using a Type C sense amplifier

F. Experimental Results: Voltage Sensing

The voltage sense amplifier of Fig. 7.9 has been fabricated in a 130nm CMOS technology as a part of the chip shown in Fig. 7.10. Fig. F.1 shows the measured yield versus the input voltage difference of the sense amplifier as theoretically discussed in Sect. 3.2.4 (refer to Fig. 3.10). According to (3.13), the yield is defined as the number of samples which result in a correct decision at a specified input voltage difference ΔV_{IN} . Using the error function, the curves have been fitted as described by (3.18). If V_{INDC} is reduced from 1.5V to 0.6V, the standard deviation of the sense amplifier's offset decreases from 19mV to 7mV. Consequently, the yield increases, e.g., from 70% to 94% at $\Delta V_{IN} = 10\text{mV}$. This agrees well with the theory of Chap. 3. It confirms that a lower input dc level V_{INDC} results in less offset and, hence, in increased yield. Figure F.1 indicates a better matching of the transistors and output capacitances of the sense amplifier compared to Fig. 3.10 because of higher yield at the same values of V_{INDC} and ΔV_{IN} . A mean offset different from zero was measured (caused by the test equipment, not ideally matched layout, and fabrication). This offset has been subtracted for better comparison to Fig. 3.10.

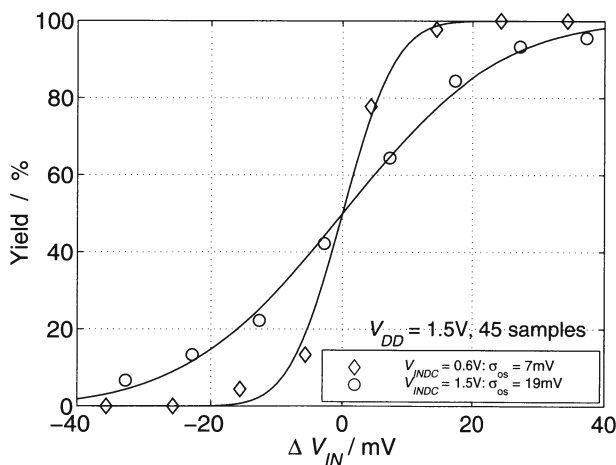


Fig. F.1. Measured yield vs. input voltage difference of the sense amplifier Fig. 7.9

Bibliography

1. Takayasu Sakurai and A. Richard Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.
2. Narain Arora, *MOSFET Models for VLSI Circuit Simulation*, Springer Verlag, Wien, 1993.
3. Christian C. Enz and Eric A. Vittoz, "MOS Transistor Modeling for Low-Voltage and Low-Power Analog IC Design," *Microelectronic Engineering*, vol. 39, pp. 59–76, 1997.
4. W. Sansen, M. Steyaert, V. Peluso, and E. Peeters, "Towards Sub-1V Analog Integrated Circuits in Submicron Standard CMOS Technologies," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1998, pp. 186–187.
5. Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 2001.
6. Dennis D. Buss, "Technology in the Internet Age," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2002, pp. 18–21.
7. Chang-Gyu Hwang, "Semiconductor Memories for IT Era," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2002, pp. 24–25.
8. Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 2000.
9. Chung S. Wang and Edward C.K. Chen, "Embedded-DRAM Technologies: Comparison and Trade-offs," *EDN magazine*, pp. 113–120, Sept. 28, 2000.
10. Patrick P. Gelsinger, "Microprocessors for the New Millenium – Challenges, Opportunities, and New Frontiers," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2001, pp. 22–25.
11. Chekib Akrouit et al., "A 480-MHz RISC Microprocessor in a 0.12- μ m Leff CMOS Technology with Copper Interconnects," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 11, pp. 1609–1615, Nov. 1998.
12. Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, 1997.
13. Stefan Rusu, "Trends and Challenges in VLSI Technology Scaling Towards 100nm," in *Proc. European Solid-State Circuits Conference*. IEEE, Sept. 2001, pp. 23–25.
14. Jeffrey A. Davis, Raguraman Venkatesan, Alain Kaloyeros, Michael Beylansky, Shukri J. Souri, Kaustav Banerjee, Krishna C. Saraswat, Arifur Rahman, Rafael Reif, and James D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proceedings of the IEEE*, pp. 305–324, Mar. 2001.

15. Christian Piguet, "Low-Power and Low-Voltage CMOS Digital Design," *Microelectronic Engineering*, vol. 39, pp. 179–208, 1997.
16. Kiyoo Itoh, *VLSI Memory Chip Design*, Springer Verlag, Berlin, 2001.
17. Veronika Eisele and Doris Schmitt-Landsiedel, "Design optimization of static memories," in *Proc. European Solid-State Circuits Conference*. IEEE, 1992.
18. Tomohisa Wada, Suresh Rajan, and Steven A. Przybylski, "An Analytical Access Time Model for On-Chip Cache Memories," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 8, pp. 1147–1156, Aug. 1992.
19. Cangsang Zhao, Uddalak Bhattacharya, Martin Denham, Jim Kolousek, Yi Lu, Yong-Gee Ng, Novat Nintunze, Kamal Sarez, and Hemmige Varadarajan, "An 18Mb, 12.3GB/s CMOS Pipeline-Burst Cache SRAM with 1.54Gb/s/pin," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1999.
20. S. Thompson, M. Alavi, R. Arghavani, A. Brand, R. Bigwood, J. Brandenburg, B. Crew, V. Dubin, M. Hussein, P. Jacob, C. Kenyon, E. Lee, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, M. Prince, R. Schweinfurth, S. Sivakumar, P. Smith, M. Settler, S. Tyagi, M. Wei, J. Xu, S. Yang, and M. Bohr, "An Enhanced 130nm Generation Logic Technology Featuring 60nm Transistors Optimized for High Performance and Low Power at 0.7 - 1.4 V," in *Technical Digest International Electron Devices Meeting, IEDM*. IEEE, Dec. 2001.
21. Tegze P. Haraszti, *CMOS Memory Circuits*, Kluwer Academic Publishers, Boston, 2000.
22. "Intel Builds World's First One Square Micron SRAM Cell," Press release, www.intel.com, March 12, 2002.
23. Craig Lage, James D. Hayden, and Chitra Subramanian, "Advanced SRAM Technology - The Race Between 4T and 6T Cells," in *Technical Digest International Electron Devices Meeting, IEDM*. IEEE, Dec. 1996, pp. 271–274.
24. Koichi Takeda et al., "A 16Mb 400MHz Loadless CMOS Four-Transistor SRAM Macro," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2000, pp. 264–265.
25. Kenji Noda, Koichi Takeda, Koujiro Matsui, Shinya Ito, Sadaaki Masuoka, Hideaki Kawamoto, Noyuki Ikezawa, Yoshiharu Aimoto, Noritsugu Nakamura, Takahiro Iwasaki, Hideo Toyoshima, and Tadahiko Horiuchi, "An Ultrahigh-Density High-Speed Loadless Four-Transistor SRAM Macro with Twisted Bitline Architecture and Triple-Well Shield," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 510–515, Mar. 2001.
26. Taiwan Semiconductor Manufacturing Company, "Embedded High-Density Memory," Product information, www.tsmc.com, 2002.
27. Hirotohi Sato et al., "A 500-MHz Pipelined Burst SRAM with Improved SER Immunity," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 11, pp. 1571–1578, Nov. 1999.
28. Ken-ichi Osada and Hisayuki Higuchi and Koichiro Ishibashi and Natotaka Hashimoto and Kenji Shiozawa, "A 2ns Access, 285MHz, Two-Port Cache Macro using Double Global Bit-Line Pair," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1997, pp. 402–403.
29. B. Bateman, C. Freeman, J. Halbert, K. Nose, G. Petrie, and E. Reese, "A 450MHz 512kB Second-Level Cache with a 3.6GB/s Data Bandwidth," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1998, pp. 358–359.
30. Kenneth W. Mai, Toshihiko Mori, Bharadwaj S. Amrutur, Ron Ho, Bennett Wilburn, Mark A. Horowitz, Isao Fukushi, Tetsuo Izawa, and Shin Mitarai, "Low-Power SRAM Design Using Half-Swing Pulse-Mode Techniques," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 11, pp. 1659–1671, Nov. 1998.

31. H. Nambu, K. Kanetani, K. Yamasaki, K. Higea, M. Usami, T. Kusunoki, K. Yamaguchi, and N. Homma, "A 1.8ns Access, 550MHz 4.5Mb CMOS SRAM," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1998, pp. 360–361.
32. T. Uetake, Y. Maki, T. Nakadaï, K. Yoshida, M. Susuki, and R. Nanjo, "A 1.0ns Access 770MHz 36Kb SRAM Macro," in *1999 Symp. on VLSI Circuits Digest of Technical Papers*, New York, June 1999, IEEE, pp. 109–110.
33. Hiroshi Shimizu, Kenji Ijitsu, Hideo Akiyoshi, Keizo Aoyama, Hirotaka Takatsuka, Kou Watanabe, Ryota Nanjo, and Yoshihiro Takao, "A 1.4ns Access 700MHz 288kb SRAM Macro with Expandable Architecture," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1999, pp. 190–191, 459.
34. Hiroaki Nambu, Kazuo Kanetani, Kaname Yamasaki, Keiichi Higeta, Masami Usami, Yasuhiro Fujimura, Kazumasa Ando, Takeshi Kusunoki, Kunihiro Yamaguchi, and Noriyuki Homma, "A 1.8-ns Access, 550-MHz, 4.5-Mb CMOS SRAM," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 11, pp. 1650–1657, Nov. 1998.
35. Evert Seevinck, Petrus J. van Beers, and Hans Ontrop, "Current-Mode Techniques for High-Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAM's," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 525–536, Apr. 1991.
36. Nobutaro Shibata, "Current Sense Amplifiers for Low-Voltage Memories," *IEICE Trans. Electron.*, vol. E79-C, no. 8, pp. 1120–1130, Aug. 1996.
37. Nishath K. Verghese, Timothy J. Schmerbeck, and David J. Allstot, *Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits*, Kluwer Academic Publishers, Boston, 1995.
38. H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, Reading, 1990.
39. Nobutaro Shibata, "Current-Sensed SRAM Techniques for Megabit-Class Integration - Progress in Operation Frequency by Using Hidden Writing-Recovery Architecture," *IEICE Trans. Electron.*, vol. E82-C, no. 11, pp. 2056–2064, Nov. 1999.
40. Y. K. Seng, "New current conveyor for high-speed low-power current sensing," *IEE Proc.-Circuits Devices Syst.*, vol. 145, no. 2, pp. 85–89, Apr. 1998.
41. Kiyofumi Ochiï, Hiroshi Yasuda, Kiyoshi Kobayashi, Takeo Kondoh, and Fujio Masuoka, "A 17ns 64K CMOS RAM with a Schmitt Trigger Sense Amplifier," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1985, pp. 64–65.
42. Tsuguo Kobayashi, Kazutaka Nogami, Tsukasa Shirotori, and Yukihiro Fujimoto, "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.
43. David J. Allstot, "A Precision Variable-Supply CMOS Comparator," *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 6, pp. 1080–1087, Dec. 1982.
44. Randall L. Geiger, Phillip E. Allen, and Noel R. Strader, *VLSI Design Techniques For Analog and Digital Circuits*, McGraw-Hill, New York, 1990.
45. H. J. Boll and William T. Lynch, "Design of a High-Performance 1024-b Switched Capacitor p-Channel IGFET Memory Chip," *IEEE Journal of Solid-State Circuits*, vol. SC-8, no. 5, pp. 310–318, Oct. 1973.
46. William T. Lynch and H. J. Boll, "Optimization of the Latching Pulse for Dynamic Flip-Flop Sensors," *IEEE Journal of Solid-State Circuits*, vol. SC-9, no. 2, pp. 49–55, Apr. 1974.

47. Nobuaki Ieda, Yasuo Ohmori, Ken Takeya, and Takao Yano, "Single Transistor MOS RAM Using a Short-Channel MOS Transistor," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 2, pp. 218–224, Apr. 1978.
48. Natsuki Kushiya, Charles Tan, Richard Clark, Jane Lin, Fred Perner, Lisa Martin, Mark Leonard, Gene Coussens, Kit Cham, and Kuang Chiu, "A 295MHz CMOS 1M (x256) Embedded SRAM using Bi-directional Read/Write Shared Sense Amps and Self-Timed Pulse Word-Line Drivers," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1995, pp. 304–305.
49. Masato Matsumiya, Shoichiro Kawashima, Makoto Sakata, Masahiko Ookura, Toru Miyabo, Toru Koga, Kazuo Itabashi, Kazuhiro Mizutani, Hiroshi Shimada, and Noriyuki Suzuki, "A 15-ns 16-Mb CMOS SRAM with Interdigitated Bit-Line Architecture," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 11, pp. 1497–1503, Nov. 1992.
50. Kevin Zhang, Ken Hose, Vivek De, and Borys Senyk, "The Scaling of Data Sensing Schemes for High Speed Cache Design in Sub-0.18 μ m Technologies," in *2000 Symp. on VLSI Circuits Digest of Technical Papers*. IEEE, June 2000.
51. Kohtaroh Gotoh, Junji Ogawa, Miyoshi Saito, Hirotaka Tamura, and Masao Taguchi, "A 0.9 V Sense-Amplifier Driver for High-Speed Gb-Scale DRAMs," in *1996 Symp. on VLSI Circuits Digest of Technical Papers*. IEEE, June 1996, pp. 108–109.
52. Hiroki Fujisawa, Tsugio Takahashi, Masayuki Nakamura, and Kazuhiko Kajigaya, "A Dual-Phase-Controlled Dynamic Latched Amplifier for High-Speed and Low-Power DRAMs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1120–1126, July 2001.
53. Heinrich Klar, *Integrierte Digitale Schaltungen MOS / BICMOS*, Springer Verlag, Berlin, 1996.
54. Atsushi Kinoshita, Shuji Murakami, Yasumasa Nishimura, and Kenji Anami, "A Study of Delay Time on Bit Lines in Megabit SRAM's," *IEICE Trans. Electron.*, vol. E75-C, no. 11, pp. 1383–1386, Nov. 1992.
55. Bharadwaj S. Amurutur and Mark A. Horowitz, "Speed and Power Scaling of SRAM's," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 175–185, Feb. 2000.
56. David Johns and Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 2000.
57. Roubik Gregorian, *Introduction to CMOS Op-Amps and Comparators*, John Wiley & Sons, New York, 1999.
58. Takeshi Suzuki et al., "Synonym Hit RAM - A 500-MHz CMOS SRAM Macro with 576-Bit Parallel Comparison and Parity Check Functions," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 163–174, Feb. 2000.
59. Jonathan Lachman and J. Michael Hill, "A 500MHz 1.5MB Cache with On-Chip CPU," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1999, pp. 192–193.
60. J. Michael Hill and Jonathan Lachman, "A 900MHz 2.25MB Cache with On-Chip CPU - Now In Cu SOI," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2001, pp. 176–177, 444.
61. Masataka Matsui, Hiroyuki Hara, Yoshiharu Uetani, Lee-Sup Kim, Tetsu Nagamatsu, Yoshinori Wanatabe, Akihiko Chiba, Kouji Matsuda, and Takayasu Sakurai, "A 200 MHz 13 mm² 2-D DCT Macrocell Using Sense-Amplifying Pipeline Flip-Flop Scheme," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1482–1490, Dec. 1994.
62. Borivoje Nikolić, Vladimir Stojanović, Vojin G. Oklobdžija, Wenyan Jia, James Chiu, and Michael Leung, "Sense Amplifier-Based Flip-Flop," in *IEEE*

- Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1999, pp. 282–283, 468.
63. Borivoje Nikolić, Vojin G. Oklobdžija, Vladimir Stojanović, Wenyan Jia, James Kar-Shing Chiu, and Michael Ming-Tak Leung, “Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, June 2000.
 64. Hiroshi Kawaguchi and Takayasu Sakurai, “A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998.
 65. Thomas Nirschl, Bernhard Wicht, and Doris Schmitt-Landsiedel, “High Speed, Low Power Design Rules for SRAM Precharge and Self-timing under Technology Variations,” in *Power and Timing Modeling, Optimization and Simulation 2001, Proceedings of the 11th Intern. Workshop*, Yverdon-les-Bains, Sept. 2001, pp. 7.3.1–7.3.10.
 66. Kenneth R. Laker and Willy M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, New York, 1994.
 67. I. N. Bronstein, K. A. Semendjajew, G. Musiol, and H. Mühlig, *Taschenbuch der Mathematik*, Verlag Harri Deutsch, Thun, 2001.
 68. Marcel J. M. Pelgrom, Aad C. J. Duinmaijer, and Anton P. G. Welbers, “Matching Properties of MOS Transistors,” *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.
 69. Marcel J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, “Transistor Matching in Analog CMOS Applications,” in *Technical Digest International Electron Devices Meeting, IEDM*. IEEE, Dec. 1998, pp. 915–918.
 70. Roland Thewes, Carsten Linnenbank, Ute Kollmer, Stefan Burges, Michelle DiLeo, Miriam Clincy, Ulrich Schaper, Ralf Brederlow, Rudolf Seibert, and Werner Weber, “On the Matching Behavior of MOSFET Small Signal Parameters,” in *Proceedings of the 2000 Intern. Conference on Microelectronic Test Structures*. IEEE, Mar. 2000, pp. 137–141.
 71. Evert Seevinck, Frans J. List, and Jan Lohstroh, “Static-Noise Margin Analysis of MOS SRAM Cells,” *IEEE Journal of Solid-State Circuits*, , no. 5, pp. 748–754, Oct. 1987.
 72. M. Eisele, J. Berthold, R. Thewes, E. Wohlrab, D. Schmitt-Landsiedel, and W. Weber, “Intra-die device parameter variations and their impact on digital CMOS gates at low supply voltages,” in *Technical Digest International Electron Devices Meeting, IEDM*. IEEE, 1995, pp. 67–69.
 73. M. Eisele, J. Berthold, and D. Schmitt-Landsiedel, “The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits,” in *Int. Symp. On Low Power Electronics and Design ISLPED*, 1996, pp. 237–242.
 74. Simon J. Lovett, Gary A. Gibbs, and Ashish Pancholy, “Yield and Matching Implications for Static RAM Memory Array and Sense-Amplifier Design,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1200–1204, Aug. 2000.
 75. Azeez J. Bhavnagarwala, Xinghai Tang, and James D. Meindl, “The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.
 76. Tomohisa Mizuno, Jun-ichi Okamura, and Akira Toriumi, “Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov. 1994.
 77. James D. Meindl, Vivek K. De, Scott Wills, John C. Ebele, Xinghai Tang, Jeffery A. Davis, Blanca Austin, and Azeez J. Bhavnagarwala, “The Impact of

- Stochastic Dopand and Interconnect Distributions on Gigascale Integration," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1997, pp. 232–233.
78. James Chen, Michael Orshansky, Chenming Hu, and C-P. Wan, "Statistical Circuit Characterization for Deep-Submicron CMOS Designs," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1998, pp. 90–91.
 79. Manfred Seifart, *Analoge Schaltungen*, Verlag Technik, Berlin, 1989.
 80. Katsuro Sasaki, Koichiro Ishibashi, Kiyotsugu Ueda, Kunihiro Komiyaji, Toshiaki Yamanaka, Naotaka Hashimoto, Hiroshi Toyoshima, Fumio Kojima, and Akihiro Shimizu, "A 7-ns 140-mW 1-Mb CMOS SRAM with Current Sense Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 11, pp. 1511–1518, Nov. 1992.
 81. Erik Bruun, "A High-Speed CMOS Current Opamp for Very Low Supply Voltage Operation," in *Proc. 1994 IEEE Intern. Symp. on Circuits and Systems*, 1994, vol. 5, pp. 509–512.
 82. João Pedro A. Carreira and José E. Franca, "High-Speed CMOS Current Comparators," in *Proc. 1994 IEEE Intern. Symp. on Circuits and Systems*, 1994, vol. 5, pp. 731–734.
 83. H. Träff, "Novel Approach to High Speed CMOS Current Comparators," *Electron. Letters*, vol. 28, no. 3, pp. 310–312, Jan. 1992.
 84. A.T.K Tang and C. Toumazou, "High performance CMOS current comparator," *Electron. Letters*, vol. 30, no. 1, pp. 5–6, Jan. 1994.
 85. G. Liñán-Cembrano, R. Del Rio-Fernández, R. Domínguez-Castro, and A. Rodríguez-Vázquez, "Robust high-accuracy high-speed continuous-time CMOS current comparator," *Electron. Letters*, vol. 33, no. 25, pp. 2082–2084, Dec. 1997.
 86. R. L. Brennan, T. R. Viswanathan, and J. V. Hanson, "The CMOS Negative Impedance Converter," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 5, pp. 1272–1275, Oct. 1988.
 87. G. C. Temes and W. H. Ki, "Fast CMOS Current Amplifier and Buffer Stage," *Electron. Letters*, vol. 23, no. 13, pp. 696–697, June 1987.
 88. Katsunori Seno, Kurt Knorpp, Lee-Lean Shu, Fumio Miyaji, Masayoshi Sasaki, Minoru Takeda, Takeshi Yokoyama, Katsushi Fujita, Tadayuki Kimura, Yoichi Tomo, Patrick Chuang, and Kazuyoshi Kobayashi, "A 9ns 16Mb CMOS SRAM with Offset Reduced Current Sense Amplifier," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 1993, pp. 248–249, 297.
 89. Katsunori Seno, Kurt Knorpp, Lee-Lean Shu, Naoki Teshima, Hiroki Kihara, Hiroshi Sato, Fumio Miyaji, Minoru Takeda, Masayoshi Sasaki, Yoichi Tomo, Patrick T. Chuang, and Kazuyoshi Kobayashi, "A 9-ns 16-Mb CMOS SRAM with Offset-Compensated Current Sense Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 11, pp. 1119–1124, Nov. 1993.
 90. Travis N. Blalock and Richard C. Jaeger, "A High-Speed Clamped Bit-Line Current-Mode Sense Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 542–548, Apr. 1991.
 91. Masanori Izumikawa, Hiroyuki Igura, Koichiro Furuta, Hiroshi Ito, Hitoshi Wakabayashi, Ken Nakajima, Tohru Mogami, Tadahiko Horiuchi, and Masakazu Yamashina, "A 0.25- μ m CMOS 0.9-V 100-MHz DSP Core," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, pp. 52–61, Jan. 1997.
 92. E. Seevinck, "A current sense-amplifier for fast CMOS SRAMs," in *1990 Symp. on VLSI Circuits Digest of Technical Papers*. IEEE, June 1990, pp. 71–72.

93. Y. K. Seng and S. S. Rofail, "1.5V high speed low power CMOS current sense amplifier," *Electron. Letters*, vol. 31, no. 23, pp. 1991–1993, Nov. 1995.
94. Jinn-Shyan Wang and Hong-Yu Lee, "A New Current-Mode Sense Amplifier for Low-Voltage Low-Power SRAM Design," in *Proc. Eleventh Annual IEEE Intern. ASIC Conference*, New York, Sept. 1998, IEEE, pp. 163–167.
95. Jae-Yoon Sim, Hongil Yoon, Ki-Chul Chun, Hyun-Seok Lee, Sang-Pyo Hong, Soo-Young Kim, Min-Soo Kim, Kyu-Chan Lee, Jei-Hwan Yoo, Dong-Il Seo, and Soo-In Cho, "Double Boosting Pump, Hybrid Current Sense Amplifier, and Binary Weighted Temperature Sensor Adjustment Schemes for 1.8V 128 Mb Mobile DRAMs," in *2002 Symp. on VLSI Circuits Digest of Technical Papers*. IEEE, June 2002.
96. Travis N. Blalock and Richard C. Jaeger, "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 618–625, Apr. 1992.
97. George R. Wilson, "A Monolithic Junction FET–n–p–n Operational Amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-3, no. 4, pp. 341–348, Dec. 1968.
98. Koichiro Ishibashi, Koichi Takasugi, Kunihiro Komiyaji, Hiroshi Toyoshima, Tashiaki Yamanaka, Akira Fukami, Naotaka Hashimoto, Nagatoshi Ohki, Akihiro Shimizu, Takashi Hashimoto, Takahiro Nagano, and Takashi Nishida, "A 6-ns 4-Mb CMOS SRAM with Offset-Voltage-Insensitive Current Sense Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 4, pp. 480–486, Apr. 1995.
99. Eckhard Braß, Ulrich Hilleringmann, and Klaus Schumacher, "System Integration of Optical Devices and Analog CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 8, pp. 1006–1010, Aug. 1994.
100. Giuseppe Palmisano and Gaetano Palumbo, "High Performance CMOS Current Comparator Design," *IEEE Trans. on Circuits and Systems II: Analog and Dig. Signal Processing*, vol. 43, no. 12, pp. 785–790, Feb. 1996.
101. G. Palmisano and G. Palumbo, "An Offset Compensated Fully Differential CMOS Current Comparator," in *Proc. 38th Midwest Symp. on Circuits and Systems*, 1996, vol. 2, pp. 1038–1041.
102. G. Palmisano, G. Palumbo, and S. Pennisi, "A High-Accuracy High-Speed CMOS Current Comparator," in *Proc. 1994 IEEE Intern. Symp. on Circuits and Systems*, 1994, vol. 5, pp. 739–742.
103. Fatih Hamzaoglu, Yibin Ye, Ali Keshavarzi, Kevin Zhang, Siva Narendra, Shekhar Borkar, Mircea Stan, and Vivek De, "Dual- V_T SRAM Cells with Full-Swing Single-Ended Bit Line Sensing for High-Performance On-Chip Cache in 0.13 μ m Technology Generation," in *ISLPED'00: Proc. 2000 Intern. Symp. on Low Power Electronics and Design*, July 2000, pp. 15–19.
104. Bernhard Wicht, Doris Schmitt-Landsiedel, Steffen Paul, and Anthony Sanders, "SRAM Current-Sense Amplifier with Fully-Compensated Bit Line Multiplexer," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2001, pp. 172–173, 443, 444.
105. Bernhard Wicht, Doris Schmitt-Landsiedel, and Steffen Paul, "Analysis and Compensation of the Bitline Multiplexer in SRAM Current Sense Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 11, pp. 1745–1755, Nov. 2001.
106. Bernhard Wicht, Doris Schmitt-Landsiedel, and Steffen Paul, "A Simple Low Voltage Current Sense Amplifier with Switchable Input Transistor," in *Proc. European Solid-State Circuits Conference*. IEEE, Sept. 2001, pp. 300–303.

107. Kenji Anami, Masahiko Yoshimoto, Hirofumi Shinohara, Yoshihiro Hirata, and Takao Nakano, "Design Consideration of a Static Memory Cell," *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 4, pp. 414–418, Aug. 1983.
108. Oliver Kiehl, *Schaltverhalten und Störsicherheit von höchstintegrierten Submikrometer-CMOS-Schaltungen*, Ph.D. thesis, Technische Universität München, 1989.
109. Jan M. Rabaey, *Digital Integrated Circuits – A Design Perspective*, Prentice-Hall, 1996.
110. Scott Thompson, Paul Packan, and Mark Bohr, "MOS Scaling: Transistor Challenges for the 21st Century," *Intel Technical Journal*, no. 3Q98, 1998, www.intel.com.
111. Kerry Bernstein, Manjul Bhushan, and Norman Rohrer, "On the Selection of the Optimal Threshold Voltages for Deep Submicron CMOS Technologies," *IBM MicroNews*, vol. 7, no. 1, pp. 29–31, First Quarter 2001, www.chips.ibm.com/micronews/vol7_no1/bernstein.html.
112. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits – Analysis and Design*, McGraw-Hill, New York, 1999.
113. Bharadwaj S. Amuratur and Mark A. Horowitz, "A Replica Technique for Wordline and Sense Control in Low-Power SRAM's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1208–1219, Aug. 1998.
114. Ryuhei Sasagawa, Isao Fukushi, Makoto Hamaminato, and Shoichiro Kawashima, "High-speed Cascode Sensing Scheme for 1.0V Contact-programming Mask ROM," in *1999 Symp. on VLSI Circuits Digest of Technical Papers*, New York, June 1999, IEEE, pp. 95–96.
115. Bernhard Wicht, Jean-Yves Larguier, and Doris Schmitt-Landsiedel, "A 1.5V 1.7ns 4kx32 SRAM with a Fully-Differential Auto-Power-Down Current Sense Amplifier," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2003.
116. Simulation results provided by Jean-Yves Larguier, Infineon Technologies, Sophia-Antipolis, France.
117. Bernhard Wicht, Ingo Martiny, Doris Schmitt-Landsiedel, Steffen Paul, and Anthony Sanders, "Speeding up CMOS Cameras and Optical Receivers by Improved Column Multiplexer," in *Optoelectronic Integrated Circuits and Packaging V, Proceedings of SPIE*. SPIE, Jan. 2001, vol. 4290, pp. 28–37.
118. James A. Hutchby, George A. Bourianoff, Victor V. Zhirnov, and Joe E. Brewer, "Extending to Road Beyond CMOS," *IEEE Circuits & Devices Magazine*, pp. 28–41, Mar. 2002.
119. K. Inomata, "Present and future of magnetic RAM technology," *IEICE Trans. Electron.*, vol. E84-C, no. 6, pp. 740–746, 2001.
120. Manzur Gill, Tyler Lowrey, and John Park, "Ovonic Unified Memory - A High-preformance Nonvolatile Memory Technology for Stand Alone Memory and Embedded Applications," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2002.
121. Feng-Tso Chien and Yi-Jen Chan, "Bandwidth Enhancement of Transimpedance Amplifier by a Capacitive-Peaking Design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 8, pp. 1167–1170, Aug. 1999.
122. Behzad Razavi, "A 622Mb/s 4.5pA/ $\sqrt{\text{Hz}}$ Transimpedance Amplifier," in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. IEEE, Feb. 2000, pp. 162–163.
123. Chao-Hsin Lu and Wei-Zen Chen, "Bandwidth Enhancement Techniques for Transimpedance Amplifiers in CMOS Technologies," in *Proc. European Solid-State Circuits Conference*. IEEE, Sept. 2001, pp. 192–195.

Index

- 1-transistor cell, 6
- 4-transistor cell, 6
- 6-T-cell, *see* memory cell
- 6-transistor cell, *see* memory cell

- access time, 2, 3, 124, 125
- access transistors, *see* transfer transistors
- address, 5, 7
- array-like structure, 127
- auto-power-down, 18, 119–121, 123

- bandwidth, 45, 56, 57, 90, 127
- biasing network, 112
- bitline, 2, 3, 5, 6, 39, 76, 81, 99, 124
 - bias current, 9, 39, 40, 72, 76, 77, 87, 91, 101, 110, 113, 116
 - capacitance, 6, 8–10, 50, 52, 53, 61, 69, 76
 - cross-section, 11
 - crossover capacitance, 76
 - dc voltage, *see* bitline voltage
 - distributed network model, 10
 - future technologies, 11
 - inductance, 6, 11
 - load, 6–8, 39, 72, 91, 110, 111, 127
 - load voltage drop, 9, 39, 43, 101
 - lumped network model, 11
 - matching, 117
 - minimum voltage, 43, 47, 67, 87
 - model, 10–13
 - multiplexer, *see* multiplexer
 - potential, *see* bitline voltage
 - resistance, 6, 10, 11
 - voltage, 6–9, 39, 40, 44, 47, 82, 92, 101, 104, 106, 107, 110
 - voltage swing, 8, 9, 11, 17, 53, 64, 115, 116
- block diagram
 - Type A, 41
 - Type B, 44
 - Type C, 54
 - Type D, 64
- body effect, 47, 82, 118
- bulk transconductance, 42, 44, 55
- busses, 127

- cache memory, 1, 17
- camera chips, 127
- capacitance mismatch, 26
- capacitive coupling, 30, 127
- cascode, 41
- cascode current sensing, *see* Type A
- cell current, 7–9, 11, 39, 40, 42, 47, 53, 76, 77, 107–108, 110, 113, 142
- cell stability, 101–107
 - future technologies, 105–107
- charge injection, 118
- CMFB, *see* common-mode feedback
- CMRR, 136
- column, 6, 81
- column multiplexer, *see* multiplexer
- common-gate transistor, 41
- common-mode feedback, 118
- common-mode gain, 48, 49, 58, 59, 68, 113, 135
- common-mode rejection, 59
- common-mode rejection ratio, *see* CMRR
- common-mode stability, 68, 78, 112, 135–138
- common-mode transfer function, 116
- comparator, 9, 15, 59, 71, 97
- compiler, 1
- complementary bitline, 6, 8, 9
- complementary bitlines, 43, 48, 58, 97, 102, 116
- control input, 88
- control theory, 49, 57
- critical bitline voltage, 104–106
- critical path, 124
- cross-coupled inverters, 17, 23, 25, 28, 35, 63
 - offset, 28

- crosstalk, 3, 9, 127
- current comparator, 64
- current gain, 129
- current mirror, 15, 16, 41, 64
- current sense amplifier, *see* current sensing
- current sensing, 3, 8–13, 20, 39–41, 101, 106
 - area, 81
 - area consumption, 121
 - basic principle, 40
 - bias current, 39, 40
 - circuit principles, 9, 39–80
 - classification, 39
 - control input, 88
 - delay, 10–13, 49, 51, 77, 82, 98, 99, 115, 144
 - delay comparison, 75
 - delay vs. supply voltage, 115, 141
 - delay vs. voltage sensing, 115
 - design, 109–121
 - design procedure, 110–113
 - equivalent circuit, 13, 82
 - input dc resistance, 40
 - input impedance, 13, 40, 81
 - input resistance, 82, 83
 - mismatch, 71
 - model, 82
 - noise margin, 94, 114, 115
 - offset, 71–74
 - output swing, 9
 - output voltage swing, 13, 17, 53, 69, 113–115, 141
 - power-down, 40, 116–121
 - precharge, 116–121
 - signal input, 88
 - timing, 119
 - transfer function, 12
 - Type A, *see* Type A
 - Type B, *see* Type B
 - Type C, *see* Type C
 - Type D, *see* Type D
 - vs. voltage sensing, 39
- current transfer function, 129, 131
 - Type A, 41–42
 - Type B, 45, 46, 48, 94
 - Type C, 55–58
 - Type D, 65, 88, 90, 91
- current-mode, 9
- cut-off frequency, 12, 42
- damping coefficient, 129
- decoupling resistor, 20
- delay crossover between current and voltage sensing, 53, 62, 70, 76, 115
- design of current sense amplifiers, 109–121
- differential amplifier, 9, 15, 44, 48, 49, 71, 117
- differential stage, 24, 28, 35
- differential voltage amplifier, *see* differential amplifier
- differential voltage gain, 48, 58, 136
- digital signal processors, 2
- diode-connected transistor, 41, 62, 63, 65
- distributed network, 10, 11
- DRAM, 1, 6, 17
- dummy bitline, 119
- dynamic voltage sense amplifiers, *see* voltage sense amplifiers, latch-type voltage sense amplifiers
- effective transconductance, 19, 25
- embedded memory, 1
- embedded SRAM, 1, 2, 127
- equalize transistors, 117
- error function, 28
- experimental results, 97–99, 102, 104, 108, 145–150
- feedback, 40, 41, 71, 88, 117, 130
 - negative, 44, 91
 - positive, 16–18, 20, 22, 54, 56, 58, 63, 102
- feedback amplifier, 44, 46, 62, 63, 77, 112, 116, 127
 - bandwidth, 46, 47, 56, 57, 60, 62, 67, 76
 - bias current, 116, 142
 - common-mode gain, 49, 58, 59, 111, 112
 - cut-off frequency, 46, 63, 112
 - design, 111–112
 - fully-differential, 48, 58, 63, 68
 - gain linearity, 127
 - gain-bandwidth product, *see* gain-bandwidth product
 - minimum output bias voltage, 47
 - non-inverting, 64, 67
 - offset, 71, 72, 77
 - phase margin, 67
 - single-ended output, 49, 59
 - speed, 53
 - step response, 51
 - transfer characteristics, 44

- voltage gain, 44, 45, 49, 51, 54, 57, 60, 62, 63, 111, 112
- figure of merit, 31
- fitting factor, 51, 61, 69, 115
- Flash EEPROM, 1
- flipflop, 20, 119
- frequency response
 - Type B, 46
 - Type D, 66
- future technologies, 76, 105–107, 127
- gain overshoot, 46, 129
- gain-bandwidth product, 52, 79, 111, 127, 142
- gate delay, 2
- Gaussian distribution, 26, 28
- Gaussian law of error propagation, 72, 73
- global variations, 26
- hierarchical architectures, 3
- hold transistors, 121
- Hurwitz stability criterion, 129
- I/O-block, 5, 6
- I/O-port, 5, 81, 112
- impedance matching, 40
- implementation aspects, 109–125
- input impedance
 - Type A, 41–42
 - Type B, 44
 - Type C, 56
- input resistance, 9, 10, 12, 13
- input/output port, 5
- interconnect delay, 2, 3
- inverter, 9, 15, 97, 104, 106, 119
 - switching level, 107
- inverter gain, 19
- large-signal analysis, 76–77
- latch, 28, 63, 101, 121
- latch-type voltage sense amplifier, 16, 18, 20–37, 110
 - conventional latch, 17, 35–36
 - delay, 22–25, 29, 31, 34, 35
 - delay deviation, 31, 33
 - design guideline, 36
 - figure of merit, 31
 - input dc voltage, 22, 24, 28, 30
 - input voltage difference, 35, 36
 - offset, 25–28, 35
 - operation current, 21–25, 28, 34, 36
 - optimum input dc voltage, 31–33
 - output voltage swing, 24
 - temperature, 34
 - transistor sizing, 34, 36
 - yield, 25–30, 34, 35
 - yield improvement, 28–30
- latching delay, 19, 23, 24
- layout area, 9, 77, 82, 91, 92, 99, 110, 112, 121
- load capacitance
 - current sensing, 9, 42, 43, 46, 63, 76, 111, 142
 - voltage sensing, 16, 17, 19, 22, 24, 26
- local variations, 25, 26, 74, 107
- log-log scale, 53, 70
- low power applications, 99, 101
- low supply voltages, 3
- low voltage applications, 9, 43, 105
- lumped network, 11
- magnetic RAM, *see* MRAM
- matching, *see* mismatch
- matching of transistors, 28, 71, 74, 117
- matching of transistors, 73
- memory cell, 5–7, 76, 101–108, 110, 125, 142
 - 1-transistor cell, 6
 - 4-transistor cell, 6
 - size, 6
 - stability, 6, 101–107
 - stability criterion, 101, 102, 105, 106
 - static noise margin, 101, 105, 107
- metastability, 18, 25, 28, 102, 103
- metastable point, *see* metastability
- metastable state, *see* metastability
- microprocessors, 2
- Miller-capacitance, 92
- mismatch, 62, 64, 74, 107, 110, 117
- Monte-Carlo simulation, 26, 28, 35, 74
- MRAM, 127
- multi-stage amplifier, 16
- multiplexer, 5, 6, 20, 43, 81–99, 111
 - area, 91, 99
 - biasing constraints, 82–84, 86–87
 - compensation, 87–99, 109, 111
 - compensation Type A, 95–96
 - compensation Type B, 94–95
 - compensation Type C, 95–96
 - compensation Type D, 88–94
 - current transfer function Type B, 94
 - current transfer function Type D, 88, 90, 91
 - equivalent circuit Type B, 94
 - equivalent circuit Type D, 88, 90
 - input current, 84

- position, 81, 82
- resistance, 9, 81–87, 92
- select signal, 88, 92, 110
- sensitivity on parameter variations, 92, 96
- transistor type, 82, 84, 86, 92
- MUX, *see* multiplexer
- negative impedance converter, 56, 96
- NIC, *see* negative impedance converter
- noise, 64
- noise margin, 6, 101, 104
- non-volatile memory, 6
- offset, 49, 68, 71–74, 77, 116, 117
- offset voltage, 25, 26, 35
 - standard deviation, 27, 28
- OUM, 127
- Ovonic Unified Memory, *see* OUM
- pass-gates, 20, 35
- phase change RAM, *see* OUM
- power consumption, 2, 3, 5, 9, 16, 18, 20, 22, 39, 40, 77, 81, 106, 110, 112, 116, 118, 119, 125
- power-down, 116–121
- precharge, 7, 9, 22, 40, 110, 113, 116–121
- precharge devices, 8, 116
- principle of multiplexer compensation, 88
- probability, 26
- probability density function, 27
- pseudo SRAM, 6
- read operation, 5, 7, 8, 103, 104, 106, 110, 125
- read-only memory, *see* ROM
- receivers, 127
- reduced transconductance, 94
- regulated cascode, 44
- regulated cascode current sensing, *see* Type B
- replica bitline, 119
- residual method, 131
- resonance frequency, 129
- ringing, 47, 67, 129
- ROM, 127
- row, 7
- Seevinck, 62
- semiconductor memory, 1
- sense amplifier, 2, 6, 8
- sense-amplifier-based flipflop, 20
- sensing
 - delay, 10–13, 74, 115
 - delay vs. supply voltage, 115, 141–144
 - differential, 8, 15, 16, 62, 71, 77
 - differential Type A, 43
 - differential Type B, 48–49
 - differential Type C, 58–59, 62
 - differential Type D, 67–68, 109
 - differential vs. single-ended, 49
 - fundamentals, 5
 - methods, 8–13
 - single-ended, 8, 77
 - single-ended Type B, 44–47, 49
 - single-ended Type C, 54–58
 - single-ended Type D, 64–68
- sensing delay, 12, 13
- Shibata, 39
- shmoo plot, 124
- signal input, 88
- signal processing speed, 1, 3
- small-signal analysis, 40, 41, 44, 58, 64, 67, 76–77
- small-signal equivalent circuit
 - Type A, 41
 - Type B, 44
 - Type C, 54
 - Type D, 64
- SoC, 1, 2, 5
- speed, 3
- SRAM, 5
 - capacity, 5
 - column architecture, 6
 - delay vs. memory size, 9
 - differential, 6, 8
 - dual-port, 122
 - embedded, 6, 127
 - fundamentals, 5
 - macro, 97, 121, 125, 145
 - single-chip, 6
 - single-ended, 6, 8
 - static noise margin, 6
- SRAM macro, 99
- stability, 56, 58, 59, 67, 68, 77, 101–107, 129–130
- standard deviation, 26
- static memory cell, *see* memory cell
- static noise margin, 6, 101, 105, 107
- static random access memory, *see* SRAM
- static voltage sense amplifiers, *see* voltage sense amplifiers
- step response, 11, 76, 131–133, 145
 - Type B, 46, 48, 50, 94

- Type C, 57, 59, 60
- Type D, 67, 68, 93–94, 97
- supply voltage, 3, 77, 110, 113, 119
- current sensing Type A, 43, 96
- current sensing Type B, 47
- current sensing Type C, 58, 96
- current sensing Type D, 67
- influence on bitline bias current, 113
- influence on sensing delay, 115, 141–144
- memory cell, 106, 107
- multiplexer, 82, 92
- voltage sensing, 25, 30, 36
- switch, 81–83, 110–112
- on-resistance, 81
- transistor type, 82, 84, 86, 92
- system-on-a-chip, *see* SoC
- temperature, 34, 92, 96, 118, 119
- transconductance, 42, 43, 52, 61, 111, 112, 114, 141, 142
- transfer transistors, 6–8, 102–104, 107, 142
- transient behavior
 - Type A, 43
 - Type B, 49
 - Type C, 59, 60
 - Type D, 66, 68
- transmission gate, 82
- two-pole transfer function, 129–130
- two-stage amplifier, 16
- Type A, 41–43, 45, 64, 65, 77–78
 - area, 42
 - bias current, 42
 - block diagram, 41
 - current transfer function, 41–42
 - delay, 42, 43
 - differential sensing, 43
 - input impedance, 41–42
 - input resistance, 42
 - low supply voltage, 43
 - minimum supply voltage, 43
 - multiplexer compensation, 95–96
 - output current, 41, 42
 - output voltage, 42
 - small-signal equivalent circuit, 41
 - step response, 42
 - transient behavior, 43
- Type B, 44–54, 77–78
 - area, 49
 - block diagram, 44
 - common-mode output, 48, 49
 - current transfer function, 45, 46, 48, 94
 - damping coefficient, 46, 66
 - dc current gain, 46
 - delay, 46, 47, 49–54, 74, 94
 - delay crossover, 53
 - delay crossover voltage sensing, 53
 - delay vs. bitline capacitance, 52
 - differential output signal, 49, 71
 - differential sensing, 48–49
 - equivalent circuit with multiplexer, 94
 - frequency response, 46
 - input impedance, 44, 53
 - input resistance, 45, 53
 - minimum delay, 52
 - minimum supply voltage, 47
 - mismatch, 74
 - multiplexer compensation, 94–95
 - multiplexer influence, 94
 - offset, 49, 68, 71–74
 - output current, 46
 - output voltage, 47, 49
 - resonance frequency, 46
 - single-ended sensing, 44–47, 49
 - small-signal equivalent circuit, 44
 - step response, 46, 48, 50, 94
 - transient behavior, 49
- Type C, 54–64, 77–78
 - block diagram, 54
 - common-mode output, 59
 - common-mode stability, 59, 63
 - current transfer function, 54–58
 - damping coefficient, 56
 - dc current gain, 56
 - delay, 57, 60–63
 - delay crossover voltage sensing, 62
 - delay vs. bitline capacitance, 62
 - differential output signal, 58
 - differential sensing, 58–59, 62
 - implementation examples, 62–64
 - input impedance, 54, 56
 - input resistance, 56
 - low supply voltage, 58, 63
 - minimum delay, 61
 - multiplexer compensation, 95–96
 - output current, 54
 - output voltage, 54, 57, 60, 62
 - resonance frequency, 56
 - single-ended sensing, 54–58
 - small-signal equivalent circuit, 54
 - stability, 62
 - stability criteria, 58, 63
 - step response, 57, 59, 60
 - transient behavior, 59, 60

Type D, 64–70, 77–78, 109

- block diagram, 64
- common-mode output, 68
- common-mode stability, 68
- current transfer function, 65, 88, 90, 91
- damping coefficient, 66
- dc current gain, 66
- delay, 65, 69–70, 74, 92, 115
- delay crossover, 70
- delay crossover voltage sensing, 70, 115
- delay vs. bitline capacitance, 69
- delay vs. supply voltage, 115
- differential output signal, 68, 71
- differential sensing, 67–68, 109
- equivalent circuit with multiplexer, 88, 90
- frequency response, 66
- input resistance, 64
- low supply voltage, 67
- minimum delay, 69
- minimum supply voltage, 67
- mismatch, 74
- multiplexer compensation, 88–94
- multiplexer influence, 88–90
- offset, 71–74
- output current, 65, 68
- output voltage, 65
- resonance frequency, 66
- single-ended sensing, 64–68
- small-signal equivalent circuit, 64
- stability condition, 68
- step response, 67, 68, 93–94, 97
- transient behavior, 66, 68

upscaled model, 103

voltage comparator, *see* comparator

voltage divider, 142

voltage sense amplifiers, 8, 9, 13, 15–37, 110, 114

- area, 121
- decision phase, 18, 19
- delay, 16, 18–20, 24
- dynamic, 16–36
- enable signal, 18, 119
- initial voltage difference, 19, 22–25, 28–30
- input voltage difference, 20, 24, 71
- latch-type, *see* latch-type voltage sense amplifier
- minimum required input voltage difference, 30, 71
- mismatch, 16, 18, 19, 25, 28
- multiplexer influence, 81, 82
- noise, 16, 18
- sensing phases, 17
- static, 15–16
- static vs. dynamic, 19
- time constant, 16, 19
- transient behavior, 17, 20, 29
- yield, 19
- voltage sensing, 8–13, 39, 71, 101, 106
 - delay, 9–13, 43, 53, 60, 70, 101, 115, 144
 - delay vs. supply voltage, 115, 141
 - equivalent circuit, 12
 - noise margin, 20

Wilson current mirror, 64

Wilson type current sensing, *see*

Type D

wordline, 2, 3, 5–7, 103, 110, 118, 119, 123, 124

write amplifier, 6, 7

write operation, 5, 7, 101, 110

write recovery, 7, 101

yield, 25, 31, 101, 110, 149

yield improvement, 28–30

yield measurements, 28, 149