A. Two-Pole Transfer Function

Often, the signal transfer, e.g. from input current i_{in} to an output current i_{out}, is governed by a two-pole transfer function like

$$G(s) = \frac{K}{(s - s_1)(s - s_2)} = K\frac{1}{s^2 + as + b} \quad . \tag{A.1}$$

In analogy to an oscillator this equation can be rewritten as

$$G(s) = \frac{G_o\omega_r^2}{s^2 + s2\omega_r D + \omega_r^2} \quad . \tag{A.2}$$

The transfer behavior is characterized by these parameters [79]:

G_o	dc value of G(s), i.e., dc and low frequency gain, $G_o = G(s = 0)$
ω_r	resonance frequency
D	damping or damping coefficient, respectively

For damping coefficients above unity the poles of (A.2) are real values, for $D = 1$ a double real pole occurs. For values $D < 1$, both poles leave the real axis and become complex conjugated. In the frequency domain this results in a gain overshot (at the resonance frequency ω_o) while in the time domain some amount of ringing can be observed.

Ringing and gain overshot relate to system stability. In general, a system is stable if all poles of the transfer function have a negative real part. In circuit design often the poles are not available explicitly and the denominator is rather represented by a polynomial. In this case the coefficients of the polynomial are utilized to analyze and maintain the stability of this system. Among others, the Hurwitz stability criterion can be applied. For two-pole functions like (A.2) it requires the coefficients a and b of the second order polynomial to be positve. Hence,

$$\mathrm{Re}\{s_1, s_2\} < 0 \quad \Longleftrightarrow \quad a, b > 0 \quad . \tag{A.3}$$

Even though these conditions are met, ringing can still be too large. As a rule of thumb, in practical applications the damping coefficient should always be greater than 0.5 [79], i.e.,

$$D > \frac{1}{2} \quad . \tag{A.4}$$

In order to achieve a fast response, the upper limit of the damping coefficient should be unity. In systems with feedback the stability is exclusively determined by the frequency response of the loop gain. As the loop gain increases it will be more difficult to maintain the condition of (A.4).

B. Step Response

A system can be described by its transfer function. In order to obtain the time domain response to a step signal at the input the residual method can be applied. With focus on current sensing a transfer function $G(s) = \frac{i_{out}}{i_{in}}$ will be assumed. With an input current step $i_{in}(s) = \frac{I_m}{s}$ of magnitude I_m the residual theorem [67] yields

$$\begin{aligned} i_{out}(t) = \mathcal{L}^{-1}\{i_{out}(s)\} &= I_m \sum_{s=0,\, s_i} \text{Res}\left[\frac{G(s)}{s} e^{st}\right] \\ &= I_m \left\{ G_o + \sum_{s=s_i} \text{Res}\left[\frac{G(s)}{s} e^{st}\right] \right\} \end{aligned} \tag{B.1}$$

with the dc gain G_o according to (A.2). If the system is stable (refer to (A.3)) a final value

$$i_{out}(t \to \infty) = I_m G_o \tag{B.2}$$

can be derived.

A pair of complex conjugated poles may occur in the form

$$\begin{aligned} s_1 &= \alpha + j\beta \\ s_2 &= \alpha - j\beta \end{aligned} \tag{B.3}$$

Based on (B.1) and (B.3) the step response for various transfer functions, which are important in the field of current sensing, are derived below.

(a) One pole, no zero

$$\boxed{G(s) = K\frac{1}{(s - s_1)} = -\frac{G_o s_1}{(s - s_1)}} \tag{B.4}$$

In this simple case the step response is given by

$$i_{out}(t) = I_m G_o (1 - e^{s_1 t}) \quad . \tag{B.5}$$

From this equation the delay until i_{out} reaches a specified value I_{out} can be calculated in the form

$$t = \frac{1}{s_1} \ln\left(1 - \frac{I_{out}}{I_m G_o}\right) \quad . \tag{B.6}$$

If the delay is referred to 63% of the final value $I_m G_o$ (see also (4.31)), the logarithmic term becomes (-1). Then the reciprocal value of the pole is a measure for the delay.

(b) One pole, one zero

$$\boxed{G(s) = K\frac{(s - s_o)}{(s - s_1)} = -\,G_o \frac{s_1}{s_o}\frac{(s - s_o)}{(s - s_1)}} \tag{B.7}$$

Equation B.1 results in a step response

$$i_{out}(t) = G_o I_m \left\{1 + \left(\frac{s_1 - s_o}{s_o}\right) \mathrm{e}^{s_1 t}\right\} \quad . \tag{B.8}$$

From this equation the delay until i_{out} reaches a given value I_{out} can be calculated in the form

$$\begin{aligned} t &= \frac{1}{s_1} \ln\left\{\left(1 - \frac{I_{out}}{I_m G_o}\right) \frac{s_o}{s_o - s_1}\right\} \\ &= \frac{1}{s_1}\left\{\ln\left(1 - \frac{I_{out}}{I_m G_o}\right) - \ln\left(\frac{s_o - s_1}{s_o}\right)\right\} \quad . \end{aligned} \tag{B.9}$$

The right hand expression of (B.9) consists of two logarithmic terms. If the delay is referred to 63% of the final value $I_m G_o$ (see also (4.31)), the first logarithmic term becomes (-1). If in addition the second term is approximated based on $\ln x \approx (x - 1)$, (B.9) simplifies to

$$t = -\frac{1}{s_1}\left(\frac{s_o - s_1}{s_o}\right) = -\frac{1}{s_1} + \frac{1}{s_o} \quad . \tag{B.10}$$

Due to the zero the delay is reduced in comparison to a one-pole system without zero, (B.6).

(c) Two poles, no zero

$$\boxed{G(s) = K\frac{1}{(s - s_1)(s - s_2)} = \frac{G_o s_1 s_2}{(s - s_1)(s - s_2)}} \tag{B.11}$$

From (B.1)

$$i_{out}(t) = G_o I_m \left\{1 + \frac{e^{s_1 t}}{\frac{s_1}{s_2} - 1} + \frac{e^{s_2 t}}{\frac{s_2}{s_1} - 1}\right\} \tag{B.12}$$

can be found. For real poles s_1 and s_2 (B.12) sufficiently describes i_{out} in the time domain. Depending on the values one pole will be dominant.

In the presence of complex conjugated poles according to (B.3), the following expression can be derived:

$$\begin{aligned} i_{out}(t) &= I_m G_o \left\{1 + \frac{(\alpha - j\beta)e^{(\alpha+j\beta)t} - (\alpha+j\beta)e^{(\alpha-j\beta)t}}{(\alpha+j\beta)-(\alpha-j\beta)}\right\} \\ &= I_m G_o \left\{1 + e^{\alpha t}\left(\frac{\alpha}{\beta}\frac{1}{2j}(e^{j\beta t} - e^{-j\beta t}) - \frac{1}{2}(e^{j\beta t} + e^{-j\beta t})\right)\right\} \\ &= I_m G_o \left\{1 + e^{\alpha t}\left(\frac{\alpha}{\beta}\sin\beta t - \cos\beta t\right)\right\} \end{aligned}$$

Comparing the coefficients of the denominator polynomial in (B.11) with the ones in (A.2),

$$(s - s_1)(s - s_2) = (s - \alpha - j\beta)(s - \alpha + j\beta) = s^2 + s2D\omega_r + \omega_r^2$$

results in

$$\begin{aligned} &\alpha = -D\omega_r \quad , \\ &\beta = \omega_e = \sqrt{\omega_r^2(1 - D^2)} \quad . \end{aligned}$$

where ω_e ($= \beta$) refers to the eigenfrequency. Hence,

$$i_{out}(t) = I_m G_o \left\{1 - e^{-D\omega_r t}\left(\frac{D\omega_r}{\omega_e}\sin\omega_e t + \cos\omega_e t\right)\right\} \quad . \tag{B.13}$$

Equation (B.13) allows to derive the step response without explicitly knowing the poles.

(d) Two poles, one zero

$$\boxed{G(s) = K\frac{(s - s_o)}{(s - s_1)(s - s_2)} = -\frac{G_o s_1 s_2}{s_o}\frac{(s - s_o)}{(s - s_1)(s - s_2)}} \tag{B.14}$$

The residual theorem of (B.1) yields

$$i_{out}(t) = I_m G_o \left\{1 - \frac{1}{s_o(s_1 - s_2)}\left(s_2(s_1 - s_o)e^{s_1 t} - s_1(s_2 - s_o)e^{s_2 t}\right)\right\} \quad . \tag{B.15}$$

While this expression is adequate for real poles, it can be further resolved if conjugated complex poles occur:

$$i_{out}(t) = G_o I_m \left\{1 - e^{-D\omega_r t}\left(\frac{D\omega_r}{\omega_e}\left(1 + \frac{\omega_r}{Ds_o}\right)\sin\omega_e t + \cos\omega_e t\right)\right\} \quad . \tag{B.16}$$

Equation (B.16) differs from (B.13) by the highlighted factor.

C. Common-Mode Stability

Differential Type C and Type D current sensing circuits as described in Sects. 4.4.2 and 4.5.2 may become instable due to finite common-mode gain of the feedback amplifier. As the stability conditions expressed by (4.62) and (4.88) are similar, this issue will be discussed with focus on Type D. For the implementation of Type D according to Fig. 4.32 common-mode stability requires

$$-A_{CM} = |A_{CM}| < \frac{1}{r_{in} g_m} \tag{C.1}$$

where A_{CM} refers to the common-mode voltage gain of the fully-differential feedback amplifier. Figure C.1 illustrates the transient behavior of the output and bitline voltages if (C.1) is violated. Within a certain delay the output voltages v_{outp}, v_{outn} approach V_{DD} while the bitline voltage v_{BL} goes to a value near 0V. The actual diffential part of the signals v_{outp} and v_{outn} is superimposed to a common-mode part (see also Fig. 4.33).

In order to satisfy (C.1) the absolute value of the common-mode gain A_{CM} has to be as low as possible. From the circuit model of Fig. C.2 for a simple differential stage the common-mode gain can be found to be

$$A_{CM} = -\frac{r_o}{2r_B + \frac{1}{g_{mn}}\left(1 + \frac{r_o + 2r_B}{r_{DS}}\right)} \tag{C.2}$$

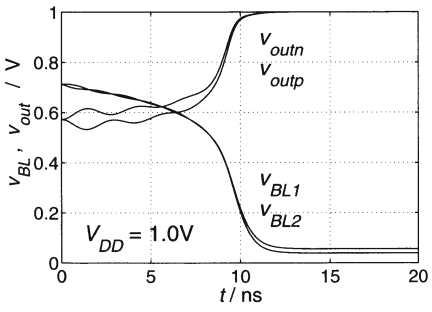

Fig. C.1. Simulated transient response of a Type D differential current sensing circuit in the presence of instability

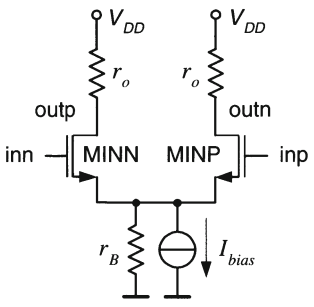

Fig. C.2. Circuit model of a simple differential amplifier

where g_{mn} and r_{DS} denote the transconductance and the output resistance of MINP and MINN. As these transistors operate in the saturation region, the denominator is dominated by r_B and the second term in the denominator can be neglected. Therefore, (C.2) can be simplified to

$$A_{CM} = -\frac{r_o}{2\,r_B} \tag{C.3}$$

which can often be found in the literature [66]. Figure C.2 results in a differential gain of

$$A_D = g_{mn}\,r_o \quad . \tag{C.4}$$

According to (C.1), it is essential to use feedback amplifier circuits with small common-mode gain. On the other hand, for good performance (sensing speed) the differential gain must not be too small. As a figure of merit the common-mode rejection ratio CMRR can be taken into account. Dividing (C.4) by (C.2) yields

$$\mathrm{CMRR} = \left|\frac{A_D}{A_{CM}}\right| = 2\,g_{mn}\,r_B \quad . \tag{C.5}$$

To achieve a large CMRR the input transistors should have a large transconductance g_{mn}. In addition, a bias current source with a large output resistance r_B is of advantage. Since the current source is basically formed by a transistor, r_B represents its drain-source resistance. The resistance r_B can be further increased as shown in Fig. C.3a. In comparison to a simple differential amplifier Fig. C.3a comprises an additional cascode transistor MC that improves the bias current source formed by transistor MB. Due to the additional series transistor an implementation for low supply voltages becomes difficult. The circuit example of Fig. C.3b achieves differential opperation by using

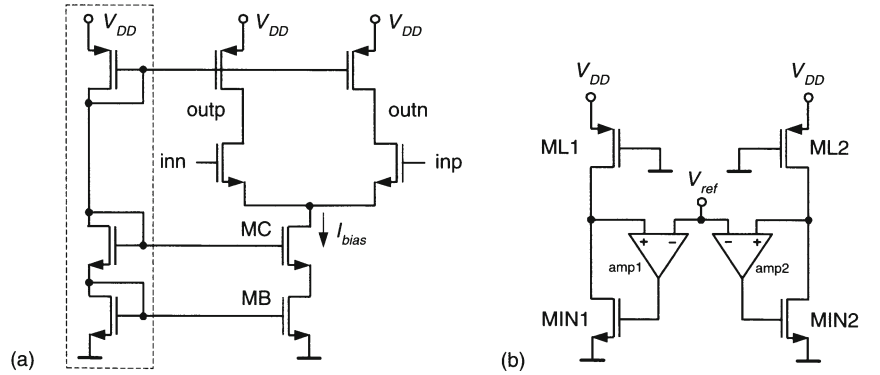

Fig. C.3. Circuits with reduced influence of the common-mode gain. (**a**) differential voltage amplifier with cascode transistor MC; (**b**) differential current sensing based on two single-ended circuits

two single-ended sensing circuits which do not suffer from common-mode instability. The use of two amplifiers increases layout area, power dissipation, and also the offset influence. In addition a reference voltage V_{ref} has to be generated. In this context it also has to be noted that sophisticated analog applications use common-mode feedback circuits to control the common-mode output voltage.

In SRAM designs most of the above circuit techniques are not suitable, because the area and power penalty and the biasing effort cannot be accepted. Consequently, there will still be a considerable common-mode gain. For a given common-mode gain A_{CM}, (C.1) requires small values of r_{in} and g_m. This is contrary to the conditions for high sensing speed. Due to the constraints regarding A_{CM}, r_{in} and g_m, common-mode stability is difficult to ensure.

On the other hand, from Fig. C.1 it can be observed that the time constant of the common-mode part is much larger than the sensing delay determined by the differential signal. Therefore an instable operation can be tolerated if the sensing takes place at the very beginning followed by an immediate deactivation of the sense amplifier. With respect to Fig. C.1 sensing can be finished below 1ns while a significant influence due to common-mode instability does not occur up to 5ns. This has to be analyzed further.

The transfer function of (4.85) consists of a common-mode and a differential part. Due to the linearity theorem of the Laplace transform [67] also the corresponding step response can be separated into a common-mode and a differential term, i_{CM} and i_D, respectively. Assuming a step magnitude I_m, this yields

$$\frac{i_{out}(t)}{I_m} = \frac{i_{CM}}{I_m} + \frac{i_D}{I_m} \tag{C.6}$$

where

$$\frac{i_{CM}}{I_m} = \frac{1}{2}\frac{A_{CM}g_m r_{in}}{1 + A_{CM}g_m r_{in}} \left\{1 - e^{-\frac{t}{C_{in}}\left(\frac{1}{r_{in}} + A_{CM}g_m\right)}\right\}$$

$$\frac{i_D}{I_m} = \frac{1}{2}\frac{A_D g_m r_{in}}{1 + A_D g_m r_{in}} \left\{1 - e^{-\frac{t}{C_{in}}\left(\frac{1}{r_{in}} + A_D g_m\right)}\right\} .$$

It has to be noted that unlike the diffential part, the exponential term of the common-mode part will become positive if (C.1) is not satisfied causing a fast increase of $i_{CM}(t)$. For a correct circuit operation, the common-mode part i_{CM} must not exceed a certain fraction of the wanted signal i_D. In order to calculate the ratio $\frac{i_{CM}}{i_D}$ at a given time, it is convenient to focus on multiples q of the time constant of i_D, i.e.,

$$t = q \frac{1}{\frac{1}{C_{in}}\left(\frac{1}{r_{in}} + A_D g_m\right)} \quad . \tag{C.7}$$

Accordingly, the current ratio becomes

$$\frac{i_{CM}}{i_D} = \frac{A_{CM}}{A_D} \frac{1 + A_D g_m r_{in}}{1 + A_{CM} g_m r_{in}} \frac{1 - e^{-q \frac{\frac{1}{r_{in}} + A_{CM} g_m}{\frac{1}{r_{in}} + A_D g_m}}}{1 - e^{-q}} \quad . \tag{C.8}$$

This ratio can be expressed as a function of $x = \frac{1}{g_m r_{in}}$, i.e.,

$$\frac{i_{CM}}{i_D} = \frac{A_{CM}}{A_D} \frac{x + A_D}{x + A_{CM}} \frac{1 - e^{-q \frac{x + A_{CM}}{x + A_D}}}{1 - e^{-q}} \tag{C.9}$$

At a given time (determined by q) this equation describes the ratio of the possibly instable common-mode signal i_{CM} to i_D. According to (C.1) the sensing circuit will be stable as long as $x > |A_{CM}|$. Figure C.4 shows a typical graph defined by (C.9) for different multiples q of the time constant of i_D. The intersection with the y-axis represents the worst case. Based on (C.9) it can be calculated by

$$\left.\frac{i_{CM}}{i_D}\right|_{x=0} = \frac{1 - e^{-q \frac{A_{CM}}{A_D}}}{1 - e^{-q}} \approx \frac{A_{CM}}{A_D} = \frac{1}{\text{CMRR}} \quad . \tag{C.10}$$

A small ratio $\frac{i_{CM}}{i_D}$ can mainly be achieved by a large common-mode rejection ratio CMRR of the feedback amplifier as it determines $\frac{A_{CM}}{A_D}$ (see (C.5)). The need for a small common-mode gain agrees to (C.1).

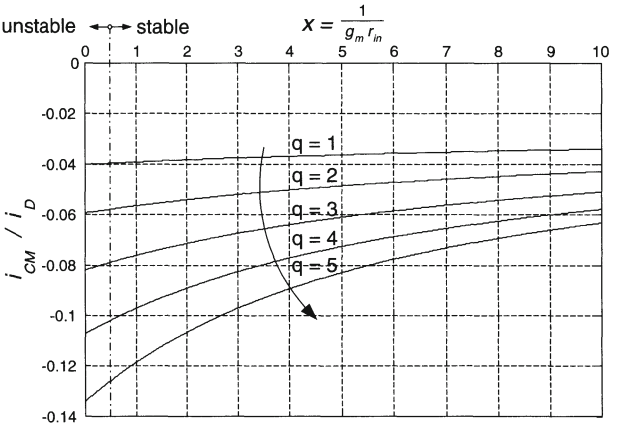

Fig. C.4. Common-mode rejection. The ratio $\frac{i_{CM}}{i_D}$ is plotted as a function of $\frac{1}{g_m r_{in}}$ at different times $t = q\tau$ with parameters $A_D = 20$, $A_{CM} = -0.5$. The maximum ratio $\left|\frac{i_{CM}}{i_D}\right|$ can be obtained from the intersection with the y-axis. This ratio increases with time and yields 4% at $q = 1$ and 13.4% at $q = 5$. Although the circuit is unstable for values below $x = -A_{CM} = 0.5$, even for $x = 0$ ($g_m \to \infty$, $r_{in} \to \infty$) a finite value of $\frac{i_{CM}}{i_D}$ can be obtained. For $q \to 0$ the ratio reaches the minimum $\left|\frac{i_{CM}}{i_D}\right| = 2.5\%$

The above investigation represents only an estimation as it does not consider the frequency dependence of common-mode and differential gain. If the frequency behavior is taken into account the time constants of both i_D and i_{CM} will increase. Even though the resulting equations will be very complex, it can be shown that the stability criterion of (C.1) holds. Moreover, while the limited bandwidth of the differential gain causes ringing of the signal i_D, ringing will not occur for the common-mode signal i_{CM}.

It can be concluded that also for common-mode instability a correct sensing operation can be achieved because the differential part of the output voltages v_{outp}, v_{outn} develops much faster than the common-mode part of these signals. The circuit will initialized by precharge as described in Sect. 7.3.

D. Delay Versus Supply Voltage

Sense amplifiers have to be able to operate at various supply voltage levels depending on the product specification. Since sensing speed is the major advantage of current sense amplifiers it is interesting to investigate how the speed depends on V_{DD} in comparison to voltage sensing. For the design example in Chap. 7 the delay has been plotted in Fig. 7.5 as a function of V_{DD}. Obviously, in that case, current sensing is more sensitive to changes of the supply voltage than voltage sensing. It has to be analyzed if this increased sensitivity of current sensing is due to this particular design or if it represents an inherent property of the sensing circuit.

In Sect. 7.2 it has been discussed that the output voltage swing ΔV_{out} of the current sensing stage should reach a value $p\,V_{DD}$ to ensure a correct decision of the voltage sense amplifier. This is based on the yield analysis of the voltage sense amplifier presented in Chap. 3 where Fig. 3.13 shows the relation between voltage swing and V_{DD}. The factor p is identical to the slope in that figure. For example, $p = 0.05$ can be extracted for a yield of 99.8%. If ΔV_{out} is substituted by $p\,V_{DD}$ the delay expression of (4.38) becomes

$$t_c(V_{DD}) = \sqrt{\frac{C_{BL}}{kA_o\omega_o}\,\frac{p\,V_{DD}}{I_m}} = C_{BL}\sqrt{\frac{p\,V_{DD}}{I_m}}\,\underbrace{\sqrt{\frac{1}{C_{BL}kA_o\omega_o}}}_{d_c} \quad . \tag{D.1}$$

Being an approximation (D.1) is valid for Type B, C and D. The second square root term d_c represents the difference to voltage sensing delay.

To allow for a comparison, the voltage sensing delay according to (2.10) can be rewritten to

$$t_v(V_{DD}) = C_{BL}\frac{p\,V_{DD}}{I_m} = C_{BL}\sqrt{\frac{p\,V_{DD}}{I_m}}\,\underbrace{\sqrt{\frac{p\,V_{DD}}{I_m}}}_{d_v} \quad . \tag{D.2}$$

The delay difference between (D.1) and (D.2) is determined by the factors d_c and d_v. The magnitude I_m of the cell current and the feedback amplifier's gain-bandwidth product $A_o\omega_o$ depend on the supply voltage.

With focus on the differential amplifier of Fig. 7.2 $A_o\omega_o$ is basically proportional to the transconductance of the input transistor of amplifier divided

by the output load capacitance C_L. As this transconductance is a function of the bias current I_B the gain-bandwidth product is given by

$$A_o\omega_o = \frac{g_m}{C_L} = \frac{1}{C_L}\sqrt{2\,\beta\,I_B} \quad . \tag{D.3}$$

In Fig. 7.2 the bias current is provided by transistor MB1. Since the biasing network forms a voltage divider, the gate potential V_G of MB1 will be a fraction of V_{DD}, i.e., $V_G = V_{DD}/n_c$ with $n_c > 1$. To first order, the factor n_c can be assumed to be constant. Therefore, the bias current of the feedback amplifier can be approximated by

$$I_B = \frac{\beta}{2}\left(\frac{V_{DD}}{n_c} - V_{th}\right)^2 \tag{D.4}$$

and (D.3) becomes

$$A_o\omega_o = \frac{\beta}{C_L}\left(\frac{V_{DD}}{n_c} - V_{th}\right) \quad . \tag{D.5}$$

For simplicity it is assumed that all transistors have the same transconductance parameter β. Equation (D.5) reveals a linear dependency on V_{DD}.

As C_{BL} and k are constants with respect to supply voltage, the delay factor d_c of (D.1) can be represented by a general approach

$$d_c = \sqrt{\frac{1}{c_1\,V_{DD} + c_2}} \quad . \tag{D.6}$$

Figure D.1a proofs the validity of the approximation of the term $C_{BL}kA_o\omega_o$ by a linear function $(c_1\,V_{DD} + c_2)$.

The factor d_v of the bitline delay during voltage sensing contains the cell current $I_m = I_{cell}$ which has been plotted in Fig. 6.9 as a function of V_{DD}. In the relevant range of V_{DD} (above 0.8V), the current is nearly proportional to V_{DD}. Therefore, in general, d_v can be expressed by

$$d_v = \sqrt{\frac{V_{DD}}{c_3\,V_{DD} + c_4}} \quad . \tag{D.7}$$

Figure D.1a reveals a good matching between the term I_{cell}/p and its linear approximation $(c_3\,V_{DD} + c_4)$. By using this linear approximation of the cell current a characteristic point is the intersection with the V_{DD}-axis. As can be seen in Fig. 6.9, this occurs at some value of V_{DD} near the threshold voltage of the transfer transistor of the memory cell (transistors MT1, MT2 in Fig. 2.2). Accordingly, the intersection refers to $V_{DD} = n_v V_{th}$ with a factor n_v similar to n_c for current sensing.

Based on d_c and d_v the sensitivity of both voltage and current sensing on changes of the supply voltage can be analyzed. For this reason the sensitivity function has to be derived which quantifies the relative deviation of d_c and, respectively, d_v on a relative change of V_{DD}. For current sensing this results in

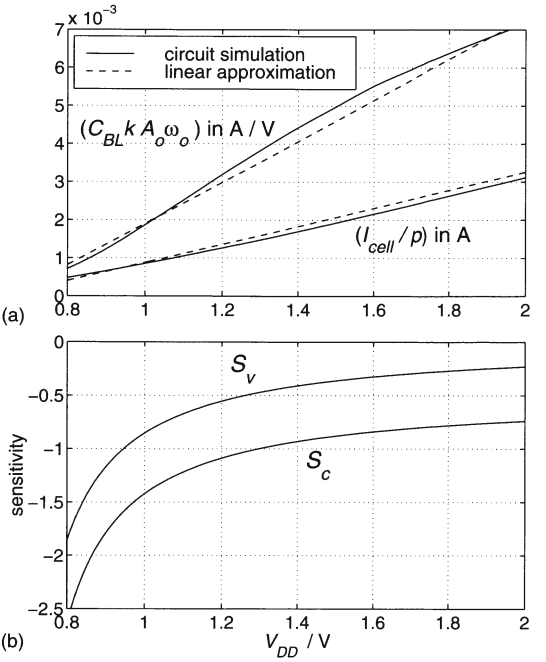

Fig. D.1. On the supply voltage dependence of the sensing delay. All curves correspond to the design example of Chap. 7 (Fig. 7.1). (**a**) Linearization of the terms $C_{BL}kA_o\omega_o$ and I_{cell}/p (obtained from simulation) by $(c_1\,V_{DD} + c_2)$ and $(c_3\,V_{DD} + c_4)$, respectively. Parameters are $c_1 = 5.4\text{mA/V}^2$, $c_2 = -3.5\text{mA/V}$, $c_3 = 2.4\text{mA/V}$, $c_4 = -1.5\text{mA}$, $p = 0.05$, $k = 0.4$, and $C_{BL} = 500\text{fF}$. (**b**) Sensitivities S_c (current sensing) and S_v (voltage sensing) of the sensing delay to changes of the supply voltage plotted as a function of V_{DD} (parameters: $n_c = 2.1$, $n_v = 2.2$, $V_{th} = 0.3\text{V}$)

$$S_c = \frac{\Delta d_c/d_c}{\Delta V_{DD}/V_{DD}} = \frac{\partial d_c}{\partial V_{DD}}\,\frac{V_{DD}}{d_c} = -\frac{1}{2}\,\frac{1}{1+\frac{c_2}{c_1 V_{DD}}} \quad . \tag{D.8}$$

From (D.1), (D.5) and (D.6) the ratio $\frac{c_2}{c_1} = -n_c V_{th}$ can be obtained and inserted into (D.8). This yields

$$S_c = -\frac{1}{2}\,\frac{1}{1-\frac{n_c V_{th}}{V_{DD}}} \quad . \tag{D.9}$$

Applying the same procedure to d_v gives

$$S_v = \frac{\Delta d_v/d_v}{\Delta V_{DD}/V_{DD}} = \frac{\partial d_v}{\partial V_{DD}}\,\frac{V_{DD}}{d_v} = \frac{1}{2}\,\frac{1}{1-\frac{c_3}{c_4 V_{DD}}} \quad . \tag{D.10}$$

The ratio of the coefficients c_3, c_4 can be calculated from the intersection of I_{cell} with the V_{DD}-axis (Fig. 6.9), defined by

$$0 = \frac{I_{cell}(V_{DD} = n_v V_{th})}{p} = c_3 n_v V_{th} + c_4 \quad . \tag{D.11}$$

As this yields $\frac{c_4}{c_3} = -n_v V_{th}$ the sensitivity becomes

$$S_v = \frac{1}{2} \frac{1}{1 - \frac{V_{DD}}{n_v V_{th}}} = -\frac{1}{2} \frac{\frac{n_v V_{th}}{V_{DD}}}{1 - \frac{n_v V_{th}}{V_{DD}}} \quad . \tag{D.12}$$

The difference between S_c and S_v explains the different increase of the sensing delay as V_{DD} is reduced. The factors n_c and n_v can be assumed to be equal, with 2.0 being a typical value. The threshold voltage V_{th} will be around 300mV. Hence, an estimation of the terms $n_c V_{th}$ and $n_v V_{th}$ results in 0.6V. As a consequence, the denominators of (D.9) and (D.12) will be identical while a significant difference is determined by the numerator. The latter remains unity for current sensing but it alters with V_{DD} for voltage sensing. With $n_v V_{th} \approx 0.6\text{V}$ the sensitivity S_v will be only 30% of S_c at $V_{DD} = 2.0\text{V}$. This agrees to Fig. D.1b where S_c and S_v are shown based on (D.9) and (D.12) for the design example of Chap. 7. If V_{DD} is reduced the absolute sensitivities increase. However, S_v will remain smaller. At $V_{DD} = 1.0\text{V}$ it can be estimated that S_v reaches 60% of S_c.

Assuming equal factors $n_c = n_v$ the difference between the sensitivities given in (D.9) and (D.12) becomes simply

$$|S_c - S_v| = \frac{1}{2} \quad . \tag{D.13}$$

This agrees well with the curves in Fig. D.1b. In consequence the current sensing delay will increase twice as much as the delay for voltage sensing if the supply voltage is reduced by the same amount. For example, if the supply voltage is reduced by half, from 2.0V to 1.0V, in Fig. 7.5 the current sensing delay rises from 166ps to 449ps. This corresponds to a delay increase by 170%. On the other hand, the voltage sensing delay increases by only 83.2% from 321ps to 588ps. However, despite the lower sensitivity, voltage sensing is still slower than current sensing.

As long as the current sensing delay is smaller than the delay of voltage sensing the larger sensitivity on V_{DD} may be tolerated in many applications. This points to an advantage of current sensing. Even though the tuning of the sensitivity S_c is limited, the desired current sensing delay can be adjusted within a wide range by means of design. Voltage sensing cannot be improved as it is defined by capacitive discharge of the bitline capacitance.

It can be concluded that the sensitivity of both sensing methods on variations of the supply voltage is characterized by just two parameters, the threshold voltage and a factor n_c or n_v, respectively. For a given technology the threshold voltage and the factor n_v are basically fixed. Only n_c can be adjusted by design since it refers to a fraction of V_{DD} generated by the voltage divider in the biasing network of the feedback amplifier (Fig. 7.2). However, in practical designs the range of n_c is limited. Therefore, the increased sensitivity of current sensing is an inherent property of the current sensing circuit caused by the feedback amplifier. It can be reduced by the use of improved feedback amplifiers at the cost of increased complexity.

E. Experimental Results: Current Sensing

Two test chips have been realized to confirm the theory covered in this book. The emphasis of this section is on the first chip with focus on current sensing. Measurements on voltage sensing from the second test chip are presented in Appendix F. Figure E.1 shows the microphotograph of the first chip, fabricated in a 0.18µm CMOS technology. The active area is 1024µm × 85µm. A 2k × 6-bit SRAM macro forms the main part. It utilizes different current sense amplifiers, i.e., Type A to C, and Type D with and without multiplexer compensation. Figure E.2 shows more details. Separate circuits (Fig. E.3) have been included for analog measurements (step response, memory cell behavior, etc.). Several experimental results have been already presented in Chaps. 5 and 6. The following figures depict additional measurements at a supply voltage of 1.8V or, if noted, at 2.0V. Figures E.4 to E.8 show the step response of the different current sensing principles which have been implemented as single ended circuits. The input (bitline) capacitance is basically determined by the capacitance of the bonding pad and package pin, which can be estimated to be approximately 2.4pF. To investigate the influence of different bitline capacitances, external discrete capacitances (below 10pF) have been added. It has to be noted that the step response is also affected by parasitics (bond wire inductance, package capacitances). These values have been taken into account during circuit simulations [37] and the results are also shown (Fig. E.4 illustrates the influence of parasitics). The sensing delay from the wordline signal to the CMOS level output of the sense amplifier is plotted in Fig. E.9 and Fig. E.10 for Type A and C, respectively. The corresponding plot for Type D is presented in Fig. 5.18. The absolute delay is affected by parasitic capacitances which cause a delay offset.

Fig. E.1. Microphotograph of the experimental 2k × 6-bit SRAM macro

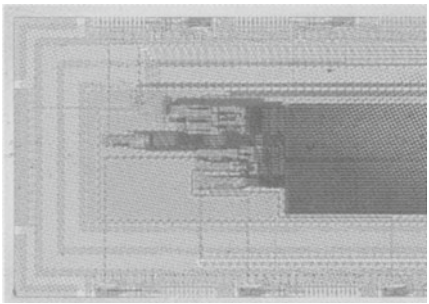

Fig. E.2. Detail photograph of the sense amplifiers on the SRAM

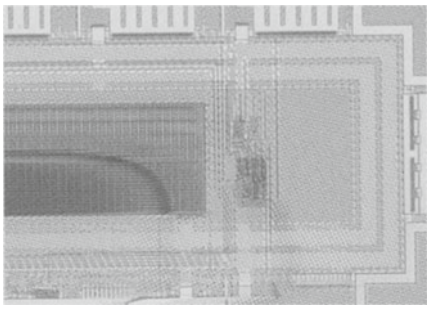

Fig. E.3. Detail photograph of the separate current sensing circuits

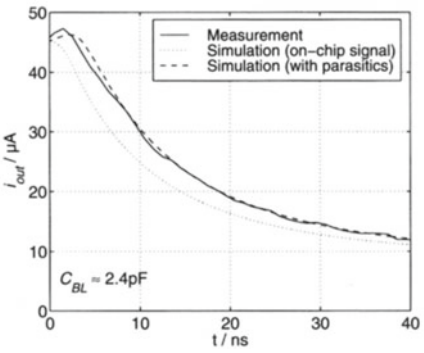

Fig. E.4. Measured and simulated step response of a Type A sensing circuit

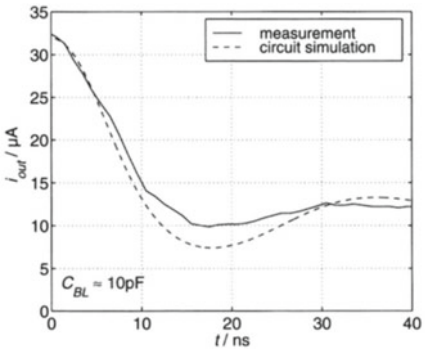

Fig. E.5. Measured and simulated step response of a Type B sensing circuit

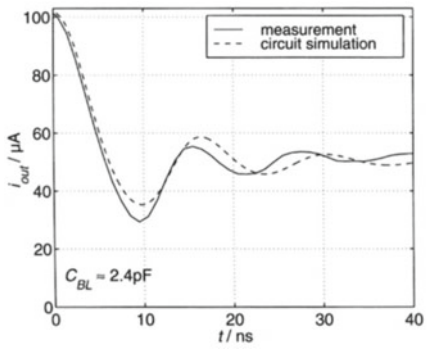

Fig. E.6. Measured and simulated step response of a Type C sensing circuit

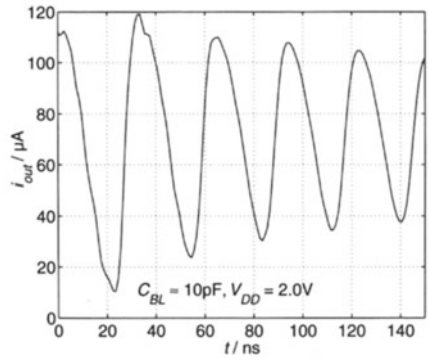

Fig. E.7. Step response of Type C operating close to a violation of the stability conditions derived in Sect. 4.4

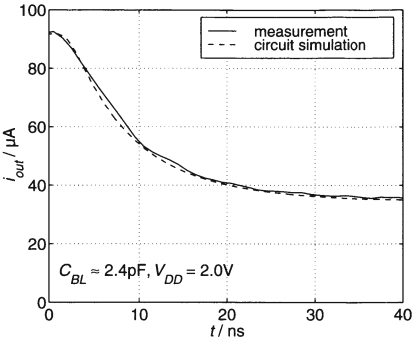

Fig. E.8. Measured and simulated step response of a Type D sensing circuit

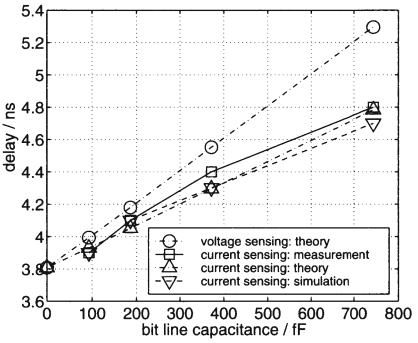

Fig. E.9. Sensing delay vs. bitline length of the SRAM macro using a Type A sense amplifier. Theoretical curves given by (4.4), (B.6) (current sensing) and (2.10) (voltage sensing) with $\Delta V_{BL} = \Delta V_{out} = 200$mV have been included. Assuming the same delay offset the theoretical delays at $C_{BL} = 0$ have been set equal

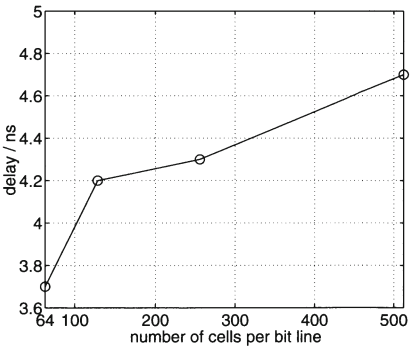

Fig. E.10. Sensing delay vs. bitline length of the SRAM macro using a Type C sense amplifier

F. Experimental Results: Voltage Sensing

The voltage sense amplifier of Fig. 7.9 has been fabricated in a 130nm CMOS technology as a part of the chip shown in Fig. 7.10. Fig. F.1 shows the measured yield versus the input voltage difference of the sense amplifier as theoretically discussed in Sect. 3.2.4 (refer to Fig. 3.10). According to (3.13), the yield is defined as the number of samples which result in a correct decision at a specified input voltage difference ΔV_{IN}. Using the error function, the curves have been fitted as described by (3.18). If V_{INDC} is reduced from 1.5V to 0.6V, the standard deviation of the sense amplifier's offset decreases from 19mV to 7mV. Consequently, the yield increases, e.g., from 70% to 94% at $\Delta V_{IN} = 10$mV. This agrees well with the theory of Chap. 3. It confirms that a lower input dc level V_{INDC} results in less offset and, hence, in increased yield. Figure F.1 indicates a better matching of the transistors and output capacitances of the sense amplifier compared to Fig. 3.10 because of higher yield at the same values of V_{INDC} and ΔV_{IN}. A mean offset different from zero was measured (caused by the test equipment, not ideally matched layout, and fabrication). This offset has been subtracted for better comparison to Fig. 3.10.

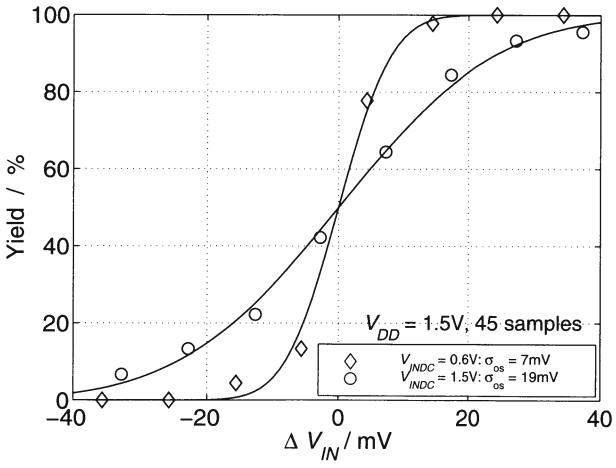

Fig. F.1. Measured yield vs. input voltage difference of the sense amplifier Fig. 7.9

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