BME2322 Logic Design Lab. Exam

1. Design a synchronous counter using JK flip flops that follows the sequence below.
    - Use the state #n given in Table 1 as your initial state where n is the last digit of your student ID (i.e., if the last digit is 3, your counter should follow 7-8-1-3-2-4-0-9-5-6 and repeat).
    - Circuit should return to the initial state if an unused state (1010-1111) occurs. Hint: Use Preset/Clear inputs.
    - Clearly show each step of your design and add comments/explanations where necessary.
    - Simulate your circuit in ORCAD and clearly show clock input and each output state on the same graph.
        - Start your simulation on an unused state.

Table 1: State Numbers

#	0	1	2	3	4	5	6	7	8	9
STATE	9	5	6	7	8	1	3	2	4	0

2. Design a non-overlapping sequence detector that detects the last digit of your student ID in binary (4-bits).
    - Use JK flip flops in your design.
    - Clearly show each step of your design and add comments/explanations where necessary.
    - Simulate your circuit in ORCAD. Set your input stream as ‘A11AA11A’ where ‘A’ ($A_3A_2A_1A_0$) is the last digit of your student ID in binary (4-bits).
    - Clearly show your input stream and your output on the same graph. Expected output is given in Table 2.

Table 2: Input Stream (top row) and Expected Output (bottom row)

A_3	A_2	A_1	A_0	1	1	A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	1	1	A_3	A_2	A_1	A_0
0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	1

Additional Notes:

You may use the same devices you used for your prelab work in OrCAD.

Compress your simulation files and your answers as a pdf file to a single zip/rar/7z file. Upload the compressed file using the form given in the announcement.