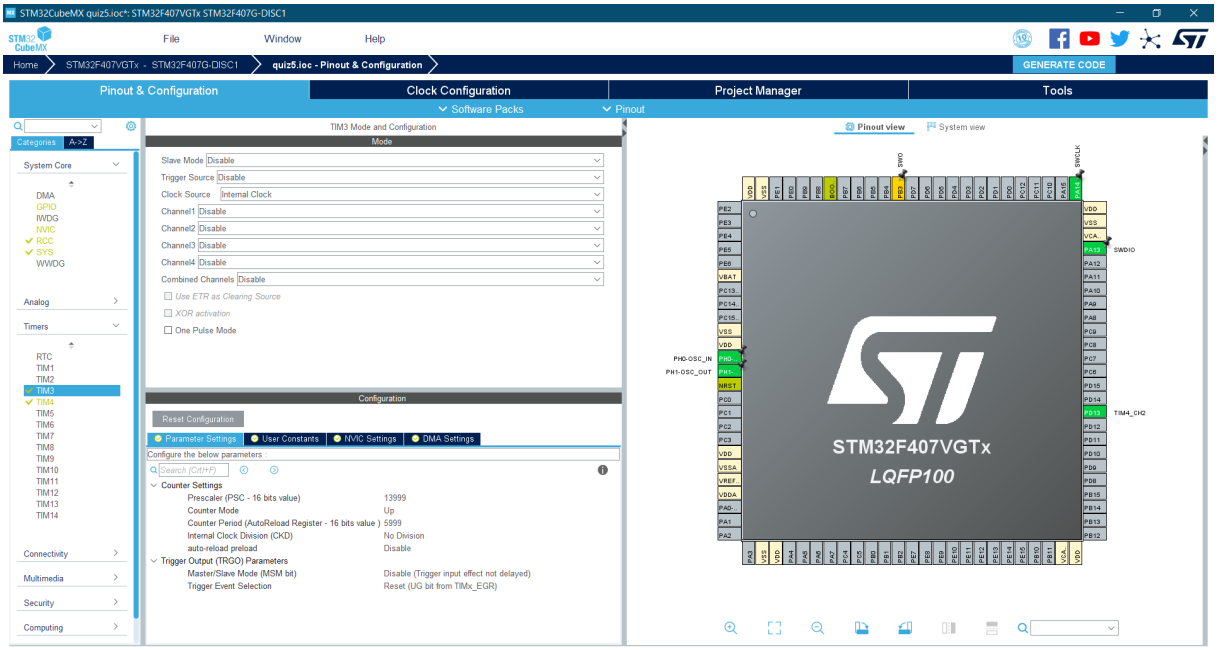
GROUP 1

TIM3:


STM32CubeMX quiz5.ioc*: STM32F407VGTx STM32F407G-DISC1
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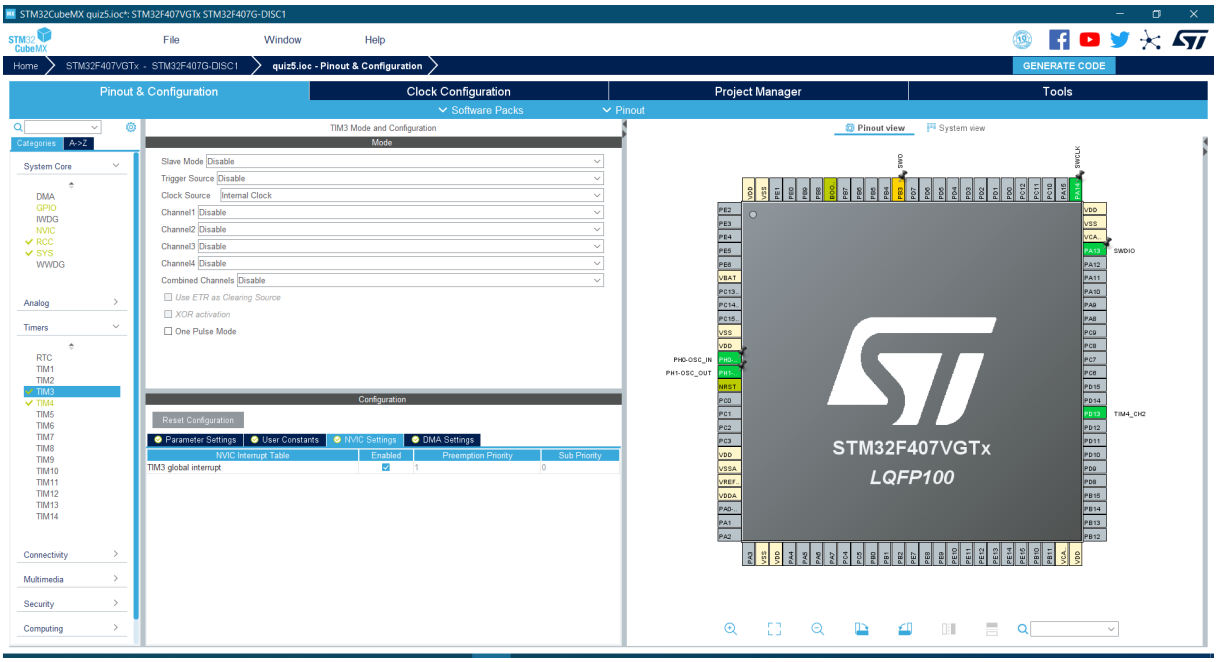
Home
STM32F407VGTx - STM32F407G-DISC1
quiz5.ioc - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
Tools
Software Packs
Pinout
TIM3 Mode and Configuration
Mode
Slave Mode Disable
Trigger Source Disable
Clock Source Internal Clock
Channel1 Disable
Channel2 Disable
Channel3 Disable
Channel4 Disable
Combined Channels Disable
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
Configure the below parameters :
Counter Settings
Prescaler (PSC - 16 bits value) 13999
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 5999
Internal Clock Division (CKD) No Division
auto-reload preload Disable
Trigger Output (TRGO) Parameters
Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection Reset (UG bit from TIMx_EGR)
Pinout view
System view
STM32F407VGTx
LQFP100


STM32CubeMX quiz5.ioc*: STM32F407VGTx STM32F407G-DISC1
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quiz5.ioc - Pinout & Configuration
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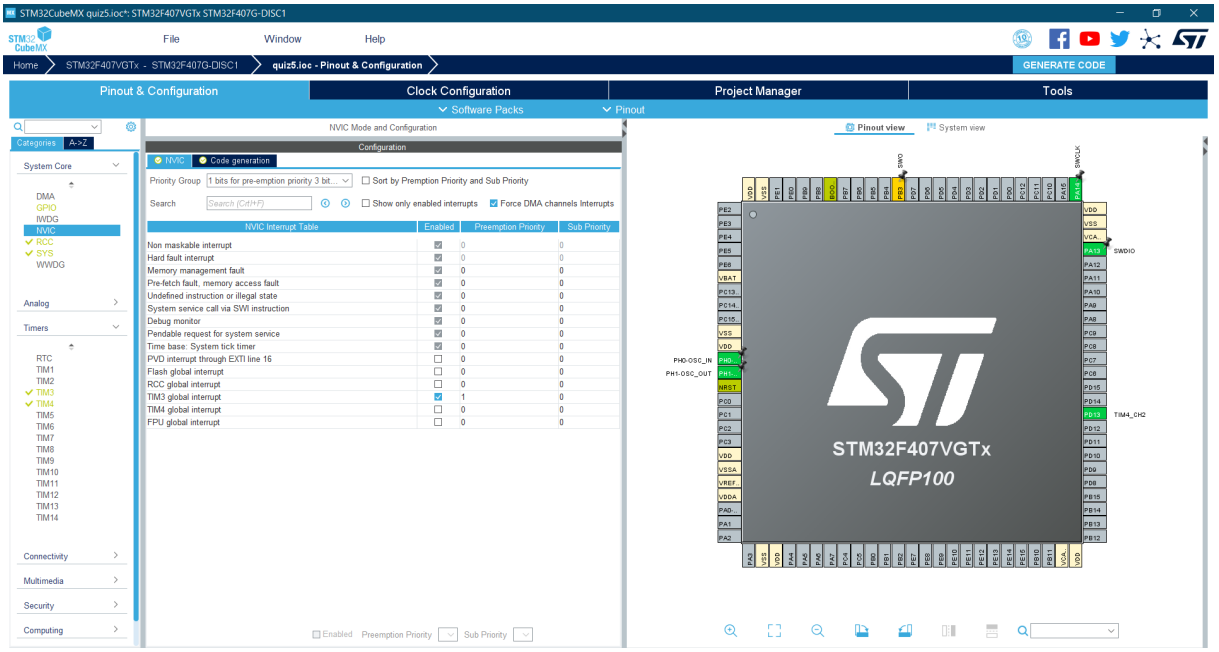
Pinout
TIM3 Mode and Configuration
Mode
Slave Mode Disable
Trigger Source Disable
Clock Source Internal Clock
Channel1 Disable
Channel2 Disable
Channel3 Disable
Channel4 Disable
Combined Channels Disable
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
NVIC Interrupt Table
Enabled
Preemption Priority
Sub Priority
TIM3 global interrupt
Pinout view
System view
STM32F407VGTx
LQFP100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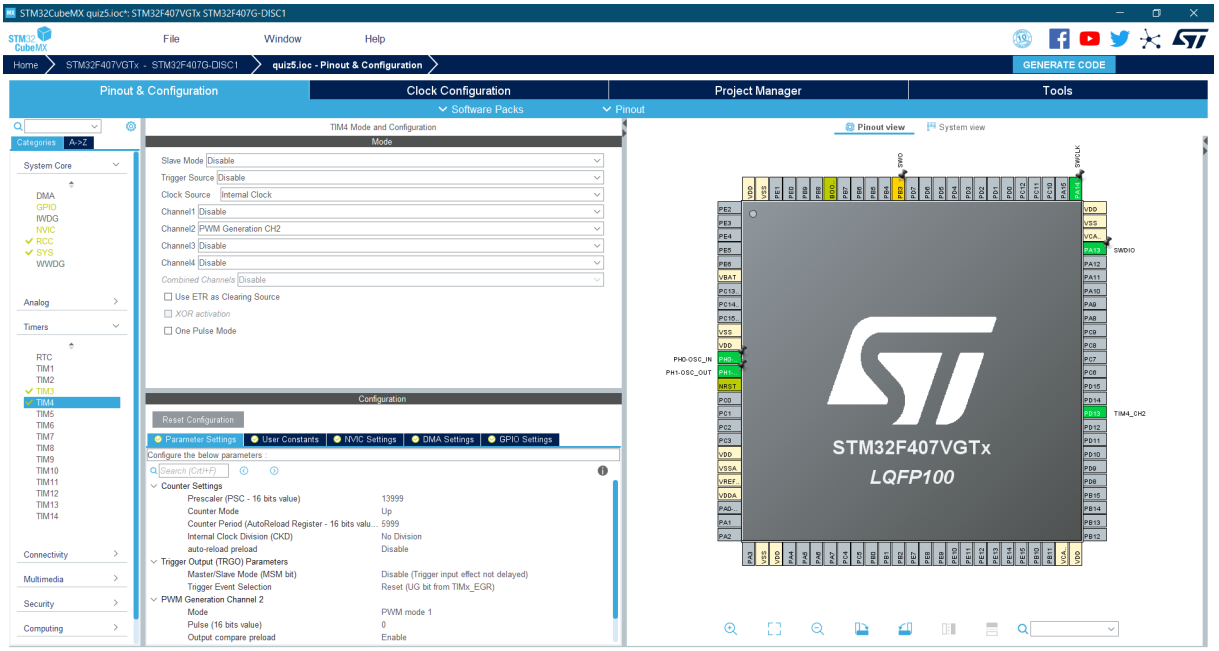
quiz5.ioc - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
Tools
Software Packs
Pinout
NVIC Mode and Configuration
Configuration
NVIC
Code generation
Priority Group
1 bits for pre-emption priority 3 bit...
Sort by Premption Priority and Sub Priority
Search
Search (Ctrl+F)
Show only enabled interrupts
Force DMA channels Interrupts
NVIC Interrupt Table
Enabled
Preemption Priority
Sub Priority
Non maskable interrupt
Hard fault interrupt
Memory management fault
Pre-fetch fault, memory access fault
Undefined instruction or illegal state
System service call via SWI instruction
Debug monitor
Pendable request for system service
Time base: System tick timer
PVD interrupt through EXTI line 16
Flash global interrupt
RCC global interrupt
TIM3 global interrupt
TIM4 global interrupt
FPU global interrupt
Categories
A->Z
System Core
DMA
GPIO
IWDG
NVIC
RCC
SYS
WWDG
Analog
Timers
RTC
TIM1
TIM2
TIM3
TIM4
TIM5
TIM6
TIM7
TIM8
TIM9
TIM10
TIM11
TIM12
TIM13
TIM14
Connectivity
Multimedia
Security
Computing
Pinout view
System view
STM32F407VGTx
LQFP100
SWDIO
SWCLK
TIM4_CH2

TIM 4:


STM32CubeMX quiz5.ioc*: STM32F407VGTx STM32F407G-DISC1
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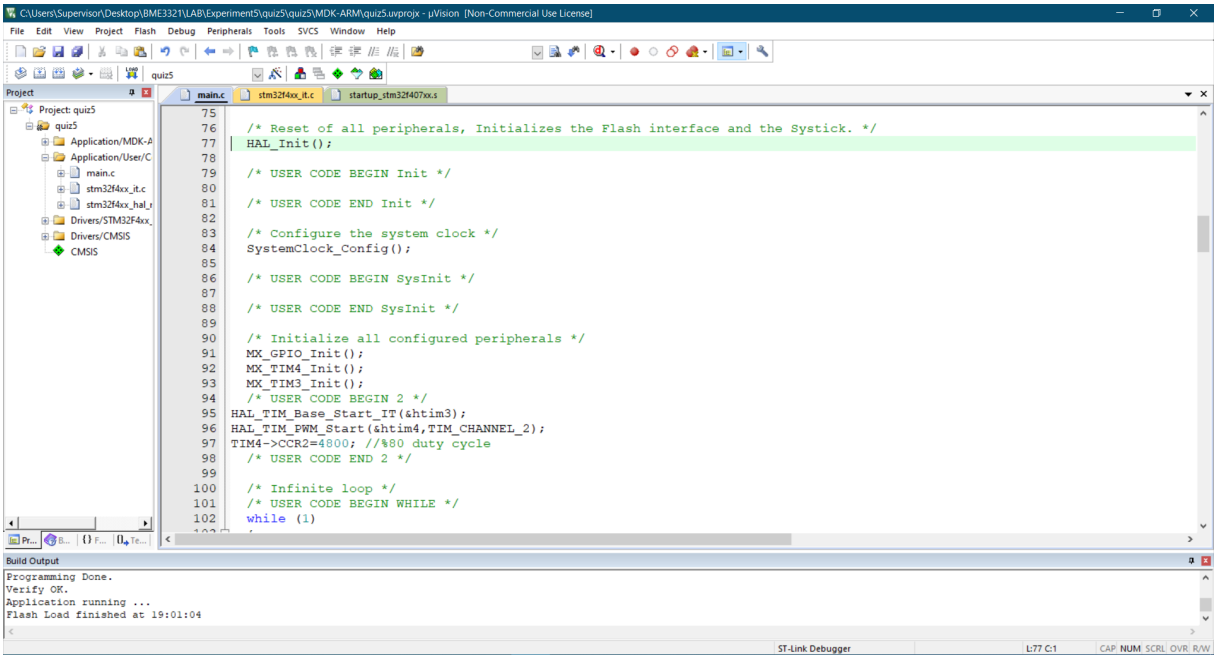
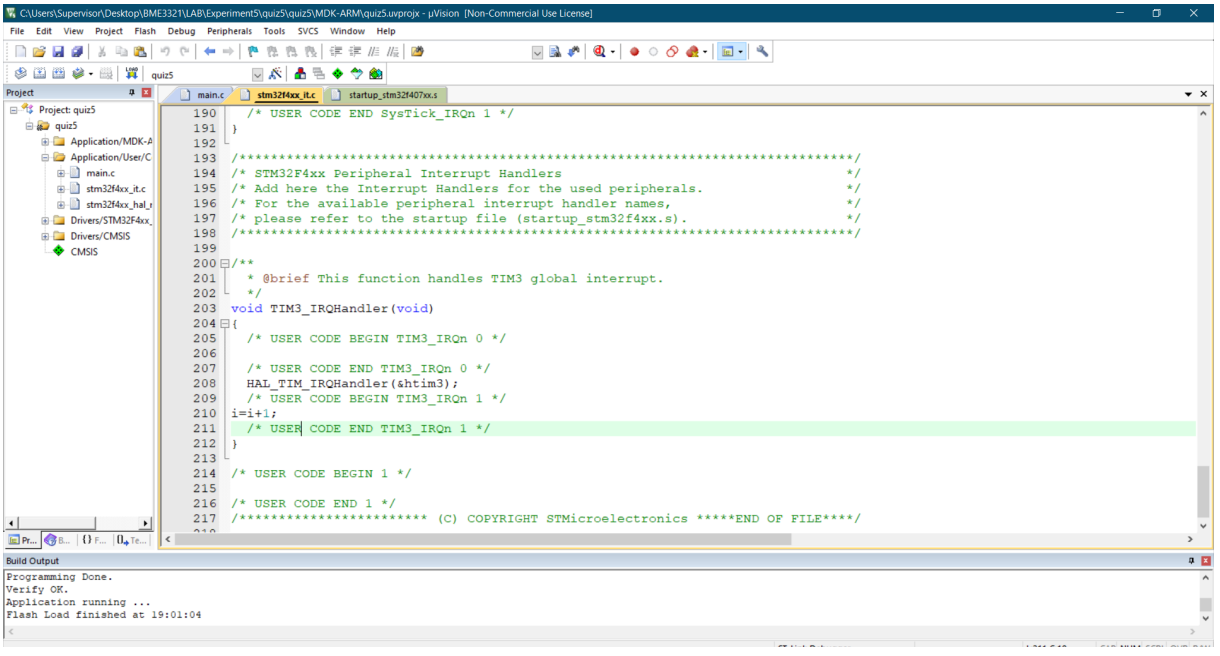
STM32F407VGTx - STM32F407G-DISC1
quiz5.ioc - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
Tools
Software Packs
Pinout
TIM4 Mode and Configuration
Mode
Slave Mode
Disable
Trigger Source
Disable
Clock Source
Internal Clock
Channel1
Disable
Channel2
PWM Generation CH2
Channel3
Disable
Channel4
Disable
Combined Channels
Disable
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
Configure the below parameters :
Search (Ctrl+F)
Counter Settings
Prescaler (PSC - 16 bits value)
13999
Counter Mode
Up
Counter Period (AutoReload Register - 16 bits valu...
5999
Internal Clock Division (CKD)
No Division
auto-reload preload
Disable
Trigger Output (TRGO) Parameters
Master/Slave Mode (MSM bit)
Disable (Trigger input effect not delayed)
Trigger Event Selection
Reset (UG bit from TIMx_EGR)
PWM Generation Channel 2
Mode
PWM mode 1
Pulse (16 bits value)
0
Output compare preload
Enable
Pinout view
System view
STM32F407VGTx
LQFP100
SWDIO
SWCLK
TIM4_CH2

Main.c :

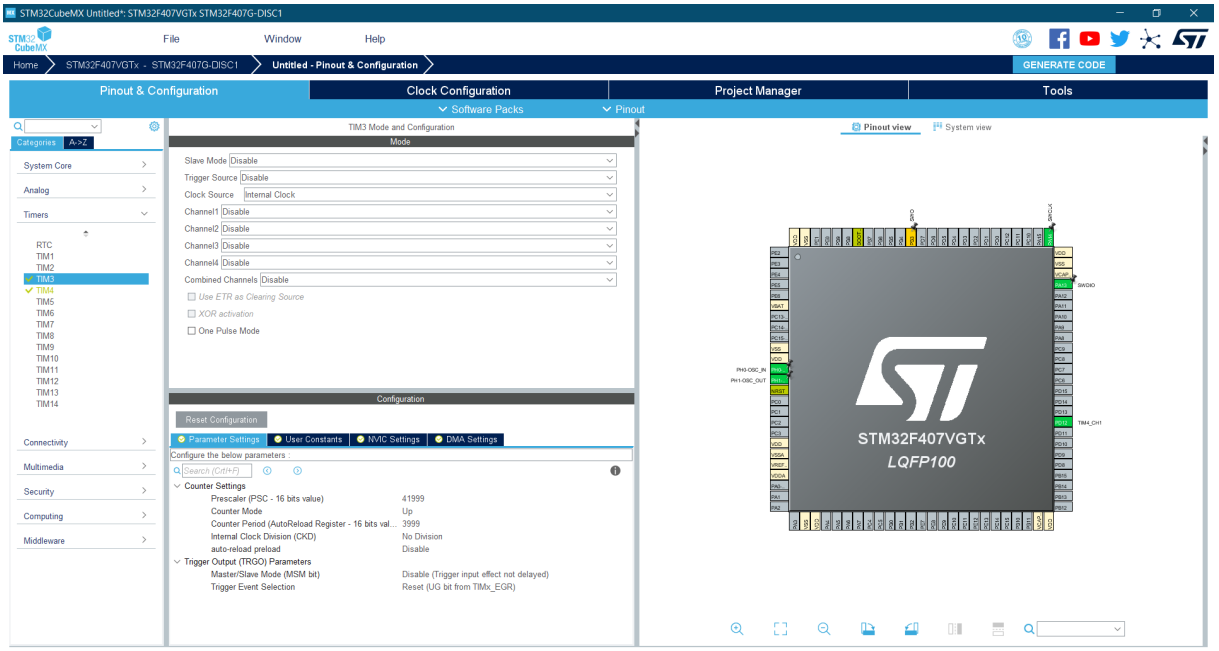


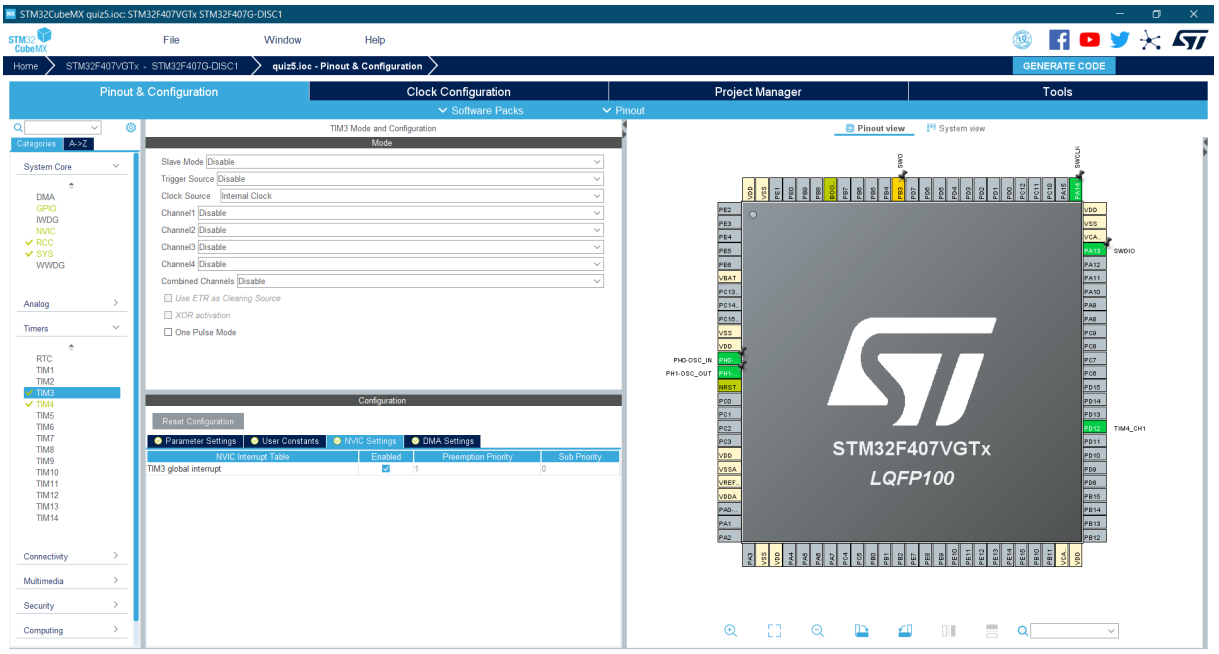
IRQHandler:



GROUP 2

TIM3:


STM32CubeMX Untitled*: STM32F407VGTx STM32F407G-DISC1
File
Window
Help
Home
STM32F407VGTx - STM32F407G-DISC1
Untitled - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
Tools
Software Packs
Pinout
TIM3 Mode and Configuration
Mode
Slave Mode Disable
Trigger Source Disable
Clock Source Internal Clock
Channel1 Disable
Channel2 Disable
Channel3 Disable
Channel4 Disable
Combined Channels Disable
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
Configure the below parameters :
Counter Settings
Prescaler (PSC - 16 bits value) 41999
Counter Mode Up
Counter Period (AutoReload Register - 16 bits val... 3999
Internal Clock Division (CKD) No Division
auto-reload preload Disable
Trigger Output (TRGO) Parameters
Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection Reset (UG bit from TIMx_EGR)
Pinout view
System view
STM32F407VGTx
LQFP100


STM32CubeMX quiz5.ioc: STM32F407VGTx STM32F407G-DISC1
File
Window
Help
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STM32F407VGTx - STM32F407G-DISC1
quiz5.ioc - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
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Pinout
TIM3 Mode and Configuration
Mode
Slave Mode Disable
Trigger Source Disable
Clock Source Internal Clock
Channel1 Disable
Channel2 Disable
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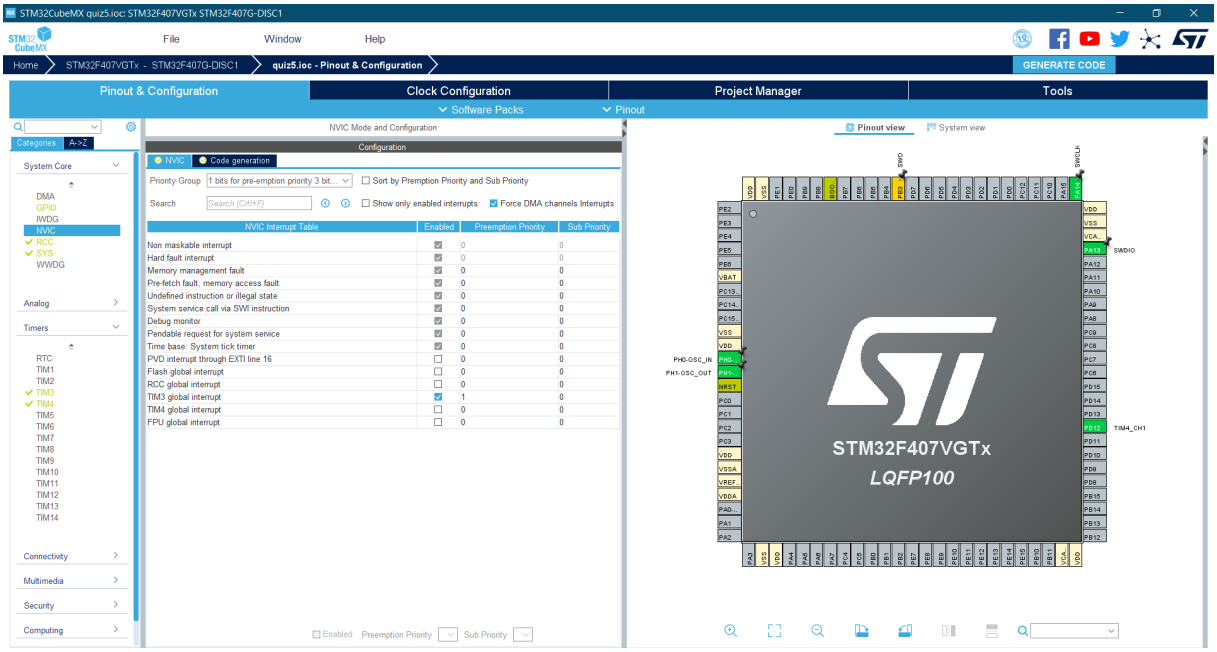
Channel4 Disable
Combined Channels Disable
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
NVIC Interrupt Table
Enabled
Preemption Priority
Sub Priority
TIM3 global interrupt
Pinout view
System view
STM32F407VGTx
LQFP100


STM32CubeMX quiz5.ioc: STM32F407VGTx STM32F407G-DISC1
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STM32F407VGTx - STM32F407G-DISC1
quiz5.ioc - Pinout & Configuration
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Code generation
Priority Group
1 bits for pre-emption priority 3 bit...
Sort by Premption Priority and Sub Priority
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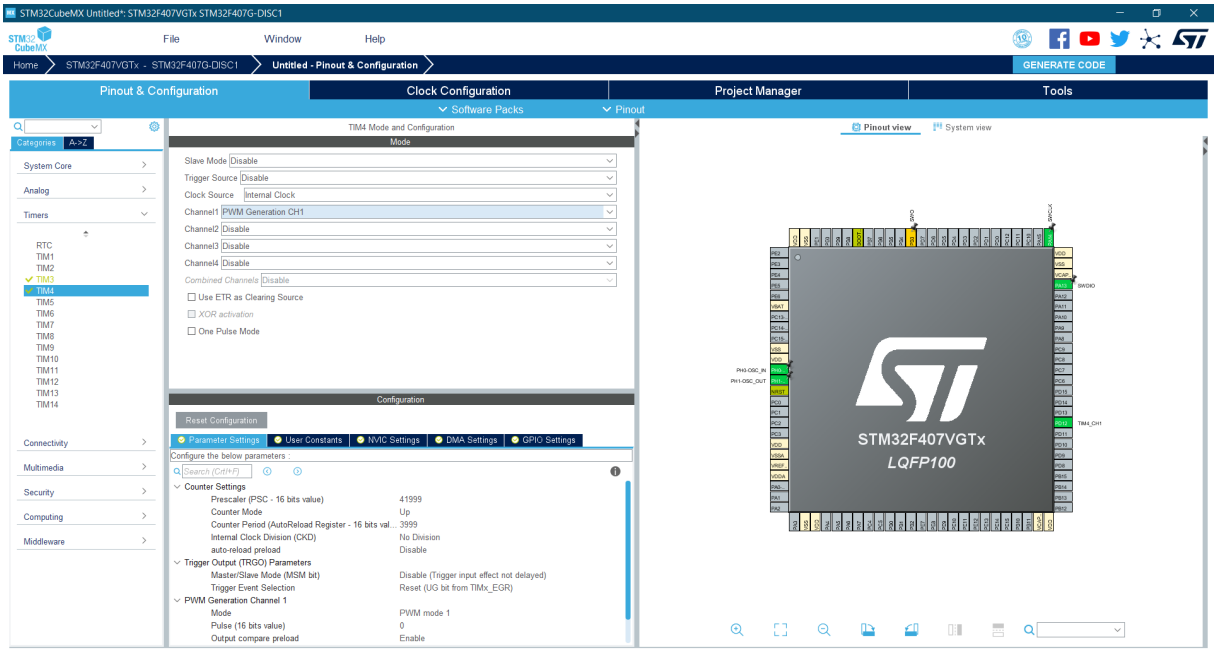
Debug monitor
Pendable request for system service
Time base: System tick timer
PVD interrupt through EXTI line 16
Flash global interrupt
RCC global interrupt
TIM3 global interrupt
TIM4 global interrupt
FPU global interrupt
Pinout view
System view
STM32F407VGTx
LQFP100
SWDIO
TIM4_CH1

TIM4:


STM32CubeMX Untitled*: STM32F407VGTx STM32F407G-DISC1
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Window
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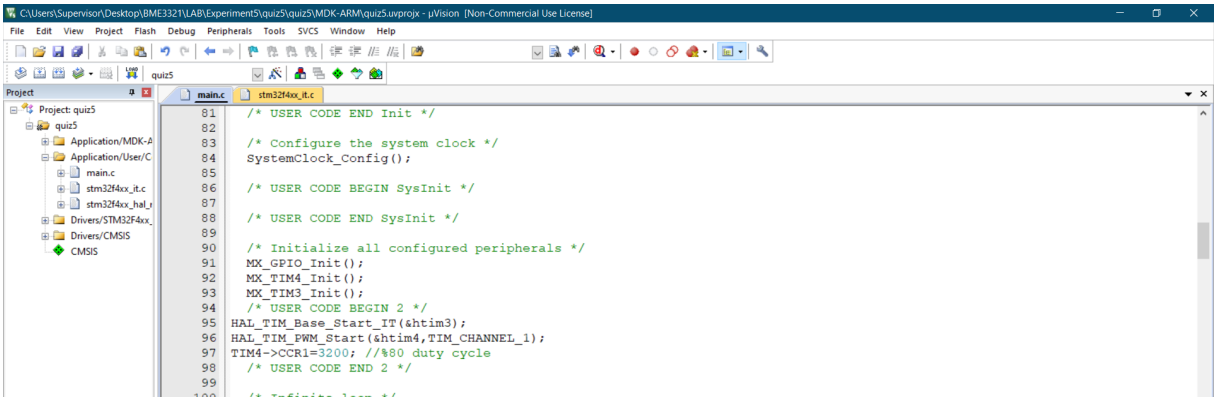
Untitled - Pinout & Configuration
GENERATE CODE
Pinout & Configuration
Clock Configuration
Project Manager
Tools
Software Packs
Pinout
TIM4 Mode and Configuration
Mode
Slave Mode
Disable
Trigger Source
Clock Source
Internal Clock
Channel1
PWM Generation CH1
Channel2
Channel3
Channel4
Combined Channels
Use ETR as Clearing Source
XOR activation
One Pulse Mode
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
Configure the below parameters :
Counter Settings
Prescaler (PSC - 16 bits value)
41999
Counter Mode
Up
Counter Period (AutoReload Register - 16 bits val...
3999
Internal Clock Division (CKD)
No Division
auto-reload preload
Disable
Trigger Output (TRGO) Parameters
Master/Slave Mode (MSM bit)
Disable (Trigger input effect not delayed)
Trigger Event Selection
Reset (UG bit from TIMx_EGR)
PWM Generation Channel 1
Mode
PWM mode 1
Pulse (16 bits value)
0
Output compare preload
Enable
Pinout view
System view
STM32F407VGTx
LQFP100
SWDIO
TIM4_CH1

Main.c :



IRQHandler :