EXPERIMENT 4: Adder, Subtractor, Multiplexer, and Demultiplexer Applications

Objectives

The objectives of Experiment 4 are

- to learn full adder applications of multiplexer and demultiplexer
- to learn adder/subtractor circuit design using 74283 IC.

Components Required:

- 7404 Inverter,
- 74LS138 Decoder/Demultiplexer,
- 74LS153 Mux,
- 7486 2-input XOR gate,
- 74283 IC 4bit binary adder,
- DIP switches, LEDs, and resistors.

Preliminary Work:

1. Study multiplexer, demultiplexer, adder, and subtractor in your class notes.
2. Design a full adder circuit using multiplexer. Show Boolean expressions and block diagram of the circuit in your report. Simulate your circuit in Pspice and show that it functions properly.
3. Design a full adder circuit using demultiplexer. Show Boolean expressions and block diagram of the circuit in your report. Simulate your circuit in Pspice and show that it functions properly.
4. Draw the block diagram of the 4-bit adder/subtractor circuit and explain how it works. Simulate the circuit given in experimental part and fill the Table 2. Add simulation results to your report for each row in the table.
   (Pay attention to the simulation notes given in the first experiment sheet)

Experimental Work:

1. Implement the 1-bit full adder circuit which you designed using 74LS138 Demultiplexer in preliminary work and verify the truth table given in Table 1.
2. Implement the 1-bit full adder circuit which you designed using 74LS153 Multiplexer in preliminary work and verify the truth table given in Table 1.
3. Implement the circuit given in Figure 1 on your breadboard. Connect inputs to switches, outputs to LEDs, and make sure that +5V and ground connections are done for all ICs. Fill the Table 2.

Table 1. Truth Table of 1-Bit Full Adder

INPUTS			OUTPUTS	
A	B	C_{in}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

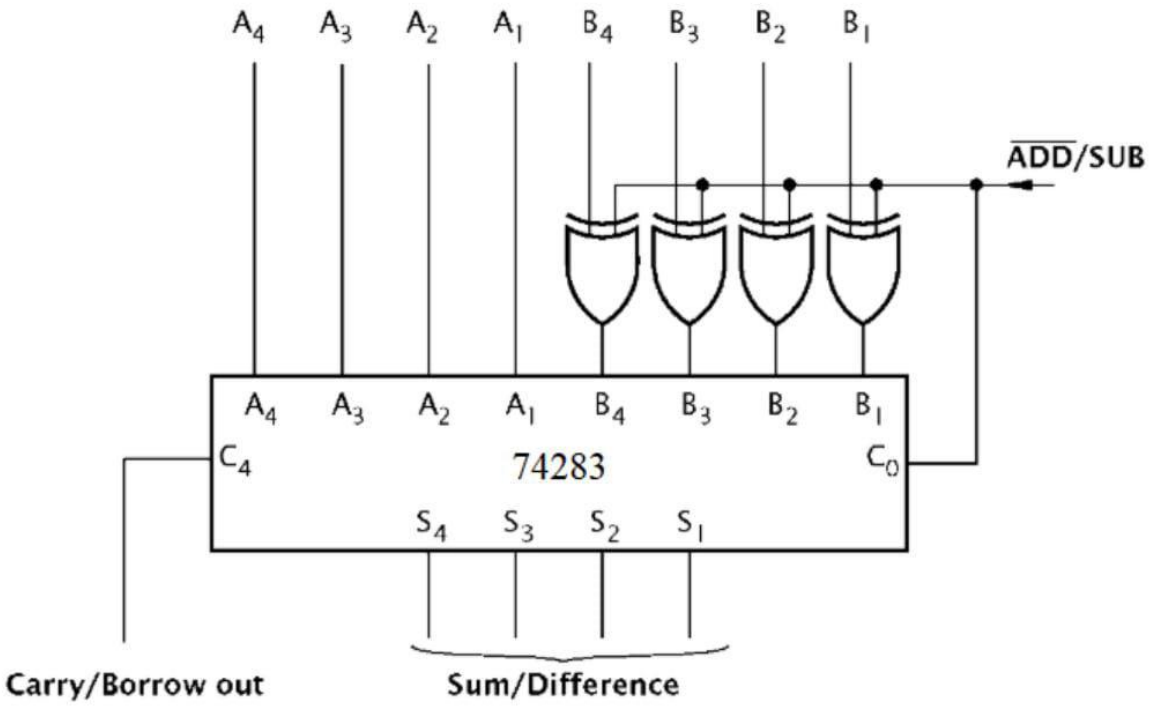

Figure 1

Table 2. Result Table of Adder/Subtractor Circuit

$\overline{A}/S$	A	B	$A_3A_2A_1A_0$	$B_3B_2B_1B_0$	C_4	$S_3S_2S_1S_0$
0	8	7				
0	11	12				
0	3	4				
1	1	5				
1	6	6				
1	14	9				