BME2322 – Logic Design

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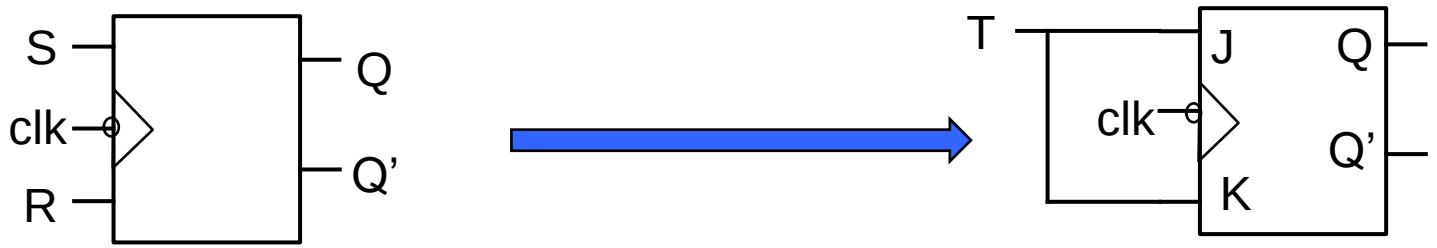
LECTURE 11

Flip-Flop Conversion

- Steps:
  - Identify the avaliable and required flip-flop.
  - Write the characteristic table for required flip-flop.
  - Write the excitation table for avaliable flip-flop.
  - Writye the Boolean expression for valiable flip-flop.
  - Draw the circuit.



JK to D flip-flop conversion

1. Available flip-flop is JK and the required flip-flop is D type.
2. Characteristic table of D flip-flop

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	D	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

3. Excitation table of JK flip-flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

4. Boolean Expression

Q_n \ D	0	1
0	0	1
1	X	X

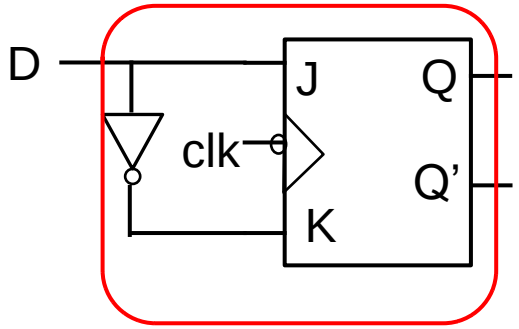
J = D

Q_n \ D	0	1
0	X	X
1	1	0

K = D’

JK to D flip-flop conversion cont.

5. Draw the circuit



T flip-flop to D flip-flop conversion

1. Available flip-flop is T and the required flip-flop is D type.
2. Characteristic table of D flip-flop

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	D	Q_{n+1}	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

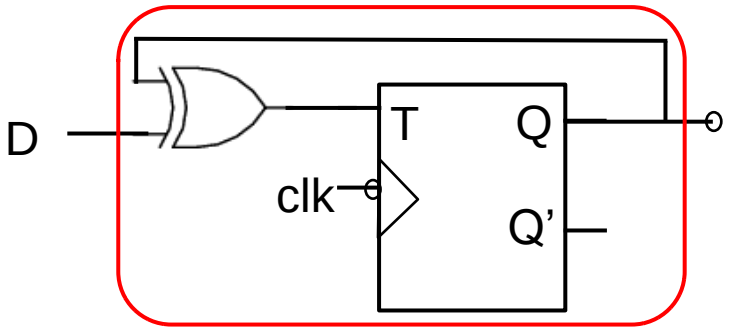
3. Excitation table of T flip-flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

4. Boolean Expression

$$T = D \oplus Q_n$$

5. Circuit Diagram



SR flip-flop to JK flip-flop conversion

1. Available flip-flop is SR and the required flip-flop is JK type.
2. Characteristic table of JK flip-flop

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

3. Excitation table of SR flip-flop

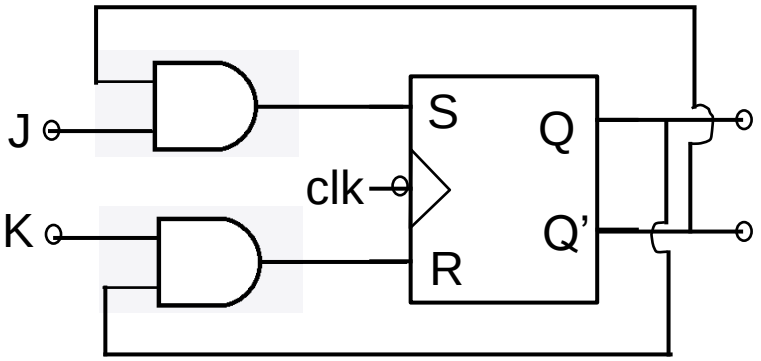
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

SR flip-flop to JK flip-flop conversion cont.

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

5. Circuit Diagram



4. Boolean Expression

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	X	0	0	X

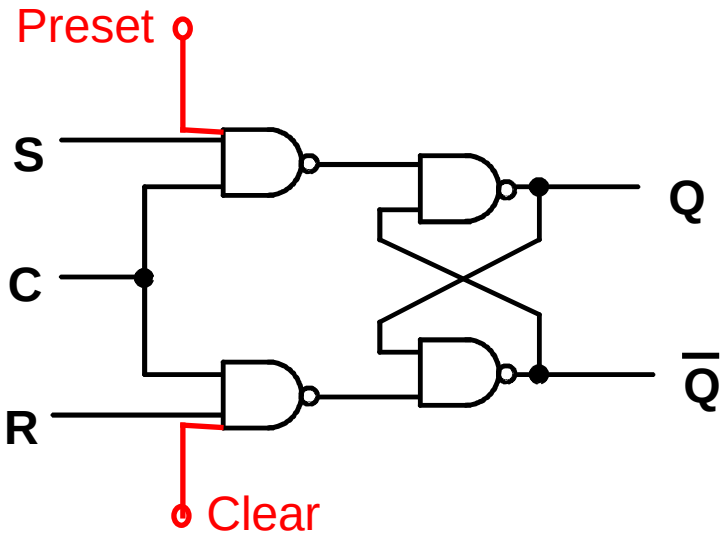
$$S = \overline{Q_n} J$$

Q_n \ JK	00	01	11	10
0	X	X	0	0
1	0	1	1	0

$$R = Q_n K$$

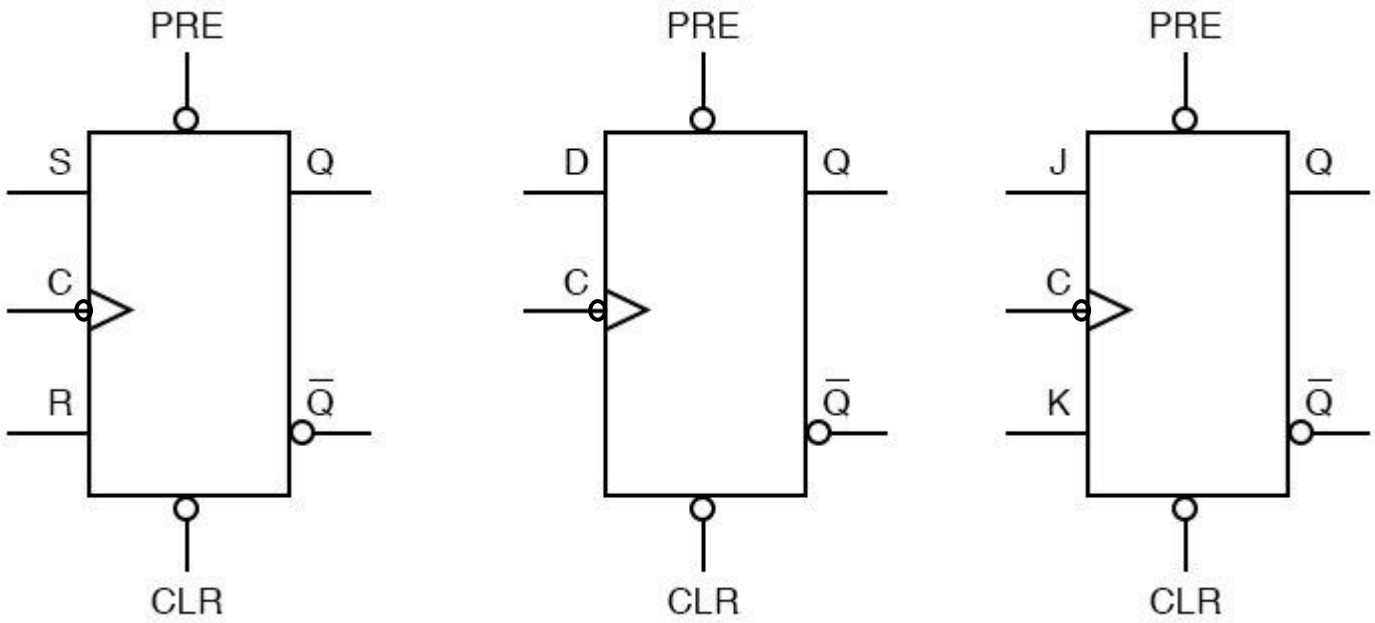
Preset and Clear inputs

- The normal data inputs to a flip flop (D, S and R, or J and K) are referred to as synchronous inputs because they have an effect on the outputs (Q and not-Q) only in step, or in sync, with the clock signal transitions.
- The 'Preset' and 'Clear' are the direct inputs or overriding inputs or asynchronous inputs.
  - Preset = 0 ➔ $Q_n = 1$
  - Clear = 0 ➔ $Q_n = 0$
- Whatever be the value of clock and synchronous inputs, 'preset' and 'clear' changes Q_n.
- They can be used in the design of counters.

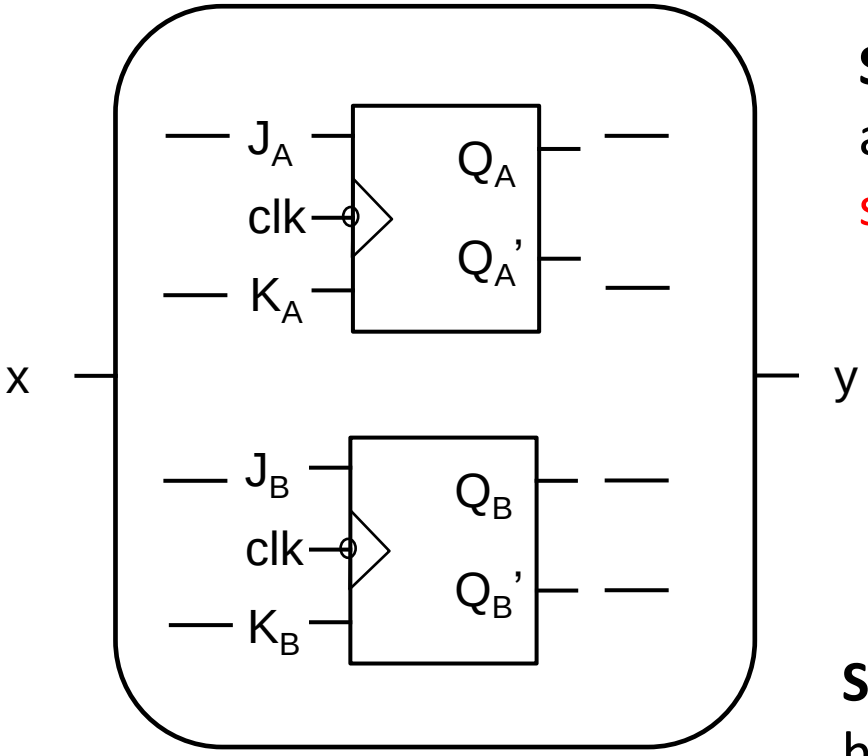


preset	clear	Qn
0	0	Not Used
0	1	1
1	0	0
1	1	perform normally

Preset and Clear inputs cont



Introduction to State Diagrams



A sequential circuit

State Table is the table which tells us about the relation between the present state, next state and the output.

Present State		Input	Next State		Output
Q_A	Q_B	x	Q^+_A	Q^+_B	y
0	0	1	1	0	1

A random case

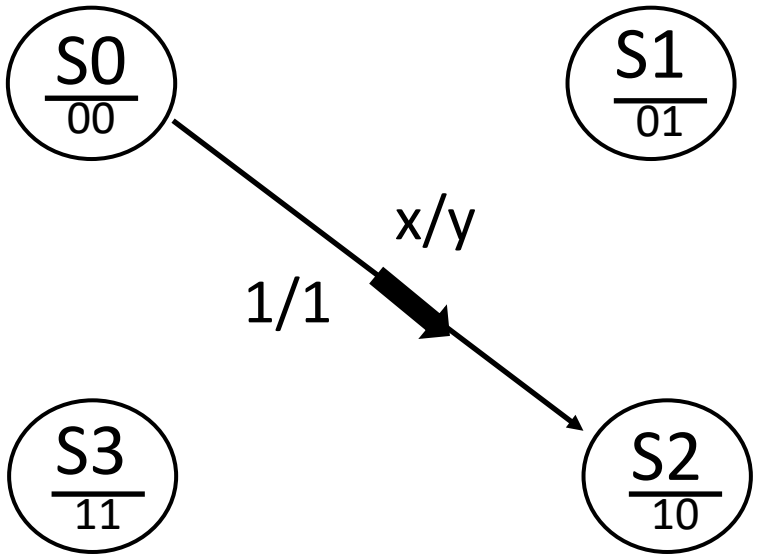
State Diagram : 2 flip-flops, so we will have $2^2 = 4$ states.

	Q_A	Q_B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

Introduction to State Diagrams cont.

	Q_A	Q_B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

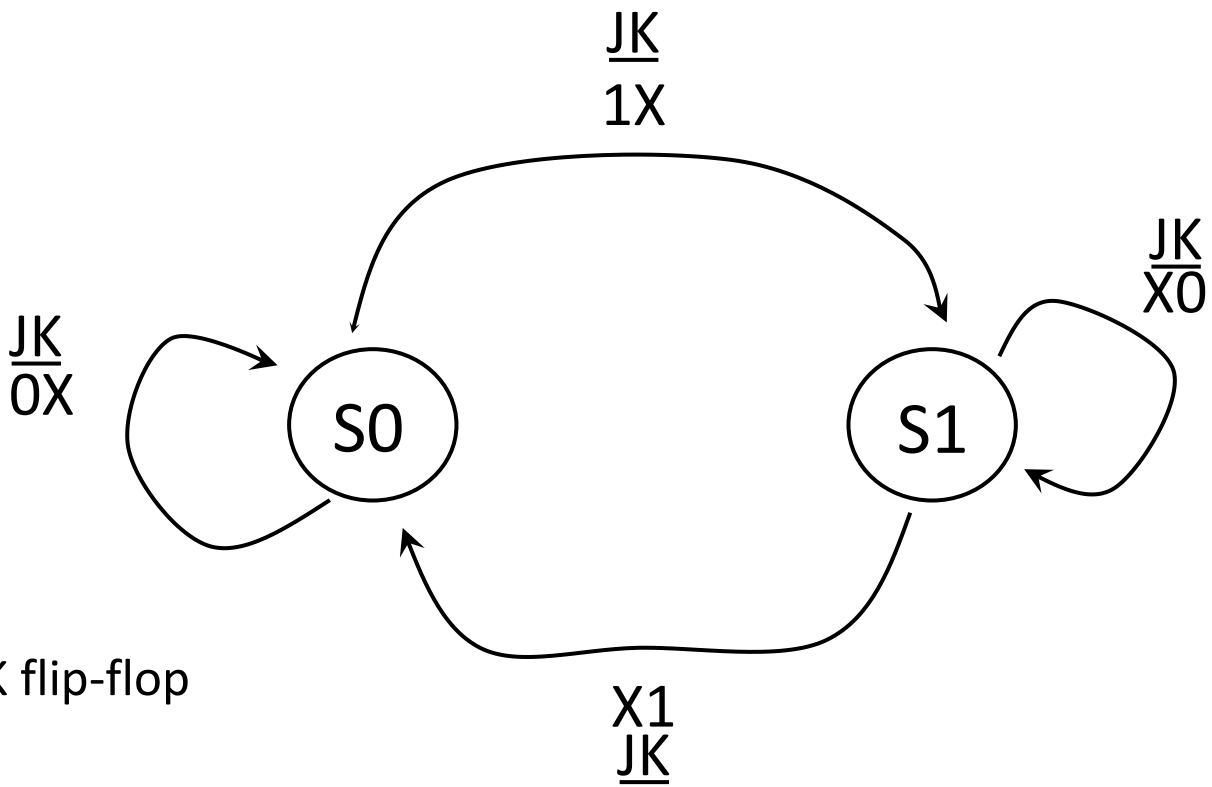
Present State		Input	Next State		Output
Q_A	Q_B	x	Q^+_A	Q^+_B	y
0	0	1	1	0	1



State diagram of JK flip-flop

P.S	Inputs		N.S
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

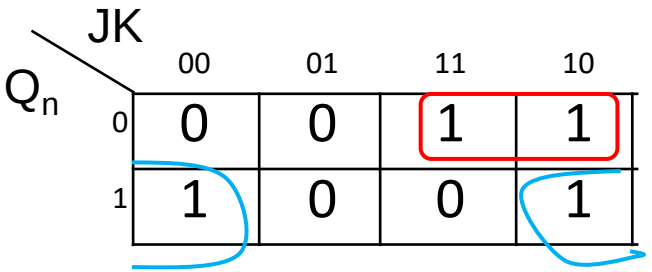
- We have two possible states;
  - S0 = 0
  - S1 = 1



State diagram of JK flip-flop

State equation of JK flip-flop

P.S	Inputs		N.S
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



$Q_{n+1}=Q_n.K'+(Q_n)'.J$

State equation

- State Equation ➔ left hand side = right hand side

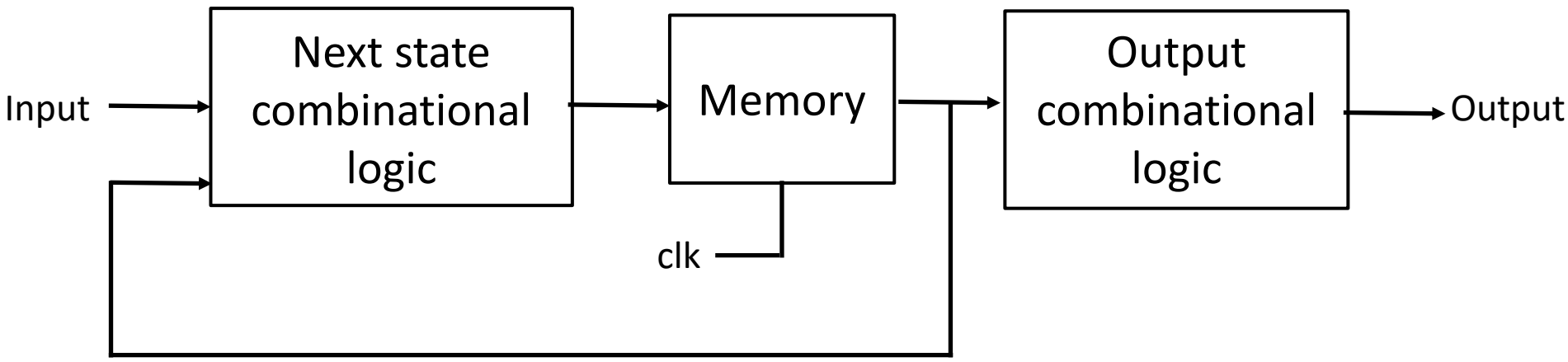
Next State

Combination of the present state and input

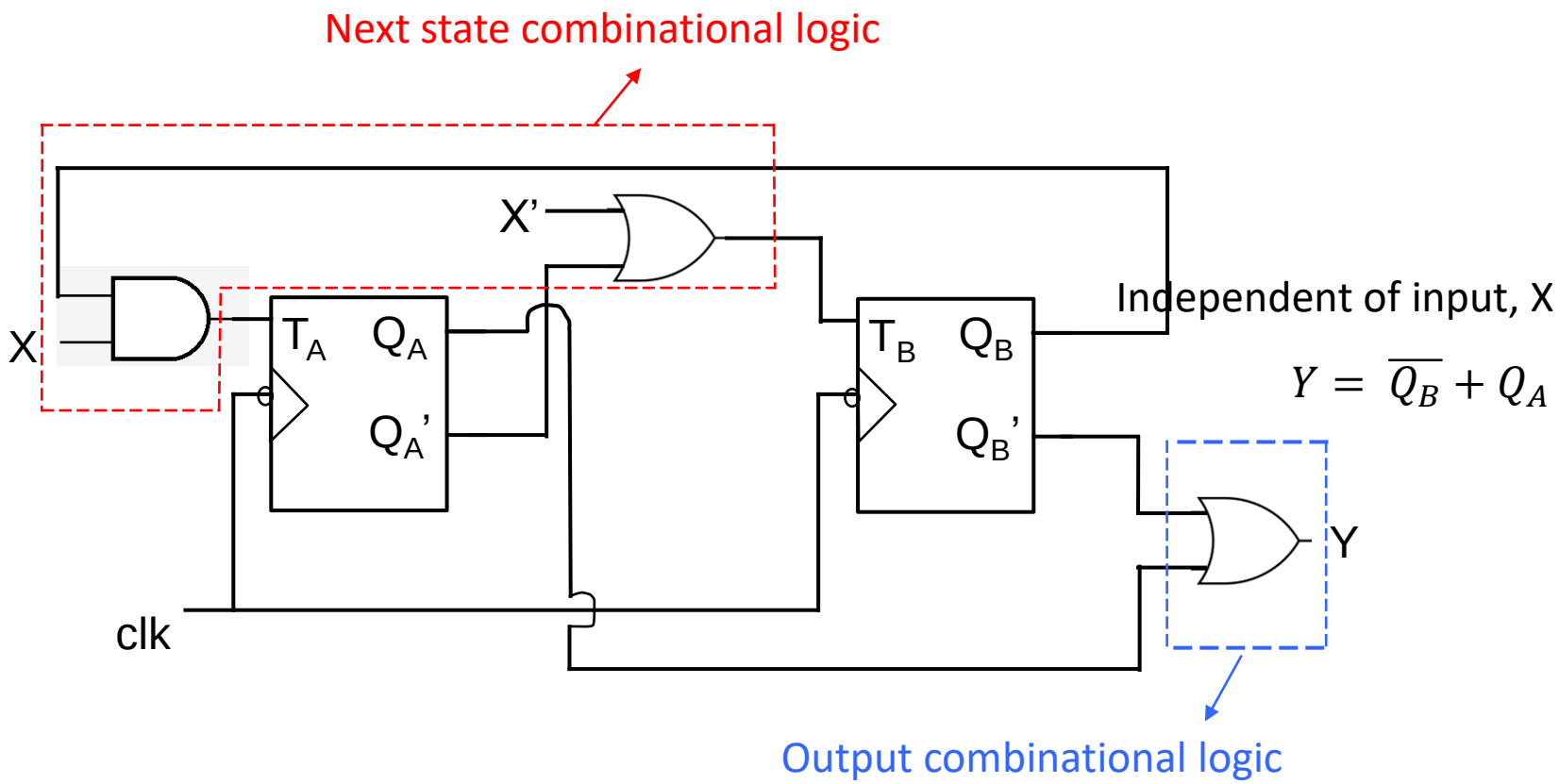
Sequential Circuit Analysis

- The output of a sequential circuit can be expressed in two different ways:
  - Moore model: Outputs= f(present state)
  - Mealy model: Outputs: f(present state, inputs)

Moore machine:

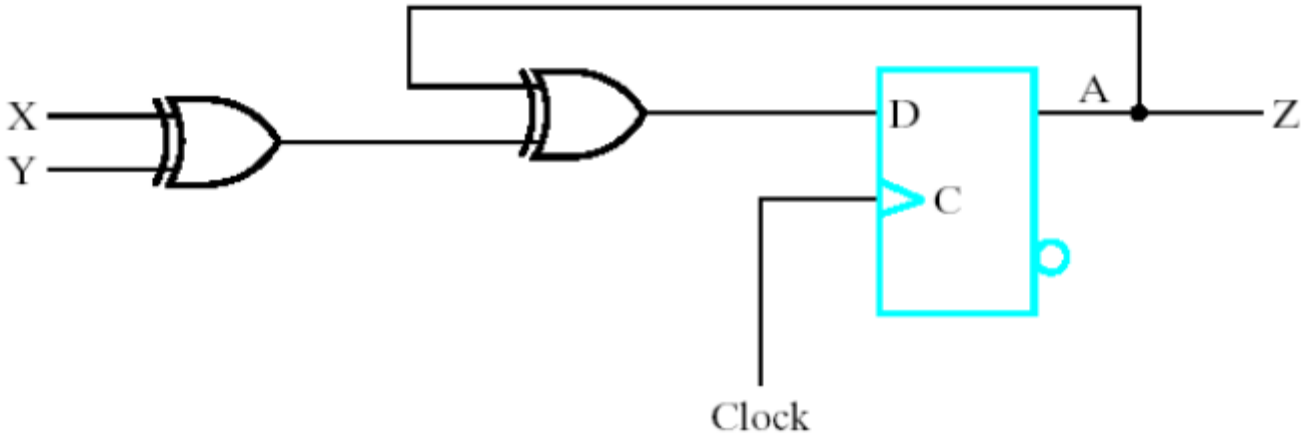


Example 1



The circuit is a Moore Machine

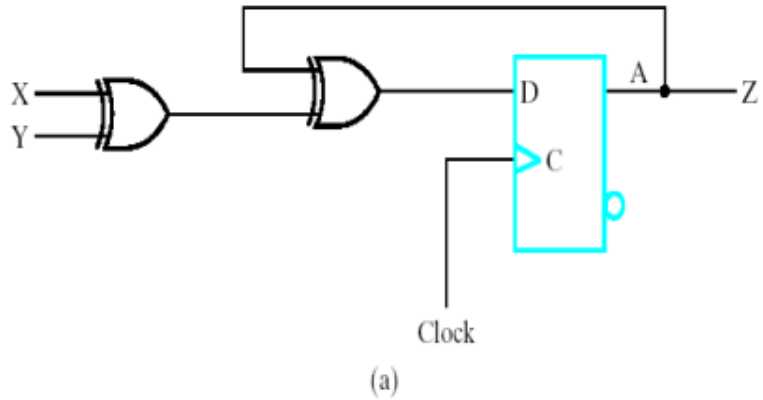
Example 2 (Moore)



(a)

- Two inputs: X and Y; One output: Z
- One state: A
- Note that Z= A, just a function of the current state

Example 2 (Moore) cont.



(a)

Present state	Inputs		Next state	Output
A	X	Y	A	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

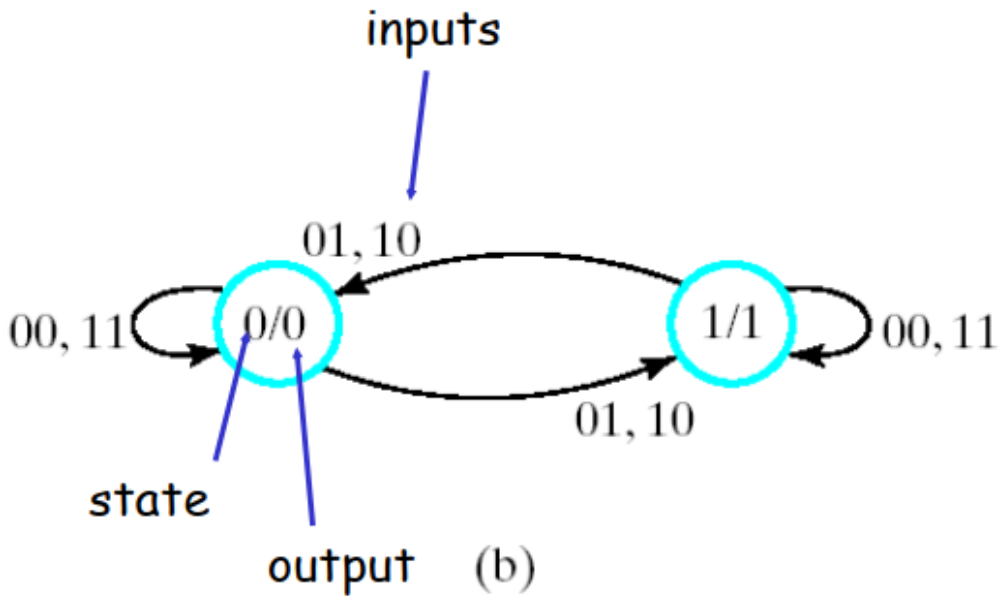
(b) State table

Present State A	Next State Inputs XY 00	01	10	11	Output Z
0	0	1	1	0	0
1	1	0	0	1	1

Example 2 (Moore) cont.

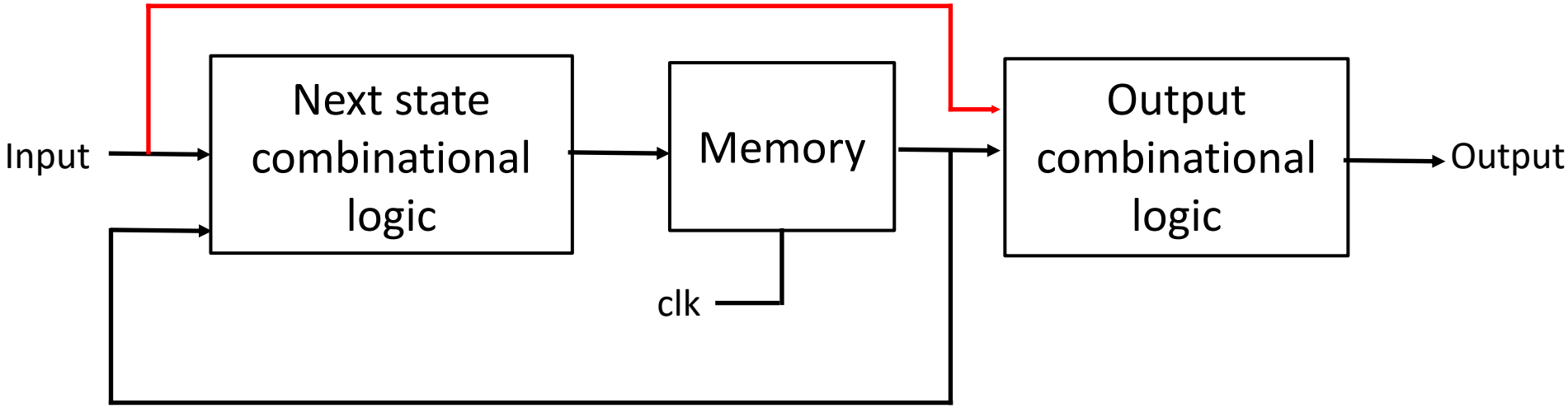
Present state	Inputs		Next state	Output
A	X	Y	A	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b) State table

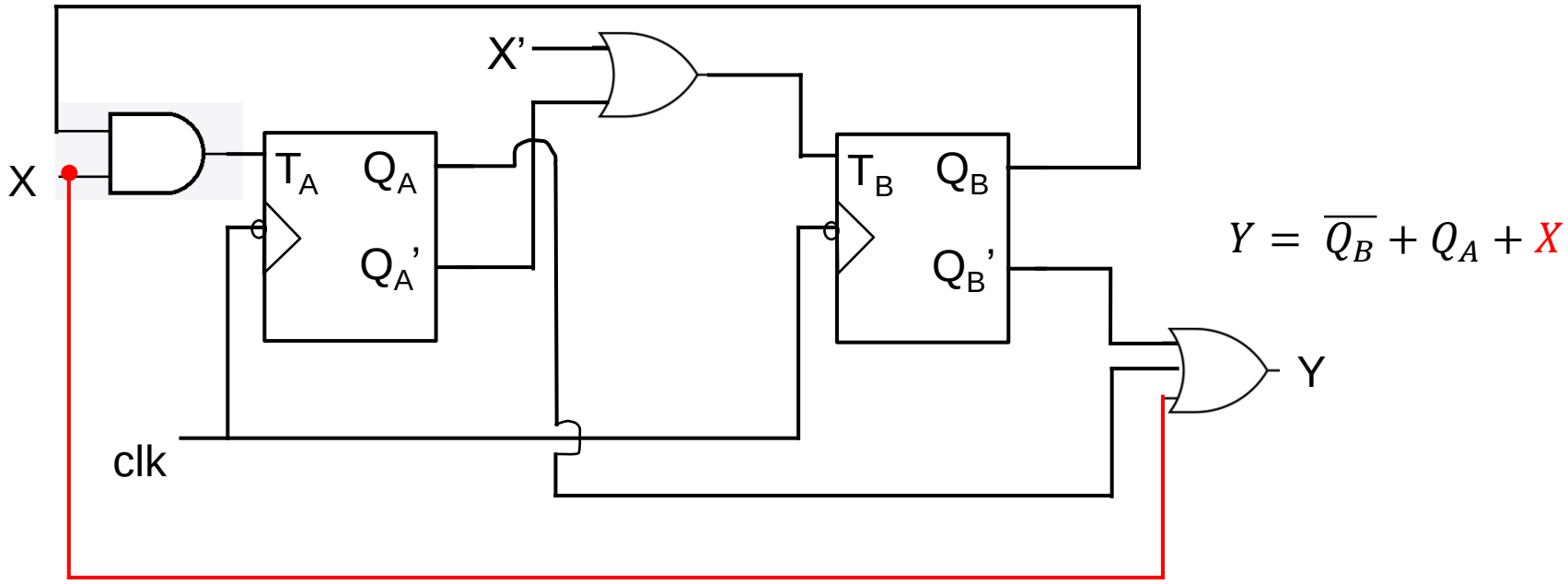


Mealy Machine

- The output is the function of present state as well as the input.

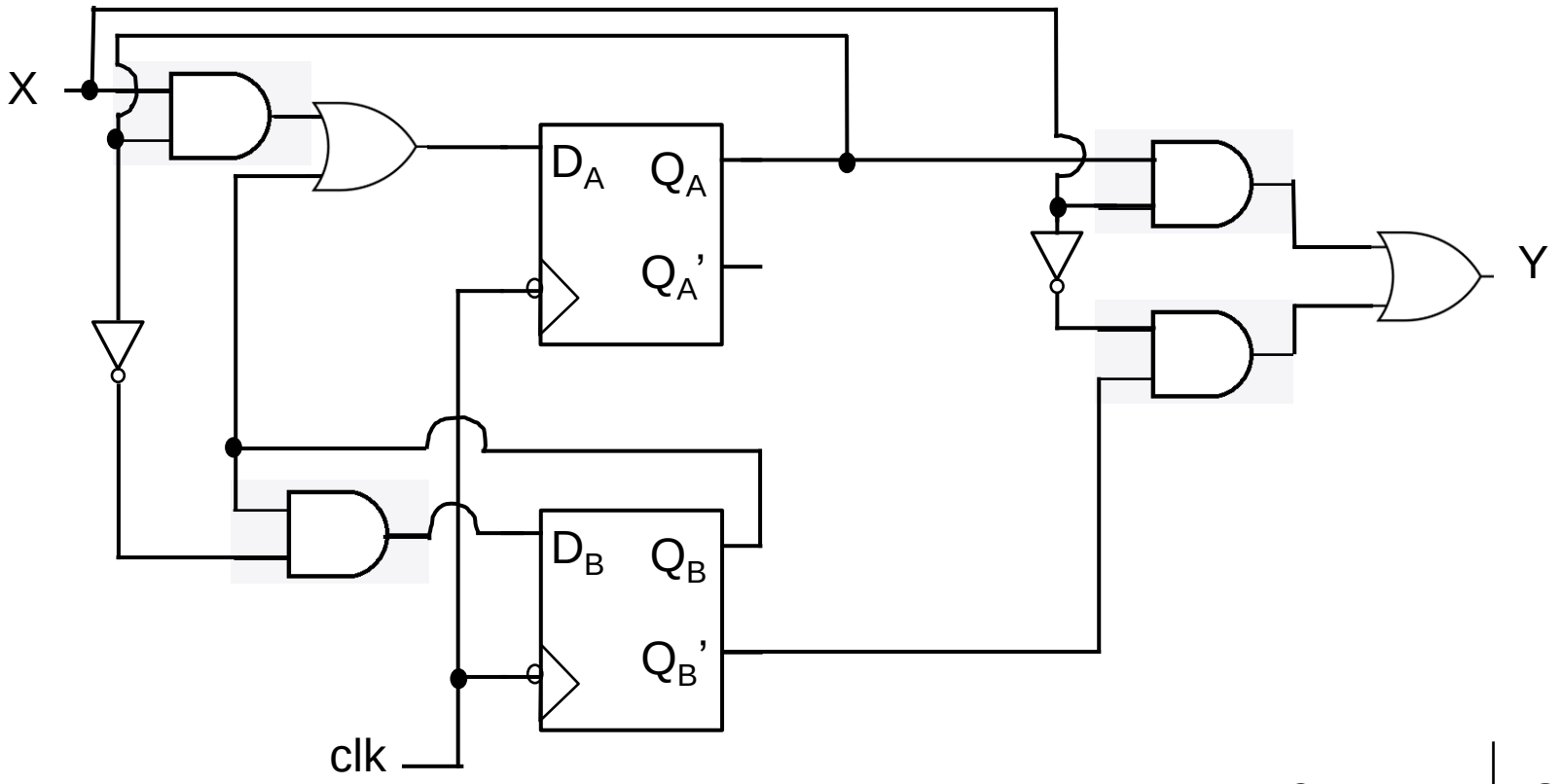


Comparision with Example 1



The circuit is a Mealy Machine

Analysis of clocked circuits with D ff



CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

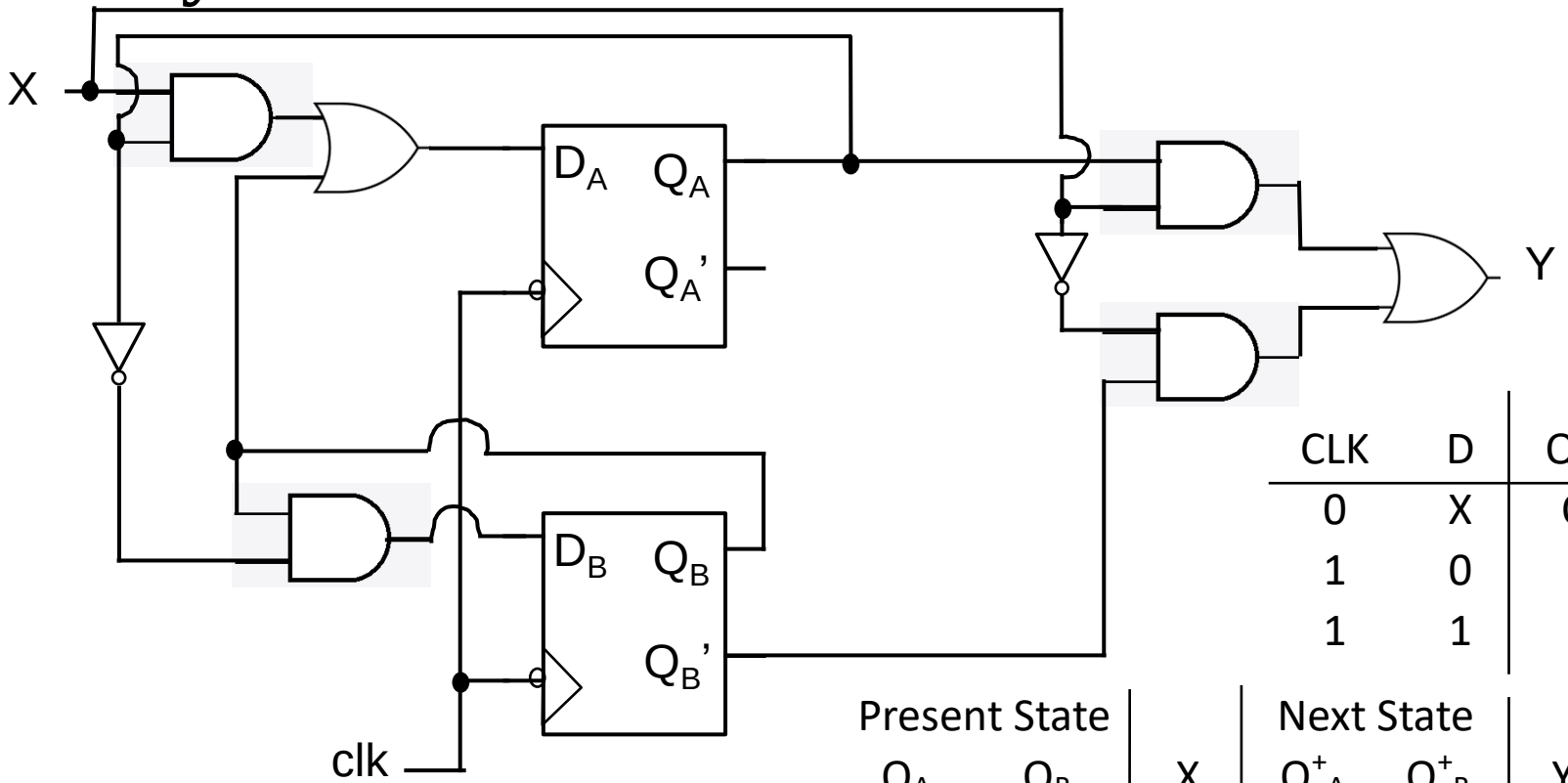
Step 1: Write Input and Output Equations

$D_A = X.Q_A + Q_B$

$D_B = \overline{Q_A}.Q_B$

$Y = X.Q_A + \bar{X}.\overline{Q_B}$

Analysis of clocked circuits with D ff cont.



CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Step 2: Find state table

Present State			Next State		
Q_A	Q_B	X	Q^+_A	Q^+_B	Y
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	0	1

$$D_A = X.Q_A + Q_B$$

$$D_B = \overline{Q_A}.Q_B$$

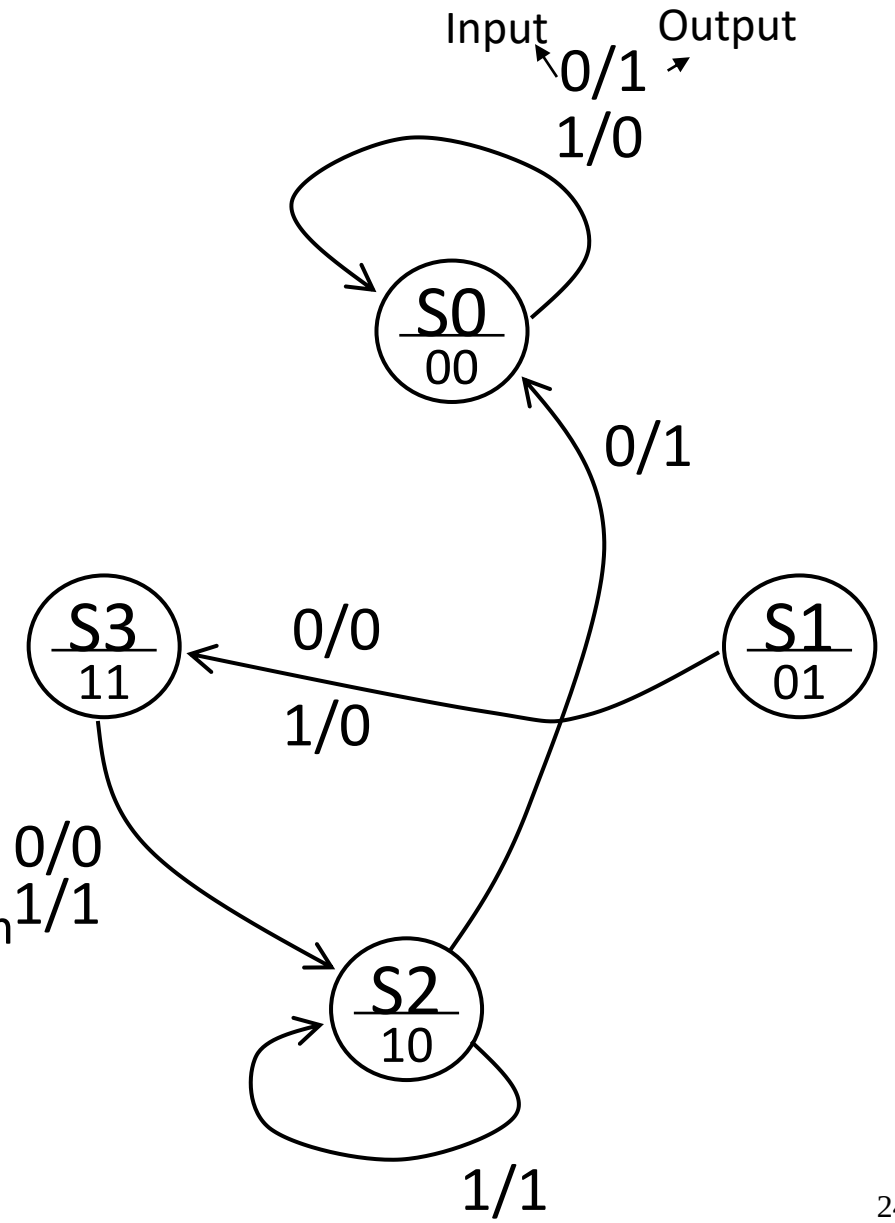
$$Y = X.Q_A + \bar{X}.\overline{Q_B}$$

Analysis of clocked circuits with D ff cont.

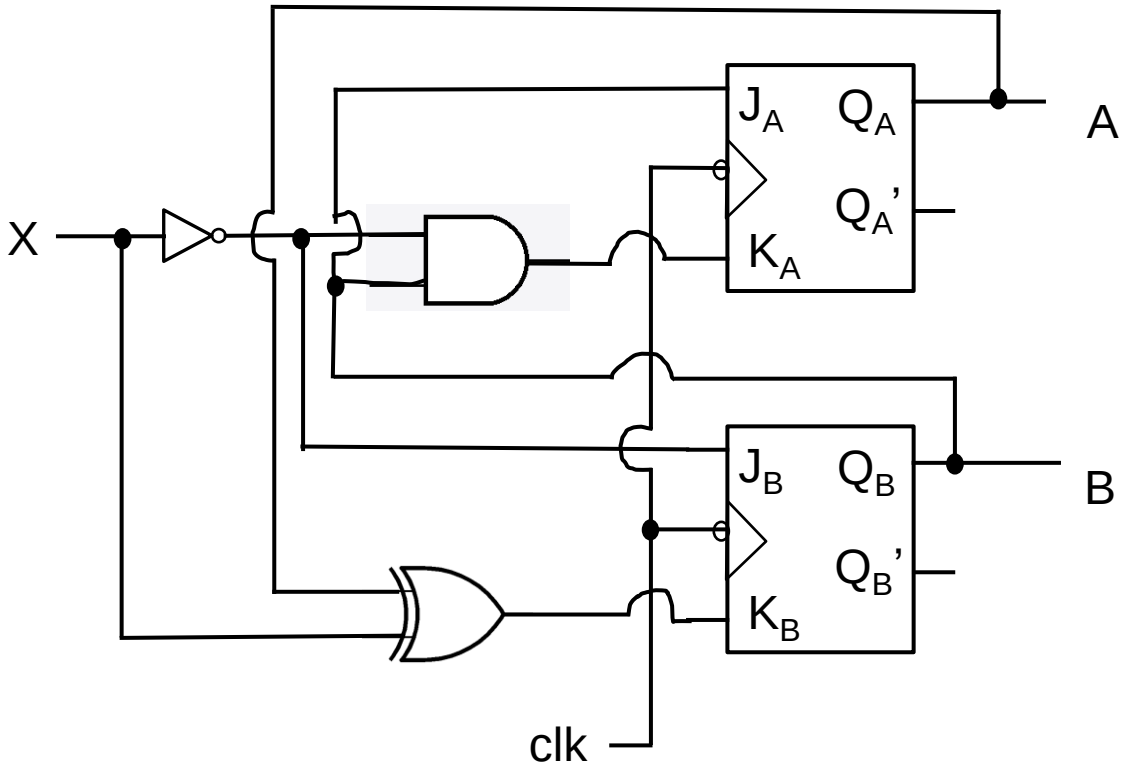
Present State			Next State		
Q_A	Q_B	X	Q^+_A	Q^+_B	Y
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	0	1

	Q_A	Q_B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

Step 3: Find state diagram



Analysis of clocked circuits with JK ff



Step 1: Input Equations, No Output Equation

$J_A = Q_B \qquad K_A = \bar{X}.J_A$

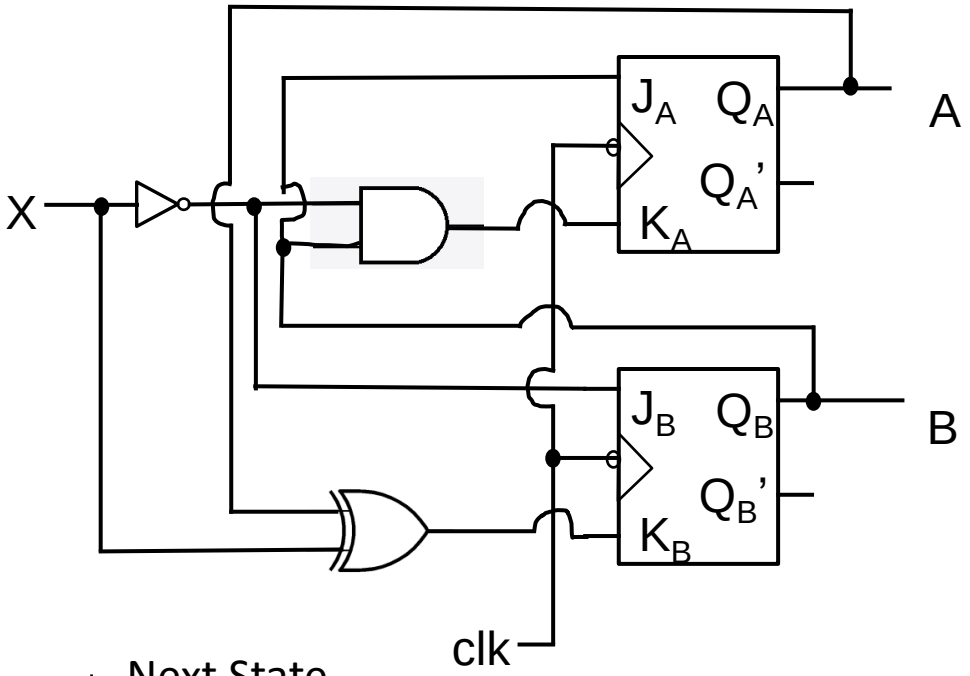
$J_B = \bar{X} \qquad K_B = X \oplus Q_A = \bar{X}.Q_A + X.\overline{Q_A}$

Analysis of clocked circuits with JK ff cont.

$J_A = Q_B \qquad K_A = \bar{X}.J_A$

$J_B = \bar{X} \qquad K_B = X \oplus Q_A = \bar{X}.Q_A + X.\overline{Q_A}$

CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$(Q_n)'$



Step 2: Find the state table

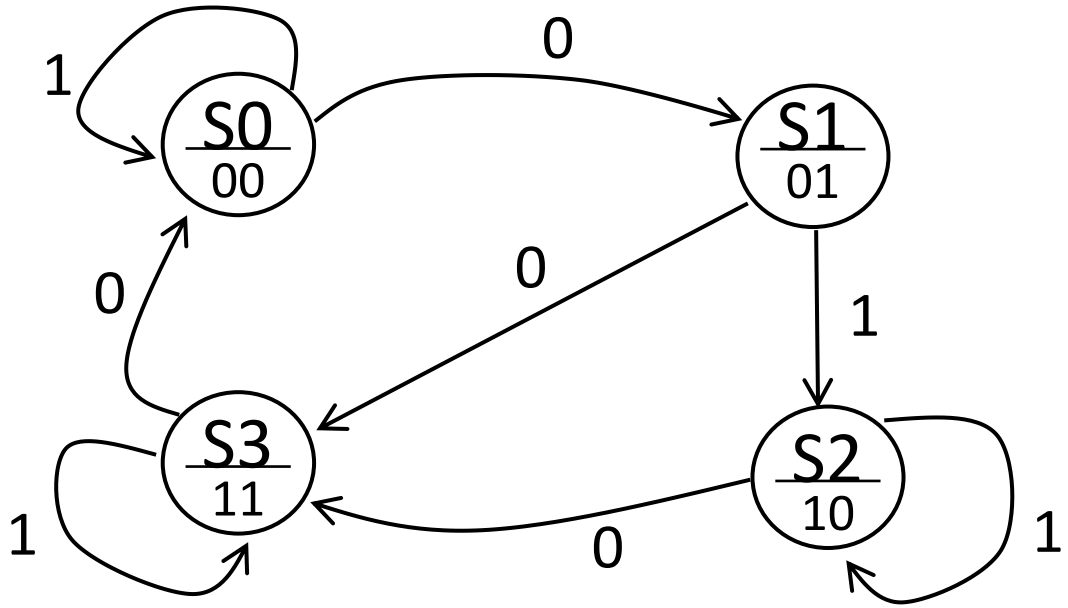
Present State							Next State	
Q_A	Q_B	X	J_A	K_A	J_B	K_B	Q^+_A	Q^+_B
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

Analysis of clocked circuits with JK ff cont.

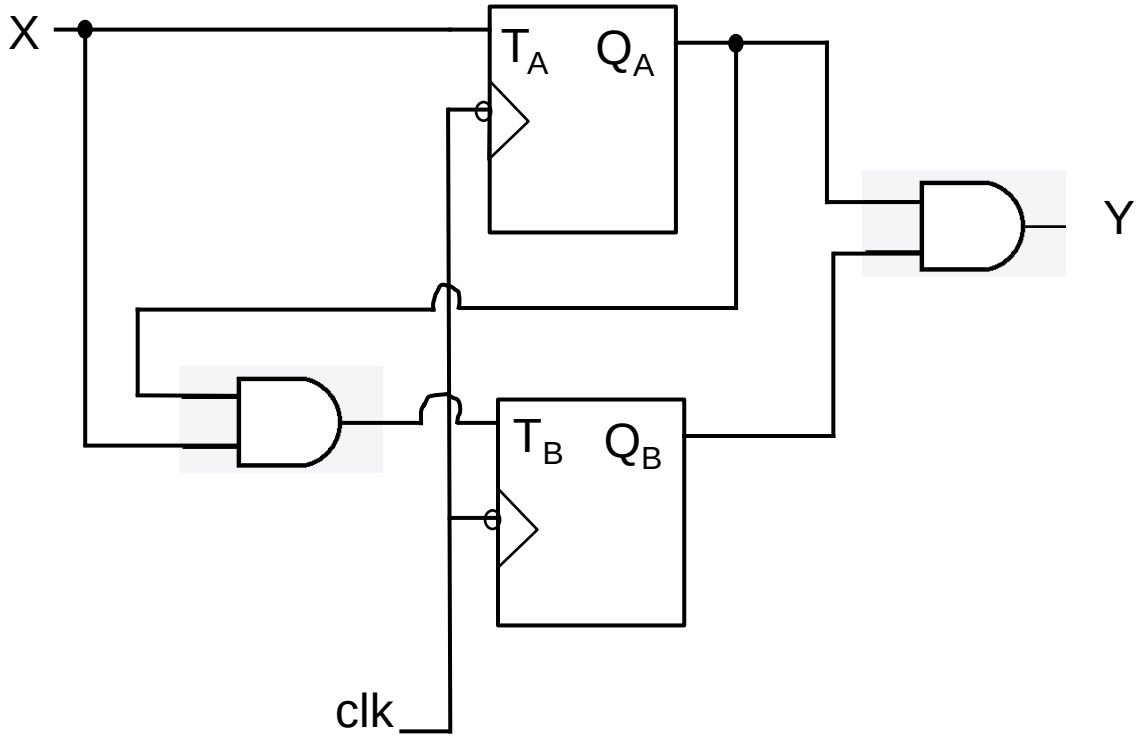
Present State							Next State	
Q_A	Q_B	X	J_A	K_A	J_B	K_B	Q^+_A	Q^+_B
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

	Q_A	Q_B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

Step 3: Find state diagram



Analysis of clocked circuits with T ff



Step 1: Input Output Combinational Equation

$T_A = X$

$T_B = X.Q_A$

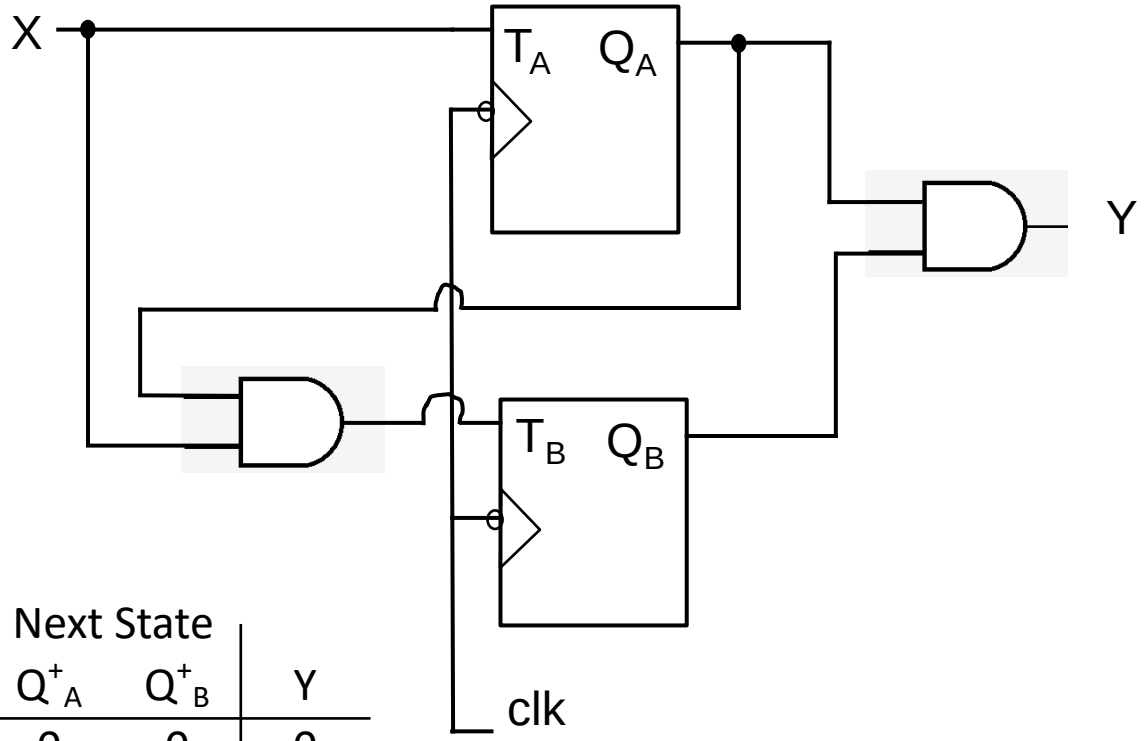
$Y = Q_A.Q_B$

Analysis of clocked circuits with T ff cont.

$T_A = X$

$T_B = X.Q_A$

$Y = Q_A.Q_B$



Step 2: Find the state table

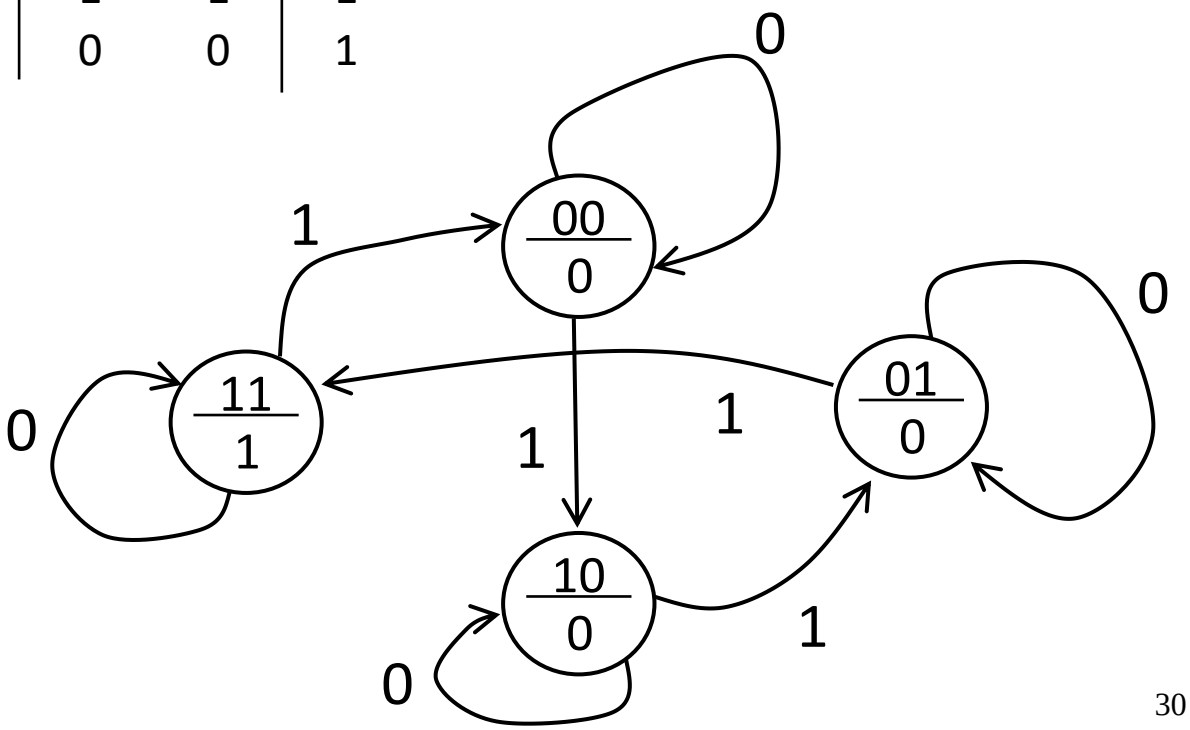
Present State					Next State		
Q_A	Q_B	X	T_A	T_B	Q^+_A	Q^+_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$(Q_n)'$

Analysis of clocked circuits with T ff cont.

Present State					Next State		
Q_A	Q_B	X	T_A	T_B	Q^+_A	Q^+_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	1
1	1	1	1	1	0	0	1

Step 3: Find state diagram



Moore Machine