EXPERIMENT 2: COMBINATIONAL CIRCUIT ANALYSIS

Objectives

The objective of Experiment 2 is

- to understand how to use logic gates to create a simply combinational logic circuit
- to analyze a combinational circuit and determine the Boolean expression from this circuit.
- to develop digital circuit building and troubleshooting skills.

Components Required:

- 7408 Quadruple 2-input AND gates,
- 7432 Quadruple 2-input OR gates,
- 7400 Quadruple 2-input NAND gates,
- 7402 Quadruple 2-input NOR gates,
- 7486 Quadruple 2-input XOR gates,
- DIP switches,
- 8 x LEDs,
- Resistors.

Preliminary Work:

1. Study class notes and prepare a truth table for each of the combinational circuits given in the experimental part. Then, write Boolean expressions for each output (G_1 … G_8 for Fig.1 and f_0 … f_2 for Fig.2) from the truth tables.
2. Perform Pspice simulations of the combinational circuits given in the experimental work. Show all the inputs and the requested outputs on the scope and verify truth tables. Add your results to your report. (**Pay attention to the simulation notes given in the first experiment sheet**)
3. Add the last page to your report to complete tables during experiments.

Experimental Work:

1. Implement the circuit given in Fig. 1 on your board. Connect your inputs and outputs respectively to switches and LEDs. All ICs must be properly connected to supply voltage and ground.
2. Fill the truth table given in Table 1.

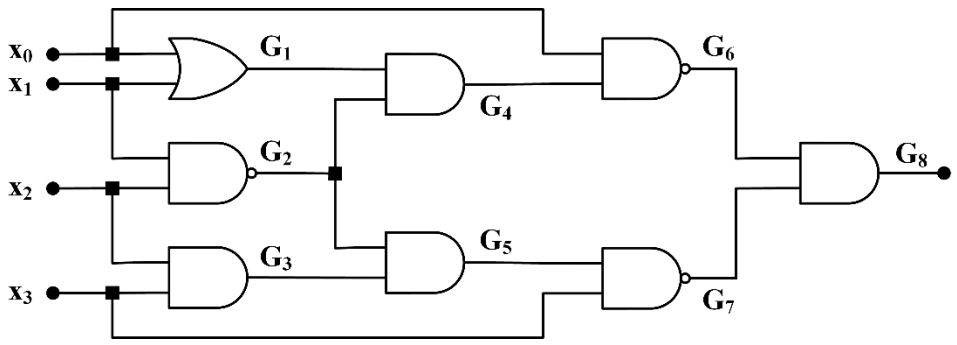

Figure 1

3. Implement the circuit given in Fig. 2 on your board. Connect your inputs and outputs respectively to switches and LEDs. All ICs must be properly connected to supply voltage and ground.
4. Fill the truth table given in Table 2.

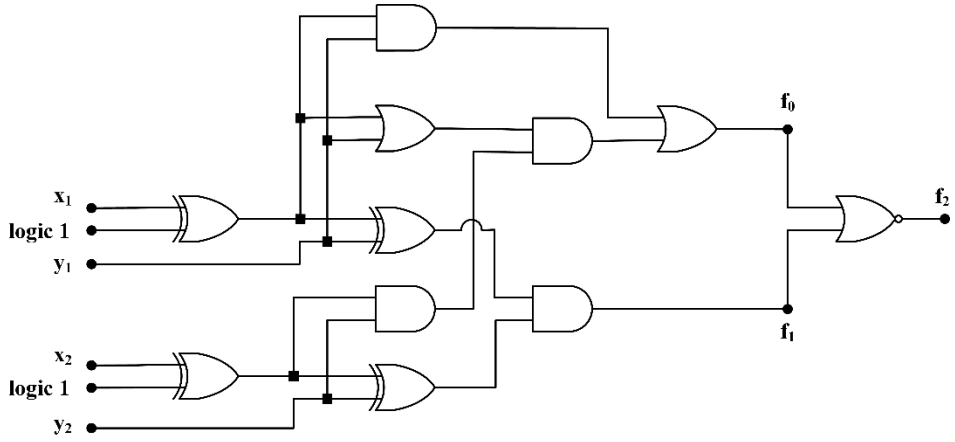

Figure 2

EXPERIMENTAL RESULTS:

Table 1. Truth table for the circuit given in Fig.1

X_3	X_2	X_1	X_0	G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								

Table 2. Truth table for the circuit given in Fig.2

X_1	X_2	Y_1	Y_2	f_0	f_1	f_2
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Comments: