EXPERIMENT 5: Synchronous and Asynchronous Counters

Objectives

The objectives of Experiment 5 are

- to design, build and test synchronous counters.
- to design, build and test asynchronous counters.

Components Required:

- 7408 – AND Gate
- 74112 – JK Flip Flop
- DIP switches, LEDs and resistors.

Preliminary Work:

1. Study synchronous and asynchronous counters in your class notes.
2. Design 4-bit synchronous up counter using JK flip flops. Determine Boolean expressions for all inputs of the flip flops from Karnaugh map. Show each step clearly in your report.
3. Design 4-bit asynchronous up counter using JK flip flops. Determine Boolean expressions for all inputs of the flip flops from Karnaugh map. Show each step clearly in your report.
4. Simulate circuits given in Fig.1 and Fig.2 in Pspice. Show CLK, Q3, Q2, Q1, Q0 on simulation plot from top to bottom respectively. Verify that the circuits function properly.
   (Pay attention to the simulation notes given in the first experiment sheet)

Experimental Work:

1. Implement the circuit given in Fig.1.
   - Make sure all ICs have +5V and ground connections.
   - Connect CLR (clear) and PR (preset) inputs properly.
   - Connect Q0, Q1, Q2, and Q3 to LEDs.
   - Connect CLK input to the debounced pushbutton.

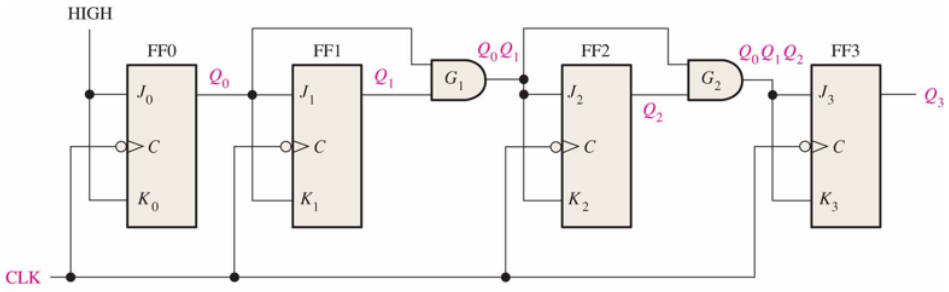

Figure 1. 4-bit Synchronous Counter

2. Implement the circuit given in Fig.2.
   - Make sure all ICs have +5V and ground connections.
   - Connect CLR (clear) and PR (preset) inputs properly.
   - Connect Q0, Q1, Q2, and Q3 to LEDs.
   - Connect CLK input to the debounced pushbutton.

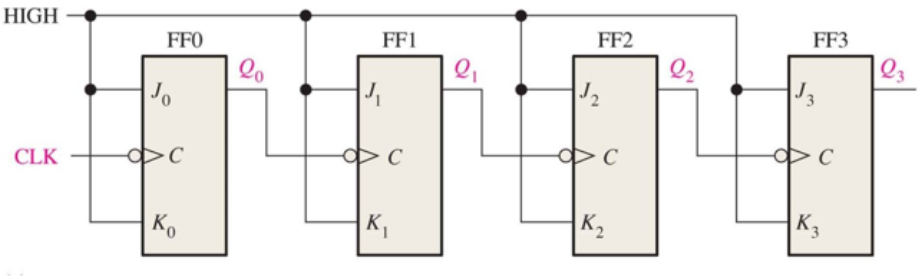

Figure 2. 4-bit Asynchronous Counter