EXPERIMENT 1A: BASIC LOGIC GATES PART 1

Objectives

The objective of Experiment 1A is to verify the truth tables of the basic logic gates (NOT, AND, OR).

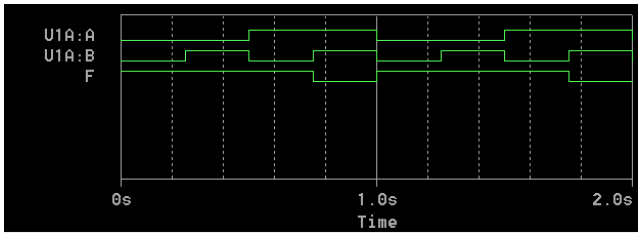
Components Required:

- 7404 Hex Inverters
- 7408 Quadruple 2-input AND gates,
- 7432 Quadruple 2-input OR gates,
- DIP switches,
- LEDs, 220Ω, 330Ω.

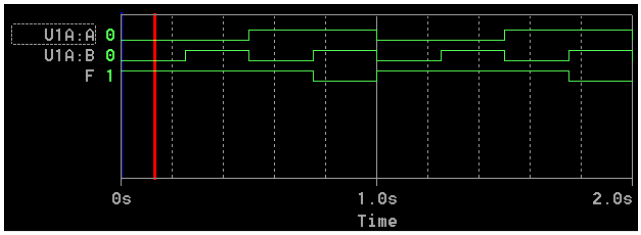
Preliminary Work:

1. Search datasheets of the ICs given above and read them. Check the pin diagrams and parameters in the datasheet (Their meaning, upper and lower limits etc.)
2. Study class notes. Prepare the truth tables for the logic gates (NOT, AND, OR) and add them to your report.
3. Generate the truth tables in Pspice and simulate your logic gates. Verify the truth tables and add the simulation results to your report (Plots must be readable). Explain each step and give your comments.

    - **Note1:** After simulation, find and click *Cascade* button under *Window* menu. Then shrink the simulation window from the corners with your mouse and show the full waveform (2 x the largest period) as given in the example below.



    - **Note2:** Click *Toggle cursor* button and show each row of the truth table on your simulation graph as given in the example below. Note the logic 0 and logic 1 next to the variables of A, B, and F.



Ex: The 1st row of the truth table		
A	**B**	**F**
0	**0**	**1**

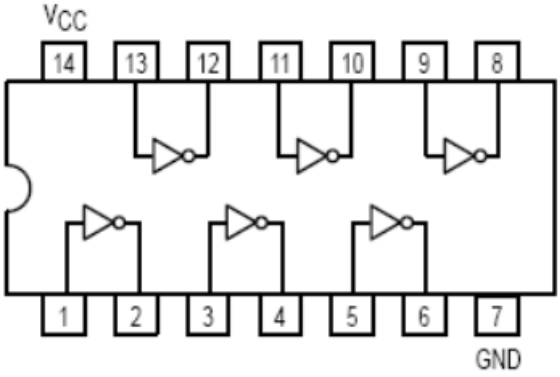
Experimental Work:

1. For each logic gate do the following steps:

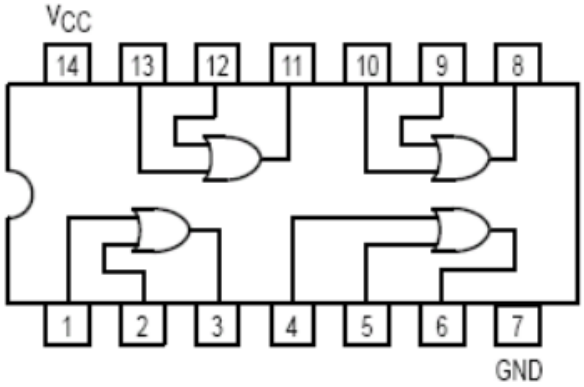
    a) Place the IC of ***NOT*** gate in a breadboard.
    b) Wire the IC to ground (0V) and power supply (+5 V).
    c) Check the datasheet of ***NOT*** gate, connect the input pins of the gate to data switches and the output pin to LED indicator.
    d) Make truth table for the studied logic gate and write down the output logic levels for the combinations of input logic levels in the truth table.
    e) Repeat the same steps for the other logic gates (AND, OR).

APPX. Pin Configuration Diagrams of Logic Gates

74LS04 – Inverter Gate (NOT Gate)



74LS32 – 2 Input OR Gate



74LS08 – 2 Input AND Gate