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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **\_\_\_ / \_\_\_ / \_\_\_\_\_\_** | **Batch No:** | **C1** |
| **Faculty Name:** |  | **Roll No:** | **16010122257** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 4**

**Title:4-bit magnitude comparator**

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| **Aim and Objective of the Experiment:** |
| To design a 2-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485 |

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| **COs to be achieved:** |
| **CO2**: Use different minimization technique and solve combinational circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Comparator:** The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.    **Two Bit Magnitude Comparator Implementation Details:**  **Truth Table**   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **A1** | **A0** | **B1** | **B0** | **A > B** | **A = B** | **A < B** | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |  |  |  |  |  |  |  | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |  | V | 0 |  |  |  |  | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | |  |  |  |  |  |  |  | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |  |  |  |  |  |  |  | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | |  |  |  |  |  |  |  | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | |  |  |  |  | 0 |  |  | | 0 | 1 | 1 | 1 | 0 | 0 | 1 | |  |  |  |  | 1 |  |  | | 0 | 1 | 1 | 1 | 1 | 0 | 1 | |  |  |  |  | 0 |  |  | | 1 | 0 | 2 | 0 | 0 | 0 | 0 | |  |  |  |  |  |  |  | | 1 | 0 | 2 | 0 | 1 | 0 | 0 | |  |  |  |  |  |  |  | | 1 | 0 | 2 | 1 | 0 | 1 | 0 | |  |  |  |  |  |  |  | | 1 | 0 | 2 | 1 | 1 | 0 | 1 | |  |  |  |  |  |  |  | | 1 | 1 | 3 | 0 | 0 | 0 | 0 | |  |  |  |  |  |  |  | | 1 | 1 | 3 | 0 | 1 | 0 | 0 | |  |  |  |  |  |  |  | | 1 | 1 | 3 | 1 | 0 | 0 | 0 | |  |  |  |  |  |  |  | | 1 | 1 | 3 | 1 | 1 | 1 | 0 | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |   **From the Truth Table:**  **(A<B)=A’B**  **(A=B)=A’B’+AB**  **(A>B)=AB’**  **Logic Diagram of 2 bit Comparator**    **Four Bit Magnitude Comparator Implementation Details**  **Pin Diagram of IC 7485**    **Logic Diagram of IC 7485**  **Comparing Table**  **IMG_20231015_141114142.jpg** |

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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 7485 on the trainer kit. 2. Connect 1st input no. to A3-A0 input slot and 2nd to B3-B0. 3. Connect the output YA>B , YA<B and YA=B to the output indicators. 4. Switch ON the power supply and monitor the output for various input combinations. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. Give some applications of magnitude comparator.   IMG_20231015_015835751.jpg   1. Explain with the help of the logic diagram how an 8 bit comparator can be implemented using IC 7485.   IMG_20231015_015225096.jpg  IMG_20231015_015515945.jpg |

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| **Conclusion:** |
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| **Signature of faculty in-charge with Date:** |