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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **26 / 10 / 2023** | **Batch No:** | **C1** |
| **Faculty Name:** |  | **Roll No:** | **16010122257** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 7**

**Title:Asynchronous Counter**

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| **Aim and Objective of the Experiment:** |
| To design and implement 3 bit Asynchronous up counter using JK Flip Flop |

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| **COs to be achieved:** |
| **CO3**: Design synchronous and asynchronous sequential circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)**    **Pin diagram of JK FF (IC 7476)** |

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| **Implementation Details** |
| **Procedure**   1. Locate IC 7476 JK FF on Digital trainer kit 2. Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC. 3. Make sure of Reset and Clear Pins connections with reference to data sheetinformation. 4. Connect a pulsar switch to the clock input. 5. Verify the working and prepare a truth table. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How JK FF need to be configured to use for counter operation?   IMG_20231026_095247546.jpg   1. What changes are required to use the same counter as 3 bit asynchronous down counter?   IMG_20231026_095744097.jpg  IMG_20231026_095848796.jpg   1. Draw the timing diagram of 3 bit Asynchronous up counter.   IMG_20231026_104450821.jpg   1. What is mod n concept used in counters?   IMG_20231026_105250681.jpg   1. For Mod-5 counter how many JK FFs are required?   IMG_20231026_105539562.jpg |

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| **Conclusion:** |
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| **Signature of faculty in-charge with Date:** |