

# Soumil Gupta

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Computer Architect

## EDUCATION

University of Illinois, Urbana-Champaign

May 2025

Bachelor of Science in Computer Engineering | GPA: 3.8/4.0 | Dean's List

### Relevant Coursework:

- **Hardware:** Computer Architecture, Digital Systems, VLSI System Design, IC Device Theory and Fabrication, Semiconductor Electronics, Digital Signal Processing, Analog Signal Processing
- **Software:** Operating Systems, Applied Parallel Programming, Communication Networks, Algorithms & Models of Computation, Data Structures & Algorithms, Computer Systems & Programming
- **AI/ML:** Artificial Intelligence, Applied Machine Learning, Deep Learning for CV, IoT & Cognitive Computing

### Technical Skills

**Languages:** C++, C, C#, Python, Java, x86 Assembly

**Tools/Environments:** CUDA, GDB, Linux, Bash/Shell, TCL, Git, Docker, Jenkins, Make, Vim, QEMU, Jupyter, LaTeX

**Libraries:** Tensorflow, Keras, PyTorch, NumPy, SciPy, Scikit-Learn, OpenCV, Pandas

**EDA/RTL DV:** SystemVerilog, SV Coverage, Intel Quartus, AMD Xilinx, Chisel, HLS, PyRTL, Vercel, Synopsys DC & VCS, Verdi, Spyglass, ModelSim/QuestaSim, Verilator, Chipyard, Cadence Virtuoso & Innovus, Gem5, Cocotb, UVM

**Interfaces & Test Methodologies:** AXI, UART, SPI, I2C, JTAG, ATPG, BIST, ATE

**Other:** ROS 1/2, RViz, Gazebo, Matlab, Simulink, Unity, Eagle CAD, Autodesk Inventor, SolidWorks

## WORK EXPERIENCE

### Research Intern | Samsung

Apr 2024 - May 2025

- Project is to **write, verify, layout, and tapeout proof-of-concept SoC** with RISC-V Cores, MESA Controller, & CGRA
- **Developed custom ISA** for MESA controller for mapping CPU programs with any **CGRA Hardware Accelerator**.
- **Built custom hardware verification framework** complete with golden model to compare DUT v. gold execution traces.
- Verified HDL modules for multiple IPs including modules on AXI protocol integration and Register Files.
- **Deployed and validated HDL code** through ModelSim, Verilator simulation, and Vivado software.
- **Participated in weekly scrums** with Samsung SAIT group, developing strong teamwork and communication skills.

### Undergraduate Teaching Assistant | Computer Systems & Programming Course, UIUC

Aug 2024 - May 2025

- Led weekly office hours, mentoring 5-10 students per session, encouraging development of critical programming and problem-solving skills, and guiding students in developing algorithms and debugging with GDB.
- **Taught C & C++ programming fundamentals**, file/device I/O, memory, signals & interrupt handling, and concurrency.

### Researcher | Autonomous & Unmanned Vehicle Systems Laboratory (AUVSL), UIUC

Dec 2022 - May 2025

- Led a team to design and implement outdoor robot localization solution leveraging Ultrawide-Band Antennas by **Writing Python & C++ packages**, deployable on Clearpath Husky & Jackal platforms.
- **Developed PyTorch scripts** to tune Adaptive Neural Fuzzy Inference System parameters, implemented SHFAF localization algorithm that improved localization accuracy by 82% to within 10 cm.
- Utilized Python to write localization software and scripts **utilizing popular libraries to analyze and process sensor data**.
- **Customized C firmware** and Utilized SPI communication protocol with Decawave UWB Sensors.
- Co-authored [IEEE paper](#) on localization methods. **Presented progress updates and results** to CERL organization under U.S. Army Corps of Engineers, exhibiting strong critical thinking and communication skills.

### Researcher | Virtual-Reality Immersive Laboratory, UIUC

Dec 2021 - May 2022

- **Developed VR application in C#** for Oculus platform to help college students visualize concepts in electromagnetism.

## HARDWARE SYSTEMS PROJECT EXPERIENCE

### RV32IM N-Way Superscalar Out-of-Order Explicit Register Renaming-Based CPU

May 2024

- Designed & verified from scratch an out-of-order N-way parameterizable processor for RISC-V 32-bit ISA with M-extension, achieving IPC of 0.51 on standard benchmark taking 62.7 mW of power at clock frequency 325 MHz.
- Implemented speculative branching with branch prediction overriding, & perceptron and Gshare branch predictors.
- Implemented cache features including next-line & stride prefetchers, post-commit store buffer with write coalescing.
- Integrated Synopsys IPs including sequential divider, and wrote Dadda advanced multiplier and shift-add multiplier.
- Wrote full processor in SystemVerilog, Simulated with Synopsys VCS, Debugged with Synopsys DC, Verdi, Spike, RVFI, Lint, Functional Coverage, Used Python to generate test programs, build toolchains with bash, GNU make

## **Bitsliced RV32I CPU in Cadence Virtuoso**

Apr 2025

- Authored FreePDK 45nm standard library (logic, muxes, flip-flops) with schematic, layout, and Liberty timing views.
- Manually laid out in Virtuoso a complete 32-bit RISC-V RV32I pipeline using a bitsliced methodology in a hierarchical library: authored one fully routed 1-bit slice—ALU, write-low/read-high register file, barrel-shifter, and cascaded comparator—and arrayed 32 slices to form the full datapath with byte-addressable memory.
- Verified extracted netlist with SystemVerilog harness, passing reference and self-written RV32I assembly suites.
- Wrote Tcl scripts for Innovus to make 2nd processor in addition to the manual layout to automate the layout process & minimize area for the entire processor, including floorplanning, placement, routing, & DRC/LVS checks.

## **IC Fabrication - Course-Based Project at UIUC**

Dec 2024

- Independently processed a silicon wafer from start to finish in an industrial cleanroom environment, performing every step—from RCA cleaning and oxidation to photolithography, etching, doping, and final metal lift-off.
- Utilized a five-mask sequence to fabricate complex devices (MOSFETs, BJTs, diodes, logic gates).
- Acquired in-depth knowledge of oxidation, photolithography, diffusion, CVD, ion beam processing, and annealing.

## **Digital Audio Workstation (DAW) with Audio Processor on FPGA**

May 2023

- Independently created DAW (like GarageBand) for creating music on Intel MAX10 FPGA that records, crops, applies audio effects, and mixes four stereo tracks on SDRAM, drives 640x480 VGA interface, and responds to USB-keyboard input. Audio effects include 6 dB gain, low-pass FIR equalization, and sample-accurate stereo-mixing.
- Engineered custom audio pipeline in C & SystemVerilog: SGTL5000 audio codec (ADC/DAC) converts analog-digital audio; I2S shifters send 32-bit stereo samples, and embedded-C I2C firmware programs codec registers.
- Researched documentation to incorporate Intel FPGA peripherals, NIOS II, and Unit-Tested functionalities.

## **AI/ML PROJECT EXPERIENCE**

### **LeNet-5 Implementation in CUDA**

May 2025

- Designed and implemented a version of LeNet-5 CNN to run on a cluster of Nvidia A40 GPUs.
- Built convolution layers with fused feature-map unrolling, tiled GEMM, and output permutation into one Tensor-Core (WMMA) kernel, removing all intermediate global-memory traffic and boosting arithmetic intensity.
- Profiled hot spots with Nsight Systems and Nsight Compute; validated memory safety using compute-sanitizer and ensured bit-exact parity against a CPU reference instrumented with gprof.
- Overlapped PCIe moves and compute via dual async CUDA streams (req0), hiding latency to 256-image batch sizes.

### **FPGA-Accelerated DNN for Autonomous Traffic Sign Recognition**

Apr 2025

- Designed a hardware-accelerated Deep Neural Network for AMD PYNQ-Z2 FPGA using Xilinx Vivado HLS.
- Implemented convolution, activation, and pooling layers with HLS pragmas to optimize dataflow and pipelining.
- Integrated the accelerator via Vivado AXI IP blocks and automated image feeding through a Python script.
- Leveraged ScaleHLS frameworks for hardware–software co-design, balancing accuracy with FPGA resource limits.

### **ResNet Implementation for Image Classification**

Feb 2025

- Implemented a deep Residual Neural Network architecture from scratch to classify images (e.g. MNIST-like data).
- Incorporated skip connections to combat vanishing gradients and enable stable training of deeper CNN layers.
- Employed TensorFlow/Keras for model development, training, and hyperparameter optimization; utilized NumPy, Matplotlib for data preparation, analysis, and visualization.
- Employed TensorFlow Lite to deploy trained models on Raspberry Pi + Google Edge TPU for IoT applications.

### **Deep Reinforcement Learning for Atari Breakout**

Apr 2024

- Implemented DQN and Double DQN agents with Python, PyTorch, and OpenAI Gym to master Atari Breakout.
- Developed a recurrent state mechanism to maintain historical context, enhancing decision-making during gameplay.
- Tuned hyperparameters and executed training on a GPU-based Linux cluster to achieve target mean scores.
- Incorporated LSTM modules to further improve temporal dependency handling and performance.

## **SOFTWARE PROJECT EXPERIENCE**

### **Unix-Like Operating System**

Dec 2023

- Engineered a UNIX-like, single-core kernel for 32-bit hardware fully from scratch using C and x86 Assembly.
- Implemented a paging-only virtual memory system, writable file system, software context switching, terminal switching, and hardware interrupts and exception handling.
- Developed device drivers for keyboard, mouse, real-time clock, & built interactive shell for executing system calls.
- Used advanced GDB techniques to efficiently debug and resolve system-level issues.
- Emulated and tested the OS in a QEMU virtual environment, ensuring safe and efficient debugging.

### **TCP Protocol Implementation**

Oct 2024

- Implemented a C-based transport protocol to emulate TCP-like behavior using UDP sockets.
- Designed sender/receiver functions to ensure accurate, high-efficiency transfer, handling packet drops & reordering.
- Setup Docker-based testing environment & Utilized Wireshark, tcpdump, & libcap to analyze network performance.