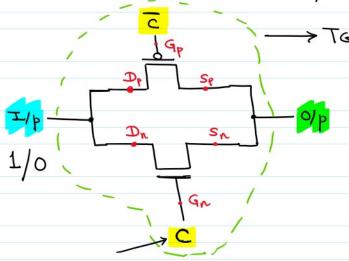
12 October 2021 08:52

Assignments:

O B.I.d :- Transmission Gate (TG)

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- => Tq is one of the four CMOS Logic Sub-families
- ⇒ Tq is a cros switch; ie:- a semiconductor s/w bull by combining 1 PMos & 1 NMos s/w
- ⇒ Tq = (1 PMOS) // (1 NMOS)
- ⇒ Being a combination of PMos & NMos, it gives both S1, so @ o/p
- ⇒ Construction: -> PMOS// NMOS



- @ If PMOS = ON } O/p = SI
- (P) It bung = OLE } Olb = MT X

- x oW = 910 f NO = 20mg +I €

Thus; to get STRONG OIP; irrespective of the value of I/p; we simultaneously S/W ON, both pmos & nmos

We give opposite values of Trigger to pmos & nmos

- > The Control signal for TG, denoted as "C" is applied to NMOU
- > The complement of "C" ie. C is applied to PMOS
- ⇒ Operation of TQ can be summarised as follows:

⇒ Operation of TG can be summarised as follows:

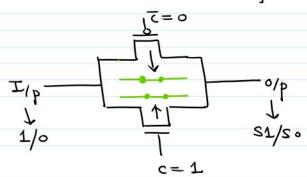
For
$$c = 1$$
 ($\overline{c} = 0$)

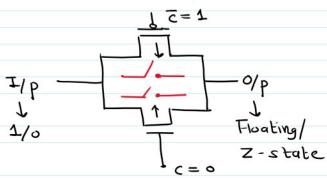
Thus = $0N$ | $p_{MOS} = 0N$

Thus = $0FF$, p_{MOS}

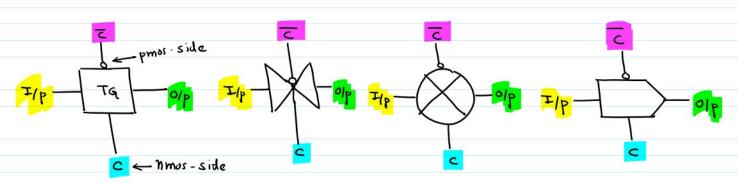
For
$$C = O(C = 1)$$

hmos = OFF, pmos = OFF

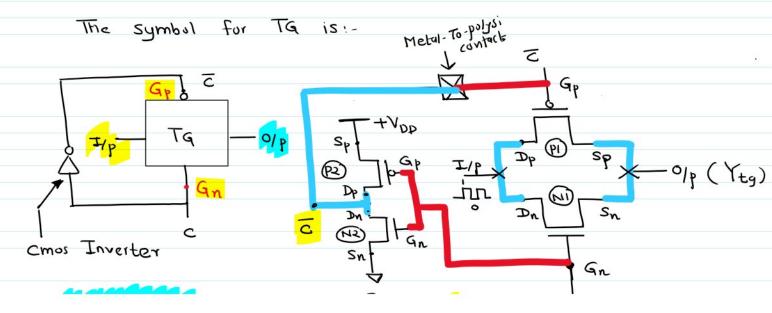




> Symbols: To has multiple Representations as follows:



> Mosfet-level schematic of Tq:-



CMOS Invester

(Flip-Horizontal the CMUS-Invir by Edit → Flip & Rotate after making it

→ To check functionality of TG:-

- 1 Apply 2.5 GHz Cluck @ I/p
- (3) For clock = 1; We should get O/p = + YDp = 1.27 (51)
- 3) For clock = 0; we should get op= -Vs1 = 0 v (s0)
- (*) Refer to the YouTube channel video for Demo of Tq-Layout