B.1.b : 2 i/p (NAND , AND) , B.1.c :2 i/p (NOR , OR) Logic Gates Using 90 nm Foundry

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✱ Assignments :- B.1.b (Using 90nm Foundry)

Ⅰ B.1.b :-

a) 2 i/p NAND

b) 2 i/p NOR

Ⅱ B.1.c :-

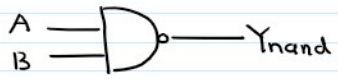
c) 2 i/p AND

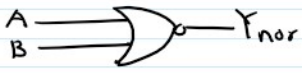
d) 2 i/p OR

✱ 2 i/p NAND, 2 i/p NOR Gates:-

2 i/p NAND **2 i/p NOR**

Symbols:





Expression:

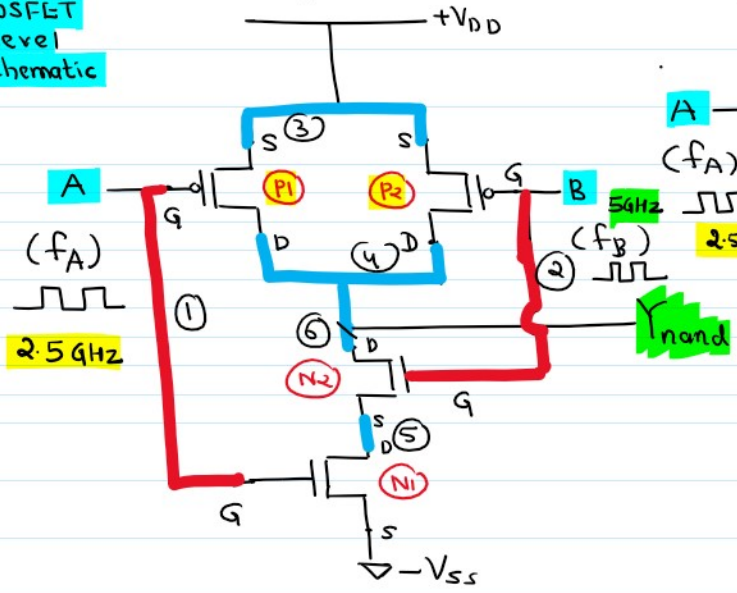
$Y_{nand} = \overline{A \cdot B}$

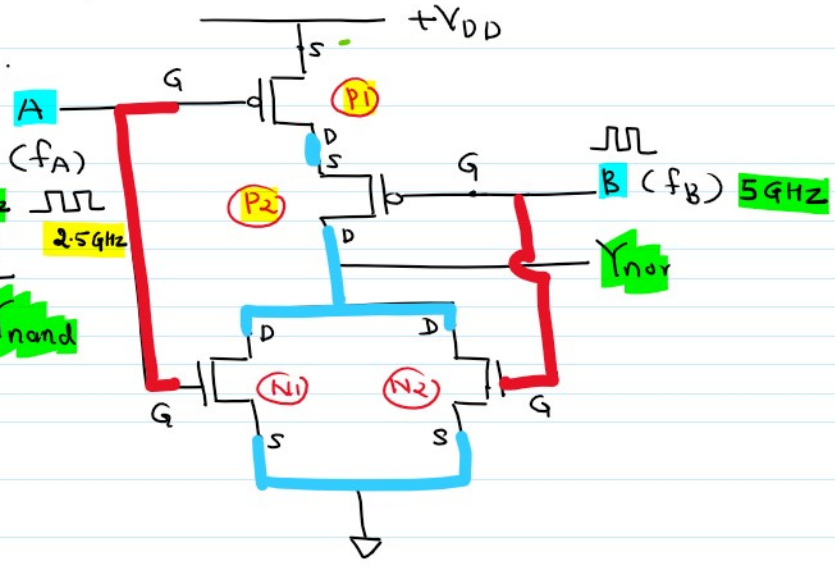
(P1//P2), (N1–N2)

$Y_{nor} = \overline{A + B}$

(P1–P2), (N1//N2)

MOSFET Level Schematic





$f_A = \frac{1}{2} \cdot f_B$

$f_A = \frac{1}{2} f_B$

A	B	Ynand
0	0	1
0	1	1

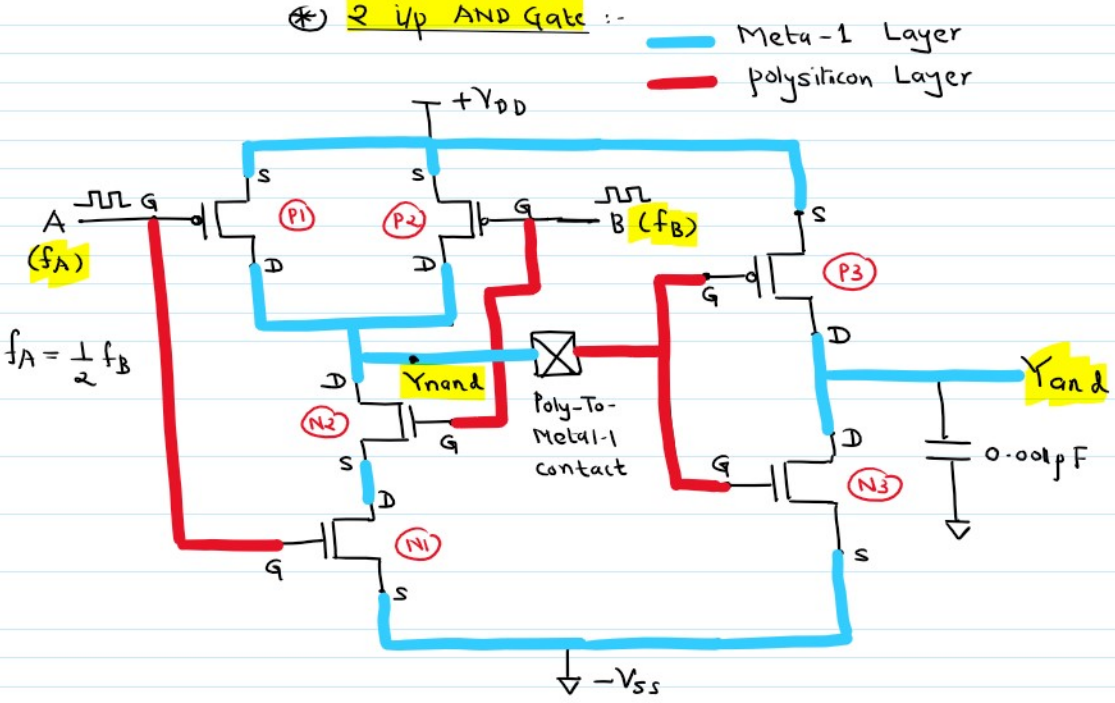
A	B	Ynor
0	0	1
0	1	0

0	0	1
0	1	1
1	0	1
1	1	0

0	0	1
0	1	0
1	0	0
1	1	0

⊛ MOSFET-Level Schematics for 2 i/p AND, 2 i/p OR Gate :-

⊛ 2 i/p AND Gate :-



⊛ 2 i/p OR Gate :-