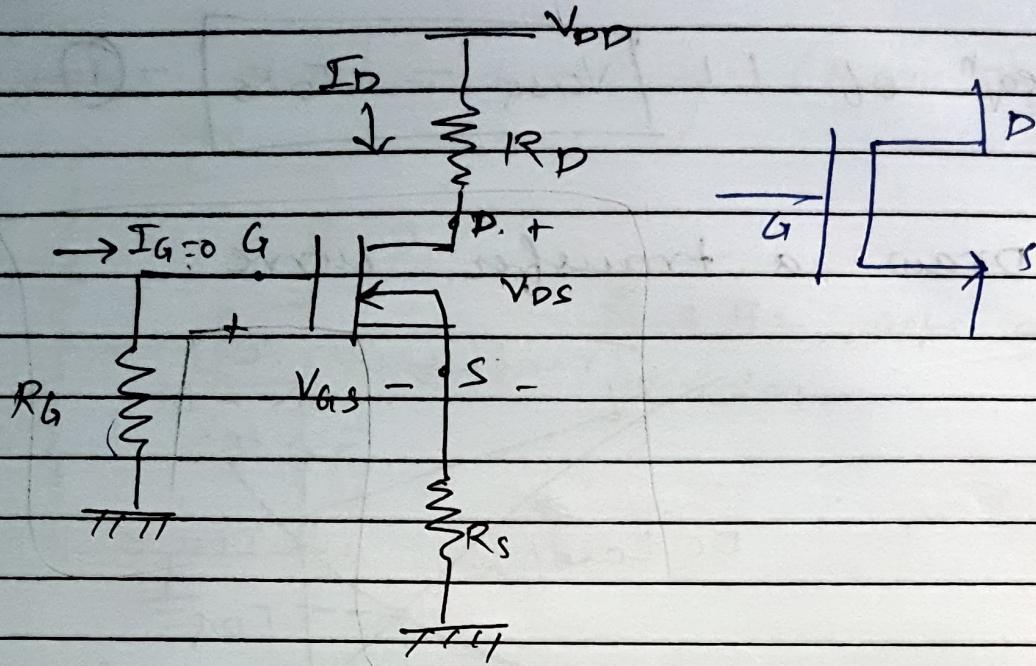


self bias clst.

(NMOS 'D'-type)



① rule to as loop.

$$-I_{GR_G} - V_{GS} - I_{DR_G} \stackrel{!}{=} 0$$

$$T_g = 0 \quad (\because \text{SiO}_2 \text{ layer})$$

$$\text{i.e } \text{V}_{0.5g} = -T_0 R_S$$

$$I_{DQ} = I_{DCC} \left(1 - \frac{V_{BS}}{V_p} \right)^2$$

ICUL to DIS loop

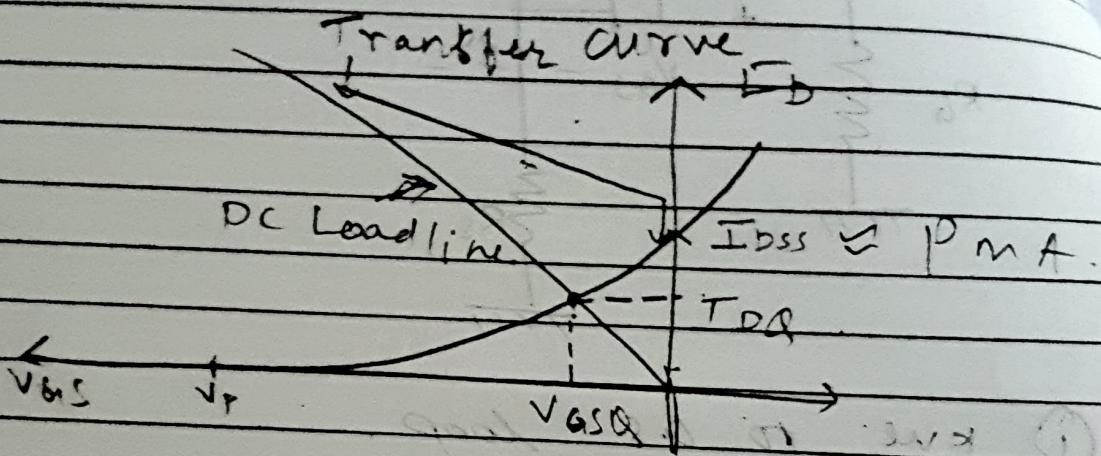
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_C) \quad , \quad (7)$$

→ To find Q_{pt} graphically.

① eqn of IL / $V_{DSQ} = -I_{DS}R_S$ - ①

② draw a transfer curve.



in eqn ①, put $I_D = 0$

$$V_{DS} = 0$$

1st : $(0,0)$

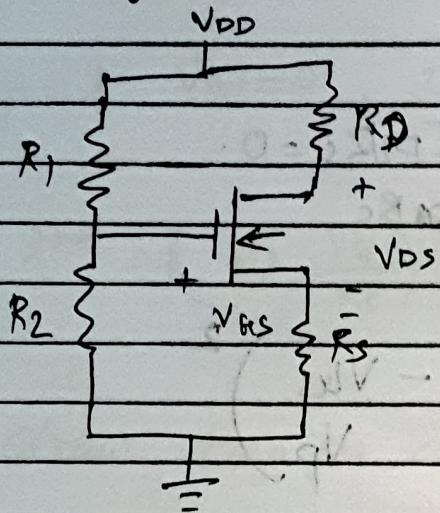
In eqn ② put $I_D = \frac{I_{DSQ}}{4}$

$$V_{DSQ} = -\frac{I_{DSQ}}{4} \times R_S$$

$$2^{nd} \text{ pt : } \left(-\frac{I_{DSQ} R_S}{4}, \frac{I_{DSQ}}{4} \right)$$

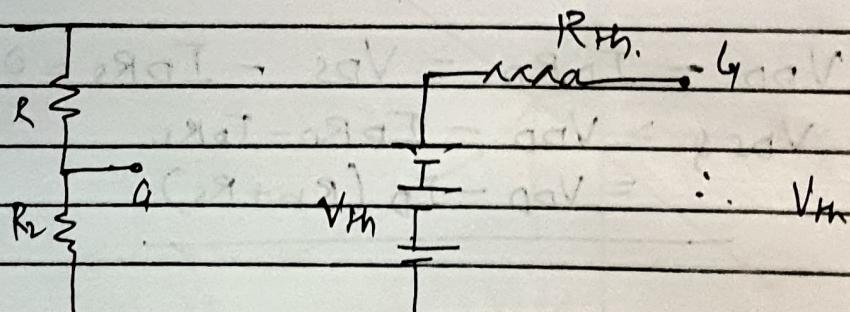
Opt is intersection of DC LL & transfer curve.

→ Voltage divider Biasing (Nmos Dtype).



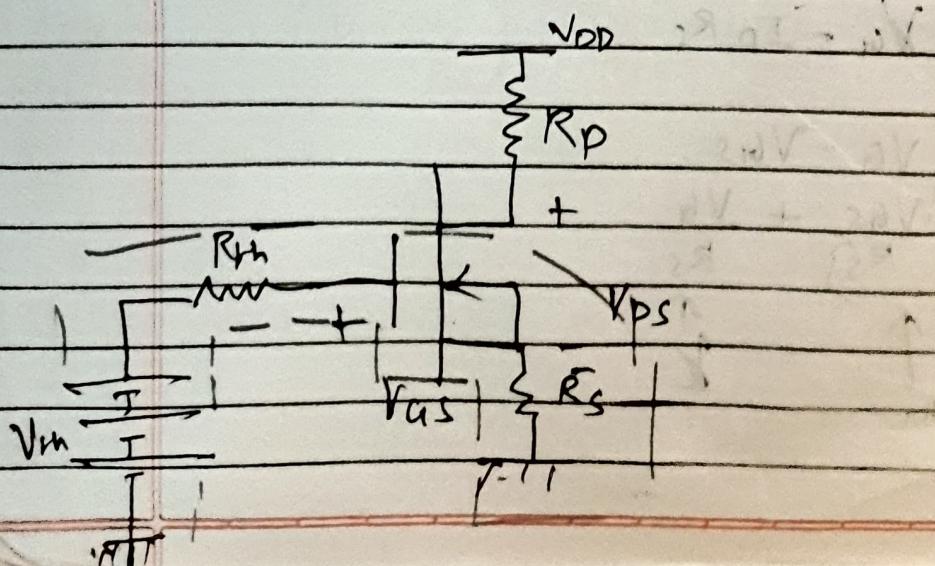
R_1 & R_2 acts as voltage divider

applying thevinin's th^m at gate,



$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$R_{th} = R_1 \parallel R_2$$



KW to G-S loop

$$\frac{V_{th} - I_D R_{th} - V_{ds} - I_D R_S = 0}{I_D = 0}$$

$$V_{th} - V_{ds} - I_D R_S = 0.$$

$$V_{ds} = V_{th} - I_D R_S$$

$$I_{Dg} = I_{DSS} \left(\frac{V_g - V_{ds}}{V_p} \right)^2$$

→ KW to D-S loop

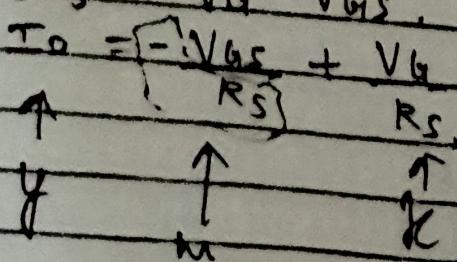
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$$

$$V_{DSg} = V_{DD} - I_D R_D - I_D R_S \\ = V_{DD} - I_D (R_D + R_S)$$

plot of pt graphically

$$V_{ds} = V_g - I_D R_S$$

$$I_D R_S = V_g - V_{ds}$$

$$I_D = \frac{V_g - V_{ds}}{R_S}$$


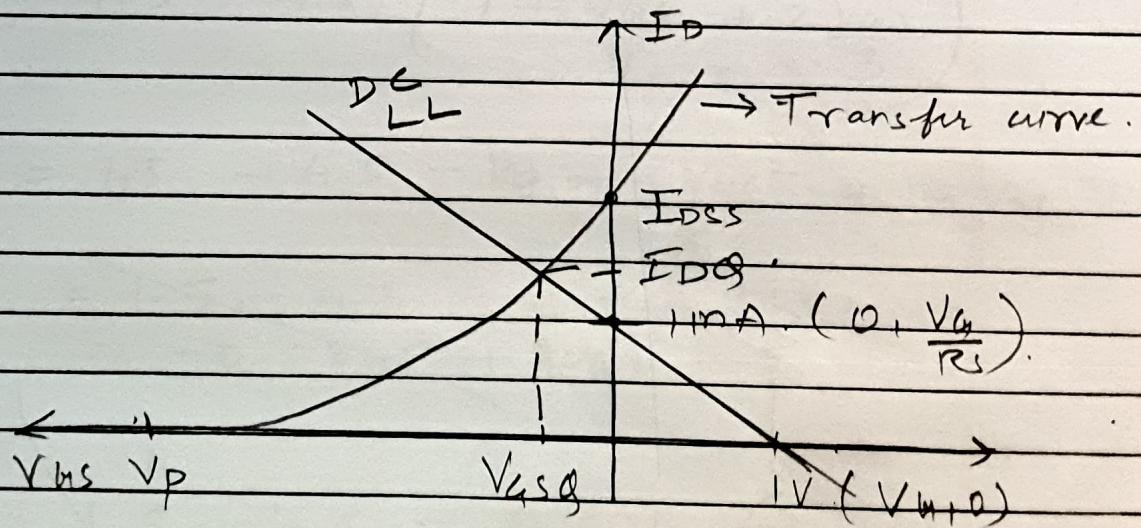
a) put $I_D = 0$, $V_{GS} \leq V_G$.

$$1^{\text{st}} : (V_G, 0)$$

b) put $V_{GS} = 0$, $I_D = \frac{V_G}{R_S}$.

$$2^{\text{nd}} : (0, \frac{V_G}{R_S})$$

\Rightarrow draw transfer curve for (Nmos - Dtype)



$$1) (V_G, 0) \quad V_G = 1V$$

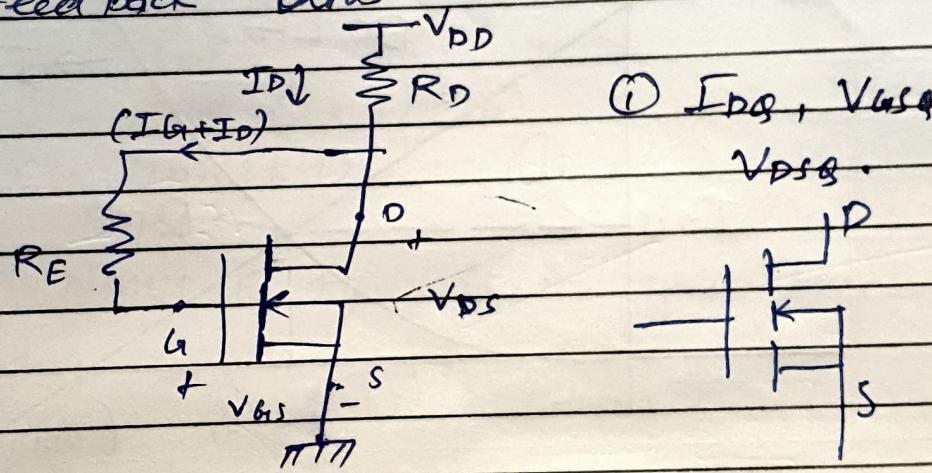
$$2) (0, \frac{V_G}{R_S}) \quad \frac{V_G}{R_S} = 1mA$$

NMOS - E type biasing type

① Drain - Feedback.

② Voltage - divider.

→ Drain Feedback bias

① I_{DQ} , V_{GSQ} , V_{DSQ} .

KVL to Gate source loop:

$$V_{DD} - (I_D + I_{G1}) R_D - I_{G1} R_G - V_{GS} = 0$$

$$V_{DD} - I_D R_D - V_{GS} = 0$$

$$I_{DQ} = k_n (V_{GS} - V_{th})^2$$

$$V_{GSQ} = V_{DD} \div I_D R_D$$

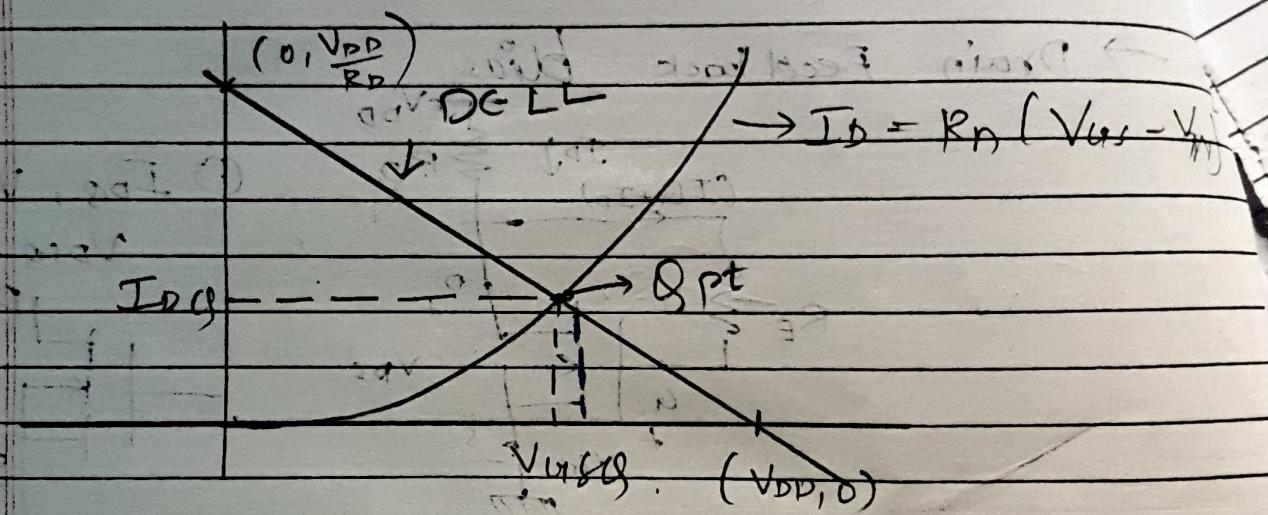
$$V_{DSQ} = V_{DD} - I_D R_D$$

Find Q_{pt}

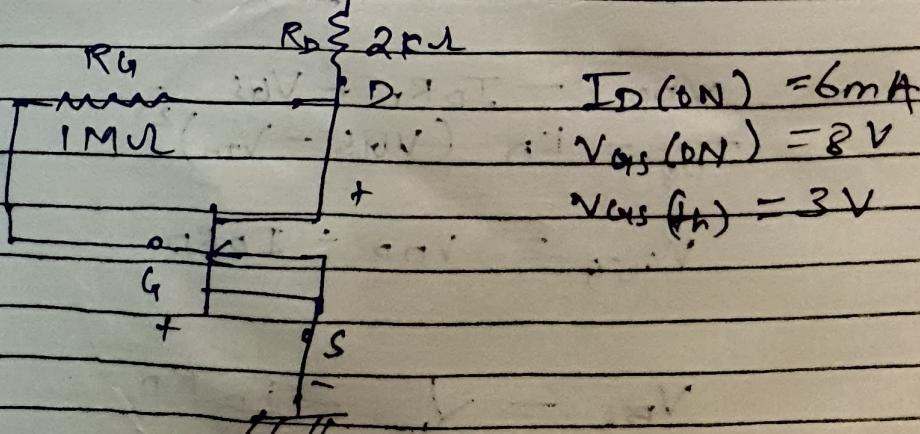
$$\textcircled{1} \quad V_{GS} = V_{DD} - I_D R_D$$

a) Put $I_D = 0 \rightarrow V_{GS} = V_{DD}$; 1st pt $\equiv (0, \frac{V_{DD}}{R_D})$

put $V_{GS} = 0 \rightarrow I_D = \frac{V_{DD}}{R_D}$; 2nd pt $\equiv (0, \frac{V_{DD}}{R_D})$



Num 1 : Find V_{GS} , I_D & V_{DS} for the ckt shown below.



solution:

$$k_n = I_{D(ON)}$$

$$[V_{GS(ON)} - V_{th}]$$

$$k_n = \frac{6 \text{ mA}}{(8-3)^2} = \frac{6 \text{ mA}}{25} = 0.24 \text{ mA/V}^2$$

$$V_{GS} = V_{DD} - I_{DRD}$$

$$= 12 \text{ V} - \cancel{2000} \cdot (2 \text{ k}^{-1}) (I_D)$$

$$V_{GS} = 12 \text{ V} - (I_D) (2 \text{ k}^{-1}) \quad \text{--- (1)}$$

assume NMOS F type is in saturation.

$$I_D = k_n (V_{GS} - V_{th})^2 = 0.24 \times 10^{-3} \cdot (V_{GS} - 3)^2 \quad \text{--- (2)}$$

put (2) in (1).

$$V_{GS} = 12 \text{ V} - \left[(0.24 \times 10^{-3}) (V_{GS} - 3)^2 \right] [2000]$$

$$= 12 \text{ V} - (480 \times 10^{-3}) (V_{GS} - 3)^2$$

$$= 12 \text{ V} - (0.48) (V_{GS}^2 + 9 - 6V_{GS})$$

$$V_{GS} = 12 \text{ V} - 0.48 V_{GS}^2 + 4.82 + 2.88 V_{GS}$$

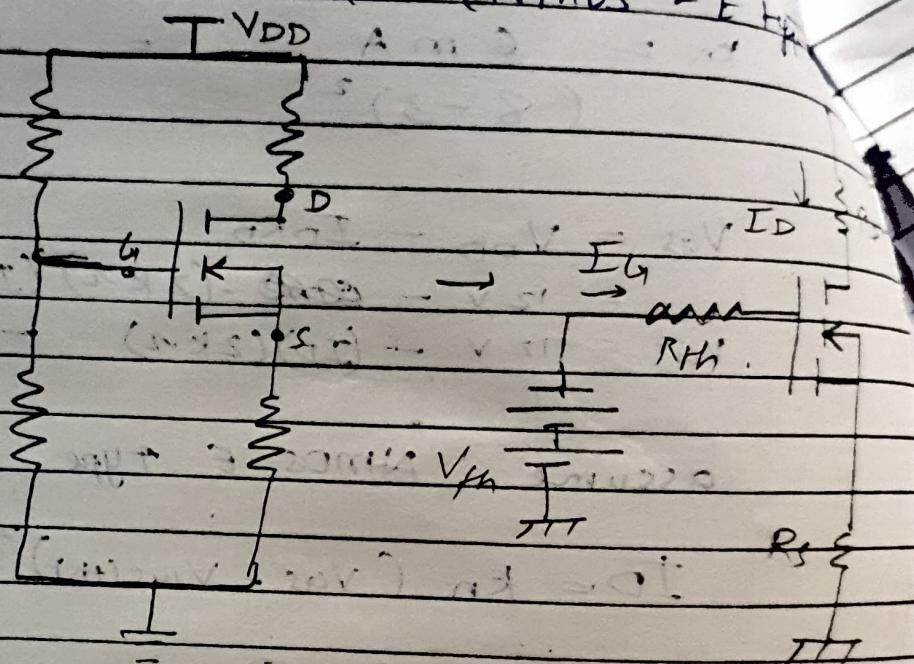
$$0.48 V_{GS}^2 - 1.88 V_{GS} - 7.68 = 0$$

$$V_{GS} = 6.412 \text{ V} \quad \checkmark \quad V_{GS} = -2.49 \text{ V.}$$

$$\therefore (V_{GS} > V_{th})$$

$$\begin{aligned}
 I_{DQ} &= K_n (V_{LSS} - V_{th})^2 \\
 &= 0.24 \times 10^{-3} (6.41 - 3)^2 \\
 &= \underline{2.79 \text{ mA}}
 \end{aligned}$$

→ Voltage divider bias (Nmos - FET)



$$V_{th} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$R_{th} = R_1 || R_2$$

① ~~ku to~~ ~~or's~~ loop

$$V_{TH} - I_4 R_{TH} - V_{DS} - I_D R_S = 0$$

$$V_{US18} = V_{th} - \sum R_s$$

$$I_D = k_n (V_{DS} - V_{th})^2 \cdot$$

KCL to D-S loop

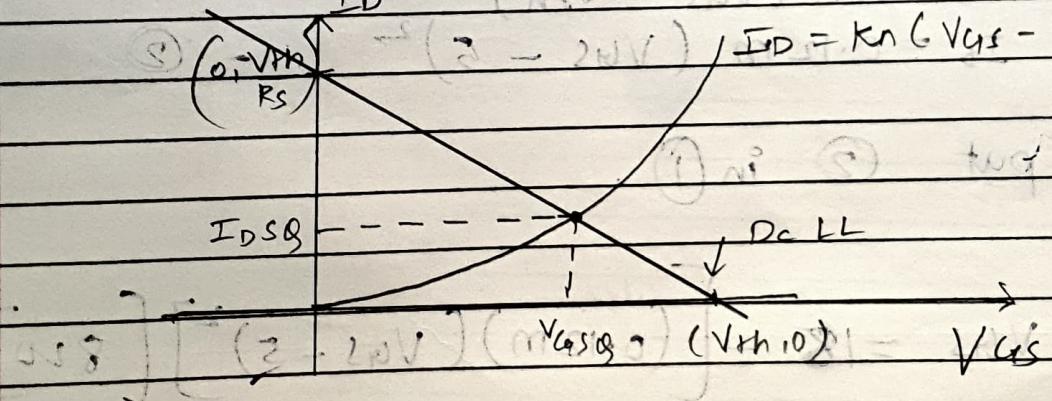
$$V_{DD} - I_{DRD}R_D - I_{DRS}R_S - V_{DSQ} =$$

$$V_{DD} - I_D(R_D + R_S) = V_{DSQ}$$

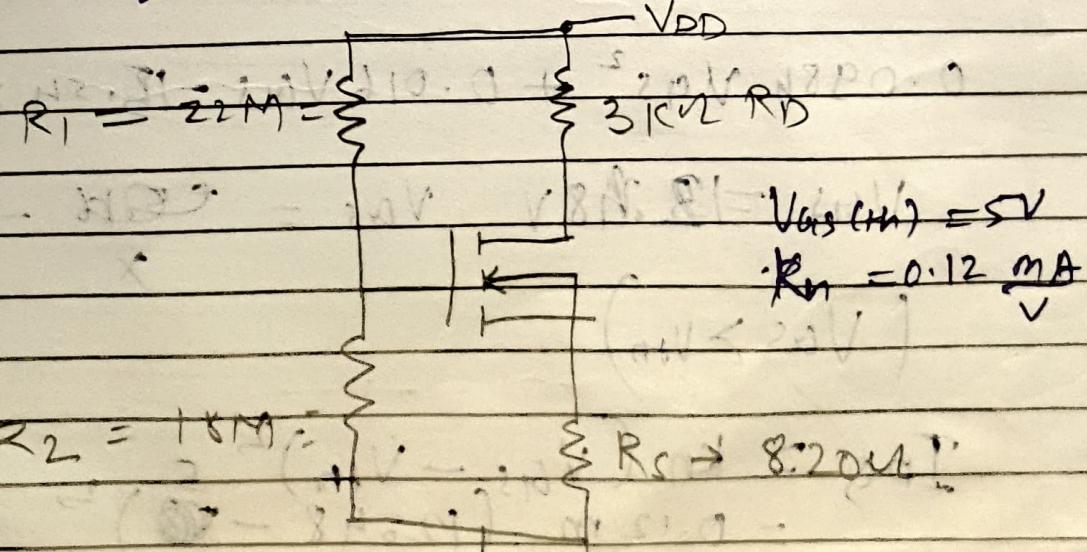
→ To find Q pt biasing.

$$V_{GS} = V_{TH} - I_{DRS}R_S - LL \text{ eqn}$$

- a) $I_D = 0 \rightarrow V_{GSQ} = V_{TH} ; 1^{\text{st}} \text{ pt } (V_{TH}, 0)$
- b) $V_{GSQ} = 0 \rightarrow I_{DQ} = \frac{V_{TH}}{R_S} ; 2^{\text{nd}} \text{ pt } (0, \frac{V_{TH}}{R_S})$



• Num ①: Find V_{GS} , I_D , V_{DSQ} for CRT.
also find region of operation driven device



$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$= \frac{18}{22 + 18} \times 40 = 18V$$

$$V_{GSS} = V_{TH} - I_D R_S$$

$$V_{GSS} = 5 - I_D (820) \quad \text{--- (1)}$$

assume: device working in saturation

$$I_D = k_n (V_{GSS} - V_{TH})^2$$

$$I_D = 0.12 m (V_{GSS} - 5)^2 \quad \text{--- (2)}$$

put (2) in (1).

$$V_{GSS} = 18 - [(0.12m)(V_{GSS} - 5)^2][820]$$

$$V_{GSS} = 18 - [0.0984 (V_{GSS}^2 + 25 - 10V_{GSS})]$$

$$V_{GSS} = 18 - [0.0984 V_{GSS}^2 - 2.46 + 0.984 V_{GSS}]$$

$$0.0984 V_{GSS}^2 + 0.016 V_{GSS} - 15.54 = 0$$

$$V_{GSS} = 12.48V \quad V_{GSS} = \cancel{15.54} - 12.64V$$

$$(V_{GSS} \geq V_{TH})$$

$$I_{DQ} = k_n (V_{GSS} - V_{TH})^2$$

$$= 0.12 m (12.48 - 5)^2 = 6.7mA$$

$$\begin{aligned}V_{DSQ} &= V_{DD} - I_D (R_S + R_D) \\&= 40 - 6.72 \text{ mA} (3 + 8) \text{ k} \\&= 40 - 6.72 \times 11 \\&= 14.32 \text{ V}\end{aligned}$$

$$V_{DSQ} > V_{TN} \quad (14.32 > 5 \text{ V})$$

$$V_{DSQ} > (V_{GSQ} - V_{TN}).$$

Given device is indeed in saturation region.