

① KVL to G-S loop,

$$-I_G R_G - V_{GS} - I_D R_S = 0$$

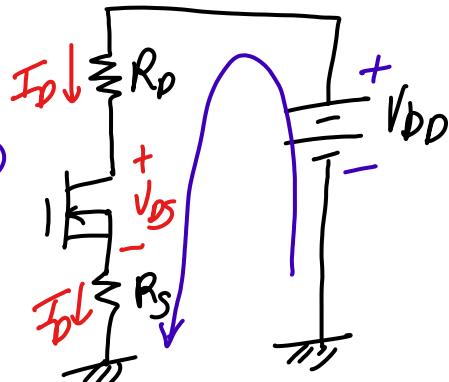
$I_G = 0$  (C:  $\text{Si}_3\text{N}_4$  layer)

$$\text{i.e. } V_{GSQ} = -I_D R_S$$

KVL to D-S loop

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$



→ To find Opt graphically,

① Eqn of load line

$$V_{GSQ} = -I_D R_S \quad \text{①}$$

$$\text{Opt} = (V_{GSQ}, I_D)$$

② Draw transfer curve for NMOS-D type

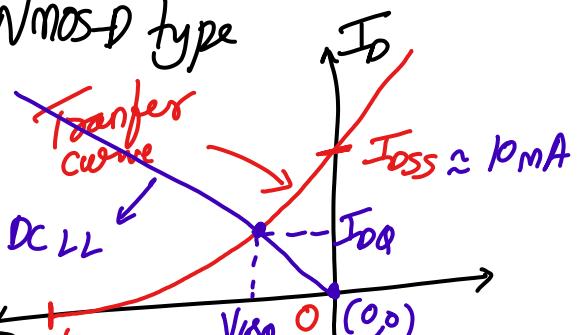
In eqn ①, put  $I_D = 0$

$$V_{GS} = 0$$

$$\text{1st pt: } (0, 0)$$

In eqn ②, put  $I_D = I_{DSS}$

$$V_{GSQ} = -\frac{I_{DSS}}{4} \times R_S$$

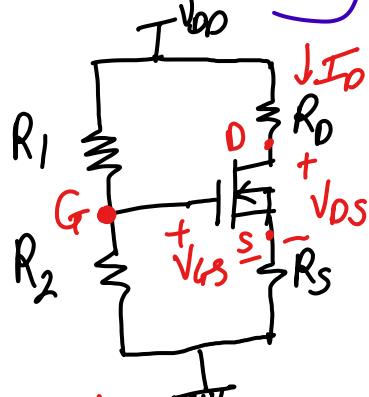


$$V_{GSQ} = -\frac{I_{DSS}}{4} \times R_S \quad \text{2nd pt: } \left(-\frac{I_{DSS}}{4} \times R_S, I_{DSS}/4\right)$$

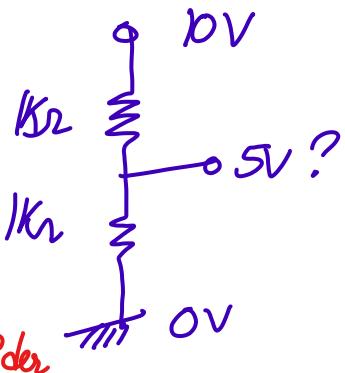
Opt is the intersection of DC load line & transfer curve

# # Voltage-divider Biasing (NMOS-D type)

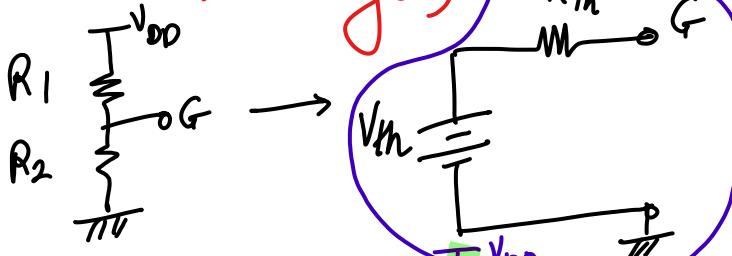
$V_{GS} \rightarrow +ve$



$R_1$  &  $R_2$  acts as voltage-divider



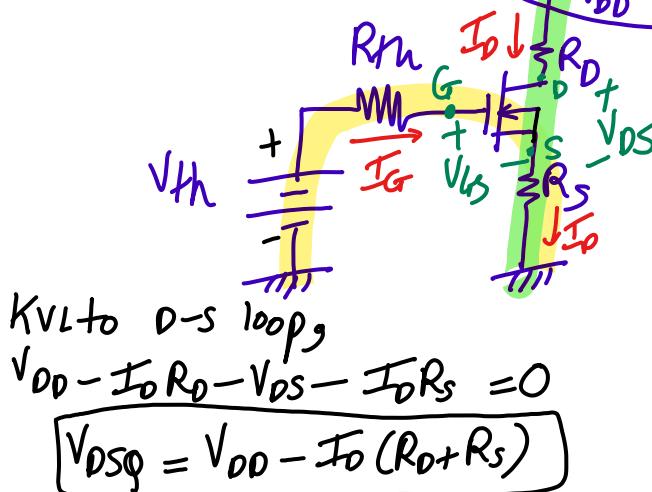
Apply Thevenin's Thm at gate,



$$V_{th} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$R_{th} = R_1 \parallel R_2$$

① KVL to G-S loop,  
 $V_{th} - I_G R_{th} - V_{GS} - I_D R_S = 0$   
 $I_G = 0$  ( $\because$  oxide layer)



$$V_{GSQ} = V_{th} - I_D R_S$$

$$I_{DQ} = I_{DSs} \left( 1 - \frac{V_{GSQ}}{V_p} \right)^2$$

To find Opt graphically,

①  $V_{GS} = V_G - I_D R_S$   $\rightarrow$  Eqn of load line

$$y = m x + c$$

$$I_D R_S = V_G - V_{GS}$$

$$I_D = -\frac{V_{GS}}{R_S} + \frac{V_G}{R_S}$$

$$m = -\frac{1}{R_S}; c = \frac{V_G}{R_S}$$

a) Put  $I_D = 0$ ;  $V_{GS} = V_G$   
1st pt:  $(V_G, 0)$

b) Put  $V_{GS} = 0$ ,  $I_D = \frac{V_G}{R_S}$   
2nd pt:  $(0, \frac{V_G}{R_S})$

→ Draw transfer curve for NMOS-D type

$$1st: (V_{GP})$$

$$2nd: (0, \frac{V_G}{R_S})$$

$$(1, 0)$$

$$(0, 1mA)$$

$$\frac{V_G}{R_S} = 1V$$

$$\frac{V_G}{R_S} = 1mA$$

$Q_{pt}$

$$V_{GS}$$

$$V_p$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad (4)$$

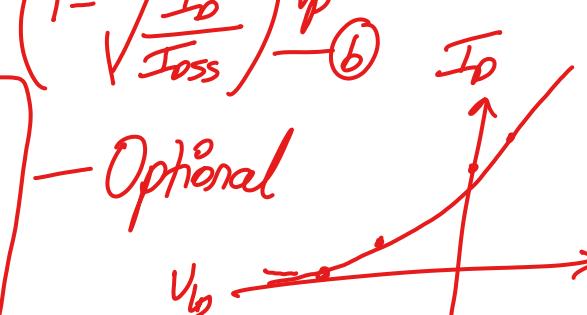
$$\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_p}$$

$$I_{DSS} = 7mA$$

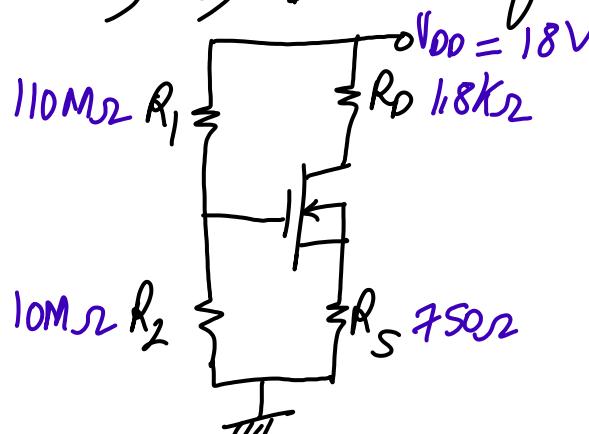
$$V_p = -3V$$

$V_{GS}$	$I_D$
0	$I_{DSS}$
$+V_p$	$I_{DSS}/2$
0	0

$$V_{GS} = \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) V_p \quad (5)$$



Numerical 1: Find  $V_G$ ,  $V_{GS}$ ,  $I_D$  &  $V_{DS}$  for ckt shown below



D-NMOS parameters

$$I_{DSS} = 6mA$$

$$V_p = -3V$$

Solution:  $V_{th} = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{10}{110 + 10} \times 18 = 1.5V$

$$V_{GSQ} = V_G - I_D R_S = 1.5 - I_D (750) \quad (1)$$

→ Assuming given device is in saturation region

$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = 6mA \left(1 + \frac{V_{GS}}{3}\right)^2 \quad (2)$$

Put eqn (2) in (1),

$$V_{GSQ} = 1.5 - 750 \times 6mA \left(1 + \frac{V_{GS}}{3}\right)^2$$

$$V_{GSQ} = 1.5 - 4.5 \left(1 + 2\frac{V_{GS}}{3} + \frac{V_{GS}^2}{9}\right)$$

$$V_{GSQ} = 1.5 - 4.5 - 3V_{GSQ} - 0.5V_{GSQ}^2$$

$$\text{i.e. } 0.5V_{GSQ}^2 + 4V_{GSQ} + 3 = 0$$

$$V_{GSQ} = -0.8377 \text{ V}$$

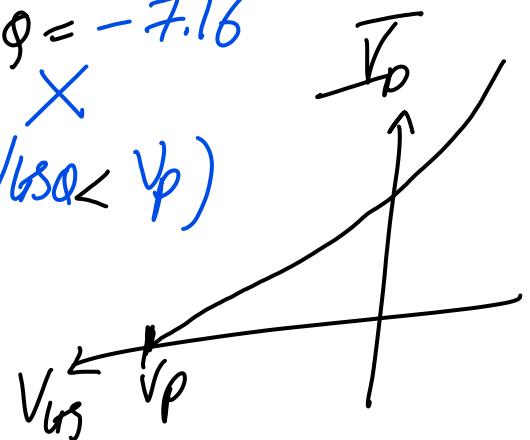
!

$(V_{GSQ} > V_p)$

$V_{GSQ} = -0.8377 \text{ V}$

$$V_{GSQ} = -7.16$$

~~$(V_{GSQ} < V_p)$~~



$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GSQ}}{V_p}\right)^2$$

$$I_{DQ} = 6 \text{ mA} \left(1 - \frac{(-0.8377)}{(-3)}\right)^2$$

$I_{DQ} = 3.11 \text{ mA}$

$$V_{DSQ} = V_{DD} - I_D (R_s + R_o) = 18 - 3.11 \text{ mA} (750 + 1.8 \text{ k})$$

$V_{DSQ} = 10.07 \text{ V}$











