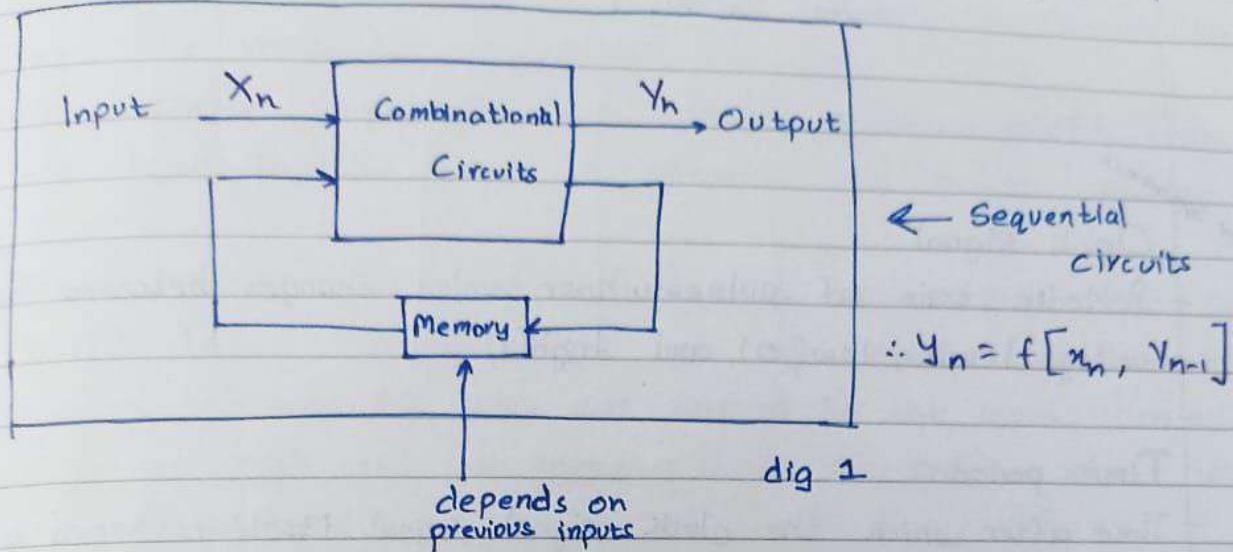


# Sequential Circuits

Date : \_\_\_\_\_

outputs depend on the present inputs and past inputs/outputs



## Sequential circuits

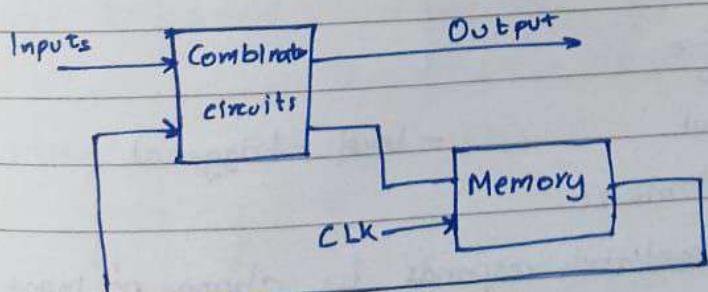
### Synchronous

circuits  
↓  
responds to the  
inputs only at  
discrete time interval

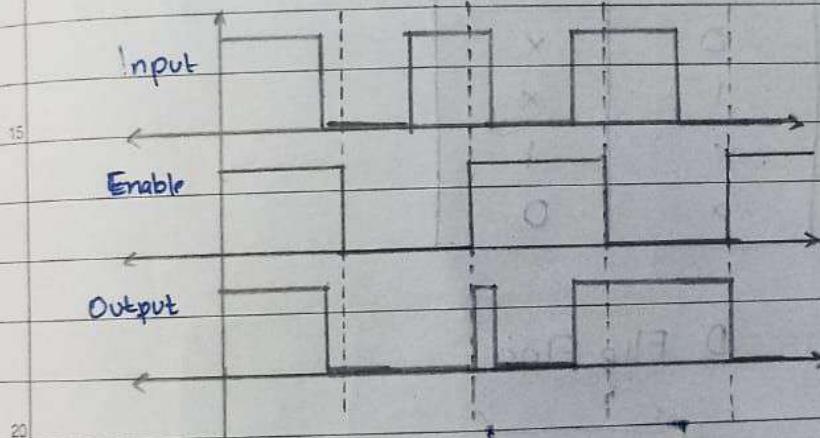
### Asynchronous

circuits  
↓  
immediately responds  
to input level changes

## ► Synchronous sequential circuits



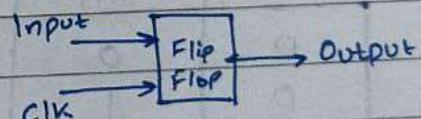
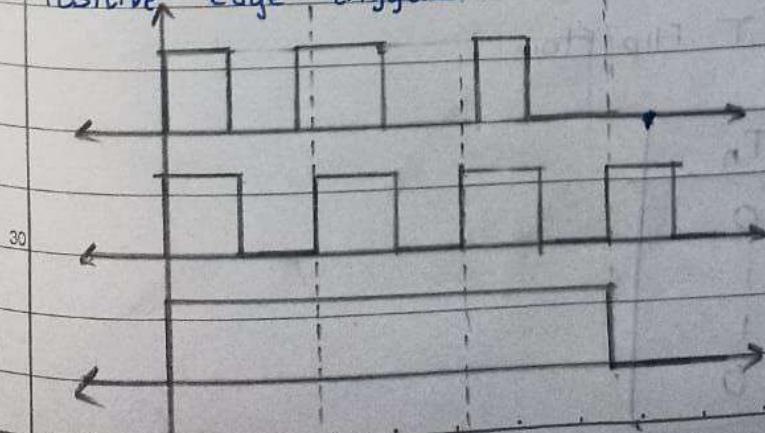
- In Gated latch
  - . When enable input is high, Latch becomes transparent to the input i.e responds immediately to input.
  - . When enable input is low, Latch becomes doesn't respond to the input, In this case it retains its previous state.
- When periodic clock signal to this enable input then same gated latch can be used as synchronous gated latch memory element. As latch will respond to the input, when clock signal is high and will remain in its previous state when clock signal is low.



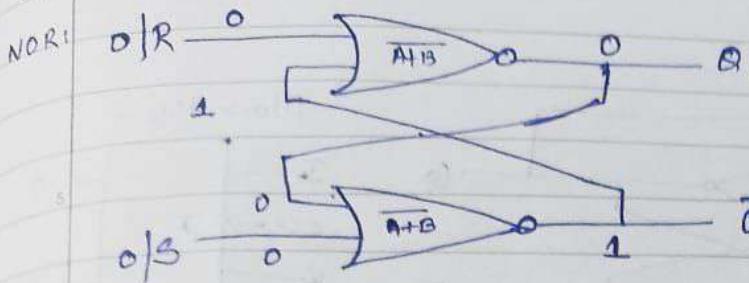
### Flip flop

- responds to input only at clock transitions
- edge triggered : At rising edge: Positive edge triggered  
At falling edge: Negative edge triggered.

- Positive edge triggered FF



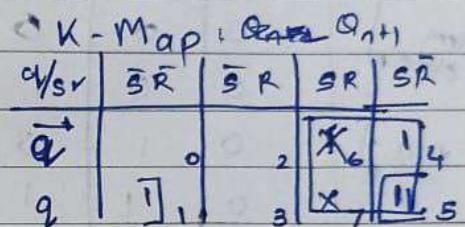
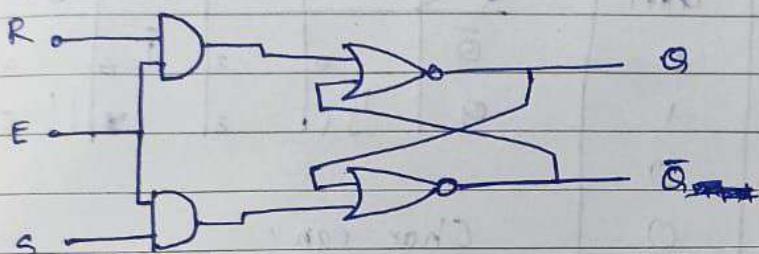
## SR Latch



Truth table

| S | R | $Q_n$ | $Q_{n+1}$          |
|---|---|-------|--------------------|
| 0 | 0 | 0     | 0                  |
| 0 | 1 | 1     | 1                  |
| 1 | 0 | 0     | 0                  |
| 1 | 1 | 1     | 0                  |
|   |   |       | g <sub>mem</sub>   |
|   |   |       | g <sub>0</sub>     |
|   |   |       | g <sub>1</sub>     |
|   |   |       | g <sub>raise</sub> |
|   |   |       | x                  |

## SR Flip Flop

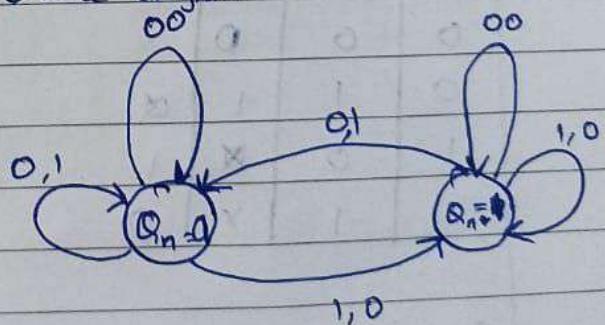


## Function table

| S | R | $Q_{n+1}$ |
|---|---|-----------|
| 0 | 0 | 0         |
| 0 | 1 | 0         |
| 1 | 0 | 1         |
| 1 | 1 | x         |

∴ We get Char. Equation  
 $Q_{n+1} = S + R' Q_n$

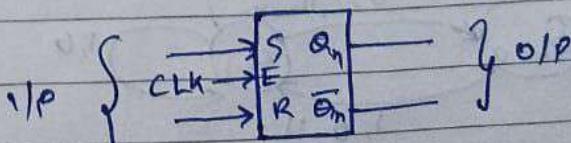
## State diagram:

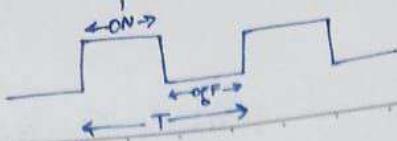


## Excitation table

| $Q_n$ | $Q_{n+1}$ | S | R |              |
|-------|-----------|---|---|--------------|
| 0     | 0         | 0 | x | → Don't care |
| 0     | 1         | 1 | 0 |              |
| 1     | 0         | 0 | 1 |              |
| 1     | 1         | x | 0 |              |

## Block diagram:





Date : \_\_\_\_\_

Asynchronous sequential circuits  
same as dig 1

for synchronous

Clock signal

- Periodic train of pulses, whose value changes between two voltage levels, low(0) and high(1)

Time period

- Time after which the clock signal repeats itself is known as Time period

Duty cycle

- Ratio of ON time to the total time period

- If Duty cycle = 50%, then ON = OFF

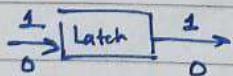
< 50% ON < OFF

> 50% ON > OFF

Memory element (1-bit info)

latch

Flip-Flops



Latch

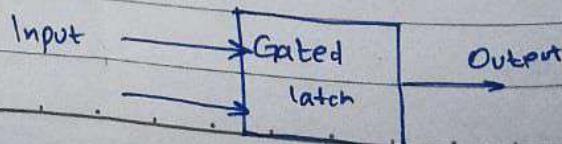
- responds immediately to input

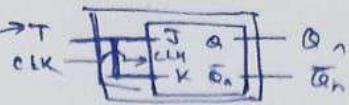
- level triggered

- Asynchronous memory element

- type of latch which immediately responds to change of input are called transparent latch

Latch that becomes transparent based on control input are known as gated latch





Date: \_\_\_\_\_

### Toggle Flip-Flop

T.T

|   | $Q_n$ | $Q_{n+1}$ |
|---|-------|-----------|
| T | 0     | 0         |
| D | 0     | 0         |
| O | 1     | 1         |
| I | 0     | 1         |
| 1 | 1     | 0         |

K-Map:

|           |   |           |   |
|-----------|---|-----------|---|
| $\bar{Q}$ | T | $\bar{T}$ | T |
| $\bar{Q}$ | 1 | 0         | 1 |
| Q         | 2 | 1         | 1 |
| Q         | 3 | 2         | 0 |

char eq,  
 $Q_{n+1} = T \oplus Q_n$

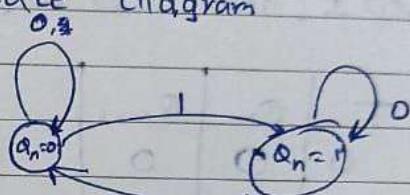
Function table

| T | $Q_{n+1}$   |
|---|-------------|
| 1 | $Q_n$       |
| 0 | $\bar{Q}_n$ |

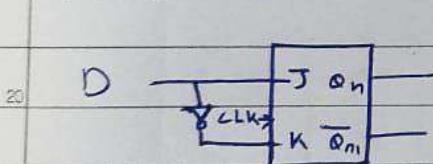
Excitation table

| $Q_n$ | $Q_{n+1}$ | T |
|-------|-----------|---|
| 0     | 0         | 0 |
| 0     | 1         | 1 |
| 1     | 0         | 1 |
| 1     | 1         | 0 |

State diagram



### Delay FF



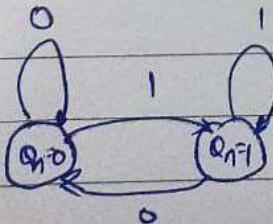
TT

| D | $Q_n$ | $Q_{n+1}$ |  | K-Map         |
|---|-------|-----------|--|---------------|
| 0 | 0     | 0         |  | $Q_{n+1} = D$ |
| 0 | 1     | 0         |  |               |
| 1 | 0     | 1         |  |               |
| 1 | 1     | 1         |  |               |

Excitation table

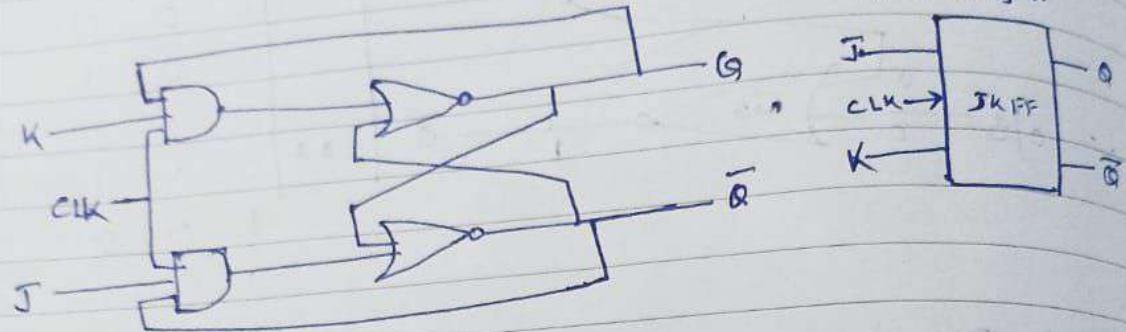
| $Q_n$ | $Q_{n+1}$ | D |
|-------|-----------|---|
| 0     | 0         | 0 |
| 0     | 1         | 1 |
| 1     | 0         | 0 |
| 1     | 1         | 1 |

30



→ consists of almost all functionalities i.e mem elem set, reset, complement  
Date: \_\_\_\_\_

### JK Flip Flop



Truth table

|          | J | K | $Q_n$ | $Q_{n+1}$ |
|----------|---|---|-------|-----------|
| mem elem | 0 | 0 | 0     | 0         |
| reset    | 0 | 0 | 1     | 1         |
| Set      | 0 | 1 | 0     | 0         |
| Toggle   | 0 | 1 | 1     | 0         |
|          | 1 | 0 | 0     | 1         |
|          | 1 | 0 | 1     | 1         |
|          | 1 | 1 | 0     | 1         |
|          | 1 | 1 | 1     | 0         |

K Map

| JK | JK' | JK | JK' | JK | JK' |
|----|-----|----|-----|----|-----|
| Q  | Q̄  | Q̄ | Q   | Q  | Q̄  |
| Q̄ | Q   | Q  | Q̄  | Q̄ | Q   |
| 1  | 1   | 0  | 0   | 2  | 1   |
| 0  | 0   | 1  | 1   | 3  | 0   |
| 1  | 0   | 0  | 1   | 4  | 1   |
| 0  | 1   | 1  | 0   | 5  | 0   |

Char eqn:

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

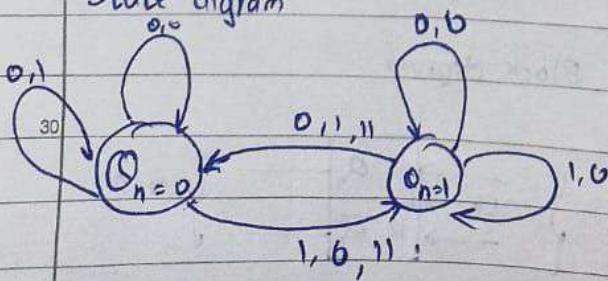
Function table:

| J | K | $Q_{n+1}$   | $Q_n$ |
|---|---|-------------|-------|
| 0 | 0 | $Q_n$       |       |
| 0 | 1 | 0           |       |
| 1 | 0 | 1           |       |
| 1 | 1 | $\bar{Q}_n$ |       |

Excitation table

| $Q_n$ | $Q_{n+1}$ | J | K |
|-------|-----------|---|---|
| 0     | 0         | 0 | X |
| 0     | 1         | 1 | X |
| 1     | 0         | X | 1 |
| 1     | 1         | X | 0 |

State diagram



## FF conversion

Steps

- i TT of target FF
- ii Excitation table of given FF
- iii Determine excitation value of target FF from TT
- iv Obtain expression for input of given FF in terms of Target

Q. Convert D FF to T FF

→ Step 1; Truth Table of T FF

| T | $Q_n$ | $Q_{n+1}$ |
|---|-------|-----------|
| 0 | 0     | 0         |
| 0 | 1     | 1         |
| 1 | 0     | 1         |
| 1 | 1     | 0         |

Step 2: Excitation table of D FF

| $Q_n$ | $Q_{n+1}$ | D |
|-------|-----------|---|
| 0     | 0         | 0 |
| 0     | 1         | 1 |
| 1     | 0         | 0 |
| 1     | 1         | 1 |

Step 3: <sup>merge</sup> Excitation table of T FF & TT of T FF

| T | $Q_n$ | $Q_{n+1}$ | D |
|---|-------|-----------|---|
| 0 | 0     | 0         | 0 |
| 0 | 1     | 1         | 1 |
| 1 | 0     | 1         | 1 |
| 1 | 1     | 0         | 0 |

— Table 1

Step 4 : To obtain simplified exp

From table ①

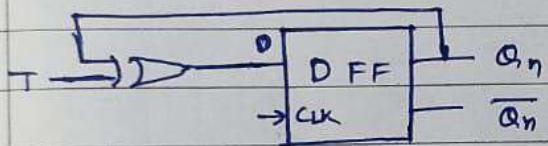
K-Map

| T | $Q_n$ | D |
|---|-------|---|
| 0 | 0     | 0 |
| 0 | 1     | 1 |
| 1 | 0     | 1 |
| 1 | 1     | 0 |

| $\bar{Q}_n$ | T | $\bar{T}$ | T |
|-------------|---|-----------|---|
| 0           | 0 | 1         | 2 |
| 1           | 1 | 1         | 3 |

$$D = T \oplus Q_n \quad \text{EX-OR}$$

∴ We get



Q Convert T FF to JK FF

→ i) T-T of JK FF      ii) - Excitation table of T FF

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|-------|-----------|
| 0 | 0 | 0     | 0         |
| 0 | 1 | 1     | 1         |
| 0 | 1 | 0     | 0         |
| 0 | 1 | 1     | 0         |

| $Q_n$ | $Q_{n+1}$ | T |
|-------|-----------|---|
| 0     | 0         | 0 |
| 0     | 1         | 1 |
| 1     | 0         | 1 |
| 1     | 1         | 0 |

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|-------|-----------|
| 1 | 0 | 1     | 1         |
| 1 | 1 | 0     | 0         |
| 1 | 1 | 1     | 0         |

| J | K | $Q_n$ | $Q_{n+1}$ | T |
|---|---|-------|-----------|---|
| 0 | 0 | 0     | 0         | 0 |
| 0 | 0 | 1     | 1         | 0 |
| 0 | 1 | 1     | 0         | 1 |
| 1 | 0 | 0     | 1         | 1 |
| 1 | 0 | 1     | 1         | 0 |
| 1 | 1 | 0     | 1         | 1 |
| 1 | 1 | 1     | 0         | 0 |

## Flip-Flops

i) Excitation table of SR Flip Flop

| outputs |           | inputs |   |
|---------|-----------|--------|---|
| $Q_n$   | $Q_{n+1}$ | S      | R |
| 0       | 0         | 0      | X |
| 0       | 1         | 1      | 0 |
| 1       | 0         | 0      | 1 |
| 1       | 1         | X      | 0 |

ii) Excitation tables of JK Flip Flop

| outputs |           | inputs |       |
|---------|-----------|--------|-------|
| $Q_n$   | $Q_{n+1}$ | $J_n$  | $K_n$ |
| 0       | 0         | 0      | X     |
| 0       | 1         | 1      | X     |
| 1       | 0         | X      | 1     |
| 1       | 1         | X      | 0     |

iii) Excitation tables of D Flip Flop

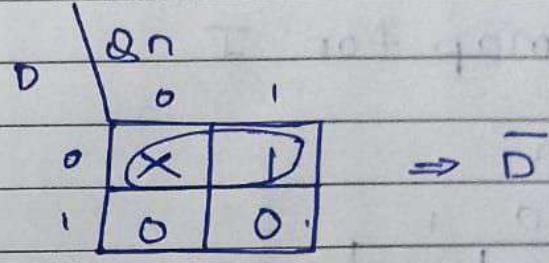
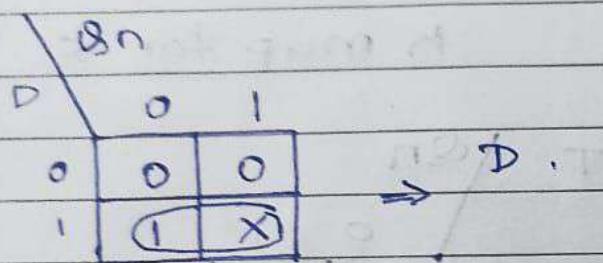
| $Q_n$ | $Q_{n+1}$ | $D_n$ |
|-------|-----------|-------|
| 0     | 0         | 0     |
| 0     | 1         | 1     |
| 1     | 0         | 0     |
| 1     | 1         | 1     |

iv) Excitation tables of T Flip Flop

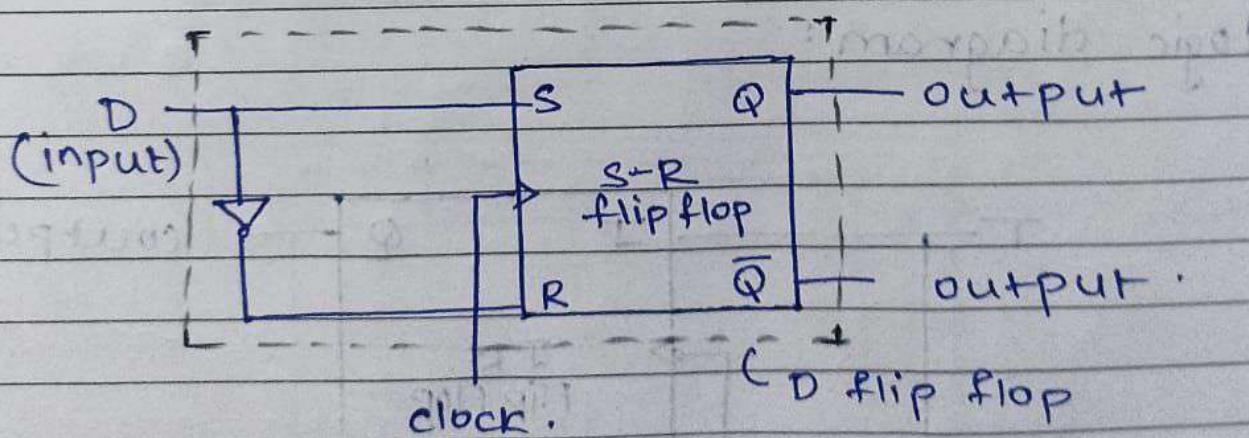
| $Q_n$ | $Q_{n+1}$ | $T_n$ |
|-------|-----------|-------|
| 0     | 0         | 0     |
| 0     | 1         | 1     |
| 1     | 0         | 1     |
| 1     | 1         | 0     |

① SR Flip Flop to D Flip Flop.

| D | B <sub>n</sub> | Q <sub>n+1</sub> | S | R |
|---|----------------|------------------|---|---|
| 0 | 0              | 0                | 0 | X |
| 1 | 0              | 1                | 1 | 0 |
| 0 | 1              | 0                | 0 | 1 |
| 1 | 1              | 1                | X | 0 |



Logic diagram.

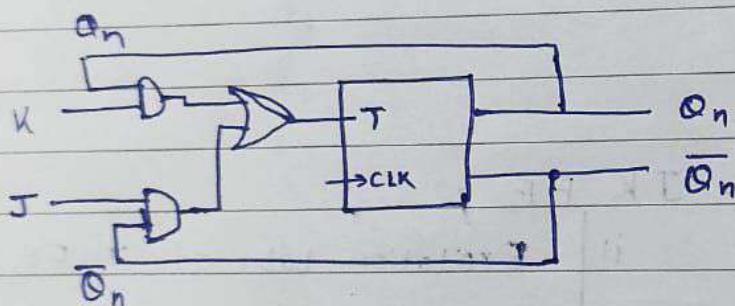


iv To obtain exp

| J | K | $Q_n$ | T |
|---|---|-------|---|
| 0 | 0 | 0     | 0 |
| 0 | 0 | 1     | 0 |
| 0 | 1 | 0     | 0 |
| 0 | 1 | 1     | 1 |
| 1 | 0 | 0     | 1 |
| 1 | 0 | 1     | 0 |
| 1 | 1 | 0     | 1 |
| 1 | 1 | 1     | 1 |

| $\bar{J} \bar{K}$ | $\bar{J} K$ | $J \bar{K}$ | $J K$ |
|-------------------|-------------|-------------|-------|
| 0                 | 0           | 1           | 0     |
| 1                 | 1           | 0           | 1     |
| 0                 | 1           | 1           | 0     |
| 1                 | 0           | 0           | 1     |

$$T = \bar{J} \bar{Q} + K Q$$



### Race-around Condition (only in JK FF)

- When the value of J and K are 1 and the clock is level triggered (positive/negative) and On time of the clock is more than its propagation delay i.e  $T_{on} \gg T_{pd}$
- therefore due to the feedback from the output to input the FF will toggle continuously
- Can be avoided :
  - by using edge triggered JK FF
  - by using master-slave FF

### 3@ SR to T Flip Flop.

T       $Q_n$        $Q_{n+1}$       S      R.

|   |   |   |   |   |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | x |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | x | 0 |

K map for S

| T | Q <sub>n</sub> | 0 | 1 |
|---|----------------|---|---|
| 0 | 0              | x |   |
| 1 | 1              | 0 | 0 |

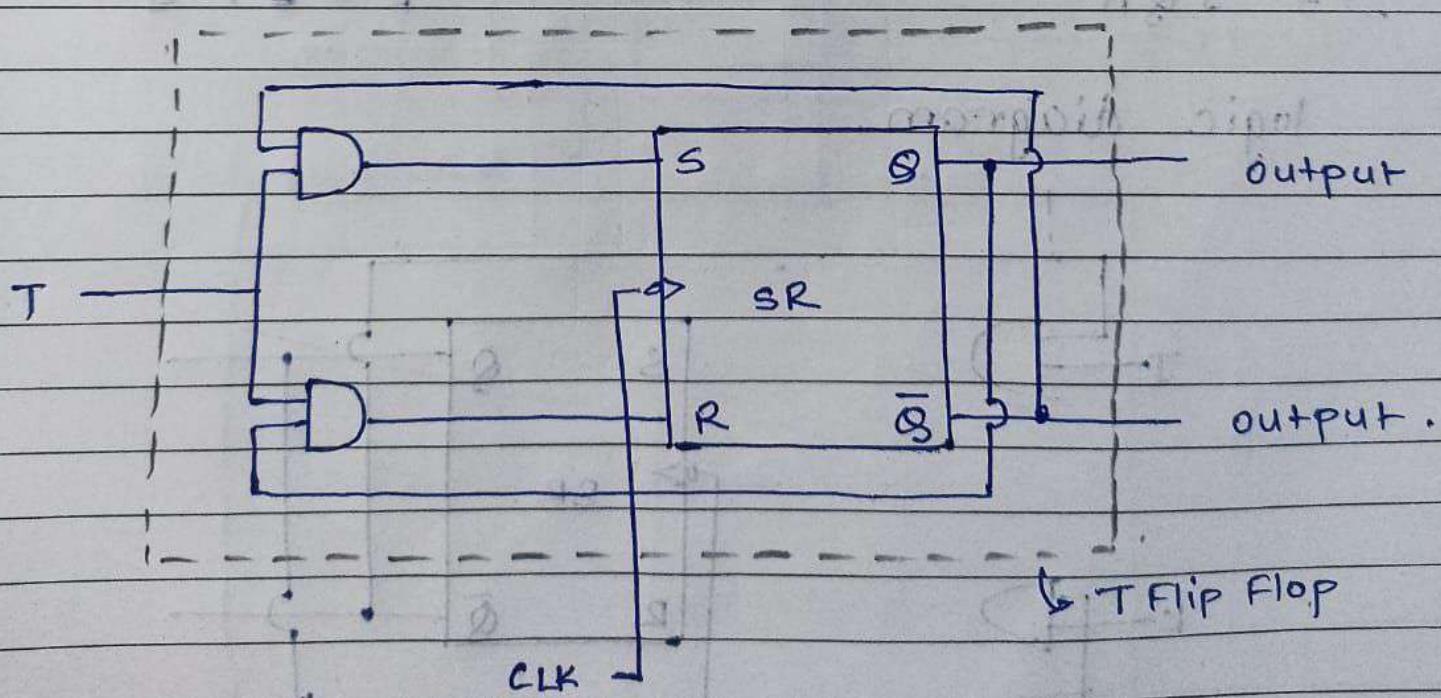
$$S = T \cdot Q_n$$

K map for R

| T | Q <sub>n</sub> | 0 | 1 |
|---|----------------|---|---|
| 0 | x              | 0 |   |
| 1 | 0              | 0 | 1 |

$$R = \bar{T} \cdot Q_n$$

logic diagram:



## 4(x) SR to JK Flip Flop

| J     | K   | $Q_n$ | $Q_{n+1}$ | S | R |
|-------|-----|-------|-----------|---|---|
| 0     | X 0 | 0     | 0         | 0 | X |
| 0     | X 1 | 0     | 0         | 0 | X |
| 1     | X 0 | 0     | 1         | 1 | 0 |
| 1     | X 1 | 0     | 1         | 1 | 0 |
| (0) X | 1   | 1     | 0         | 0 | 1 |
| (1) X | 1   | 1     | 0         | 0 | 1 |
| (0) X | 0   | 1     | 1         | X | 0 |
| (1) X | 0   | 1     | 1         | X | 0 |

$K Q_n.$

| J | 00 | 01 | 11 | 10 |
|---|----|----|----|----|
| 0 | 0  | X  | 0  | 0  |
| 1 | X  | 0  | 0  | 0  |

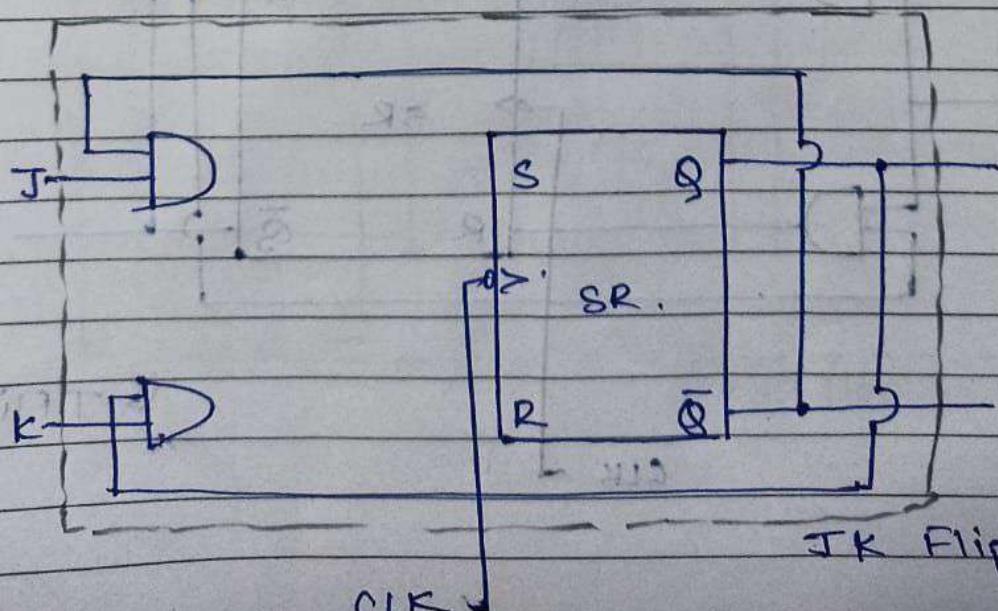
$J \backslash K Q_n$

| J | 00 | 01 | 11 | 10 |
|---|----|----|----|----|
| 0 | X  | 0  | 0  | X  |
| 1 | 0  | 0  | 0  | 0  |

$$S = J \bar{Q}_n$$

$$R = \bar{K} Q_n$$

logic diagram.



2)

JK → T

Flip Flop.

| T | $Q_n$ | $Q_{n+1}$ | J | K |
|---|-------|-----------|---|---|
| 0 | 0     | 0         | 0 | X |
| 1 | 0     | 1         | 1 | X |
| 1 | 1     | 0         | X | 1 |
| 0 | 1     | 1         | X | 0 |

Kmap for J

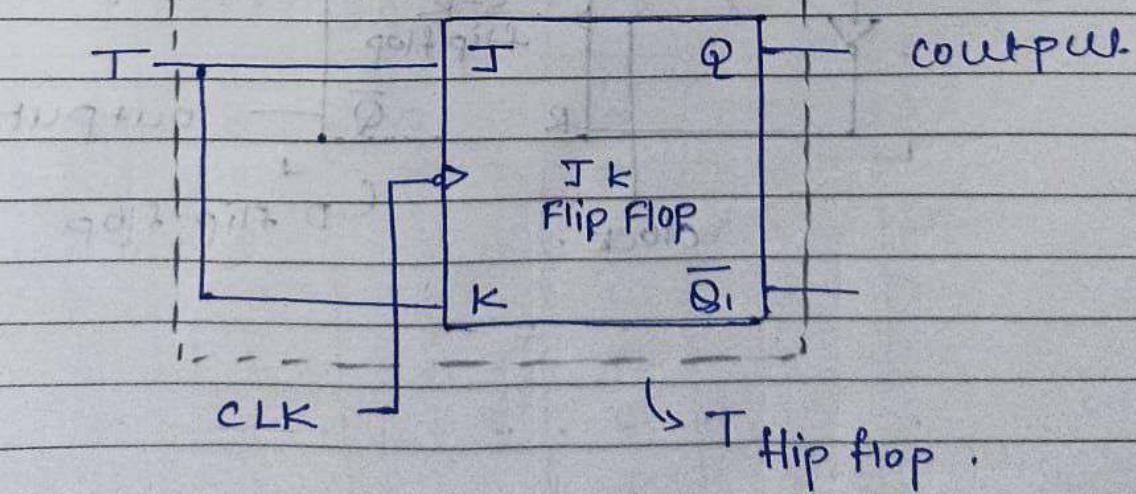
| T | $Q_n$ | 0   | 1   |
|---|-------|-----|-----|
| 0 | 0     | 0   | X   |
| 1 | 1     | (1) | (X) |

$$= T$$

| T | $Q_n$ | 0   | 1 |
|---|-------|-----|---|
| 0 | X     | 0   | 0 |
| 1 | (X)   | (1) | 0 |

$$= T$$

Logic diagram:



6\*) Convert T Flip Flop to D Flip Flop.

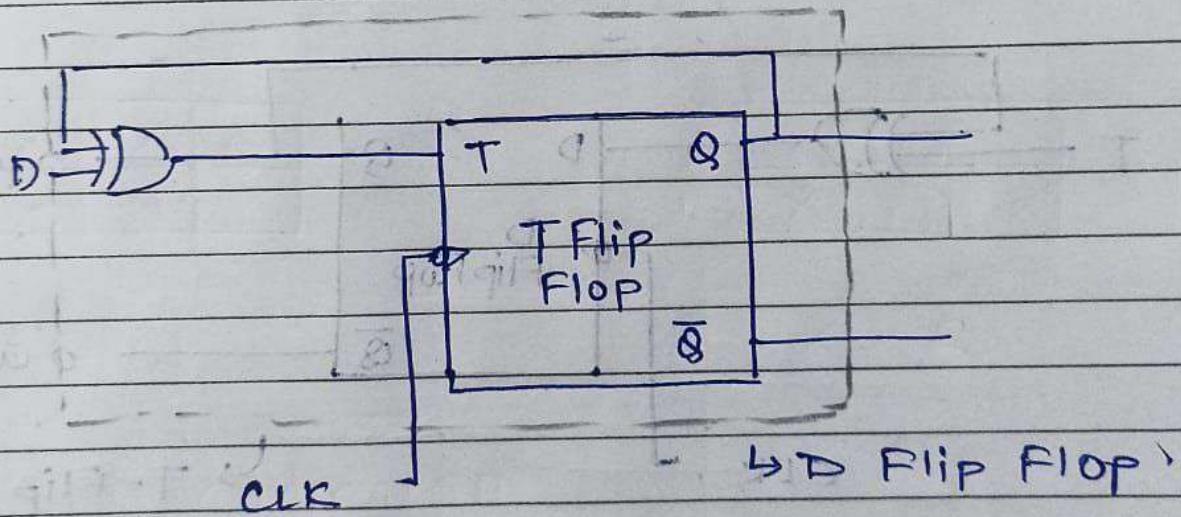
| D | $Q_n$ | $Q_{n+1}$ | T |
|---|-------|-----------|---|
| 0 | 0     | 0         | 0 |
| 1 | 0     | 1         | 1 |
| 0 | 1     | 0         | 1 |
| 1 | 1     | 1         | 0 |

$D \quad Q_n$

|   |   |   |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |

$$T = D \bar{Q}_n + \bar{D} Q_n$$

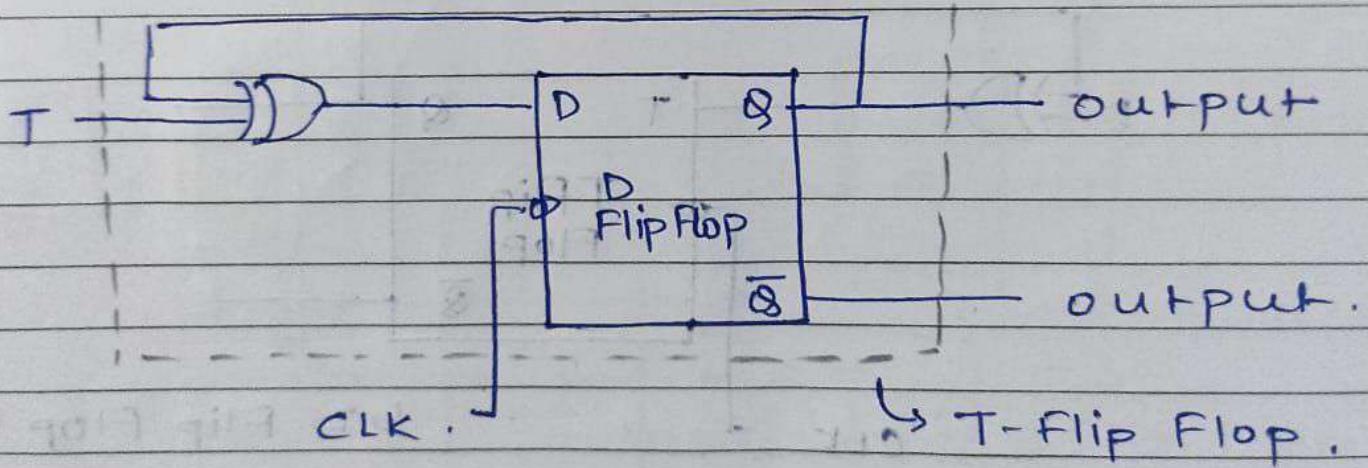
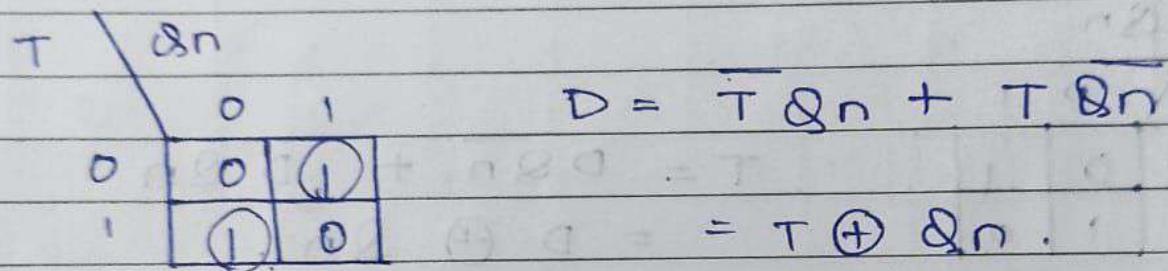
$$= D \oplus Q_n$$



## 5) D Flip Flop to T Flip Flop

| T | $Q_n$ | $Q_{n+1}$ | D |
|---|-------|-----------|---|
| 0 | 0     | 0         | 0 |
| 1 | 0     | 1         | 1 |
| 1 | 1     | 0         | 0 |
| 0 | 1     | 1         | 1 |

K map for output D.



8 (a) JK to SR Flip Flop

| S | R | J | Q <sub>n+1</sub> | J | K |
|---|---|---|------------------|---|---|
| 0 | 0 | 0 | 0                | 0 | X |
| 0 | 1 | 0 | 0                | 0 | X |
| 1 | 0 | 0 | 1                | 1 | X |
| 1 | 0 | 0 | 1                | 1 | X |
| 0 | 1 | 1 | 0                | X | J |
| 0 | 1 | 1 | 0                | X | J |
| 0 | 0 | 1 | 1                | X | 0 |
| 1 | 0 | 1 | 1                | X | 0 |

'J'

'K'

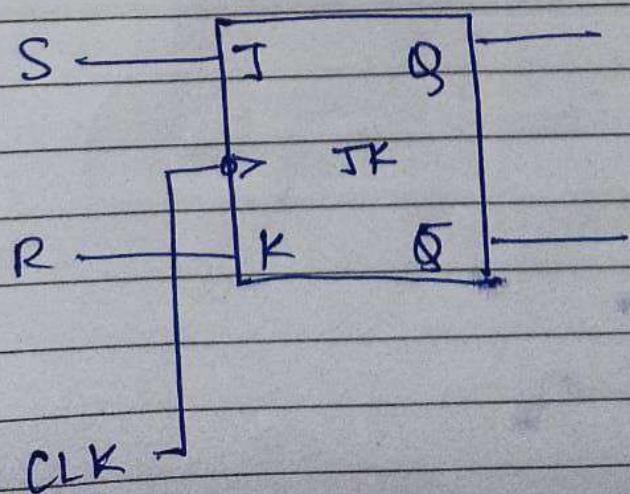
| R & S |   | Q <sub>n</sub> | J = S |
|-------|---|----------------|-------|
| S     | R | Q <sub>n</sub> | J = S |
| 0     | 0 | 0              | 0     |
| 1     | X | X              | X     |

| R & S |   | Q <sub>n</sub> | J = S |
|-------|---|----------------|-------|
| S     | R | Q <sub>n</sub> | J = S |
| 0     | 0 | 0              | 0     |
| 1     | X | 0              | 1     |

J = S

K = R

logic diagram

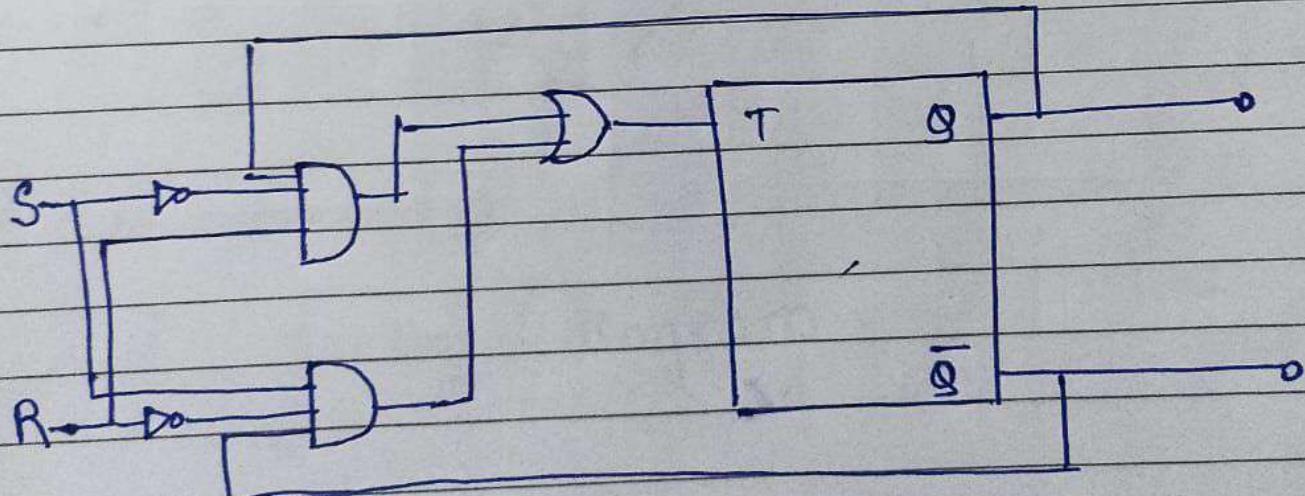


9(\*) T to SR.

| S      | R      | Q | $Q_{n+1}$ | T |
|--------|--------|---|-----------|---|
| 0      | $x(0)$ | 0 | 0         | 0 |
| 1      | 0      | 0 | 1         | 1 |
| 0      | 1      | 1 | 0         | 1 |
| $x(0)$ | 0      | 1 | 1         | 0 |

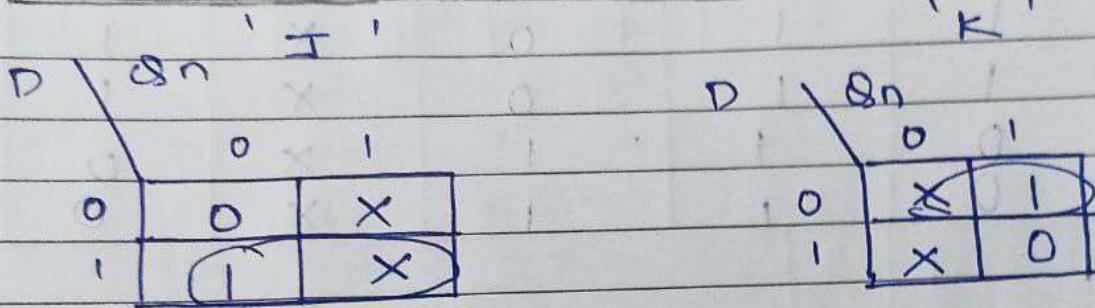
| FQ |   | 00 | 01 | 11 | 10 |
|----|---|----|----|----|----|
| S  | R | 0  | 0  | 1  | 0  |
| 0  | 0 | 1  | 0  | 1  | 0  |
| 1  | 1 | 0  | 0  | 0  | 0  |

$$T = \overline{S} \overline{R} Q + \overline{S} R \bar{Q} .$$



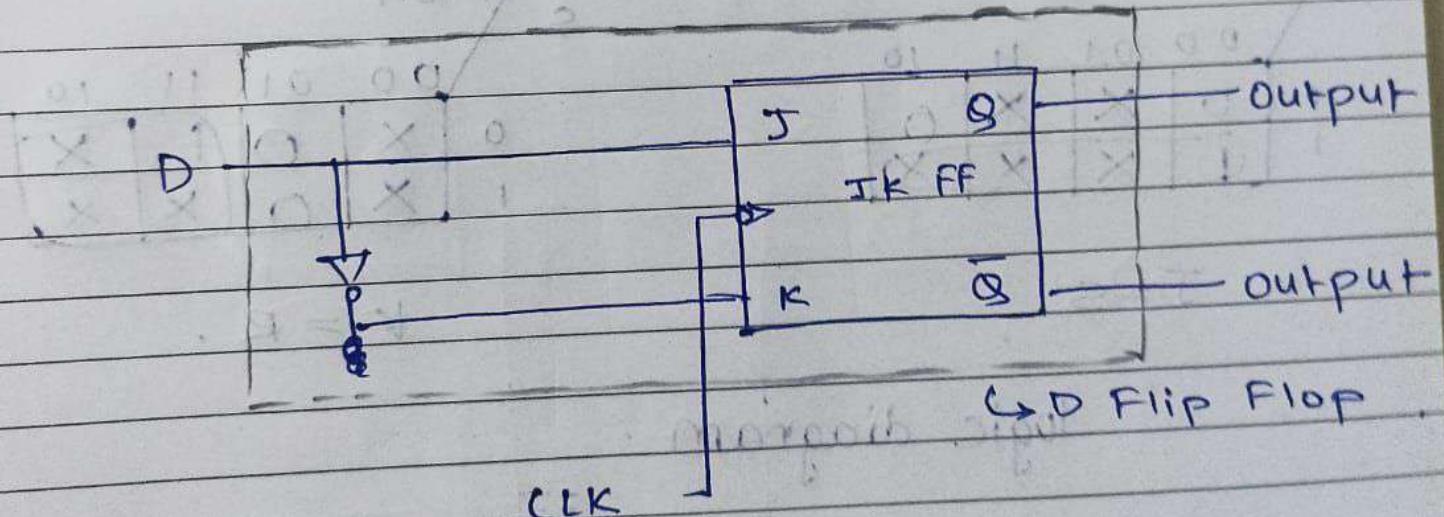
7\*) JK to D.

| D | $Q_n$ | $Q_{n+1}$ | J | K |
|---|-------|-----------|---|---|
| 0 | 0     | 0         | 0 | x |
| 1 | 0     | 1         | 1 | x |
| 0 | 1     | 0         | x | 1 |
| 1 | 1     | 1         | x | 0 |



$$J = D$$

$$K = \bar{D}$$



⑪ \* D to SR

| S     | R      | Q | $Q_{n+1}$ | D |
|-------|--------|---|-----------|---|
| 0     | $D(x)$ | 0 | 0         | 0 |
| 1     | 0      | 0 | 1         | 1 |
| 0     | 1      | 1 | 0         | 0 |
| (x) 0 | 0      | 1 | 1         | 1 |

| S | R | Q, $Q_{n+1}$ | D |
|---|---|--------------|---|
| 0 | X |              |   |
| 1 | X |              |   |
| 0 | 0 |              |   |
| X | 1 |              |   |
| X | 0 |              |   |

| S | R | Q | $Q_n$ | D |
|---|---|---|-------|---|
| 0 | 0 | 0 | 0     | 0 |
| 0 | 1 | 0 | 0     | 0 |
| 1 | 0 | 0 | 1     | 1 |
| 1 | 0 | 0 | 1     | 1 |
| 0 | 1 | 1 | 0     | 0 |
| 0 | 1 | 1 | 0     | 0 |
| 0 | 0 | 1 | 1     | 1 |
| 1 | 0 | 1 | 1     | 1 |

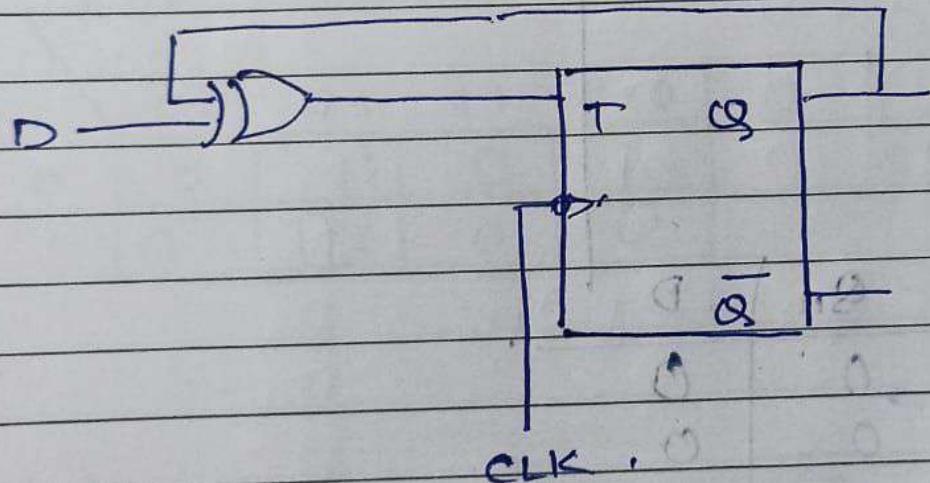
10\*) T to D.

| D | S | $Q_n$ | T |
|---|---|-------|---|
| 0 | 0 | 0     | 0 |
| 1 | 0 | 1     | 1 |
| 0 | 1 | 0     | 1 |
| 1 | 1 | 1     | 0 |

$Q_n$

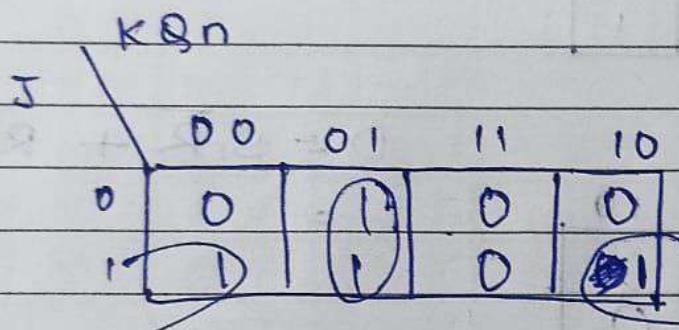
|   |   |   |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

$$T = D \oplus Q_n$$

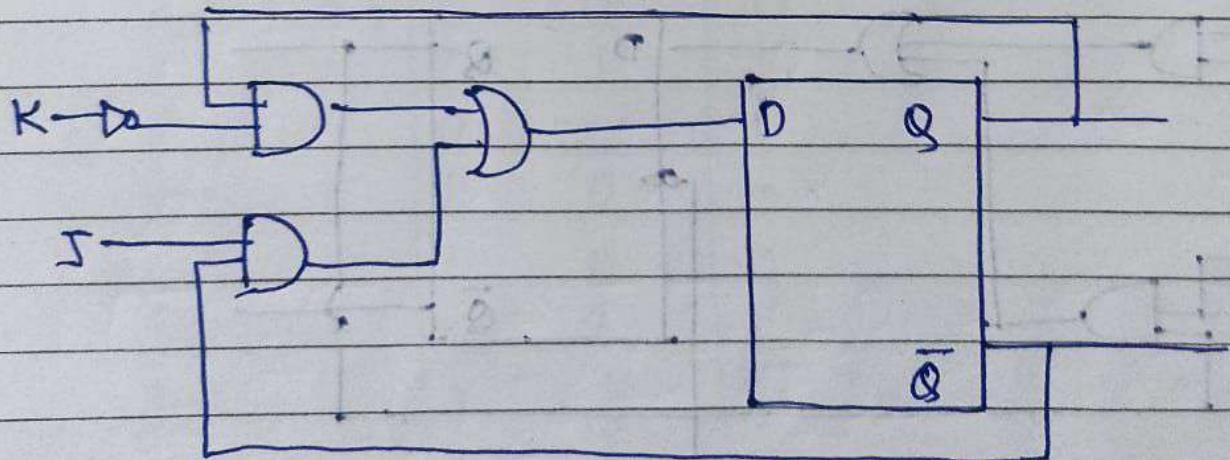


\* D to JK.

| J  | K | S | $Q_n$ | D |
|----|---|---|-------|---|
| 0  | X | 0 | 0     | 0 |
| 0  | X | 1 | 0     | 0 |
| 1  | X | 0 | 0     | 1 |
| 1  | X | 1 | 0     | 1 |
| 0X | 1 | 1 | 0     | 0 |
| 1X | 1 | 1 | 0     | 0 |
| 0X | 0 | 1 | 1     | 1 |
| 1X | 0 | 1 | 1     | 0 |



$$D = \bar{K}Q_n + JQ_n$$

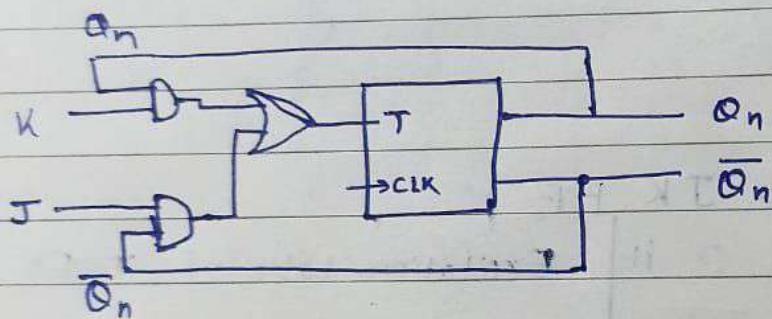


iv To obtain exp

| J | K | $Q_n$ | T |
|---|---|-------|---|
| 0 | 0 | 0     | 0 |
| 0 | 0 | 1     | 0 |
| 0 | 1 | 0     | 0 |
| 0 | 1 | 1     | 1 |
| 1 | 0 | 0     | 1 |
| 1 | 0 | 1     | 0 |
| 1 | 1 | 0     | 1 |
| 1 | 1 | 1     | 1 |

|             | $\bar{J}\bar{K}$ | $\bar{J}K$ | $J\bar{K}$ | $JK$ |
|-------------|------------------|------------|------------|------|
| $\bar{Q}_n$ | 0                | 1          | 1          | 0    |
| $Q_n$       | 1                | 0          | 0          | 1    |
| $\bar{Q}_n$ | 1                | 1          | 0          | 1    |
| $Q_n$       | 0                | 0          | 1          | 0    |

$$T = \bar{J}\bar{Q} + KQ$$



Race-around Condition (only in JK FF)

- When the value of J and K are 1 and the clock is level triggered (positive/negative) and On time of the clock is more than its propagation delay i.e  $T_{on} \gg T_{pd}$
- therefore due to the feedback from the output to input the FF will toggle continuously
- Can be avoided :
  - by using edge triggered JK FF
  - by using master-slave FF

(K 12)

D + JK

| J     | K     | Q | $Q_n$ | D. |
|-------|-------|---|-------|----|
| 0     | 0 (X) | 0 | 0     | 0  |
| 1     | 1 (X) | 0 | 1     | 1  |
| (X) 0 | 1     | 1 | 0     | 0  |
| (X) 1 | 0     | 1 | 1     | 1  |

J K Q

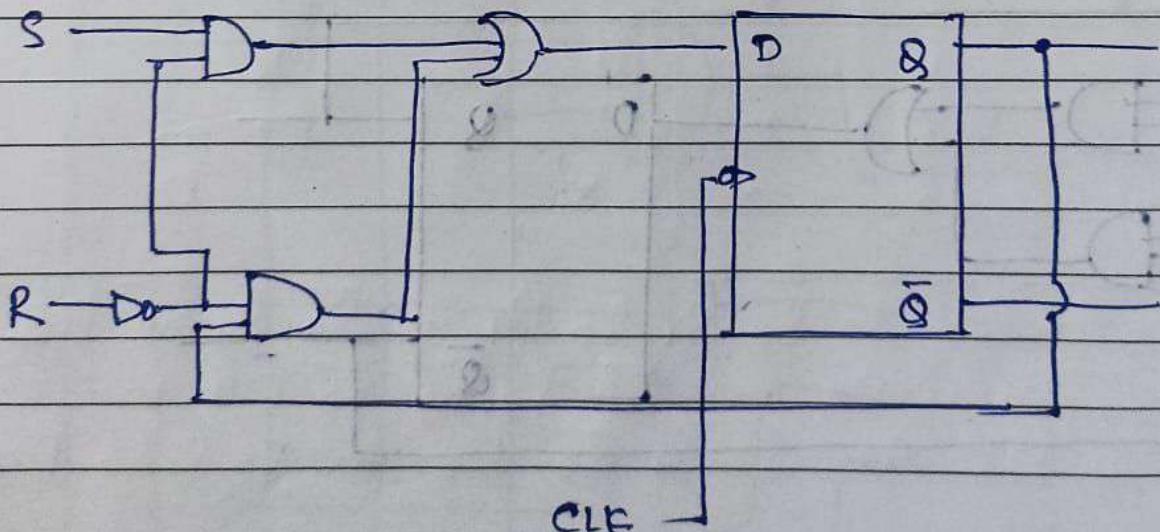
|   | 00 | 01 | 11 | 10 |
|---|----|----|----|----|
| 0 | 0  | 0  | 0  | 1  |
| 1 | 1  | 1  | 1  | 1  |

S R  $Q_n$

|   | 00 | 01 | 11 | 10 |
|---|----|----|----|----|
| 0 | 0  | 0  | 0  | 0  |
| 1 | 1  | 0  | 0  | 0  |

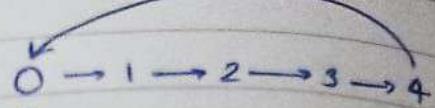
$$D = S \bar{R} + \bar{R} Q_n$$

$$S \bar{R} + \bar{R} Q_n = 0$$



Q. Mod 5 asynchronous counter

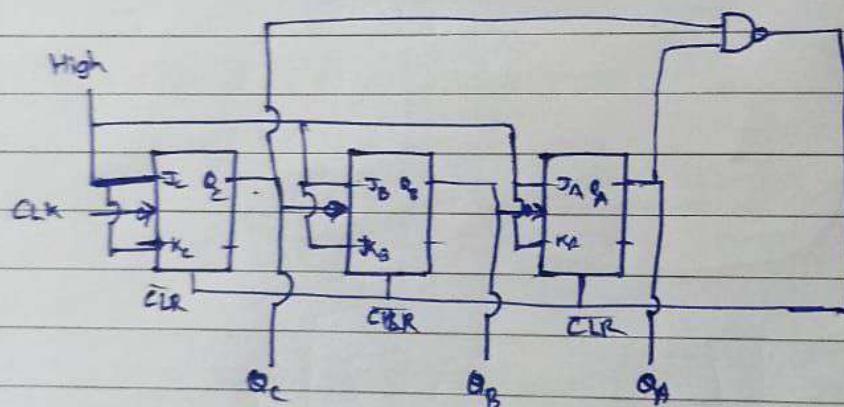
Step 1: No. of JK FF required =  $2^3$   
= 8 as 5 states



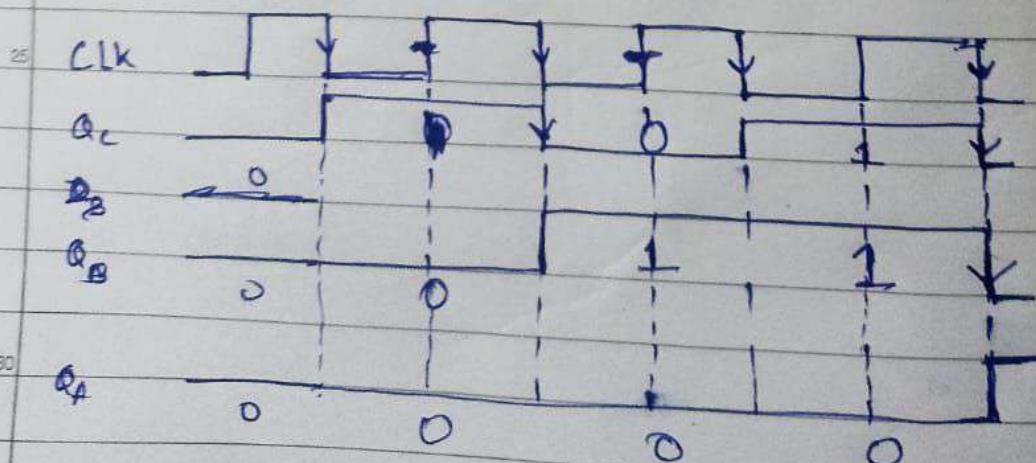
Step 2: Truth table

| CLK | $Q_A$ | $Q_B$ | $Q_C$ | Output |     |
|-----|-------|-------|-------|--------|-----|
|     |       |       |       | Reset  | Set |
| 0   | 0     | 0     | 0     | 1      |     |
| 1   | 0     | 0     | 1     |        | 1   |
| 1   | 0     | 1     | 0     |        |     |
| 1   | 0     | 1     | 1     |        |     |
| 1   | 1     | 0     | 0     |        |     |
|     | 1     | 1     | 0     | 1      |     |

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|-------|-----------|
| 0 | x | 0     | 0         |
| 1 | x | 0     | 1         |
| x | 1 | 1     | 0         |
| x | 0 | 1     | 1         |



Timing diagram

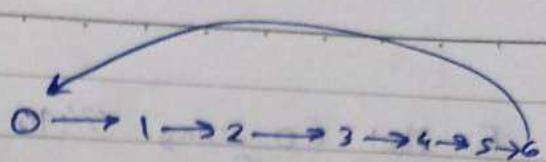


Date : \_\_\_\_\_

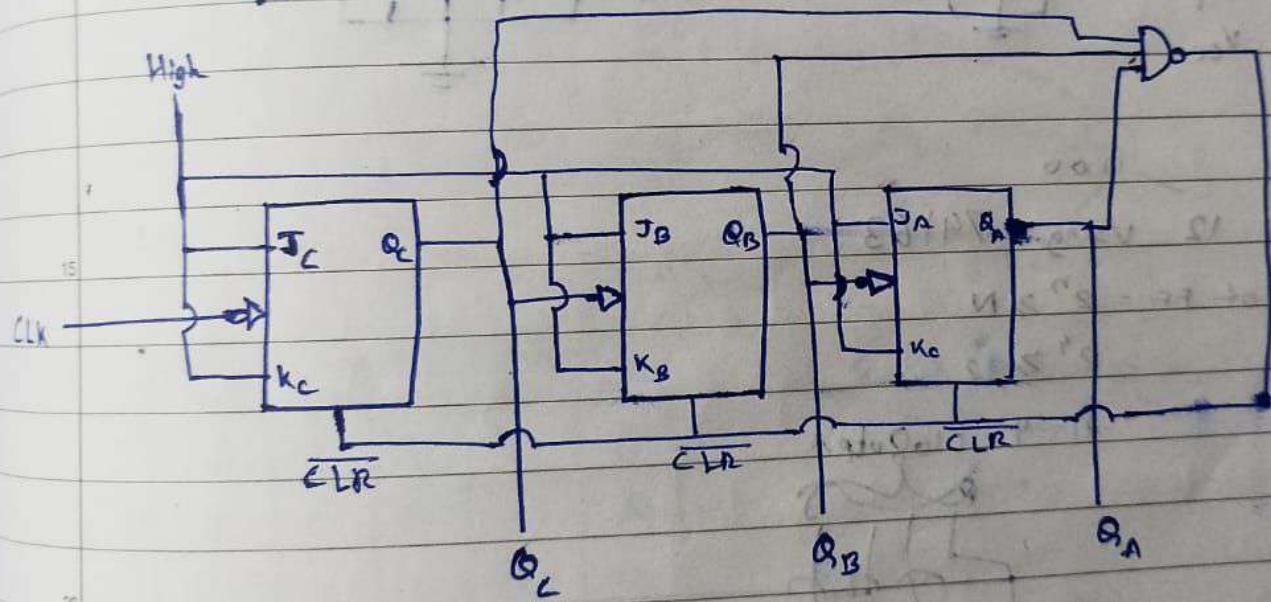
Q. Mod 7 asynchronous counter

No of JK FF  $\sim 2^3$

= 8 as 7 states required



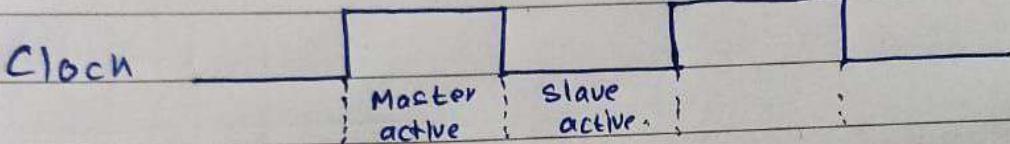
| $Q_n$ | $Q_{n+1}$ | J | K |
|-------|-----------|---|---|
| 0     | 0 ; 0     | 0 | X |
| 0     | 1         | 1 | X |
| 1     | 0         | X | 1 |
| 1     | 1         | X | 0 |



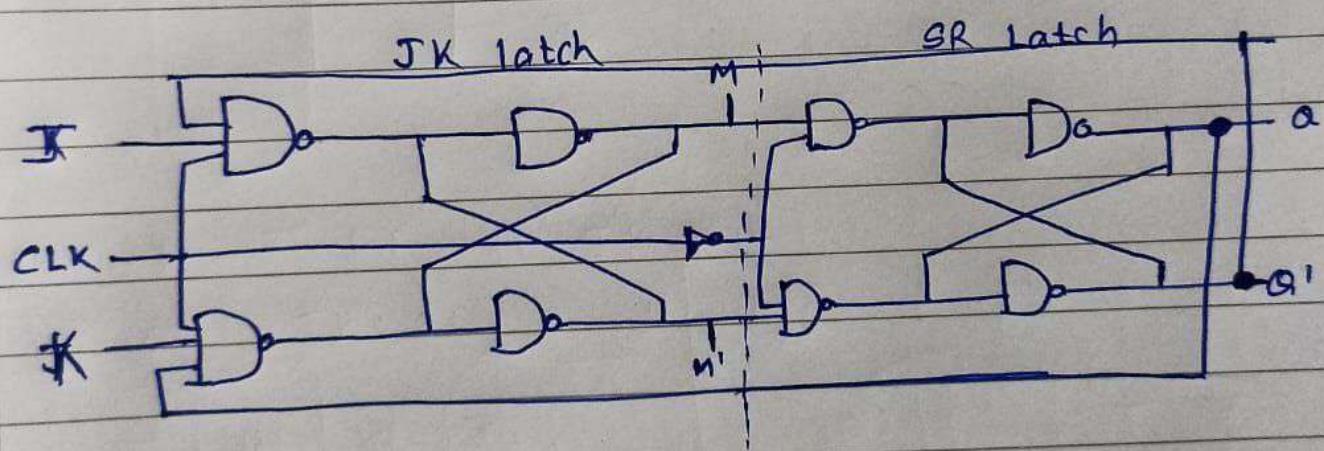
## Master-Slave JK FF

- Used to over-come race around condition
- combination of clocked JK latch and clocked SR latch
- clocked JK latch acts as the master & SR as slave
- master is positive triggered but slave will respond to negative trigger due to presence of inverter.
- which make JK FF ~~not~~ level triggered.

10



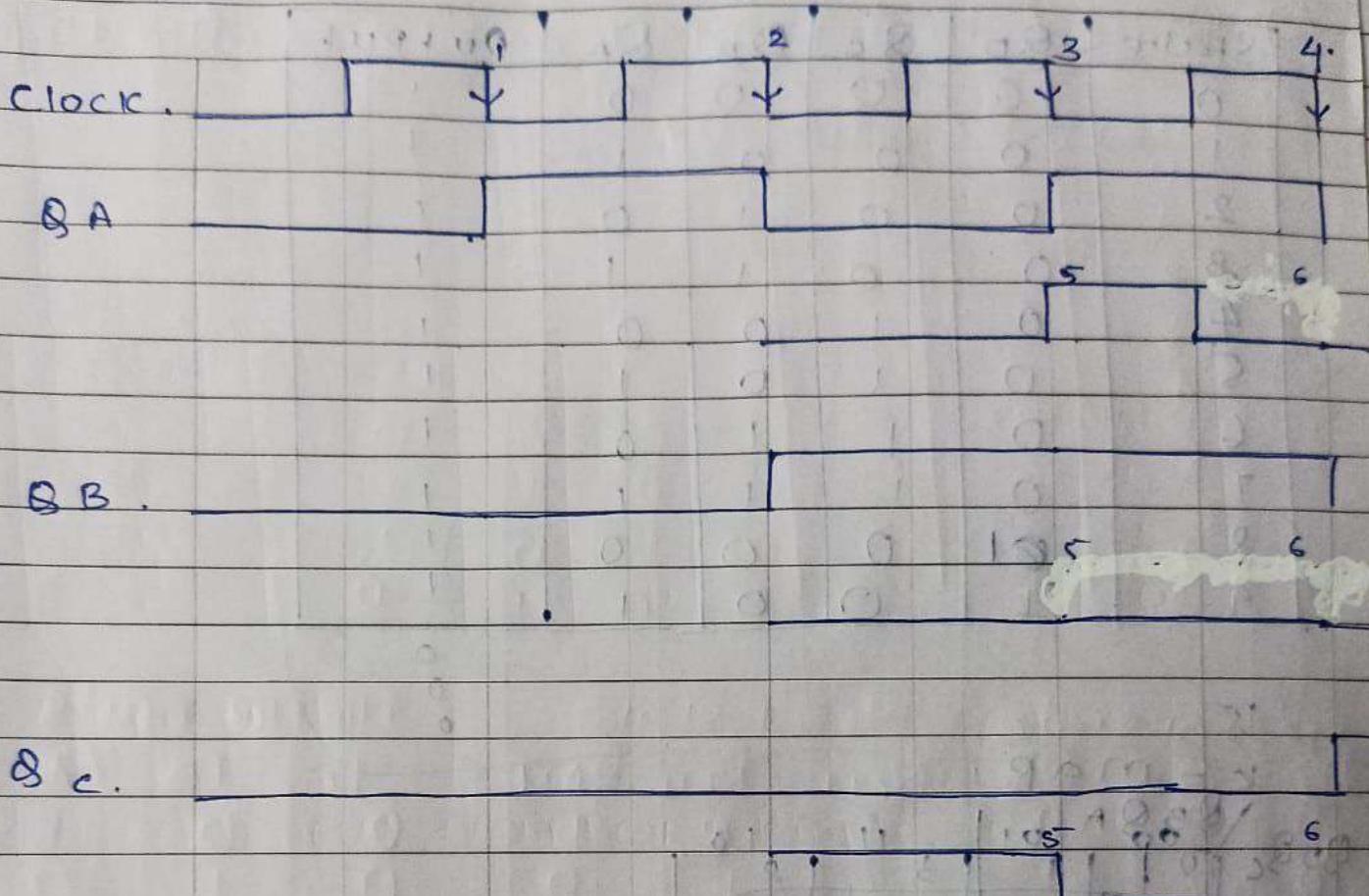
15



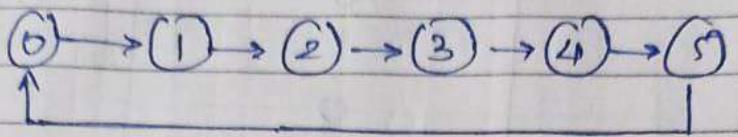
20

25

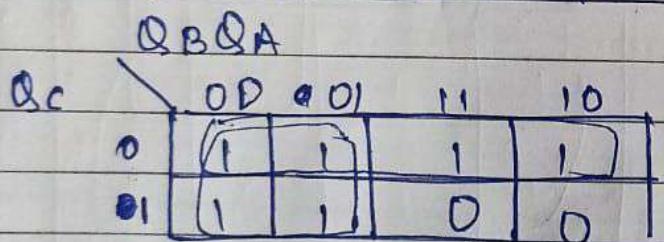
Timing diagram :



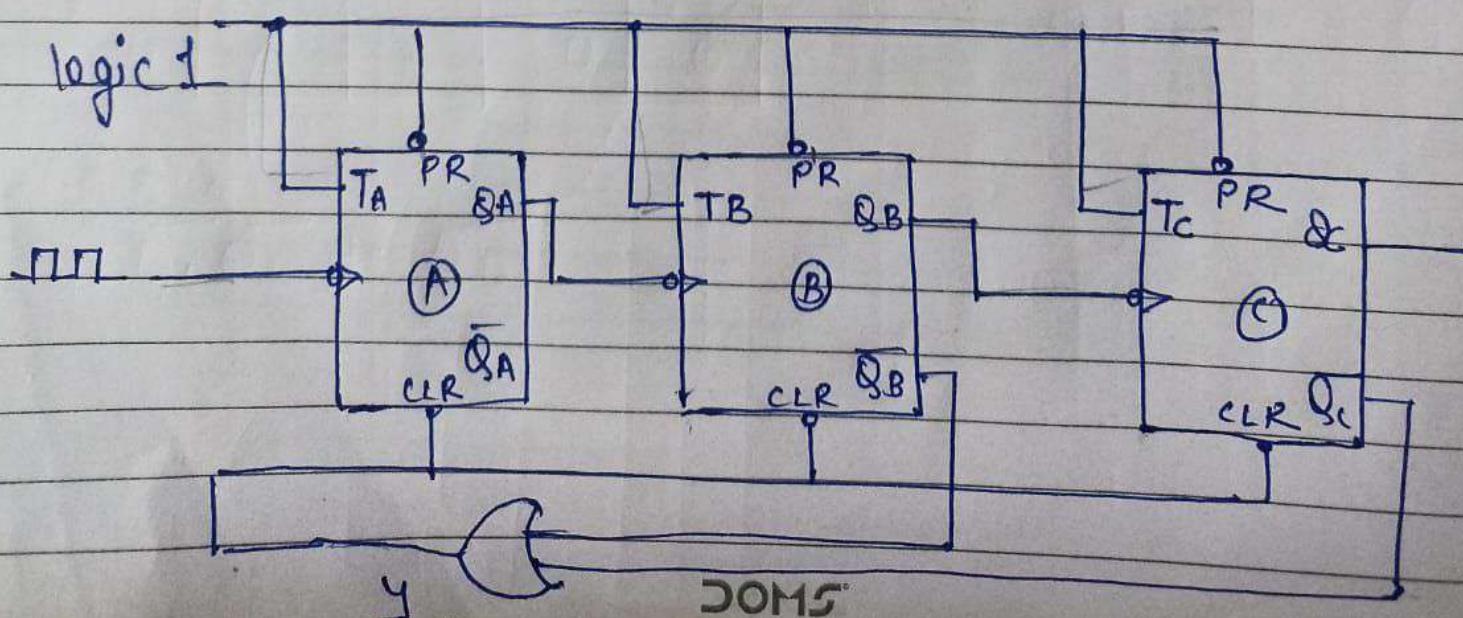
Q) Design a modulo-6 ripple counter, using a 3-bit ripple counter.

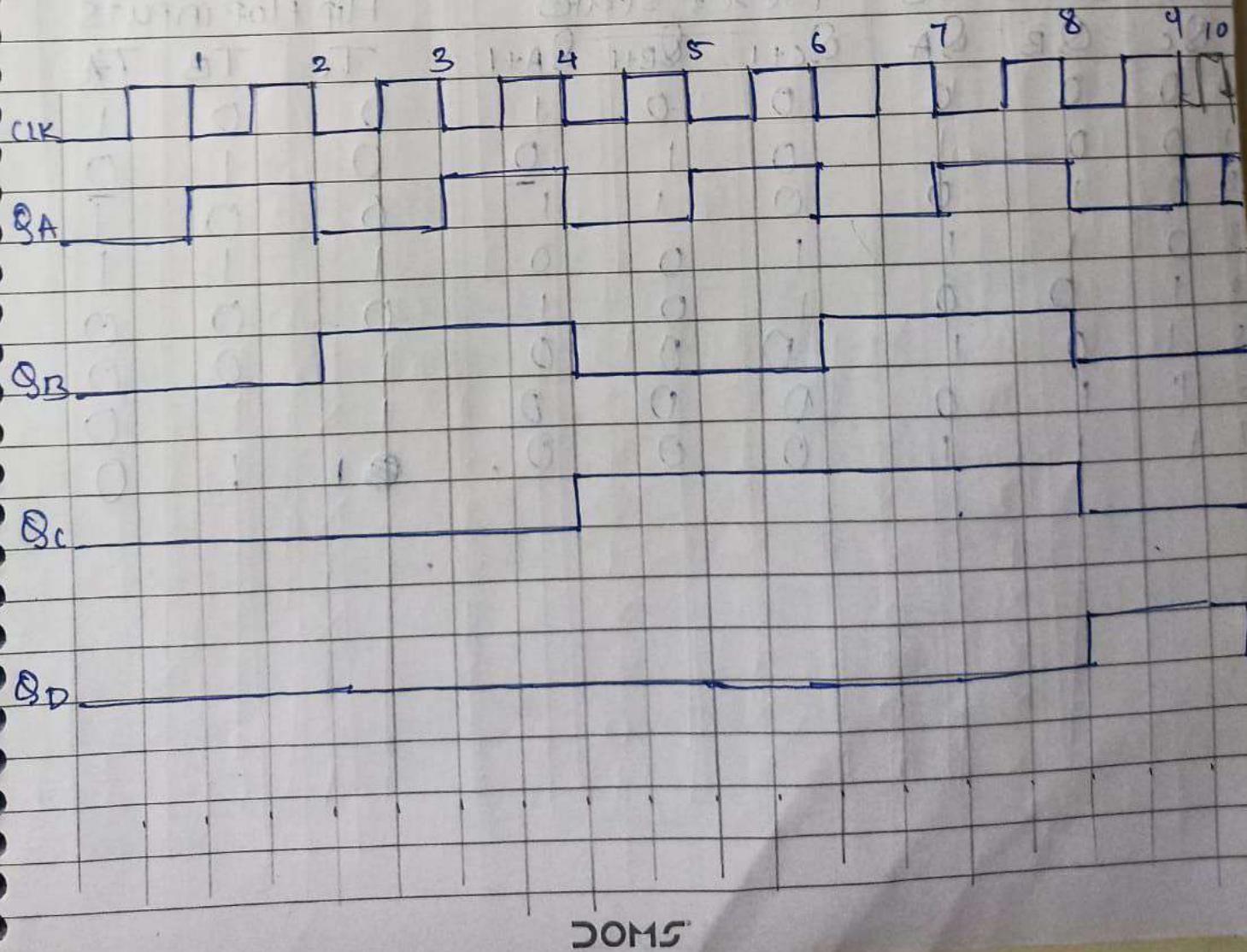
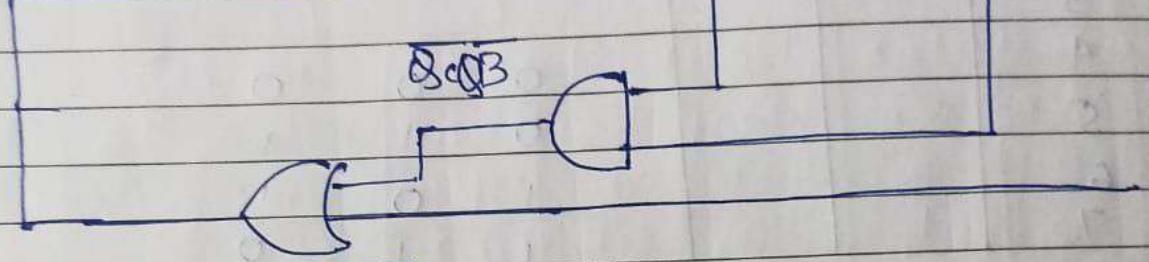
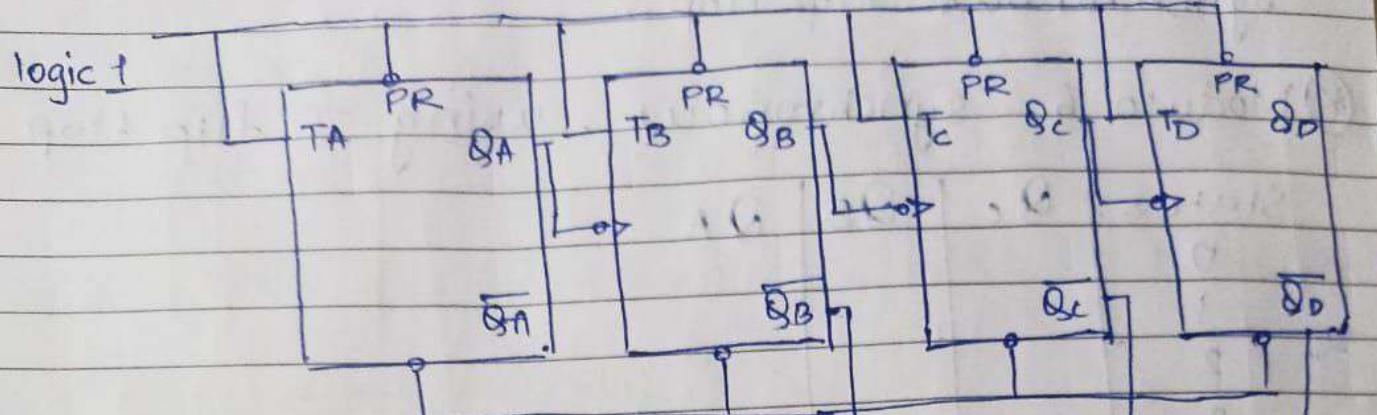


| State | flip flop output |       |       | Output Y or<br>Reset logic |
|-------|------------------|-------|-------|----------------------------|
|       | $Q_C$            | $Q_B$ | $Q_A$ |                            |
| 0     | 0                | 0     | 0     | Y = 1                      |
| 1     | 0                | 0     | 1     | 0                          |
| 2     | 0                | 1     | 0     | 1                          |
| 3     | 0                | 1     | 1     | 0                          |
| 4     | 1                | 0     | 0     | 1                          |
| 5     | 1                | 0     | 1     | 1                          |
| 6     | 1                | 1     | 0     | 0                          |
| 7     | 1                | 1     | 1     | 0                          |



$$= \overline{Q_C} + \overline{Q_B}$$

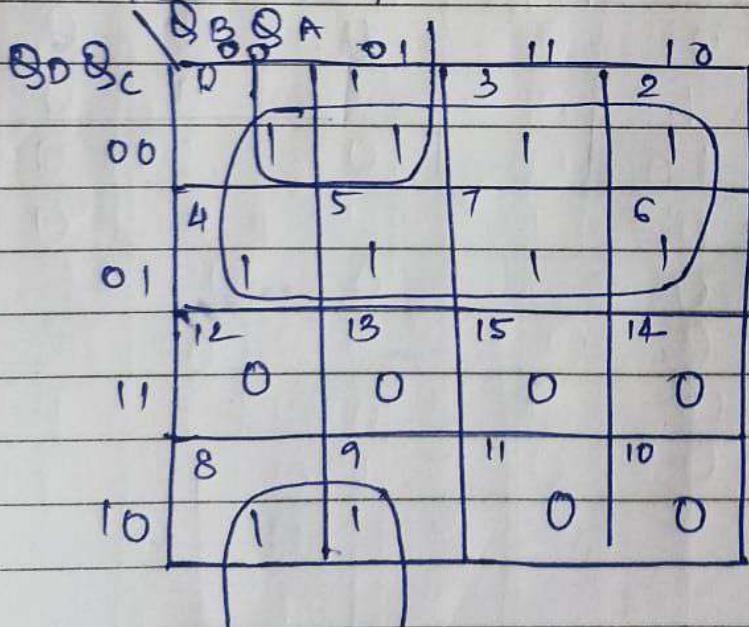




(K) Decade counter. Modulous 10

| State | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ | Output |
|-------|-------|-------|-------|-------|--------|
| 0     | 0     | 0     | 0     | 0     | 1      |
| 1     | 0     | 0     | 0     | 1     | 1      |
| 2     | 0     | 0     | 1     | 0     | 1      |
| 3     | 0     | 0     | 1     | 1     | 1      |
| 4     | 0     | 1     | 0     | 0     | 1      |
| 5     | 0     | 1     | 0     | 1     | 1      |
| 6     | 0     | 1     | 1     | 0     | 1      |
| 7     | 0     | 1     | 1     | 1     | 1      |
| 8     | 1     | 0     | 0     | 0     | 1      |
| 9     | 1     | 0     | 0     | 1     | 1      |
| 10    | 1     | 0     | 0     | 1     | 1      |
| 11    | 0     | 0     | 0     | 0     | 1      |
| 12    | 0     | 0     | 0     | 0     | 1      |
| 13    | 0     | 0     | 0     | 0     | 1      |
| 14    | 0     | 0     | 0     | 0     | 1      |
| 15    | 0     | 0     | 0     | 0     | 1      |

K-map:



$$Z = \overline{Q_C Q_B} + \overline{Q_D}$$

$T_C$

|     | 00 | 01 | 11 | 10 |
|-----|----|----|----|----|
| Q_C | 0  | 0  | 0  | 0  |
|     | 0  | 0  | 0  | 0  |
|     | 0  | 0  | 0  | 0  |
|     | 0  | 0  | 0  | 0  |

$T_B$

|     | 00 | 01 | 11 | 10 |
|-----|----|----|----|----|
| Q_C | 0  | 1  | 1  | 0  |
|     | 0  | 0  | 1  | 1  |
|     | 0  | 0  | 1  | 1  |
|     | 0  | 0  | 1  | 1  |

$$T_C = Q_C Q_A + Q_C Q_B + Q_B Q_A$$

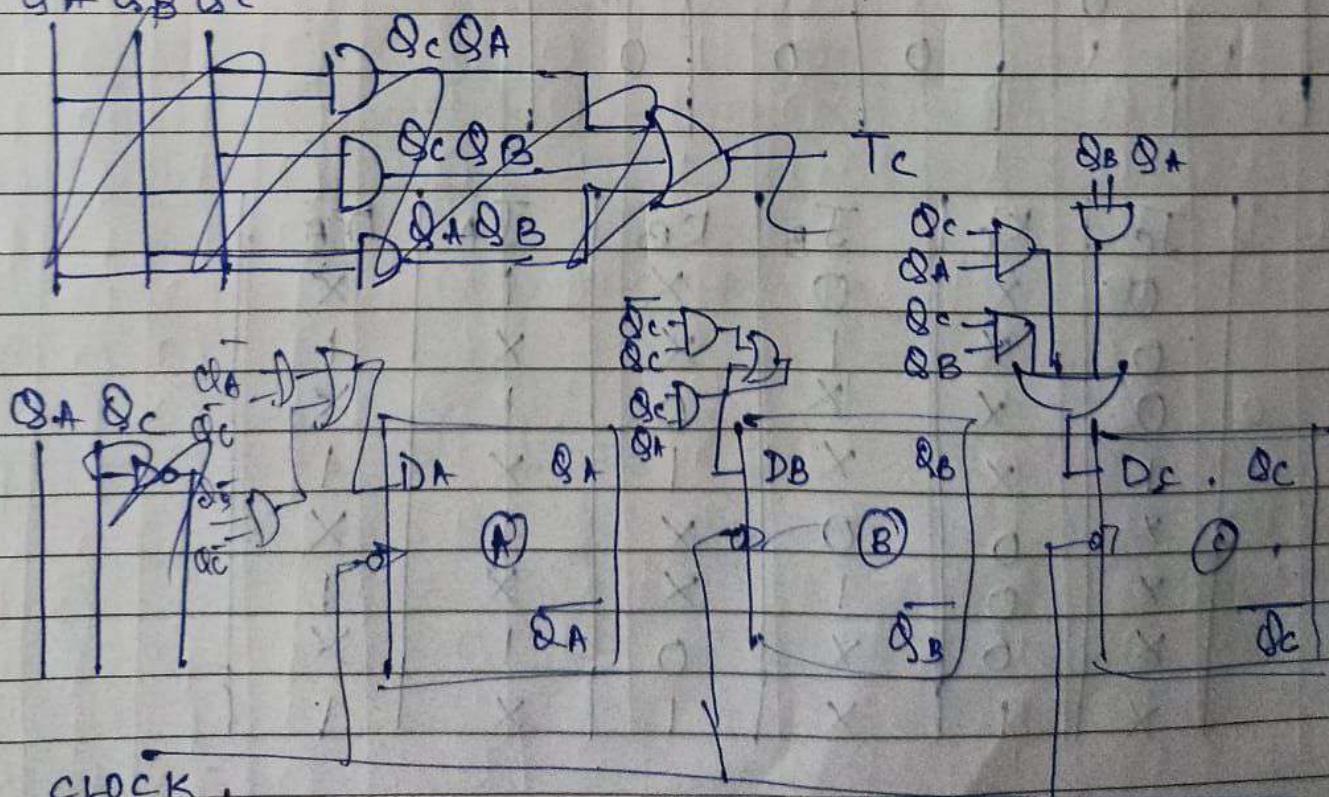
$$T_B = \bar{Q}_C Q_A + Q_C Q_A$$

$T_A$

|     | 00 | 01 | 11 | 10 |
|-----|----|----|----|----|
| Q_C | 0  | 1  | 0  | 1  |
|     | 0  | 0  | 0  | 0  |
|     | 0  | 0  | 0  | 0  |
|     | 0  | 0  | 0  | 0  |

$$T_A = \bar{Q}_C \bar{Q}_A + Q_B \bar{Q}_C$$

$Q_A Q_B Q_C$



DOMS

Q) Design a mod 6 synchronous counter using JK flip flop.

Present      Next      J      K

|   |   |   |   |
|---|---|---|---|
| 0 | 0 | 0 | X |
|---|---|---|---|

|   |   |   |   |
|---|---|---|---|
| 0 | 1 | 1 | X |
|---|---|---|---|

|   |   |   |   |
|---|---|---|---|
| 1 | 0 | X | 1 |
|---|---|---|---|

|   |   |   |   |
|---|---|---|---|
| 1 | 1 | X | 0 |
|---|---|---|---|

Present states

|       |       |       |
|-------|-------|-------|
| $Q_C$ | $Q_B$ | $Q_A$ |
|-------|-------|-------|

|   |   |   |
|---|---|---|
| 0 | 0 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 0 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 1 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 1 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 0 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 0 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 1 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 1 | 1 |
|---|---|---|

Next states

|           |           |           |
|-----------|-----------|-----------|
| $Q_{C+1}$ | $Q_{B+1}$ | $Q_{A+1}$ |
|-----------|-----------|-----------|

|   |   |   |
|---|---|---|
| 0 | 0 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 1 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 1 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 0 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 0 | 1 |
|---|---|---|

|   |   |   |
|---|---|---|
| 1 | 1 | 0 |
|---|---|---|

|   |   |   |
|---|---|---|
| 0 | 0 | 0 |
|---|---|---|

Inputs

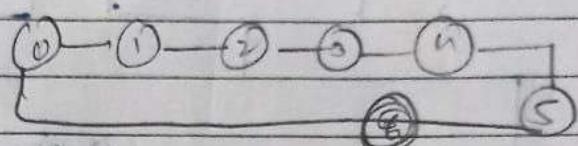
$J_C / J_B / J_A$

| $J_C$ | $K_C$ | $J_B$ | $K_B$ | $J_A$ | $K_A$ |
|-------|-------|-------|-------|-------|-------|
| 0     | X     | 0     | X     | 1     | X     |
| 0     | X     | 1     | X     | X     | 1     |
| 0     | X     | X     | 0     | 1     | X     |
| 1     | X     | X     | 1     | X     | 1     |
| X     | 0     | 0     | X     | 1     | X     |
| X     | 0     | 1     | X     | X     | 1     |
| X     | 0     | X     | 0     | 1     | X     |
| X     | 1     | X     | 1     | X     | 1     |

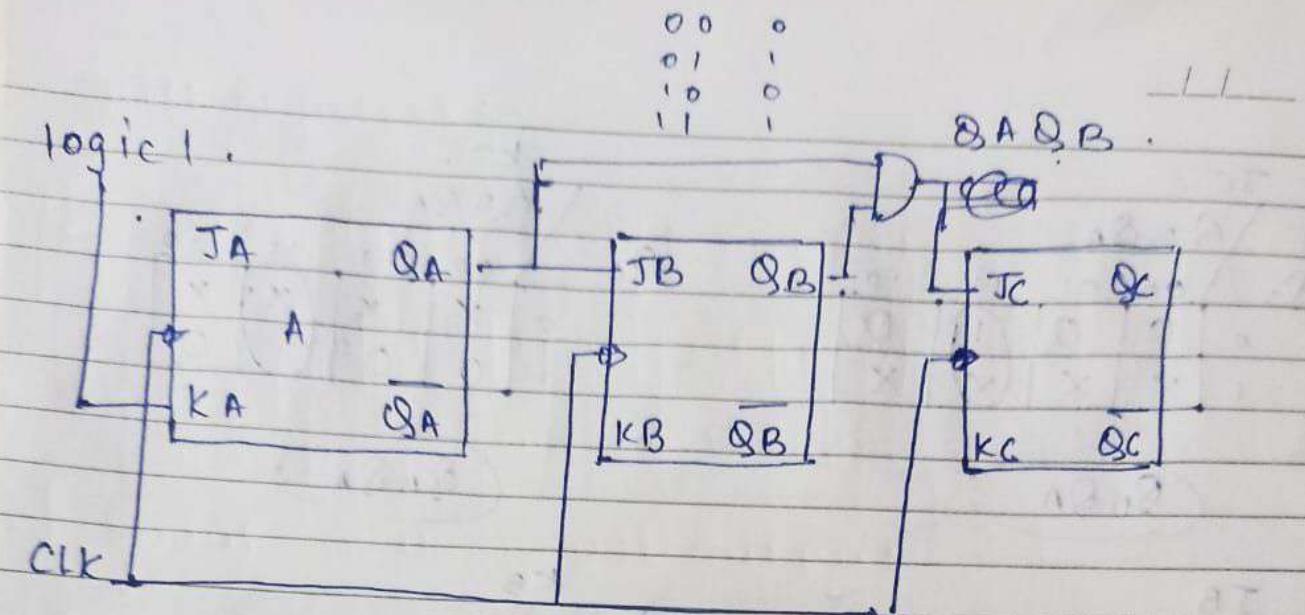
Synchronous flip flop:

④ Modulo 6 synchronous, using T flip flop

| States | $Q_C$ | $Q_B$ | $Q_A$ |
|--------|-------|-------|-------|
| 0      | .     | .     | .     |
| 1      | .     | .     | .     |
| 2      | .     | .     | .     |
| 3      | .     | .     | .     |
| 4      | 0     | 0     | 0     |
| 5      | 0     | 1     | 1     |
| 6      | 1     | 0     | 1     |
| 7      | 1     | 1     | 0     |



| Present State | Next State |       |           | Flip flop inputs |           |       |       |       |
|---------------|------------|-------|-----------|------------------|-----------|-------|-------|-------|
| $Q_C$         | $Q_B$      | $Q_A$ | $Q_{C+1}$ | $Q_{B+1}$        | $Q_{A+1}$ | $T_C$ | $T_B$ | $T_A$ |
| 0             | 0          | 0     | 0         | 0                | 1         | 0     | 0     | 1     |
| 1             | 0          | 0     | 1         | 0                | 1         | 0     | 1     | 0     |
| 2             | 0          | 1     | 0         | 0                | 1         | 1     | 0     | 1     |
| 3             | 0          | 1     | 1         | 1                | 0         | 0     | 1     | 1     |
| 4             | 1          | 0     | 0         | 1                | 0         | 1     | 0     | 0     |
| 5             | 1          | 0     | 1         | 0                | 0         | 0     | 0     | 0     |
| 6             | 1          | 1     | 0         | 0                | 0         | 0     | 1     | 0     |
| 7             | 1          | 1     | 1         | 0                | 0         | 0     | 1     | 0     |



Q) Design a 4-bit binary synchronous counter with D-flip flop.

| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ | $Q_{D+1}$ | $Q_{C+1}$ | $Q_{B+1}$ | $Q_{A+1}$ | $D_D$ | $D_C$ | $D_B$ | $D_A$ |
|-------|-------|-------|-------|-----------|-----------|-----------|-----------|-------|-------|-------|-------|
| 0 0   | 0     | 0     | 0     | 0         | 0         | 0         | 1         | 0     | 0     | 0     | 1     |
| 1 0   | 0     | 0     | 1     | 0         | 0         | 1         | 0         | 0     | 0     | 0     | 0     |
| 2 0   | 0     | 1     | 0     | 0         | 0         | 1         | 1         | 0     | 0     | 1     | 0     |
| 3 0   | 0     | 1     | 1     | 0         | 1         | 0         | 0         | 0     | 1     | 0     | 1     |
| 4 0   | 1     | 0     | 0     | 0         | 1         | 0         | 0         | 0     | 1     | 0     | 0     |
| 5 0   | 1     | 0     | 1     | 0         | 1         | 1         | 0         | 0     | 0     | 1     | 0     |
| 6 0   | 1     | 1     | 0     | 0         | 1         | 1         | 1         | 0     | 1     | 1     | 0     |
| 7 0   | 1     | 1     | 1     | 1         | 0         | 0         | 0         | 1     | 0     | 0     | 0     |
| 8 1   | 0     | 0     | 0     | 1         | 0         | 0         | 1         | 1     | 0     | 0     | 0     |
| 9 1   | 0     | 0     | 1     | 1         | 0         | 1         | 0         | 1     | 0     | 1     | 0     |
| 10 1  | 0     | 1     | 0     | 1         | 0         | 1         | 1         | 1     | 0     | 1     | 1     |
| 11 1  | 0     | 1     | 1     | 1         | 1         | 0         | 0         | 1     | 1     | 0     | 0     |
| 12 1  | 1     | 0     | 0     | 1         | 1         | 0         | 1         | 1     | 1     | 0     | 1     |
| 13 1  | 1     | 0     | 1     | 1         | 1         | 1         | 0         | 1     | 1     | 1     | 0     |
| 14 1  | 1     | 1     | 0     | 1         | 0         | 1         | 1         | 1     | 0     | 1     | 1     |
| 15 1  | 1     | 1     | 1     | 1         | 0         | 0         | 0         | 0     | 0     | 0     | 0     |

$\overline{Q_B} Q_A$

$\overline{Q_C} Q_A$

| DC | BA | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| 00 | 0  | 1  | 3  | 2  | 0  |
| 01 | 0  | 0  | 1  | 0  | 0  |
| 11 | 1  | 1  | 0  | 1  | 0  |
| 10 | 0  | 1  | 1  | 0  | 1  |

$\overline{Q_C} Q_B Q_A + Q_C \overline{Q_A} + Q_C \overline{Q_B}$

DC BA

| DC | BA | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| 00 | 0  | 0  | 1  | 0  | 0  |
| 01 | 1  | 1  | 0  | 0  | 1  |
| 11 | 0  | 1  | 0  | 1  | 0  |
| 10 | D  | D  | 10 | D  | D  |

$+ Q_D Q_C Q_B Q_A$

DC BA  $\overline{B} A D D + \overline{Q} B Q D$   
 $+ Q_D \overline{Q}_C$

| DC | BA | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| 00 | 0  | 1  | 0  | 1  | 0  |
| 01 | 0  | 1  | 0  | 1  | 0  |
| 11 | 0  | 1  | 0  | 1  | 0  |
| 10 | 0  | 1  | 0  | 0  | 0  |

| DC | BA | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| 00 | 1  | 0  | 0  | 1  | 0  |
| 01 | 1  | 0  | 0  | 1  | 0  |
| 11 | 1  | 0  | 0  | 1  | 0  |
| 10 | 1  | 0  | 0  | 1  | 0  |

$\overline{P} B D A + D B \overline{A} \overline{A}$

$(DB + DA)$

$(DA)$

JC.

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | 0  | 0  | 1  | 0  |
| 1     | x  | x  | x  | x  |

QB QA

KC,  
QB QA

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | x  | x  | x  | x  |
| 1     | 0  | 0  | 1  | 0  |

QB QA

JB

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | 0  | 1  | x  | x  |
| 1     | 0  | 1  | x  | x  |

KB

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | x  | x  | 1  | 0  |
| 1     | x  | x  | 1  | 0  |

(QA)

(QA)

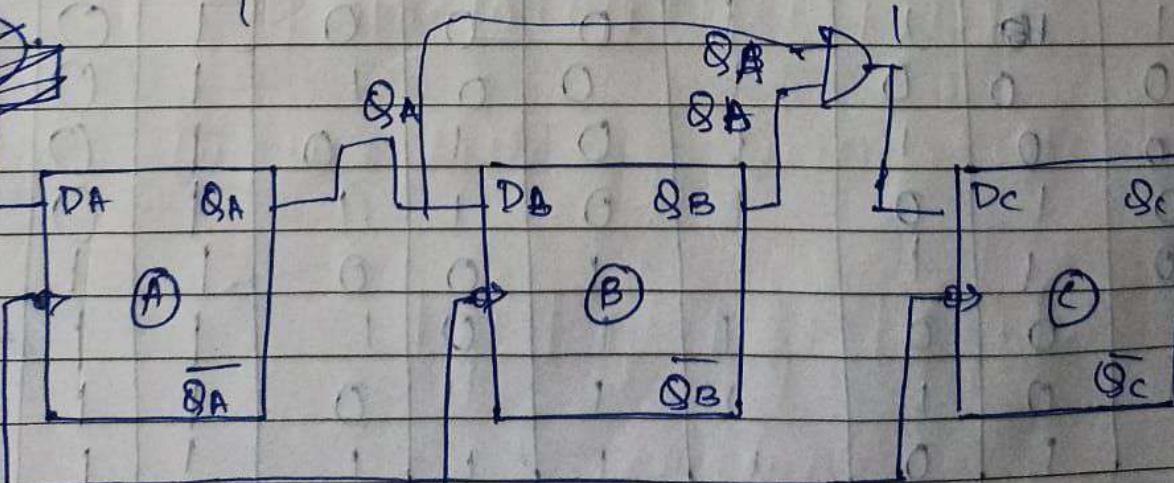
JA.

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | 1  | x  | x  | 0  |
| 1     | 1  | x  | x  | 1  |

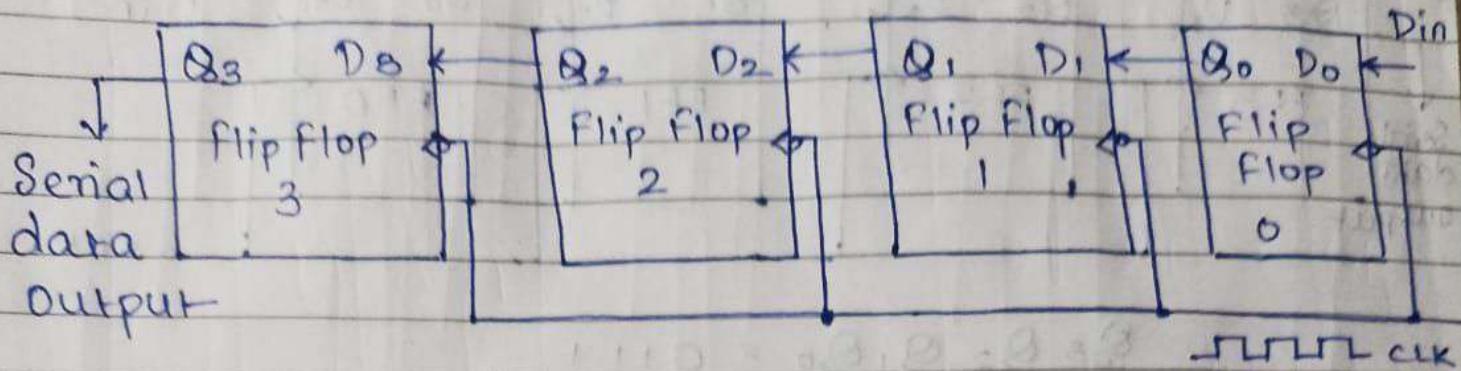
KA

| QB QA |    |    |    |    |
|-------|----|----|----|----|
| Qc    | 00 | 01 | 11 | 10 |
| 0     | x  | 1  | 1  | x  |
| 1     | x  | 1  | 1  | x  |

QB  
QA  
logic



Shift left mode.



$Q_3, Q_2, Q_1, Q_0$

$Q_3, Q_2, Q_1, Q_0$

Initial

0 0 0 0

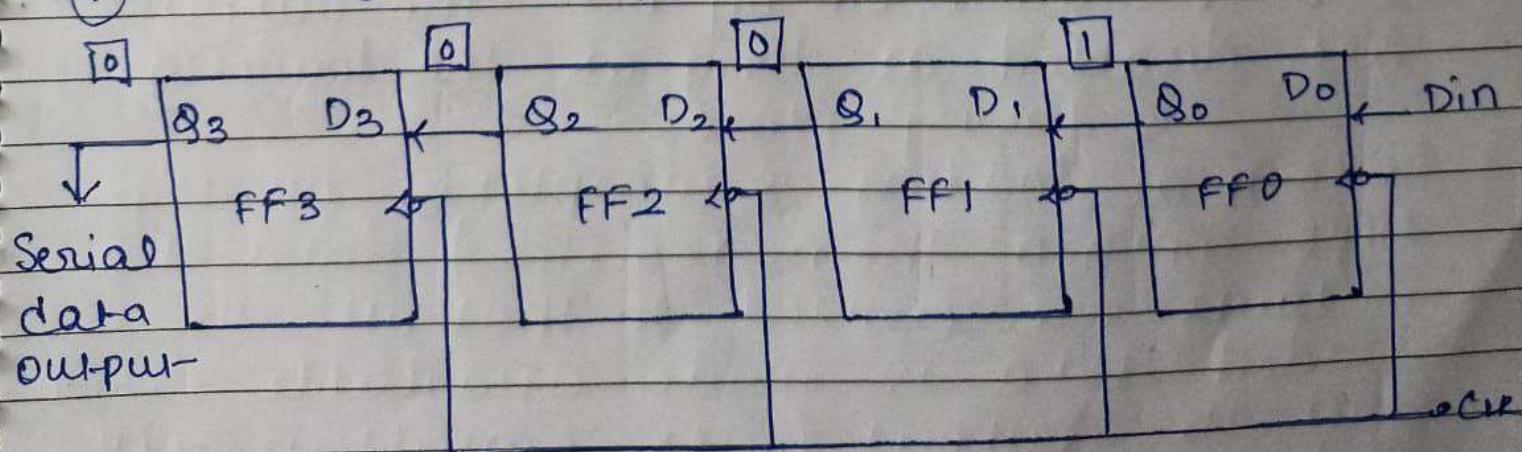
1 0 0 0 1

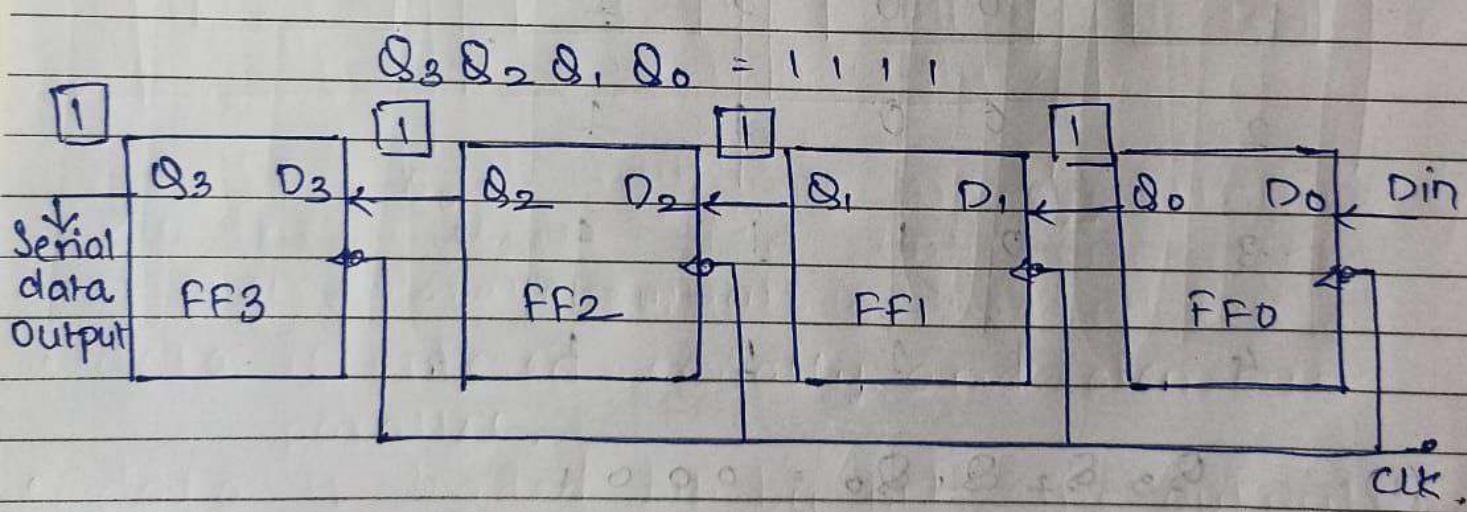
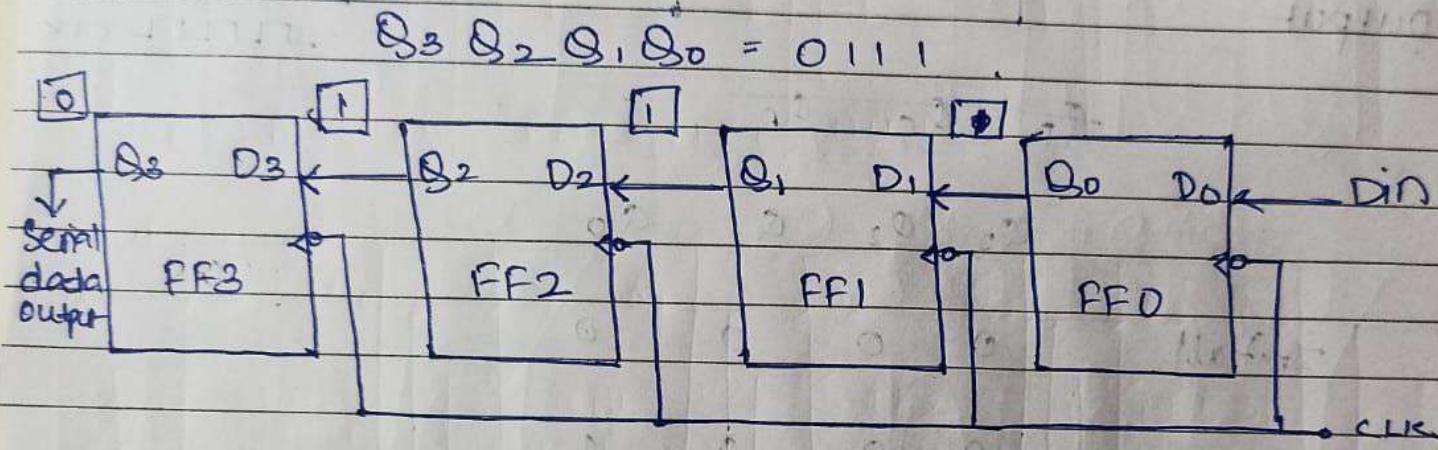
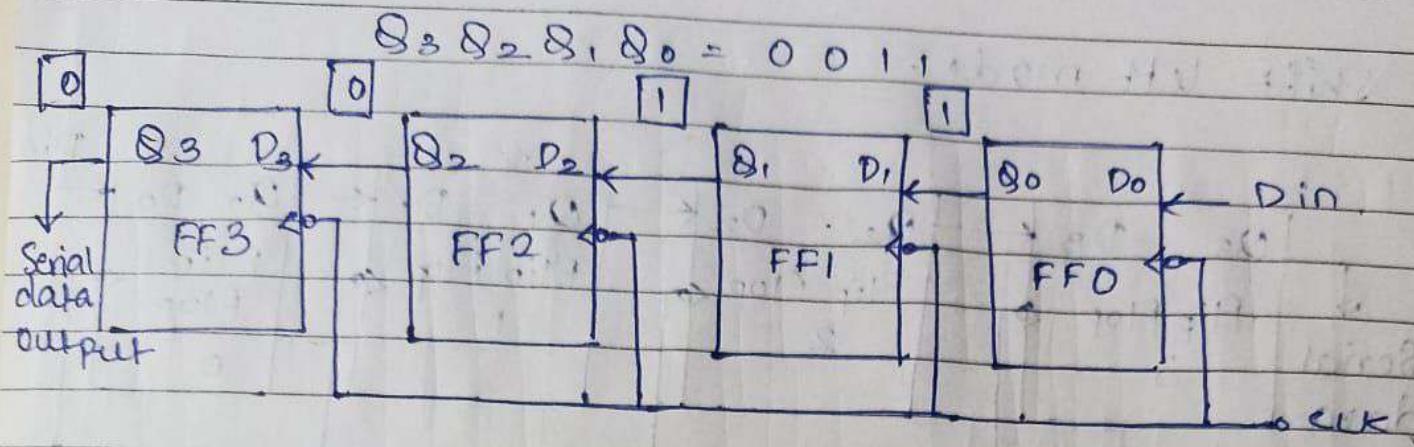
-2 0 0 1 1

3 0 1 1 1

4 1 1 1 1

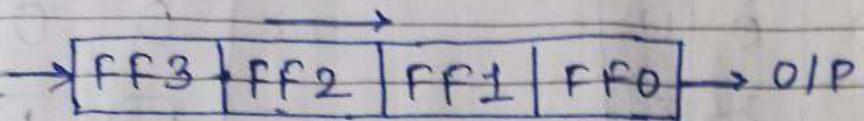
$$(1) \quad Q_3 Q_2 Q_1 Q_0 = 0001$$





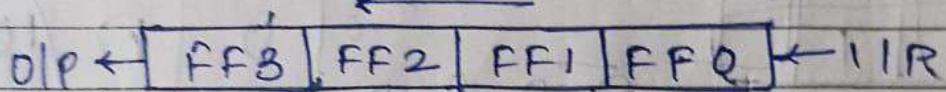
## Shift Registers.

1] Serial input- serial output.



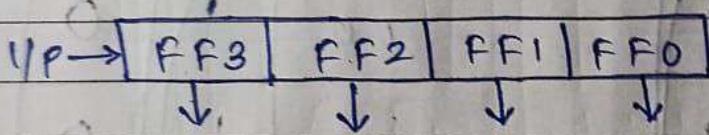
Serial shift Right

2] Serial input- serial output-

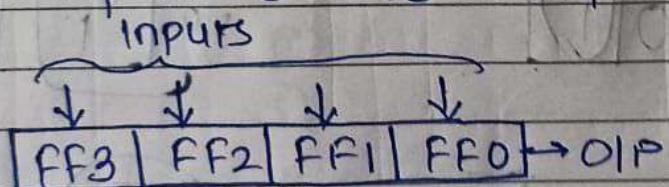


Serial shift Left

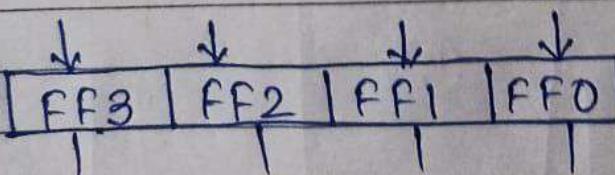
3] Serial input- parallel output

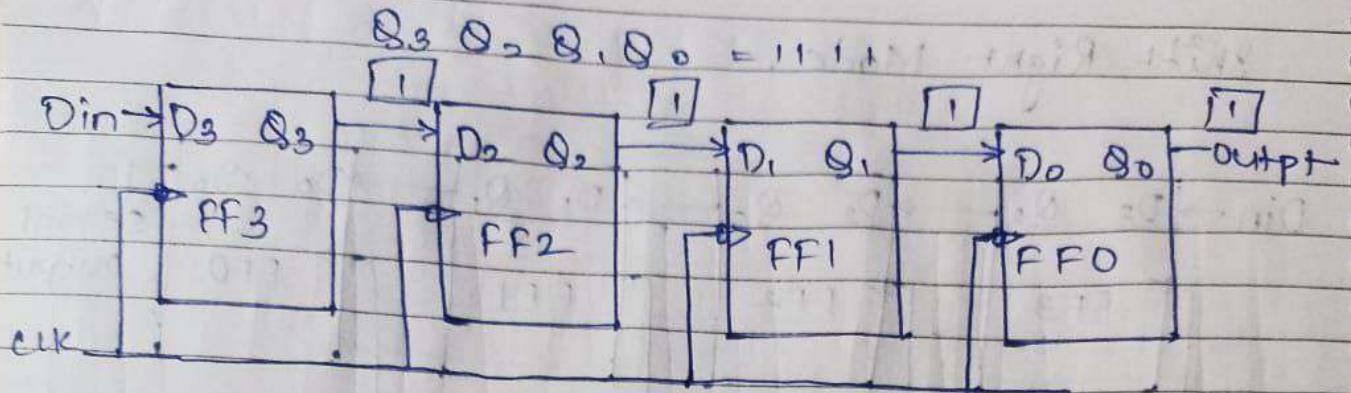


4] Parallel input- serial output

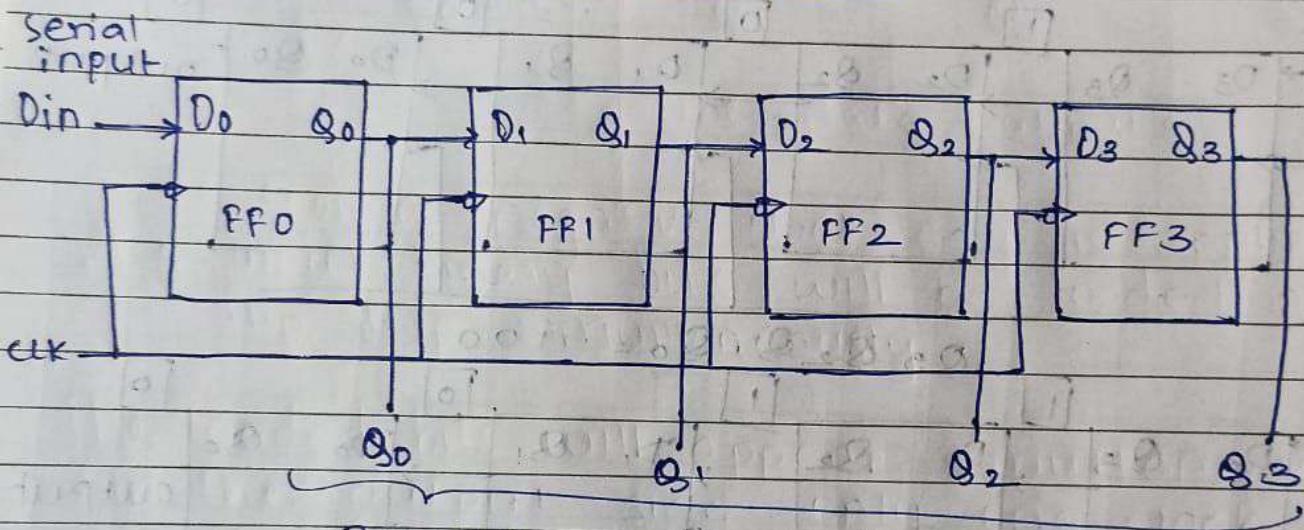


5] Parallel input- parallel output





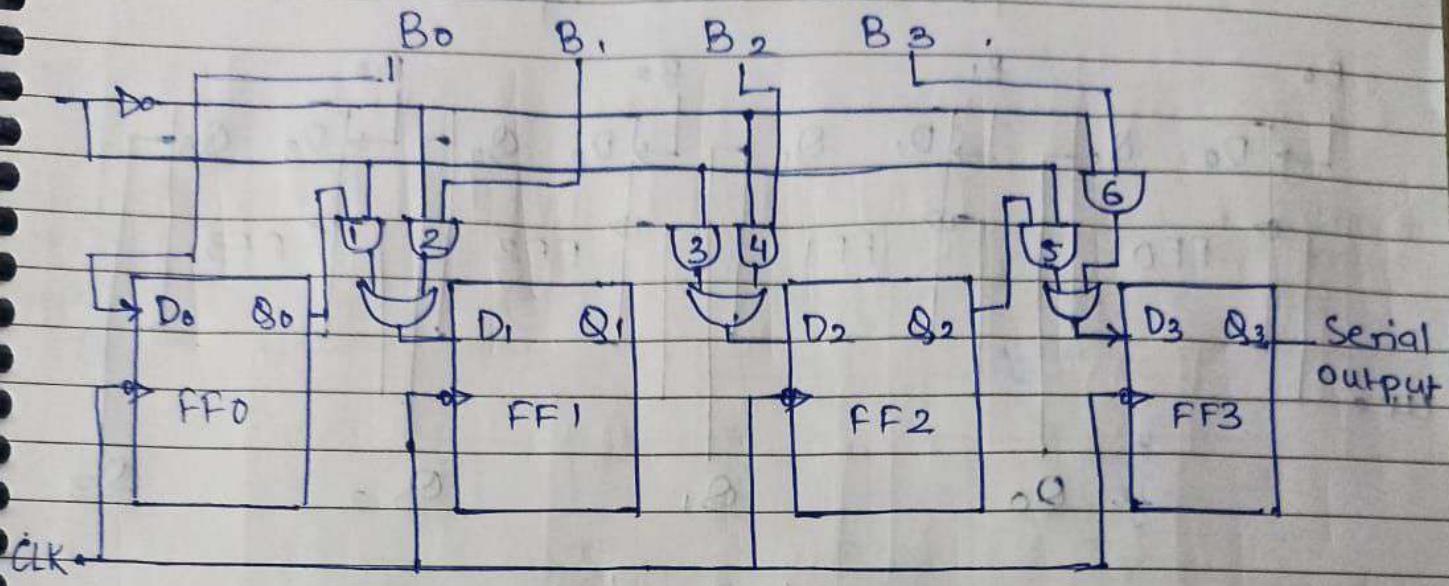
### \* SERIAL IN PARALLEL OUT



Parallel outputs.

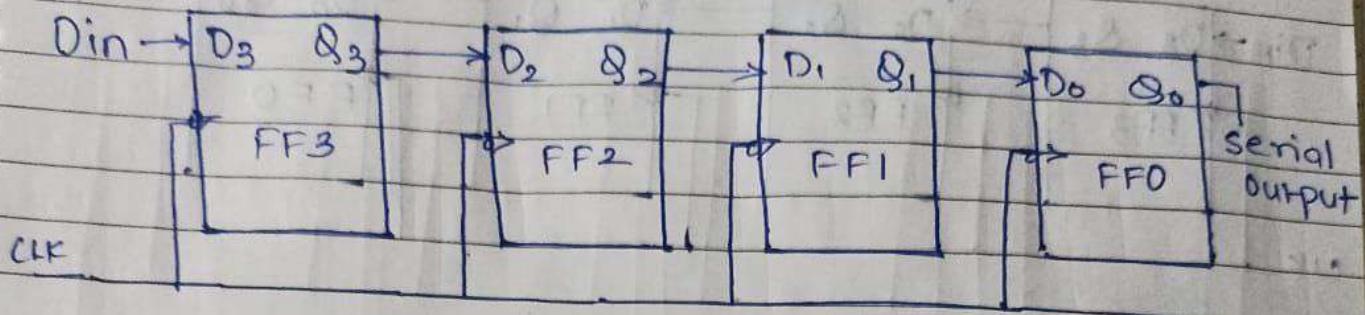
- data is entered serially and taken out parallel.
- data is loaded bit by bit. The outputs are disabled as long as the loading is taking place.
- As soon as loading is complete, all flip flops contain their required data the outputs are enabled so that all the loaded data is made available over all the output lines simultaneously.
- speed of operation of SISO is same as DOMS      SIPO .

## Parallel in serial out

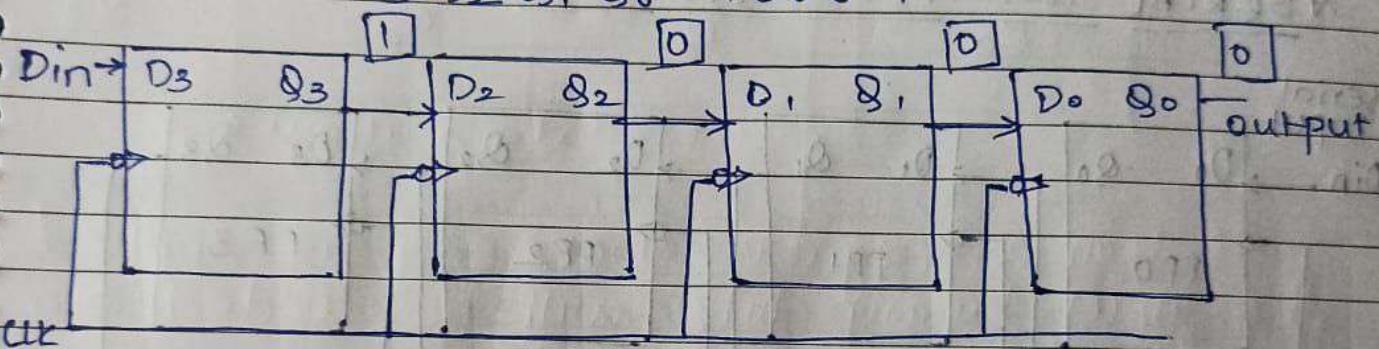


- When shift/load line is low (0) the AND gates 2, 4, 6 become active.  $B_0, B_1, B_2, B_3$  will get loaded into the corresponding flip-flops. Parallel loading takes place.
- When shift/load line is high (1) gates 1, 3, 5 become active. Therefore shifting data from left to right.

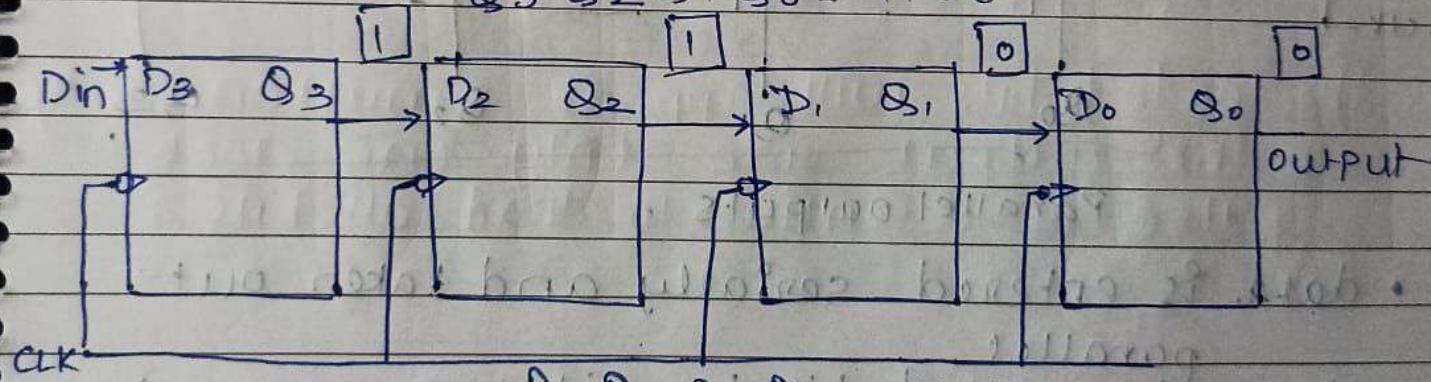
Shift Right Mode.



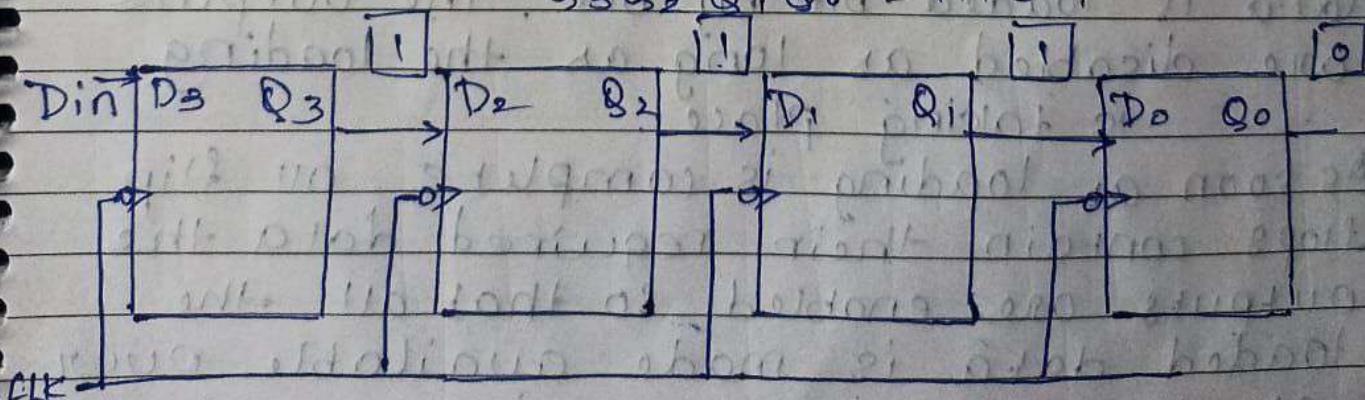
$$Q_3 \ Q_2 \ Q_1 \ Q_0 = 1000$$



$$Q_3 \ Q_2 \ Q_1 \ Q_0 = 1100$$



$$Q_3 \ Q_2 \ Q_1 \ Q_0 = 1110$$



- Ring counter is a special type of shift register.

Operation -

- Initially low clear pulse is applied to all the flip flops.
- Hence FF1, FF2, FF3 will reset but FFO will be present. So the output of shift register are:

$$Q_3 Q_2 Q_1 Q_0 = 0000 \quad 1000$$

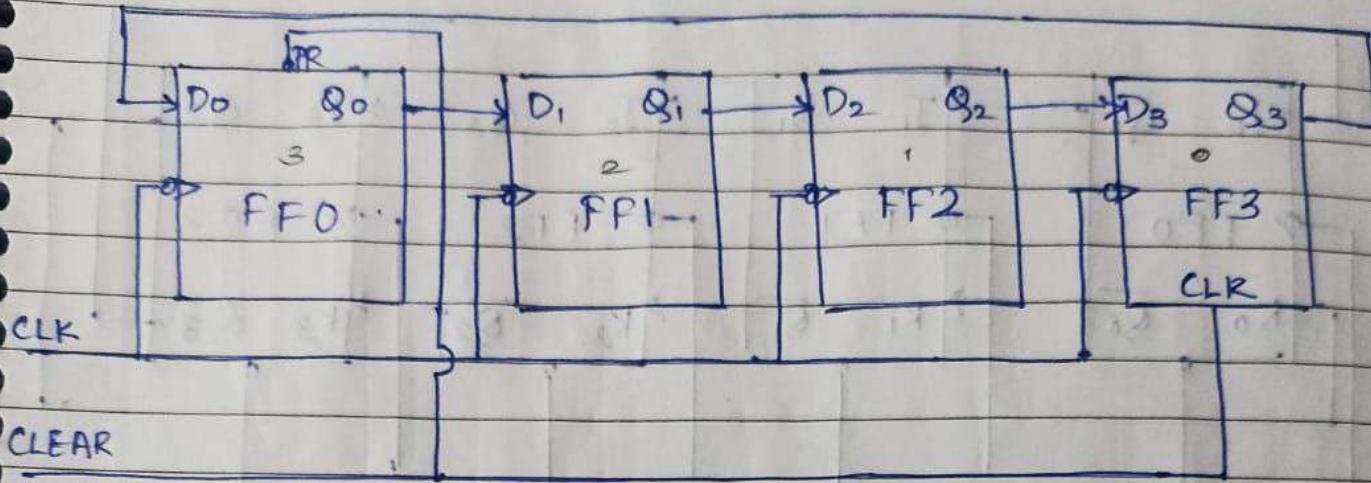
$$Q_3 Q_2 Q_1 Q_0 = 0100$$

$$Q_3 Q_2 Q_1 Q_0 = 0010$$

TT :

| CLR | CLK | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|-----|-----|-------|-------|-------|-------|
| 1   | X   | 1     | 0     | 0     | 0     |
| 1   | ↓   | 0     | 1     | 0     | 0     |
| 1   | ↓   | 0     | 0     | 1     | 0     |
| 1   | ↓   | 0     | 0     | 0     | 1     |
|     | ↓   | 1     | 0     | 0     | 0     |

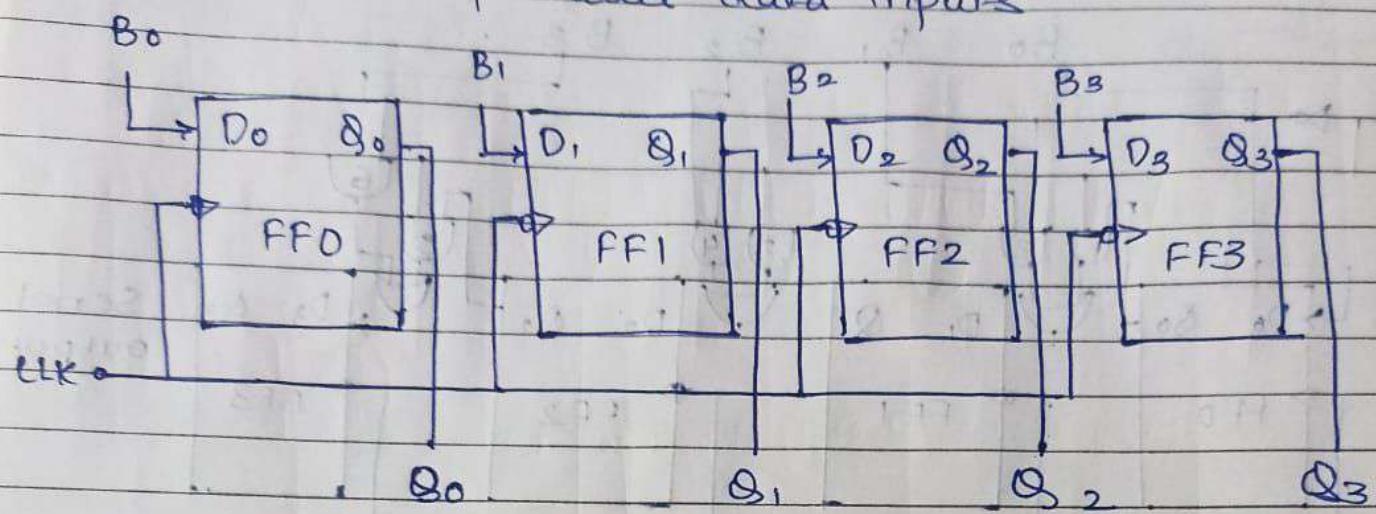
## Ring counter



- each flip flop is connected in a circular manner. Each flip flop output is connected to input of next flip flop in the sequence, and the output of last flip flop is fed back to the input of first flip flop, forming a closed loop. This creates a cyclic shift of data bits through the flip flops.

## \* Parallel in Parallel out

parallel data inputs



parallel data outputs .

As soon as negative clock edge is applied  
the input binary bits will be loaded into  
flip flop simultaneously ,

the loaded bits will appear simultaneously  
to the output side . only one clock  
pulse is essential to load all bits .

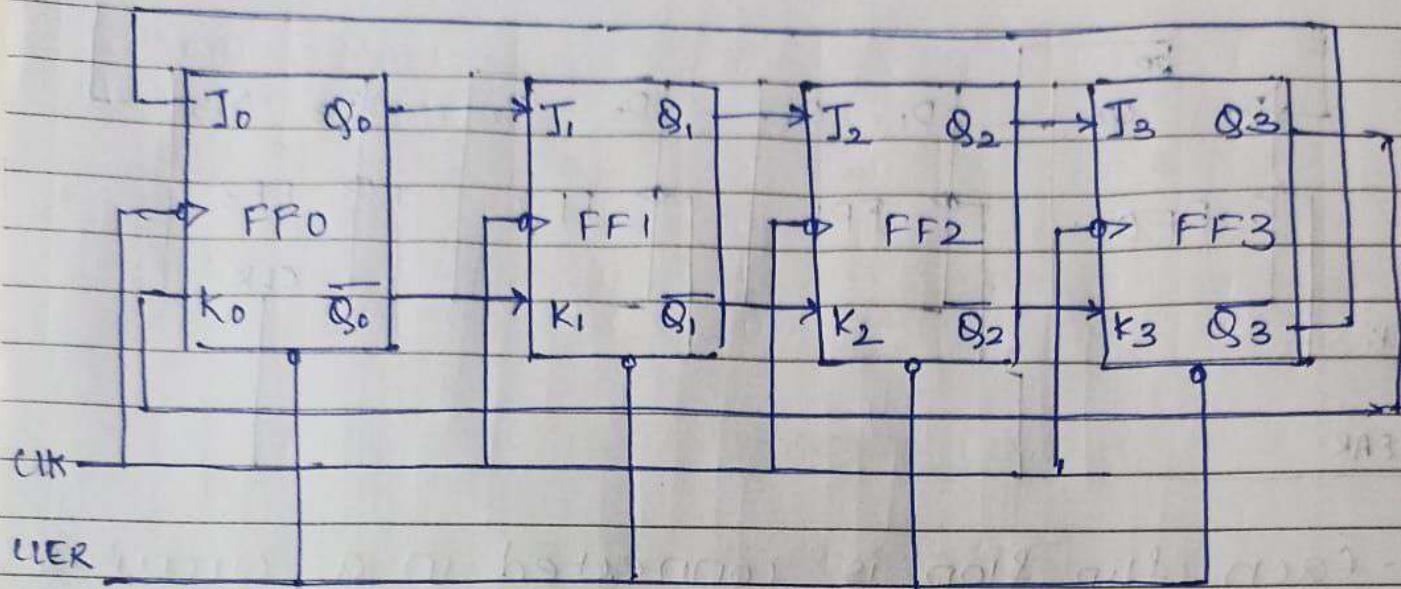
- In the next negative clock cycle  $\bar{Q}_3 = 1$

$$Q_0, Q_1, Q_2, Q_3 = 1, 1, 0, 0$$

TR : .

| clear | CRC.         | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | state no. |
|-------|--------------|-------|-------|-------|-------|-----------|
| 1     | Initially    | 0     | 0     | 0     | 0     | 1         |
| 1     | $\downarrow$ | 1     | 0     | 0     | 0     | 2         |
| 1     | $\downarrow$ | 1     | 1     | 0     | 0     | 3         |
| 1     | $\downarrow$ | 1     | 1     | 1     | 0     | 4         |
| 1     | $\downarrow$ | 1     | 1     | 1     | 1     | 5         |
| 1     | $\downarrow$ | 0     | 1     | 1     | 1     | 6         |
| 1     | $\downarrow$ | 0     | 0     | 1     | 1     | 7         |
| 1     | $\downarrow$ | 0     | 0     | 0     | 1     | 8         |
| 1     | $\downarrow$ | 0     | 0     | 0     | 0     | 1         |

## Johnson's counter :



- In ring counter output of last flip flop is connected directly to first flip flop.
- But in Johnson's counter outputs are cross coupled to inputs . i.e.  $Q_3$  is connected to  $K_0$  and  $Q_0$  is connected to  $K_3$  . the circuit is called as twisted ring counter or johnson's counter .
- Initially a short negative going pulse is applied to the clear input of all flip flops .  
 $\therefore Q_0 \ Q_1 \ Q_2 \ Q_3 = 0000$  .
- As soon as first negative edge of clock arrives .  
 $Q_3 = 1$  will go to  $Q_0$  .

$$Q_0 \ Q_1 \ Q_2 \ Q_3 = 1 \ 0 \ 0 \ 0 ,$$