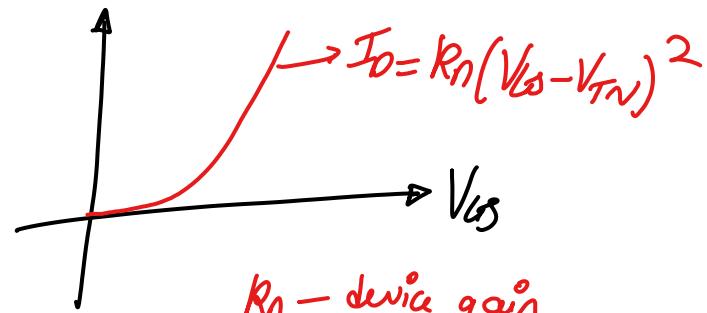


NMOS-E type biasing ckt's:

$$V_{GS} > V_{TN}$$

\downarrow

$$V_{GS} \rightarrow \text{tve}$$



k_n - device gain
 V_{TN} - threshold voltage

- ① Drain-f/b bias
- ② Voltage-divider bias

Drain-feedback bias (NMOS-E type)

KVL to G-S loop,

$$V_{DD} - (I_D + I_G)R_D - I_G R_G - V_{GS} = 0$$

$I_G \approx 0$

$$V_{DD} - I_D R_D - V_{GS} = 0$$

$$V_{GSQ} = V_{DD} - I_D R_D$$

$$I_{DQ} = k_n (V_{GS} - V_{TN})^2$$

$$I_D, V_{GSQ}, V_{GSQ}$$

$$I_G = 0$$

(oxide layer)

KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

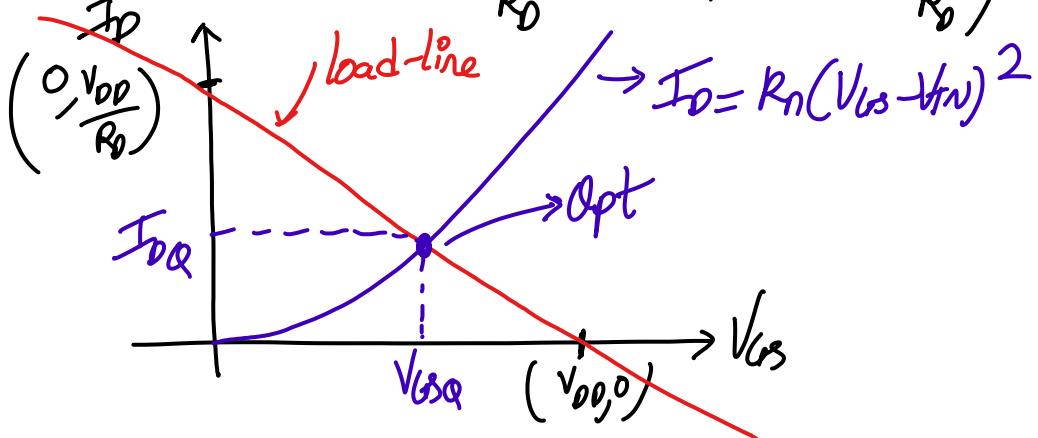
$$V_{DSQ} = V_{DD} - I_D R_D$$

→ To find Opt graphically,

$$① V_{GS} = V_{DD} - I_D R_D \quad \text{load-line equation}$$

$$a) \text{ Put } I_D = 0 \rightarrow V_{GS} = V_{DD} ; \text{ 1st pt} \equiv (V_{DD}, 0)$$

$$b) \text{ Put } V_{GS} = 0 \rightarrow I_D = \frac{V_{DD}}{R_D} ; \text{ 2nd pt} \equiv (0, \frac{V_{DD}}{R_D})$$

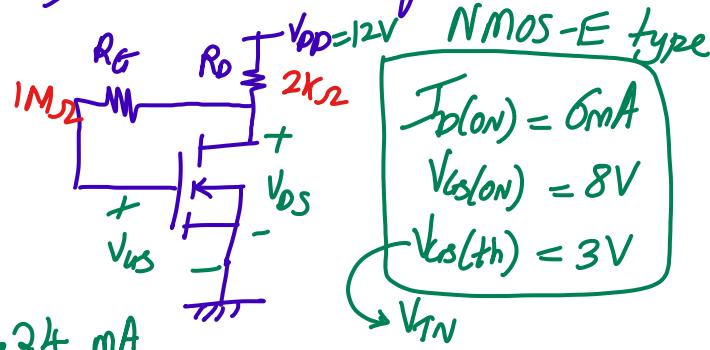


Numerical 1:- Find V_{GS} , I_D and V_{DS} for the ckt shown below:-

Solution:

$$R_n = \frac{I_{D(on)}}{\left[V_{GS(on)} - V_{GS(th)} \right]^2}$$

$$R_n = \frac{6 \text{ mA}}{(8-3)^2} = 0.24 \frac{\text{mA}}{\text{V}^2}$$



$$\rightarrow V_{GS} = V_{DD} - I_D R_D ; V_{GS} = 12 - I_D (2000) \quad \text{--- (1)}$$

Assuming NMOS-E type device is in saturation region

$$I_D = R_n (V_{GS} - V_{GS(th)})^2 = 0.24 \times 10^{-3} (V_{GS} - 3)^2 \quad \text{--- (2)}$$

$$\text{Put (2) in (1), we get} \rightarrow V_{GS} = 12 - 0.48 (V_{GS} - 3)^2$$

$$\rightarrow V_{GS} = 12 - 0.48 (V_{GS}^2 - 6V_{GS} + 9)$$

$$\rightarrow V_{GS} = 12 - 0.48 V_{GS}^2 + 2.88 V_{GS} - 4.32$$

$$\rightarrow 0.48 V_{GS}^2 - 1.88 V_{GS} - 7.68 = 0$$

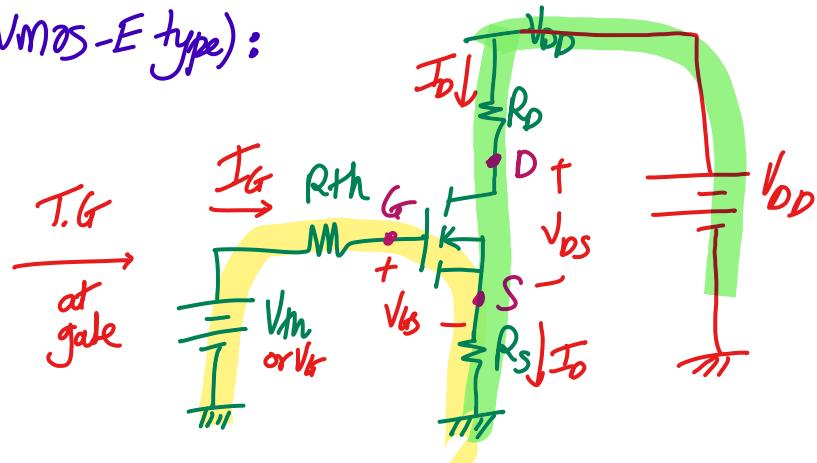
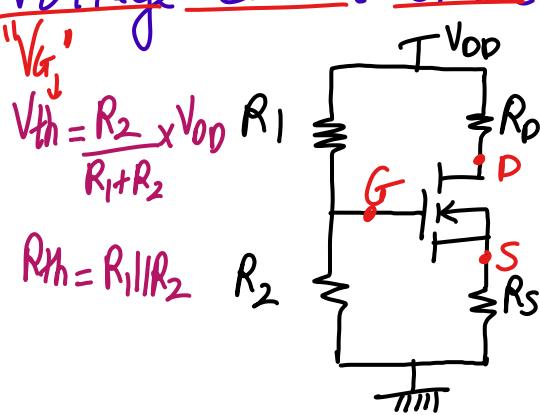
$$\begin{aligned} V_{GSQ} &= \frac{6.41}{V} & V_{GSQ} &= \frac{-2.49}{V} \\ (\because V_{GS} > V_{TN}) & & \text{Reject!} & \end{aligned}$$

$$V_{DSQ} = 6.41 \text{ V} = V_{DS(on)}$$

$$I_{DQ} = R_n (V_{GSQ} - V_{TN})^2 = 0.24 \times 10^{-3} (6.41 - 3)^2$$

$$I_{DQ} = 2.79 \text{ mA}$$

Voltage-div. dev. bias (NMOS-E type):



KVL to G-S loop, $V_{th} - I_G R_{th} - V_{bs} - I_D R_S = 0$; $I_G = 0$

$$V_{bsq} = V_{th} - I_D R_S; I_D = R_n (V_{bs} - V_{tn})^2$$

KVL to D-S loop, $V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$$V_{DSq} = V_{DD} - I_D (R_D + R_S)$$

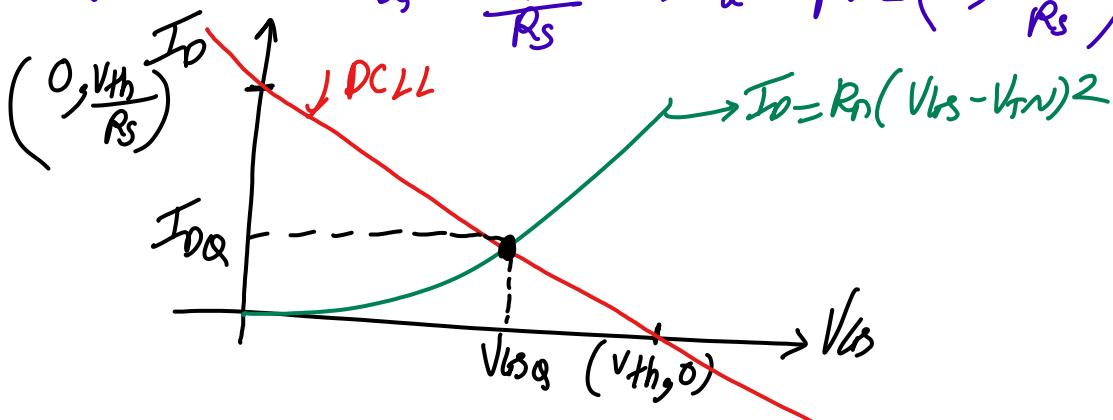
→ To find Q-pt graphically,

$$V_{bsq} = V_{th} - I_D R_S$$

— load-line equation

a) $I_D = 0 \rightarrow V_{bsq} = V_{th} \rightarrow 1^{st} \text{ pt} \equiv (V_{th}, 0)$

b) $V_{bsq} = 0 \rightarrow I_D = \frac{V_{th}}{R_S} \rightarrow 2^{nd} \text{ pt} \equiv (0, \frac{V_{th}}{R_S})$



Numerical 1: Find V_{bs} , I_D , V_{DS} for ckt shown below:-

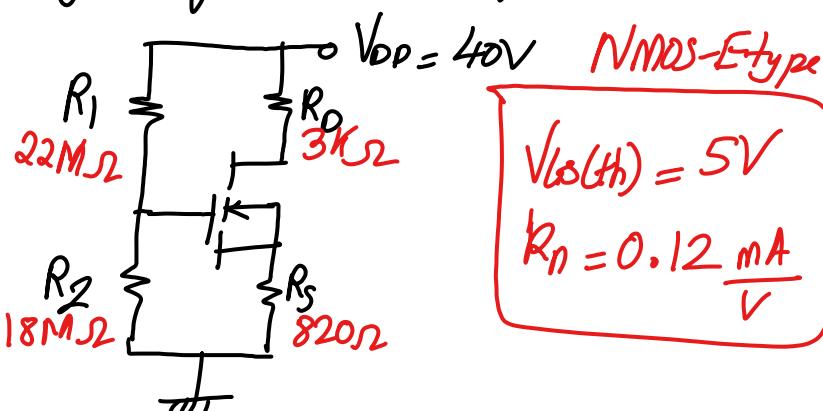
Also, find region of operation of given device


NMOS-E

Solution:

a) $V_{th} = \frac{R_2}{R_1 + R_2} V_{DD}$

$$V_{th} = \frac{18}{22+18} \times 40 = 18 \text{ V}$$



$$V_{bs(th)} = 5V$$

$$R_n = 0.12 \frac{mA}{V}$$

b) $V_{bsq} = V_{th} - I_D R_S = 18 - I_D (820) \quad \text{--- (1)}$

c) Assuming given device is working in saturation region

$$d) I_{DQ} = k_n (V_{BS} - V_{TN})^2 \quad V_{TN} = V_{BS(\text{th})} = V_{TO}$$

$$I_{DQ} = 0.12 \times 10^{-3} (V_{BSQ} - 5)^2 - ②$$

e) Put eqn ② in eqn ①, we get

$$V_{BSQ} = 18 - 820 \times 0.12 \times 10^{-3} (V_{BSQ}^2 - 10V_{BSQ} + 25)$$

$$V_{BSQ} = 18 - 0.0984 (V_{BSQ}^2 - 10V_{BSQ} + 25)$$

$$V_{BSQ} = 18 - 0.0984 V_{BSQ}^2 + 0.984 V_{BSQ} - 246$$

$$\rightarrow 0.0984 V_{BSQ}^2 + 0.016 V_{BSQ} - 15.54 = 0$$

:

$$\checkmark V_{BSQ} = 12.48 \text{ V} \quad \text{or} \quad V_{BSQ} = -12.64 \text{ V}$$

(V_{BS} > V_{TN}) Reject

$$\rightarrow I_{DQ} = k_n (V_{BS} - V_{TN})^2 = 0.12 \times 10^{-3} (12.48 - 5)^2$$

$$I_{DQ} = 6.72 \text{ mA}$$

$$\rightarrow V_{DSQ} = V_{DD} - I_D (R_o + R_s) = 40 - 6.72 \times 10^{-3} (3k + 820)$$

$$V_{DSQ} = 14.32 \text{ V}$$

$$\rightarrow \begin{cases} V_{BSQ} > V_{TN} \quad (12.48 \text{ V} > 5 \text{ V}) \end{cases} \checkmark$$

$$\begin{cases} V_{BSQ} > (V_{BSQ} - V_{TN}) \rightarrow [14.32 > (12.48 - 5)] \end{cases} \checkmark$$

Given device is indeed in saturation region

— X —

