Course Code		Course Type	LTP
CSA2003	DIGITAL LOGIC AND COMPUTER ARCHITECTURE	Credits	4

Course Objectives:

- To prove the knowledge of combinational circuit design.
- To impart the knowledge of Sequential circuit design.
- To impart the Computer Organization and Design.

Course Outcomes:

- Design and analyze combinational & sequential circuits
- Understand counters and sequence generators.
- Understand the basics of instructions sets and their impact on processor design.
- Demonstrate an understanding of the design of the functional units of a digital computer system.
- Design a pipeline for consistent execution of instructions with minimum hazards.

Student Outcomes (SO): a, b, c, e, l

a. An ability to apply the knowledge of mathematics, science, and computing appropriate to the discipline.

b. An ability to analyze a problem, identify and define the computing requirements appropriate to its solution.

c. An ability to design, implement, and evaluate a system / computer-based system, process, component, or program to meet desired needs.

e. An ability to identify, formulate, and solve engineering problems.

l. An ability to apply mathematical foundations, algorithmic principles, and computer science theory in the modeling and design of computer-based systems (CS)

Module No.	Module Description	Hours	SO
1	**Principles of combinational logic:** Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.	6	b, e
2	**Sequential Circuits**: Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Multiplexer , De-Multiplexer. Analysis and design of clocked sequential circuits – Design – Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.	10	b, c, l
3	**Basic Computer Organization and Design:**Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt-Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.	10	a, b, e
4	**Memory and Addressing unit:** Control memory, Address sequencing, design of control unit-General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.	10	b, c, e

5	**Data Representation:** Data types, Complements, Fixed Point Representation, Floating Point Representation. Computer Arithmetic**:** Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations-Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.	7	b,c, e, l
6	**Guest Lecture on Contemporary Topics**	**2**	
	Total Hours	**45**	

Mode of Teaching and Learning: Flipped Class Room, Activity Based Teaching/Learning, Digital/Computer based models, wherever possible to augment lecture for practice/tutorial and minimum 2 hours lectures by industry experts on contemporary topics

Mode of Evaluation and assessment: The assessment and evaluation components may consist of unannounced open book examinations, quizzes, student's portfolio generation and assessment, and any other innovative assessment practices followed by faculty, in addition to the Continuous Assessment Tests and Term End Examinations

Text Book(s)

1.	Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
2.	Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI.
3	Digital Logic Applications and Design John M Yarbrough Cengage Learning 2011

Reference Books

1.	Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.
2.	Digital Principles and Design Donald D Givone McGraw Hill Education 1 st Edition, 2002

Indicative List of Experiments

No.	Description of Experiment	SO
1	Design and verify the truth table of logic gates	**l**
2	To simplify the given expression and to realize it using Basic gates and Universal gate	**l**
3	. To Design and implement the circuit for the following 4-bit Code conversion. i) Binary to Gray Code ii) Gray to Binary Code	**l**
4	To realize a. Half Adder and Full Adder b. Half Subtractor and Full Subtractor by using Basic gates and NAND gates	**l**
5	a. Truth Table verification of 1) RS Flip Flop 2) T type Flip Flop. 3) D type Flip Flop. 4) JK Flip Flop. b. Conversion of one type of Flip flop to another.	**l**
6	. a.To design and set up a 4:1 Multiplexer (MUX) using only NAND gates. b. To design and set up a 1:4 Demultiplexer(DE-MUX) using only NAND gates.	**1**

7	Implementation of a 3 bit SIPO and SISO shift register using flip flops.	**1**
8	Implementation of a 3 bit PIPO and PISO shift register using flip flops	**l**
9	Design and verify the 4-bit synchronous counter	**l**
10	Design and verify the 4-bit asynchronous counter.	**l**

Recommendation by the Board of Studies on	
Approval by Academic council on	
Compiled by	**Dr.Saravanan S**