Hardware–Software Co-Design of a Mixed-Signal AI Accelerator for Edge Robotics

1. Project Overview

Objective:

To design and implement a Smart Sensor System capable of real-time fault detection in robotics by integrating an Analog Front-End (AFE) and a custom Digital Hardware Accelerator on a single chip, eliminating the need for power-hungry external processors.

Key Innovation:

A mixed-signal co-design approach that combines transistor-level analog design (Cadence Virtuoso) with RTL-based digital logic (Verilog), bridged by an 8-bit quantization scheme.

2. System Architecture

- Analog Domain (Cadence): Signal sensing, amplification, and filtering
- Software Domain (Python): AI training, weight optimization, quantization
- Digital Domain (Verilog/FPGA): Low-power inference and control logic

3. Phase-by-Phase Implementation Plan

Phase 1: AI Model Development (Python)

- Dataset: 1D vibration time-series data (normal vs faulty states)
- Model: Multi-Layer Perceptron (MLP)
- Quantization: 32-bit float → 8-bit INT8
- Deliverable: weights.hex

Phase 2: Analog Front-End Design (Cadence Virtuoso)

- Two-Stage CMOS Operational Amplifier
- Input: 2–5 mV weak sensor signal
- Gain > 60 dB with noise filtering
- Output: 0–1.8 V clean signal
- Deliverable: transient response .csv

Phase 3: Data Conversion Interface

- Python-based virtual ADC
- Mapping 0–1.8 V → 0–255 (8-bit)
- Deliverable: sensor_data.hex

Phase 4: Verilog Hardware Accelerator

- MAC Unit for multiply-accumulate operations
- Sensor ROM for input simulation
- Control FSM for synchronized processing
- Deliverable: accelerator_top.v

Phase 5: Simulation and Power Analysis

- Tool: Xilinx Vivado
- Functional verification with testbench
- Accuracy comparison with Python model
- Dynamic and static power analysis

Phase 6: FPGA Physical Implementation

- Platform: Artix-7 / Zynq-7000
- Synthesis, implementation, and bitstream generation
- LED indicators for classification output

4. Research Novelty and Impact

- Complete hardware–software co-design workflow
- Low-power edge AI inference using INT8 quantization
- Mixed-signal integration from analog circuits to digital logic

5. Hardware Specifications

Parameter	Specification
Technology Node	180nm CMOS (Analog) / 28nm FPGA (Digital)
Data Precision	8-bit Integer (INT8)
Clock Frequency	50–100 MHz
Power Consumption	< 50 mW (Target)
Response Time	< 1 microsecond

6. Conclusion

The project demonstrates a specialized mixed-signal AI accelerator for robotics that optimizes the entire signal chain from analog sensing to digital decision-making. The system achieves low latency, low power consumption, and real-time fault detection, making it suitable for next-generation autonomous edge devices.