Objective

The design of MOD-13, synchronous, binary ‘up’ counter (using TannerEDA software for simulation purposes).

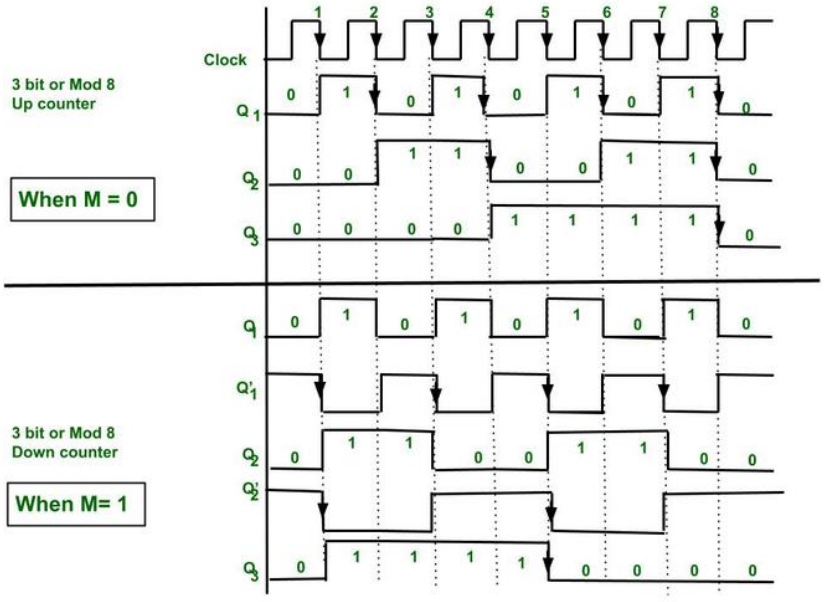
Abstract

A short report has been made on process of designing and synthesizing a MOD-13 synchronous-up counter using 250nm technology transistors. The design has used sequential logic in the form of flip-flops, and logic gates. Simulations of circuit functions are carried out and verified against its theoretical solutions. The functions are then integrated with flip flops to generate a “count-up” counter. The counter begins at 0, its first state, and advances by one state until 12, before returning to its first state.

Theory

A digital counter is an electronic device that counts from 0 to 2^N-1 bits. Digital counters are usually driven by a clock pulse signal, and implemented using various electronic components such as flip-flops, registers, and logic gates. The job of a counter is to count by advancing the contents of the counter by one count with each clock pulse.

The most widely used scheme is a sequential circuit consisting of flip flops and a clock signal. A wide array of flip flops can be used to design counters based on specifications or applications. A ‘count-up’ counter is one which advances its sequence of numbers (states) by ‘one’ when activated by a clock input.



Digital counters have different kinds, each is suitable for a certain application, they can be broadly classified into two groups: synchronous counters and asynchronous(ripple) counters.

Synchronous counters

A synchronous counter is a category under the general digital counters, that uses a clock signal to synchronize the state changes of its output signals. All states of the counter change to its next state, advancing up or down, whenever the edge of the clock is triggered.

Asynchronous counters

In such counters, the state changes propagate sequentially from one flip-flop to another, causing a ‘ripple-effect’ through the counter.

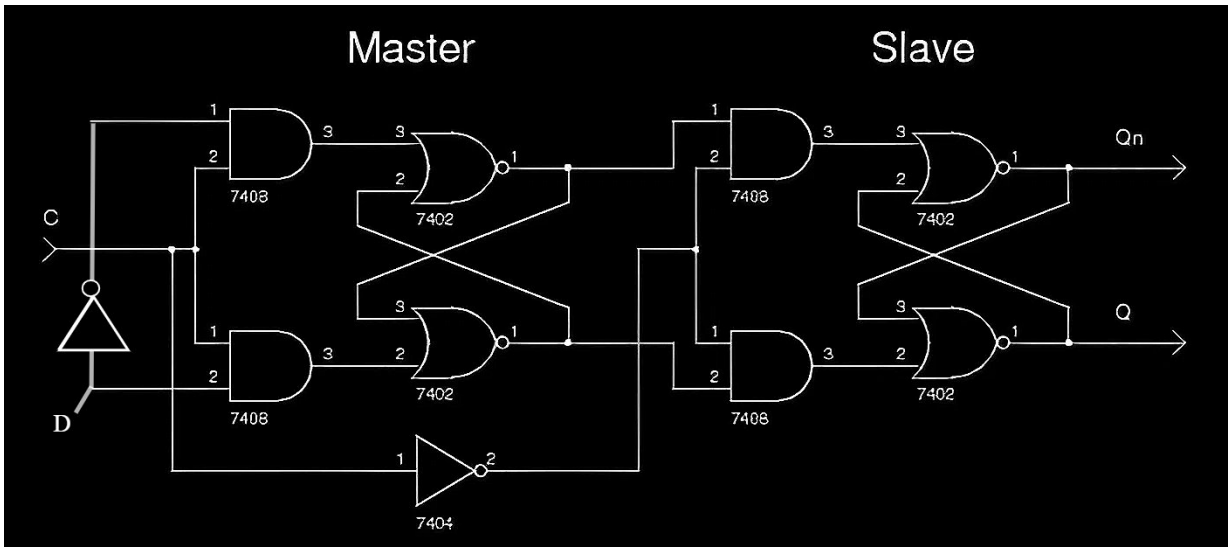
MOD-N counter

Modulus Counters, or simply MOD counters, are defined based on the number of states that the counter will sequence through before returning back to its original value. In the case of mod-13 ‘up’ counter, the counter shall advance by one state, from 0 to 12 (12 states), before returning to its first state 0. The state changes are done in binary form, where each flip-flop stores 1-bit of the binary form.

D Flip-Flop

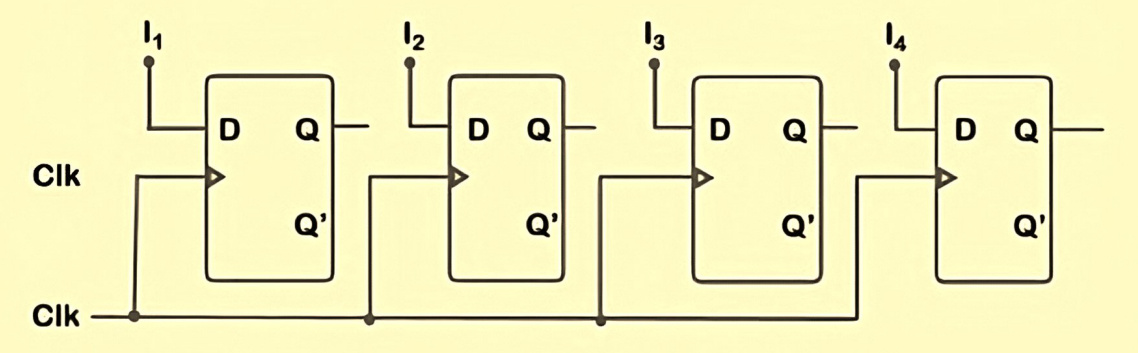
D flip-flop or Data flip flop is a type of flip Flop that has only one data input that is **D,** and one clock pulse input with two outputs **Q** and **Q bar ($\overline{Q}$).** It is the basic Building Block of counters in general.

A **master-slave** flip-flop comprises two latches – a **master** latch, and a **slave** latch. This configuration eliminates any transparency in the flip-flop: a change occurring in primary inputs is never reflected directly to the outputs, since opposite phase clocks are used to activate the M and S latches.



Master-Slave D-Flip Flop

In our project, we shall consider a MOD-13, synchronous 'up' counter using **master slave D-Flip Flop**.The computation of number of flip-flops, given by the relation $2^N \geq M$, for a mod-M counter, has resulted in requirement of **4** 'D master-slave' flip-flops.



Example of 4-bit Counter

Design of a MOD-13 counter

Input	Current State		Next State	
D	Q	$\bar{Q}$	Q_{next}	$\bar{Q}_{next}$
0	0	1	0	1
0	1	0	0	1
1	0	1	1	0
1	1	0	1	0

Q	Q_{next}	D
0	0	0
1	0	0
0	1	1
1	1	1

The truth table is shown below:

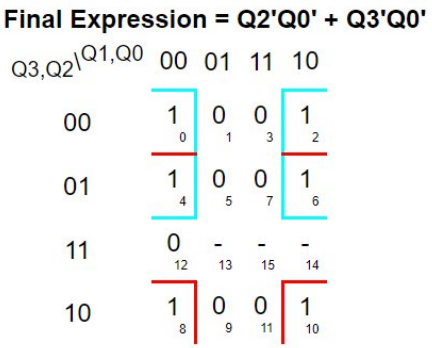
	Present state				Next state			
No	Q3	Q2	Q1	Q0	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
10	1	0	1	0	1	0	1	1
11	1	0	1	1	1	1	0	0
12	1	1	0	0	0	0	0	0
13	1	1	0	1	x	x	x	x
14	1	1	1	0	x	x	x	x
15	1	1	1	1	x	x	x	x

Karnaugh-maps for output expressions

The flip-flop output expressions can be obtained using Karnaugh-maps, as following:

1. Expression for D0 input of first flip-flop

D0	Q1Q0				
Q3Q2		00	01	11	10
	00	1	0	0	1
	01	1	0	0	1
	11	0	X	X	X
	10	1	0	0	1

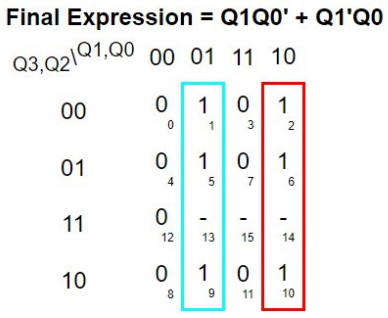


Simplifying the Boolean expression, we get:

$$\boldsymbol{D0 = \overline{Q0}\left(\overline{Q3} + \overline{Q2}\right)}$$

2. Expression for D1 input of second flip-flop

D1	Q1Q0				
Q3Q2		00	01	11	10
	00	0	1	0	1
	01	0	1	0	1
	11	0	X	X	X
	10	0	1	0	1



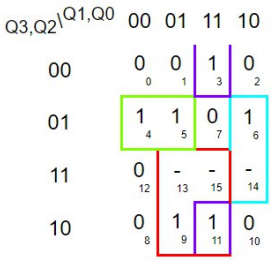
Simplifying the expression,

$$\boldsymbol{D1 = \overline{Q1} \oplus \overline{Q0}}$$

3. Expression for D2 of 3rd flip-flop

D2	Q1Q0				
Q3Q2		00	01	11	10
	00	0	0	1	0
	01	1	1	0	1
	11	0	X	X	X
	10	0	1	1	0

Final Expression = Q3Q0 + Q3'Q2Q1' + Q2Q1Q0' + Q2'Q1Q0



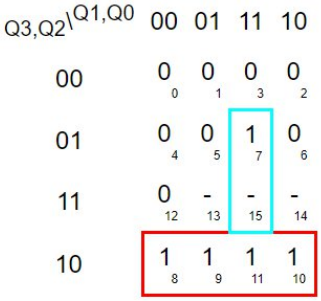
Simplifying the expression,

$$D2 = \overline{Q2}Q1Q0 + \overline{Q3}Q2\left(\overline{Q1} + \overline{Q0}\right)$$

4. Expression for D3 of 4th flip-flop

D3	Q1Q0				
Q3Q2		00	01	11	10
	00	0	0	0	0
	01	0	0	1	0
	11	0	X	X	X
	10	1	1	1	1

Final Expression = Q3Q2' + Q2Q1Q0

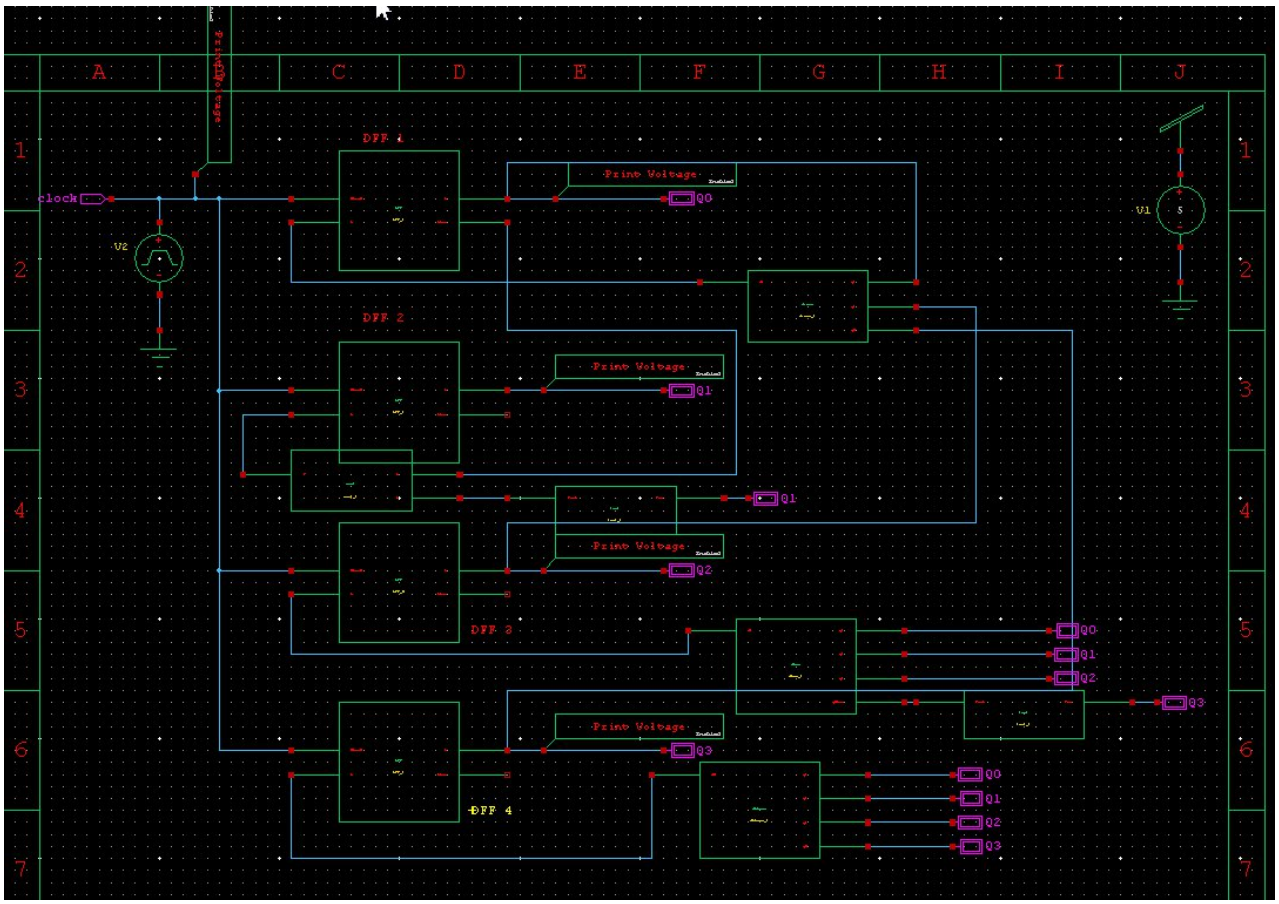


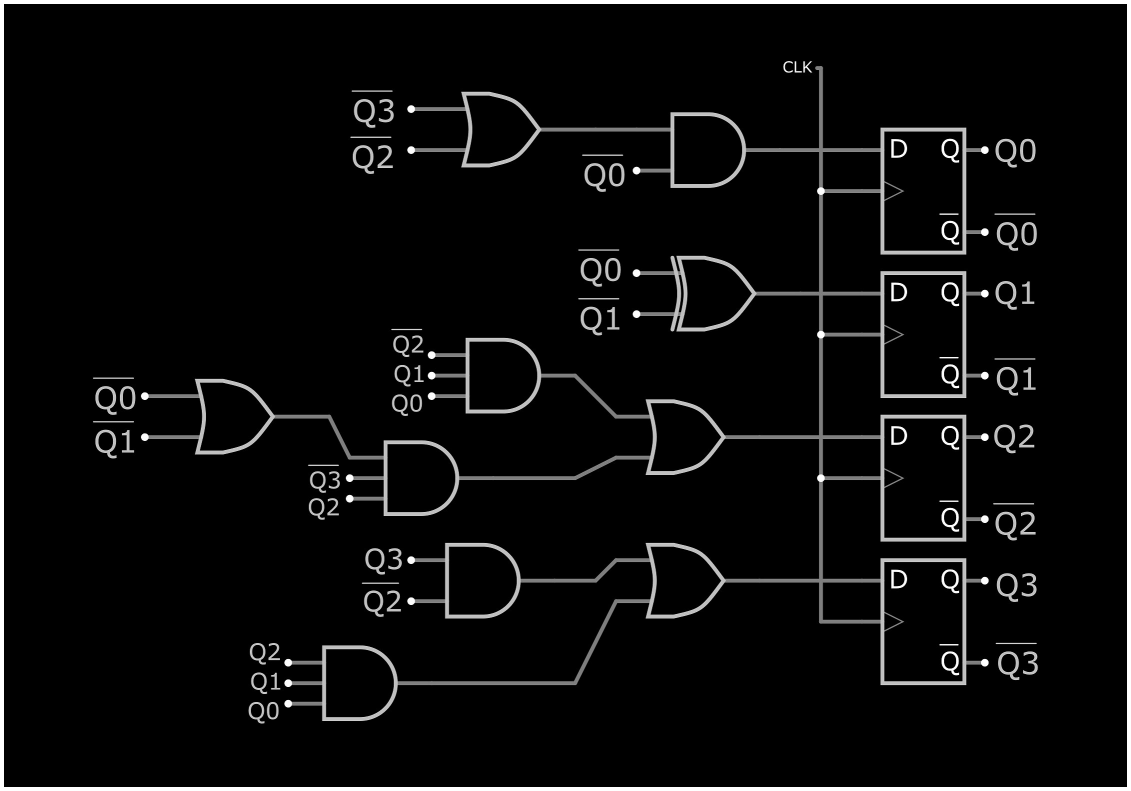
Simplifying the expression,

$$D3 = Q3\overline{Q2} + Q2Q1Q0$$

IMPLEMENTATION AND RESULTS

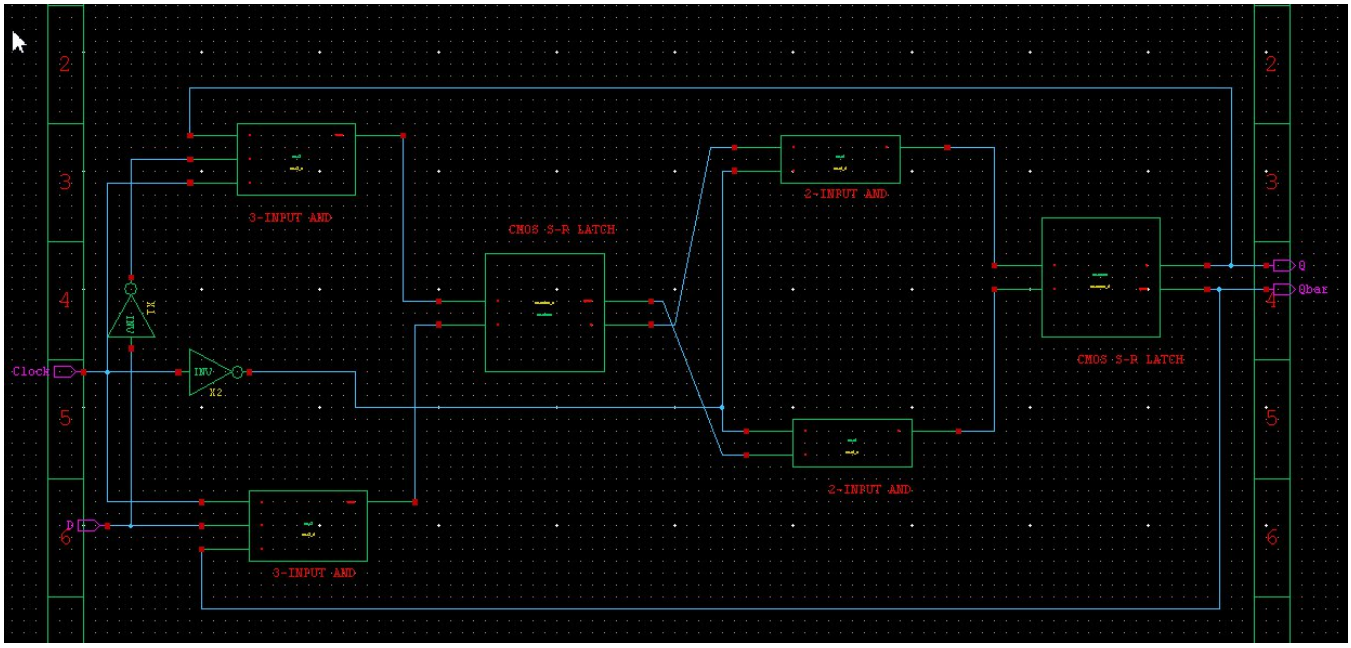
CIRCUIT SCHEMATIC



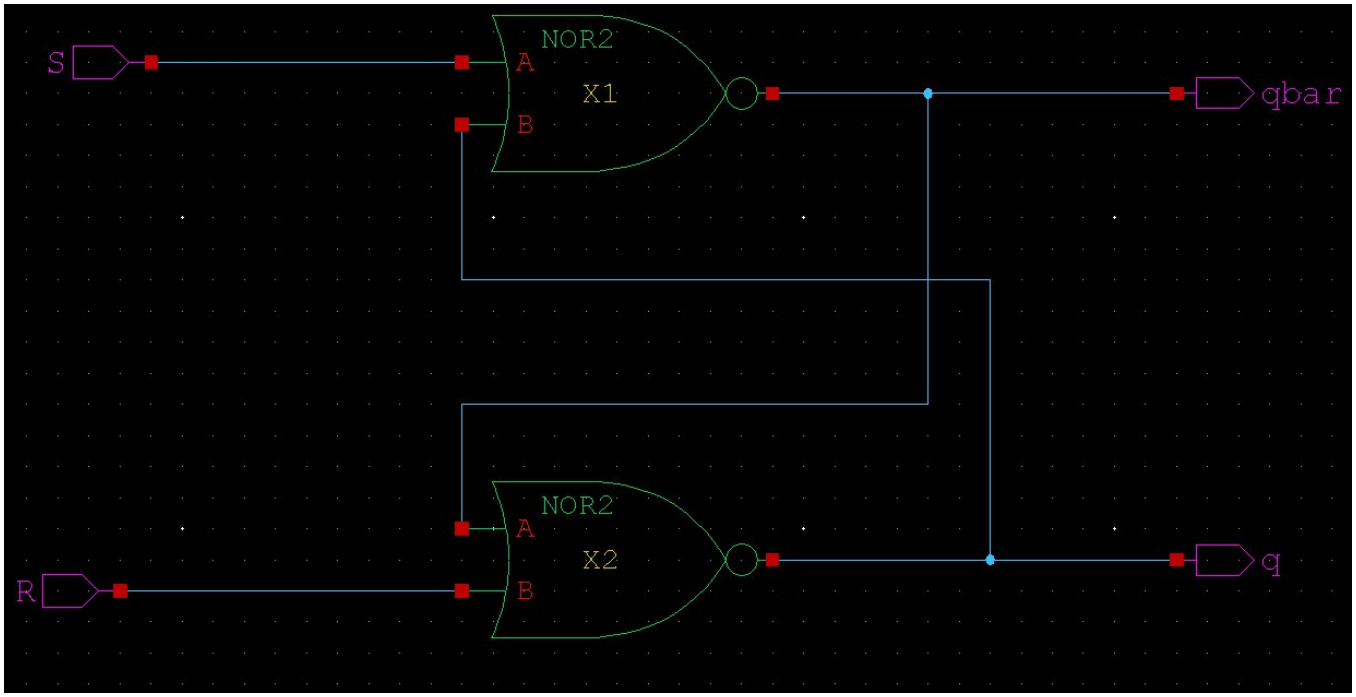


SEQUENTIAL LOGIC

D – FLIP FLOP UTILISING MASTER-SLAVE FLIP FLOP LOGIC

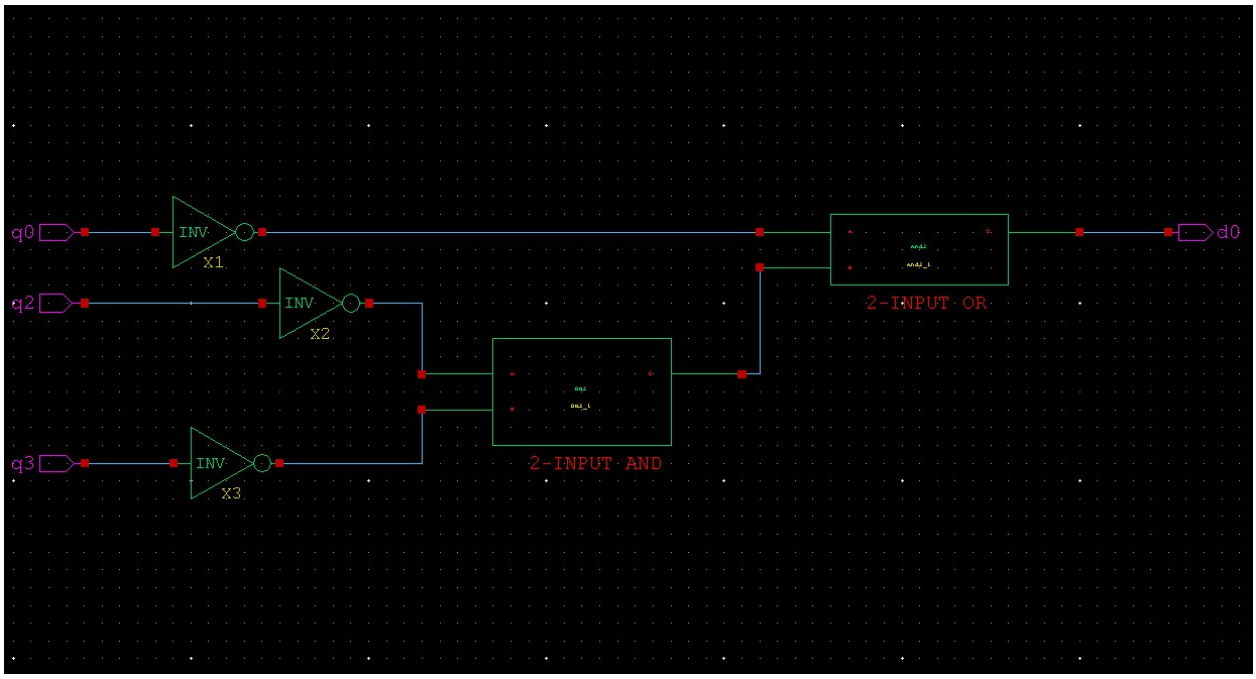


CMOS S-R LATCH

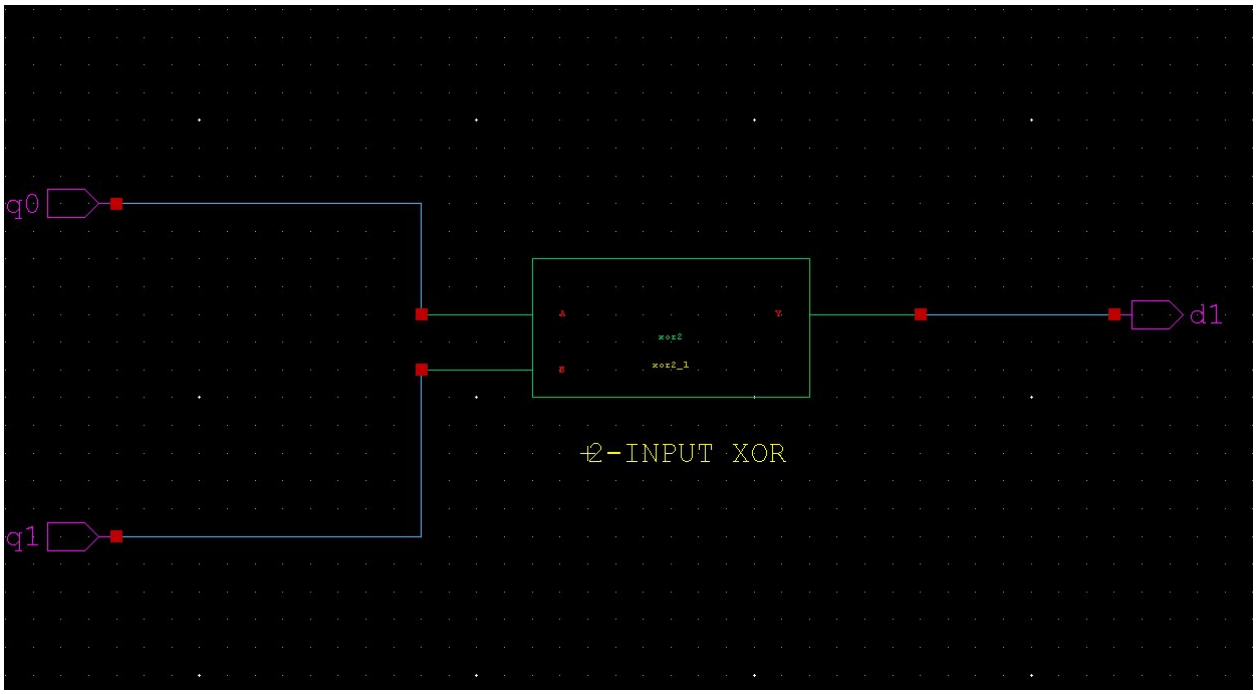


COUNTER – D INPUTS' EXPRESSION SCHEMATICS

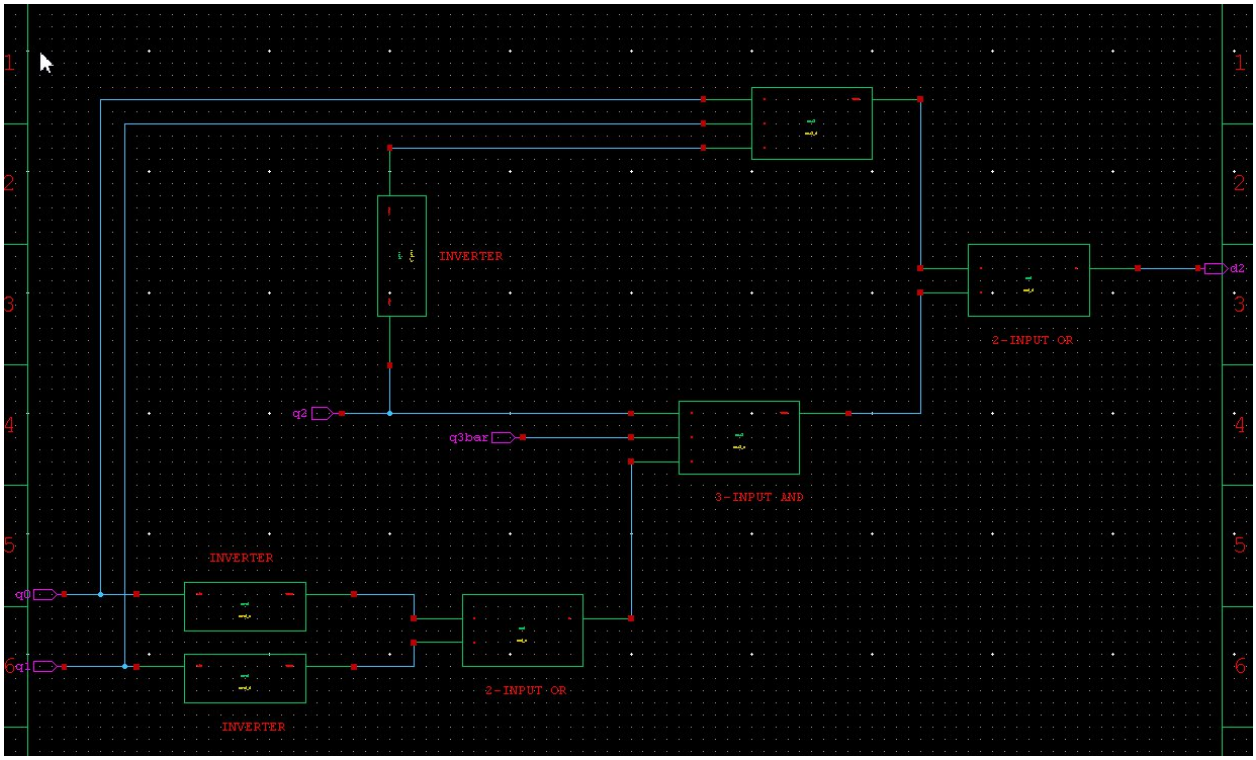
1. D0



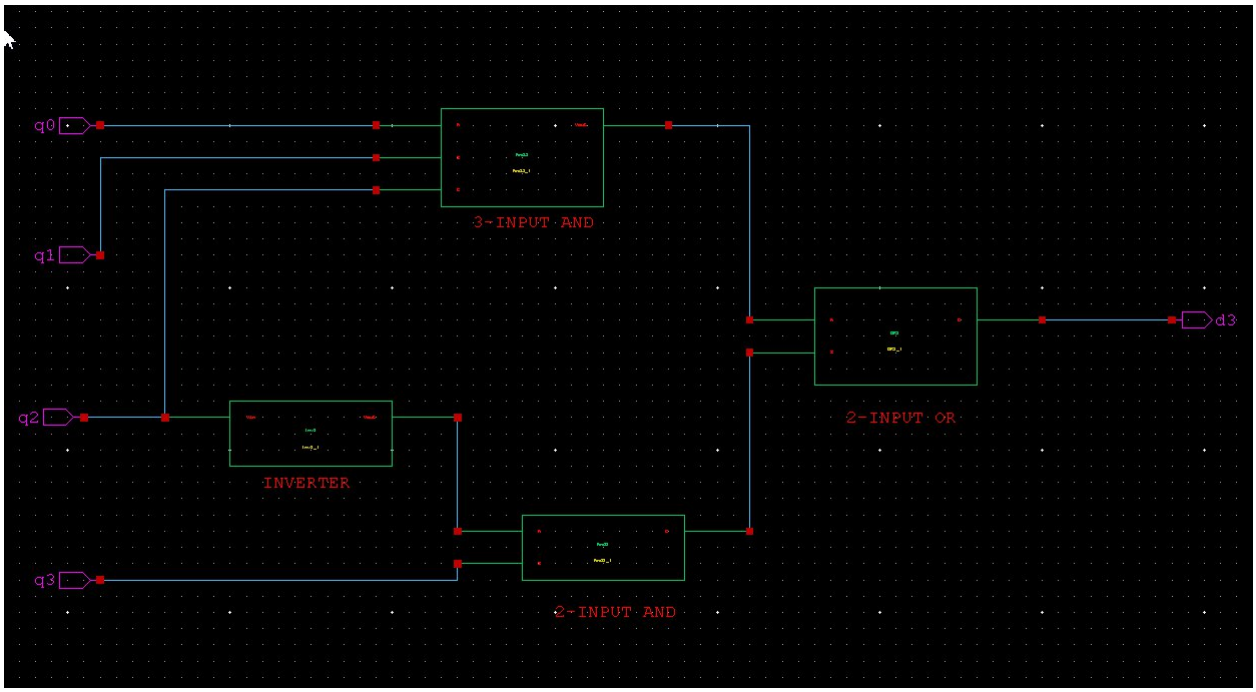
2. D1



3. D2

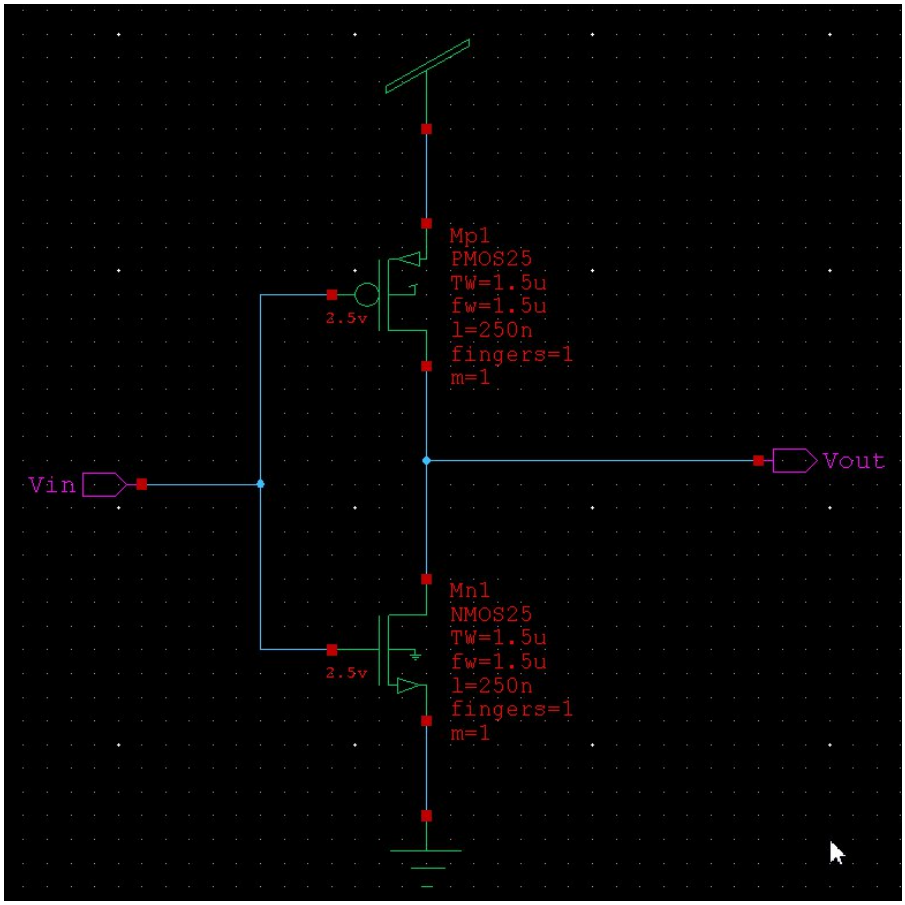

INVERTER
q2
q3bar
3-INPUT AND
2-INPUT OR
d2
INVERTER
q0
q1
2-INPUT OR
INVERTER

4. D3


q0
3-INPUT AND
q1
d3
2-INPUT OR
q2
INVERTER
q3
2-INPUT AND

COMBINATIONAL LOGIC

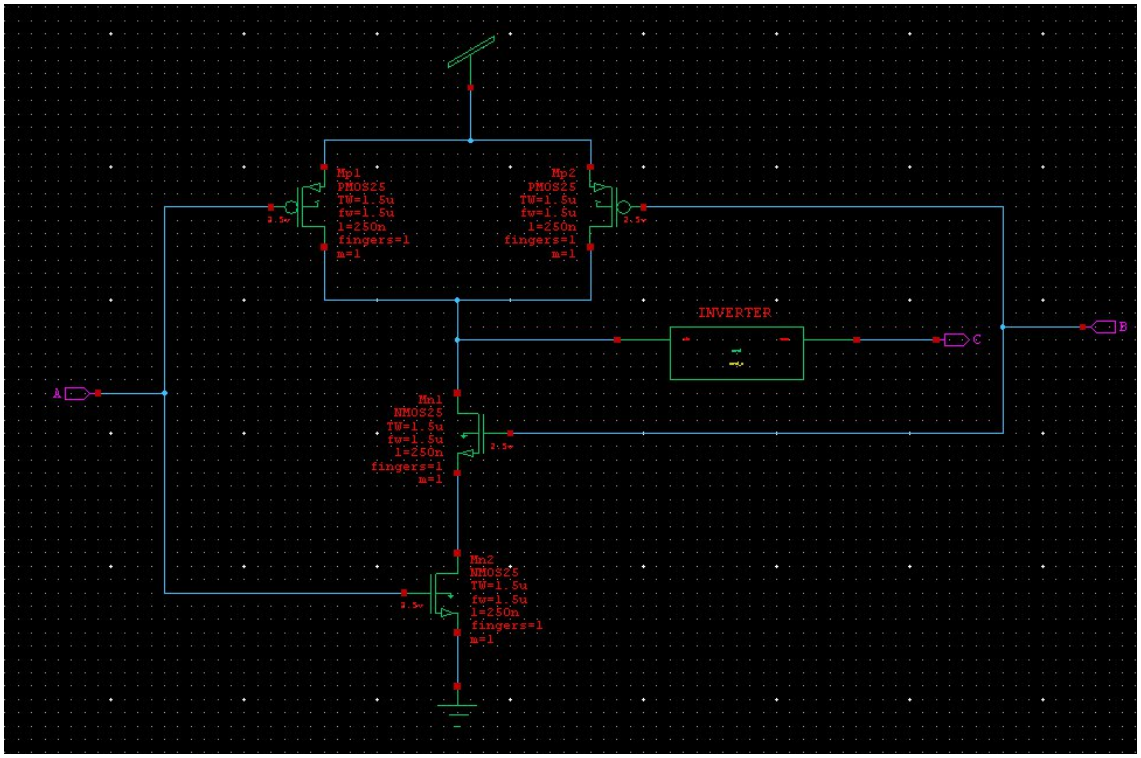
CMOS INVERTER



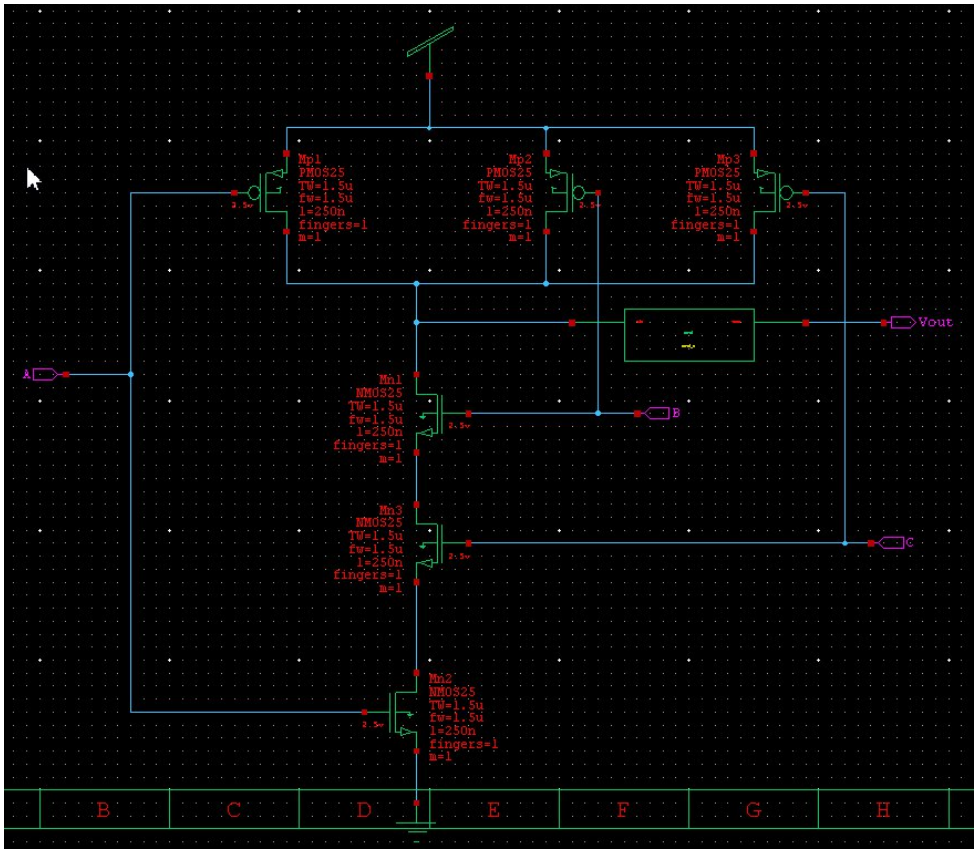
The CMOS logic circuit is the foundational logic behind the design of every sequential and combinational logic used in the project, for the simulation of mod-13 synchronous ‘up’ counter. The CMOS circuit comprises a pull-up network (pMOS) and a pull-down network (nMOS).

The CMOS inverter performs the same functionality as a normal, static inverter. A category of CMOS inverter – the BiCMOS inverter is advantageous in design process due to its fast circuits and low power dissipation.

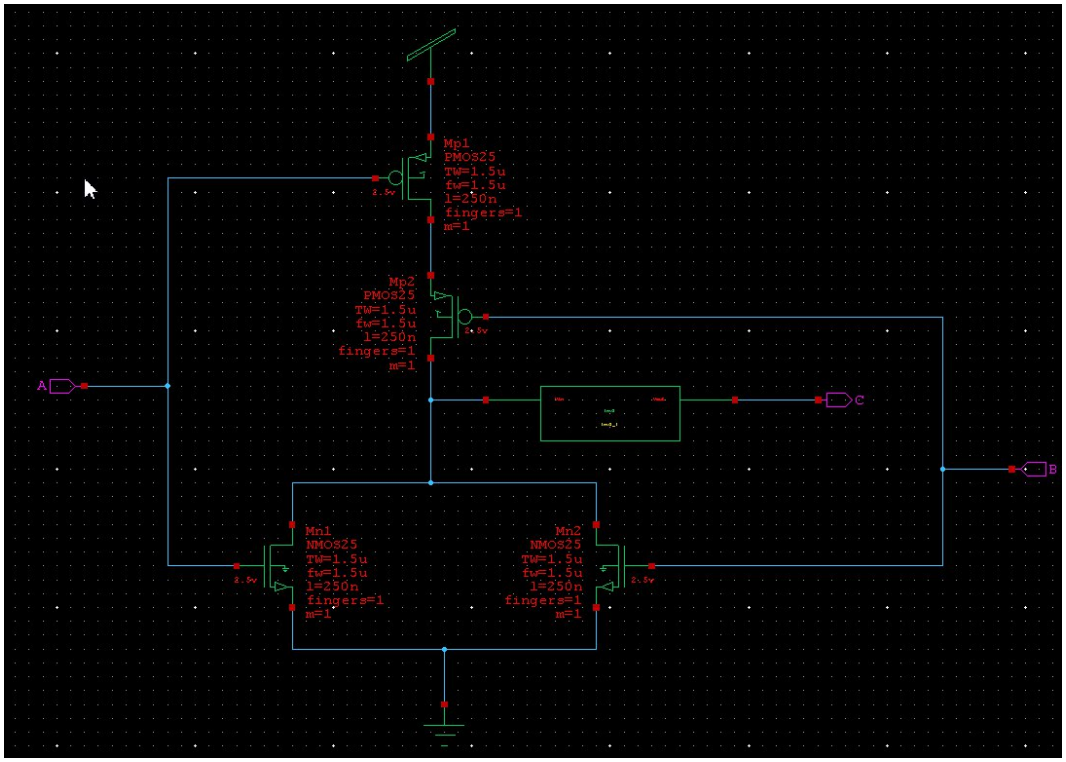
1. 2-INPUT AND GATE



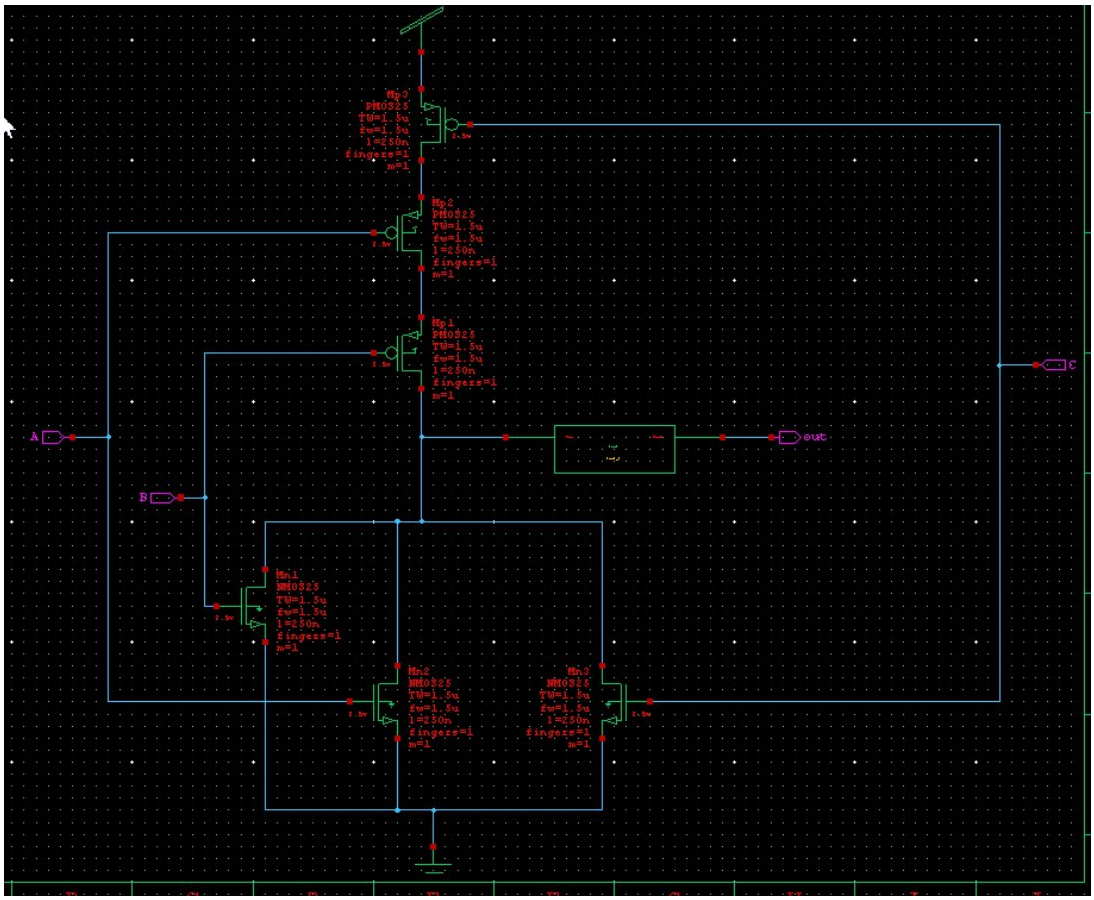
2. 3-INPUT AND GATE



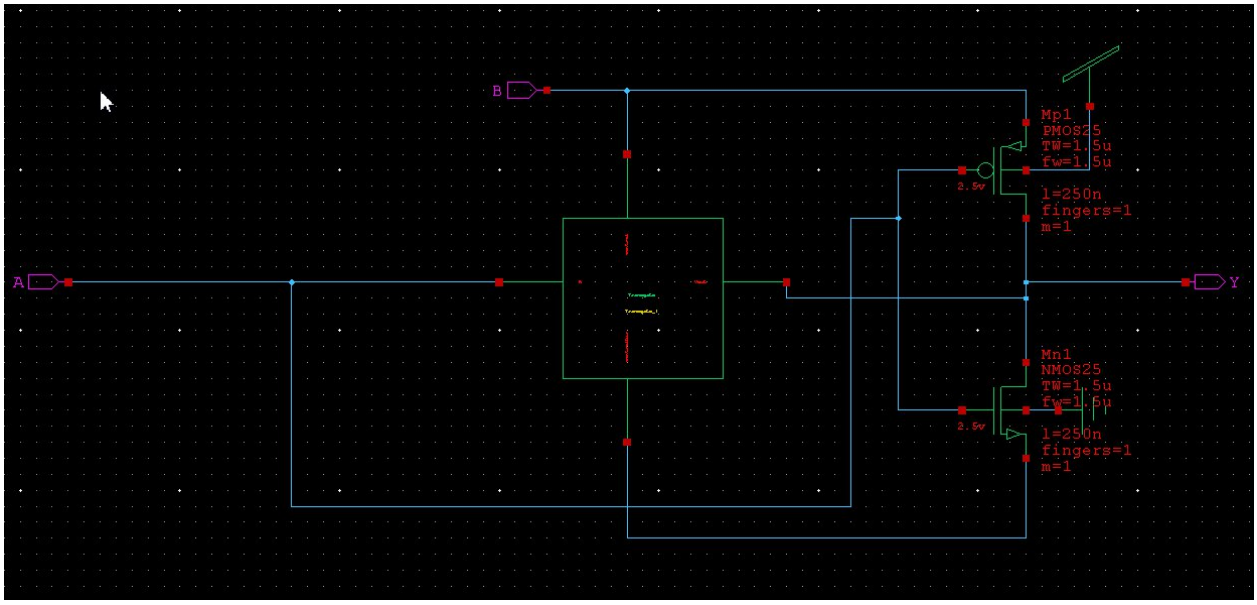
3. 2-INPUT OR GATE



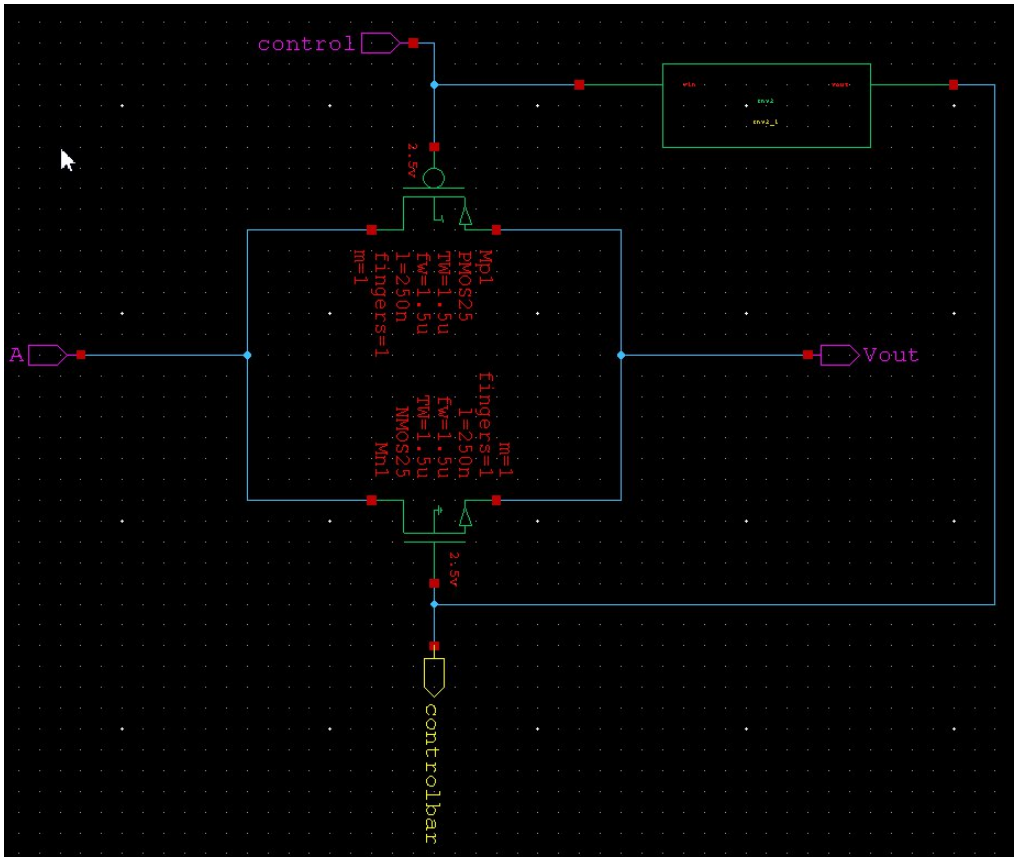
4. 3-INPUT OR GATE



5. 2-INPUT XOR GATE



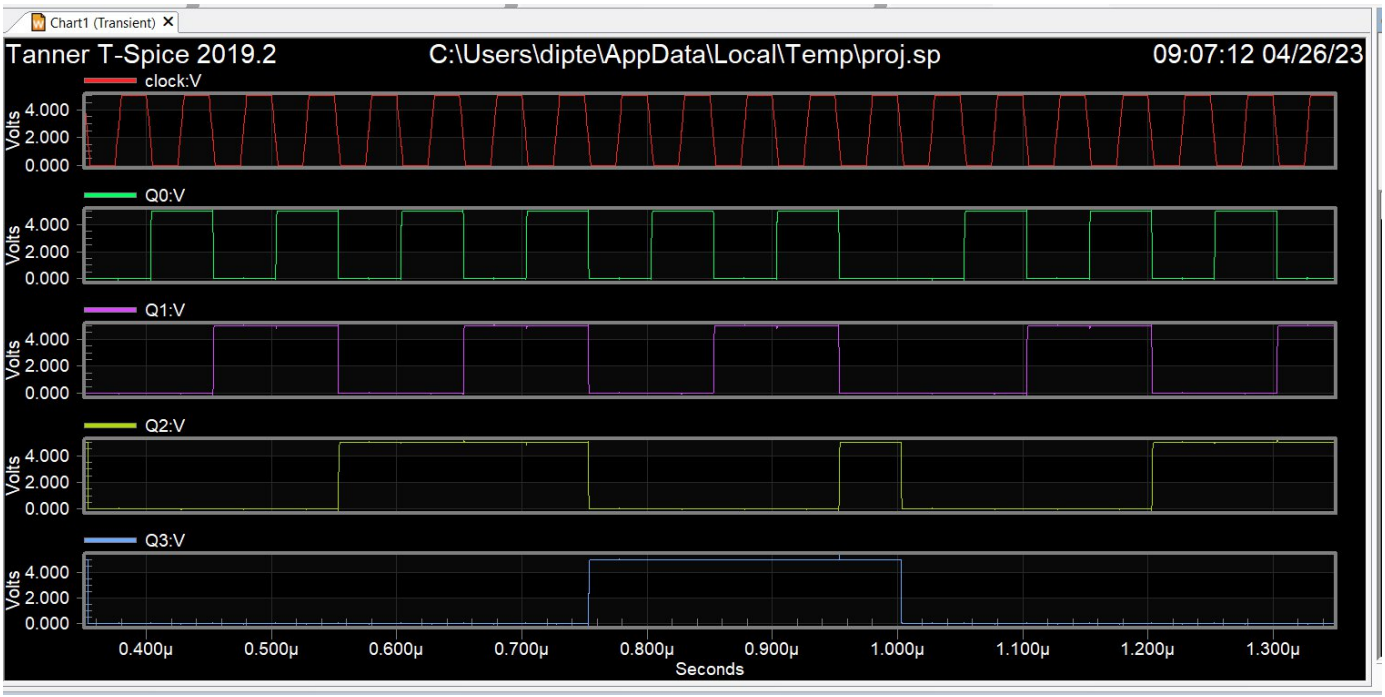
6. TRANSMISSION GATE



RESULTS

The waveform from simulation suggests that the counter starts from the first state, that is 0, and advances by one state at every **negative edge of the clock.** The final state seems to rest at **1100,** that is the binary equivalent of decimal number **12.** The counter then ‘restarts’ or refreshes back to zero and counts ‘up’ again. There is no external signal behaving as a trigger in the circuit.

MOD-13 COUNTER WAVEFORM



Applications

1. Motion control of the machine
2. Rotating Shaft Encoders
3. Alarm systems
4. Set time in camera to take the picture
5. digital to analog (DAC) converters
6. Digital clocks and multiplexing circuits