



K.S.Institute of Technology, Bangalore

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

ASSIGNMENT QUESTIONS

Academic Year	2021-2022		
Batch	2018-2022		
Year/Semester/section	IV/VII 'A' & 'B'		
Course Code-Title	18CS733/ Advanced Computer Architectures		
Name of the Instructors	Dr. Vijayalaxmi Mekali	Dept	CSE

Assignment No: 2		Total marks:10		
Date of Issue: 21-12-2021		Date of Submission: 3-1-2022		
Sl.No	Assignment Questions	K Level	CO	Marks
1.	Model the Register-to-Register and Memory-to-Memory Architectural types a Vector processors.	Applying (K3)	CO2	1
2.	List and Explain the characteristics of Symbolic Processors.	Applying (K3)	CO2	1
3.	Illustrate the following a. Daisy chained arbitration technique b. Distributed arbitration technique	Applying (K3)	CO3	1
4.	List the various Cache mapping schemes. Make use of a neat diagram to explain all the mapping techniques	Applying (K3)	CO3	1
5.	Illustrate the following techniques associated with cache and memory architecture a. Low order memory interleaving. b. High order memory interleaving. c. Memory bandwidth and fault tolerance	Applying (K3)	CO3	1
6.	Model the synchronous and Asynchronous bus timing protocols	Applying (K3)	CO3	1
7.	Illustrate the features of nonlinear pipeline processor with feed forward and feed backwards connection	Applying (K3)	CO3	1

8.	<p>Consider the following reservation table for a 4-state pipeline with a clock cycle $\tau = 2ns$</p> <table border="1"> <tr> <td></td><td>1</td><td>2</td><td>3</td><td>4</td></tr> <tr> <td>S1</td><td>X</td><td></td><td></td><td>X</td></tr> <tr> <td>S2</td><td></td><td>X</td><td></td><td></td></tr> <tr> <td>S3</td><td></td><td></td><td>X</td><td></td></tr> </table> <p>Solve the following</p> <ol style="list-style-type: none"> Forbidden latencies and the initial collision vector Draw the state transition diagram for scheduling the pipeline. Determine the MAL(Minimum Average Latency) with shorted greedy cycle Pipeline throughput corresponding to MAL and to given τ. 		1	2	3	4	S1	X			X	S2		X			S3			X		Applying (K3)	CO3	1
	1	2	3	4																				
S1	X			X																				
S2		X																						
S3			X																					
9	Model the hierarchical bus system with neat diagram	Applying (K3)	CO4	1																				
10.	Illustrate the working of crossbar networks and multiport memory with a neat diagram.	Applying (K3)	CO4	1																				

Course in charge

HOD