Suggestion
CA4
Subject: Computer Organization.

1. What is program counter?
Ans: A program counter (PC) is a CPU register in the computer processor which has the address of the next instruction to be executed from memory. It is a digital counter needed for faster execution of tasks as well as for tracking the current execution point.

2. Floating point representation is used to store what type of value?
Ans: Real Intergers.

3. Is Excess – 3 code is weighted code?
Ans: No. (The excess-3 code (or XS3) is a non-weighted code used to express code used to express decimal numbers.)
Example-2 −Convert decimal number 15.46 into Excess-3 code.
According to excess-3 code we need to add 3 to both digit in the decimal number then convert into 4-bit binary number for result of each digit. Therefore,
= 15.46+33.33=48.79 =0100 1000.0111 1001 which is required excess-3 code for given decimal number 15.46.

4. $(2FADC)_{16}$ is equivalent to $(\underline{00101111101011011100})_2$.

5. The Self – contained sequence of instructions that performs a given computational task is called **function**.

6. Microinstructions are stored in control memory groups, with each group specifying a **Routine**.

7. An interface that provides a method for transferring binary information between internal storage and external devices is called **I / O interface**.

8. If the value $V(x)$ of the target operand is contained in the address field itself, the addressing mode is **direct addressing mode**.

9. The instruction which copy information from one location to another either in the processor's internal register set or in the external main memory are called **Data Transfer Instruction**.

10. The performance of cache memory is frequently measured in terms of a quantity called **Latency ratio.**

11. Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called **relative addressing mode**.

12. **TRAP** is a non – maskable interrupt.

13. What are the parameter which influence the characteristics of a microprocessor?
Ans: Clock Speed, Word Size, Instruction Set.

14. The addressing mode used in an instruction of the form ADD X, Y, is **index addressing** mode.

15. Simplify the following expression using Boolean algebra. X= AB + AB'
Ans: AB + AB' =A(B + B') = A(1) = A.

16. How many flip – flops will be complemented in a 10 – bit binary ripple counter to reach the next count after 1001100111?
Ans: a. First of all add 1 to the given binary number.
　　 b. Then check how many bits are complemented after the addition operation.
　　 c. The number of bits complemented = No. of flip flop complemented outputs.
So, Binary Number = 1001100111 + 1 = 1001101000. So 4 – bits are complemented. Therefore **4 flipflops** are required.

17. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexer. How many selection inputs are there in each multiplexer?

18. An instruction is stored at location 300 with its address fields at location 301. The address field has the value 400. A processor register R1 contain the number 200.
Evaluate the effective address if the addressing mode of the instruction is (a) Direct (b) Immediate (c) Relative (d) Register Indirect (e) Index with R1 as the Index register.

Ans: (a) Direct addressing: Direct addressing means that the address field contains the address of memory location the instruction is supposed to work with (where an operand "resides"). Effective address would therefore be 400.
(b) Immediate addressing: Immediate addressing means that the address field contains the operand itself. Effective address would therefore be 301.
(c) Relative addressing: Relative addressing means that the address field contains offset to be added to the program counter to address a memory location of the operand. Effective address would therefore be 301 + 400 = 701.
(d) Register indirect addressing: Register indirect addressing means that the address of an operand is in the register. The address field in this case contains just another operand. Effective address would therefore be in R1 = 200.
(e) Indexed addressing: There are several possible indexed addressing modes but in this case (the is an address field) it is so called "indexed absolute" addressing. In indexed absolute addressing the effective address is calculated by taking the contents of the address field and adding the contents of the index register. Effective address would therefore be 400 + R1 = 400 + 200 = 600.

19. A computer uses RAM Chips of 1024*1 capacity
a) How many chips are needed and how should their address line be connected to provide a memory capacity of 1024*8
b) How many chips are needed to provide a memory capacity of 16KB
Ans: - a. Memory size is 1024 bytes = 8 x 1024 x 1 RAM = > 8 chips
 All has same address lines and output is one bit from every chip.

b. 16 K bytes = 16 x 1024 x 8 => 128 chips. 16 groups of 8 chips which have same address / chip select lines.

20. What is Page Fault?
Ans: Occurs when a program attempts to access data or code that is in its address space, but is not currently located in the system RAM.

21. What is Cycle Stealing?
Ans: A method of accessing computer memory (RAM) or bus without interfering with the CPU.

22. What is meant by vector interrupt?
Ans: The interrupt source supplies the branch information to the processor through an interrupt vector.

23. If memory access takes 20ns with cache and 110 ns without it (cache uses a 10ns memory), then the hit ratio is **90%**
Ans: Explanation: Data: $T_{avg} = 20$ ns, T1 = 10 ns, T2 = 110 ns
    Formula: $T_{avg} = T1 + (1 - H)*T2$
    Calculation: $20 = 10 + (1 - H)*110 \therefore H = 0.9090 = 90\%$

24. What is the control unit's function in the CPU?
Ans: To controls the sequence of operations.

25. Memory access in RISC architecture is limited to instructions **STA (Store Accumulator) and LDA (Loading the accumulator)**

26. Data Hazards occur **when pipeline changes the order of read / write access to operands.**

27. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
Ans: Program Register.

28. Pipeline strategy is called implement **instruction decoding**.

29. A stack pointer is **a 16 – bit register in the microprocessor that indicate the beginning of the stack memory**.

30. The branch logic that provides decision making capabilities in the control unit is known as **unconditional transfer**.

31. Fragmentation is **dividing main memory into equal size fragments**.

32. **Static RAM** memories must be refreshed many times per second.

33. A memory buffer used to accommodate a speed differential is called **cache**.

34. Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called **Paging**.

35. Address of page table in memory is pointed by **program counter**.

36. SIMD represents an organization that **includes many processing unit under the supervision of a common control unit**.

37. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. The rotational latency refers **to the time it takes for the platter to make a full rotation**.

38. $(2FAOC)_{16}$ is equivalent to $(0010\ 1111\ 1010\ 0000\ 1100)_2$

39. The average time required to reach a storage location in memory and obtain its contents is called the **access time**.

40. Von Neumann architecture is **SISD**.

41. Write Through technique is used in **cache memory** for updating data.

42. In signed – magnitude binary division, if the dividend is $(11100)_2$ and divisor is $(10011)_2$, then the result is **$(10100)_2$**.

43. Logic X – OR operation of $(4AC0)_H$ & $(B53F)_H$ result is **FFFF**.

44. When CPU is executing a program that is part of the Operating System, it is said to be in **system mode**.

45. PSW (Program Status Word) is saved in stack when there is an **interrupt recognized**.

46. 'Aging registers' are **Counters which indicate how long ago their associated page have been referenced**.

47. BSA instruction is **branch and save return address**.

48. State whether TRUE or FALSE. (i) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers. (ii) An arithmetic shift left multiplies a signed binary number by 2.
Ans: **True, False**.

49. A group of bits that tell the computer to perform a specific operation is called **Instruction code**.

50. The communication between the components in a microcomputer take place via the address and **data bus**.

51. A micro program sequencer **generates the address of next micro instruction to be executed**.

52. The content of the program counter is added to the address part of the instruction in order to obtain effective address is called **relative address mode**.

53. The Winchester disk is a **Disk Stack**.

54. A bootstrap is a **small initialization program to start up a computer**.

55. Memory address refers to the successive memory words and machine is called as **word addressable**.