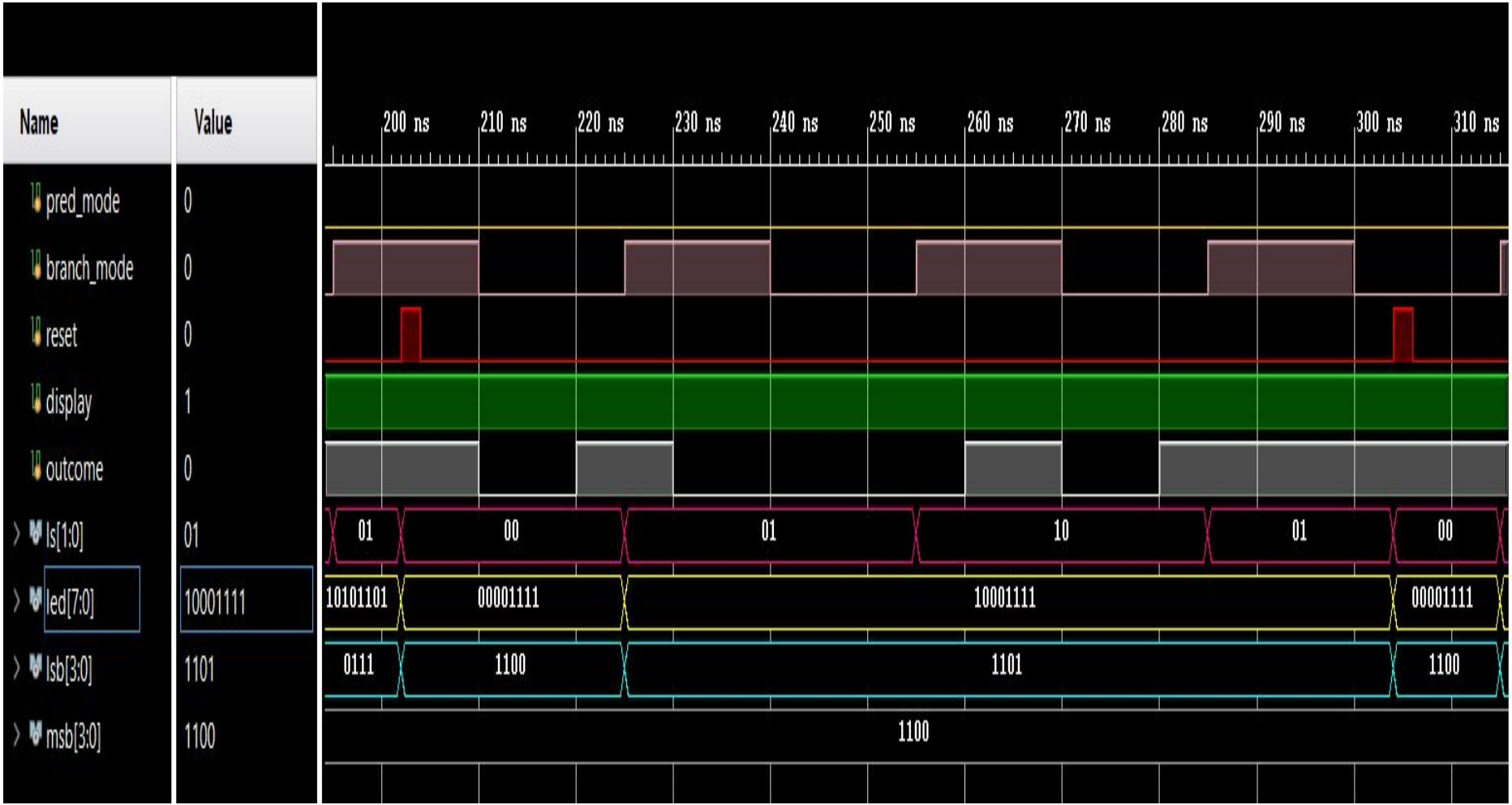
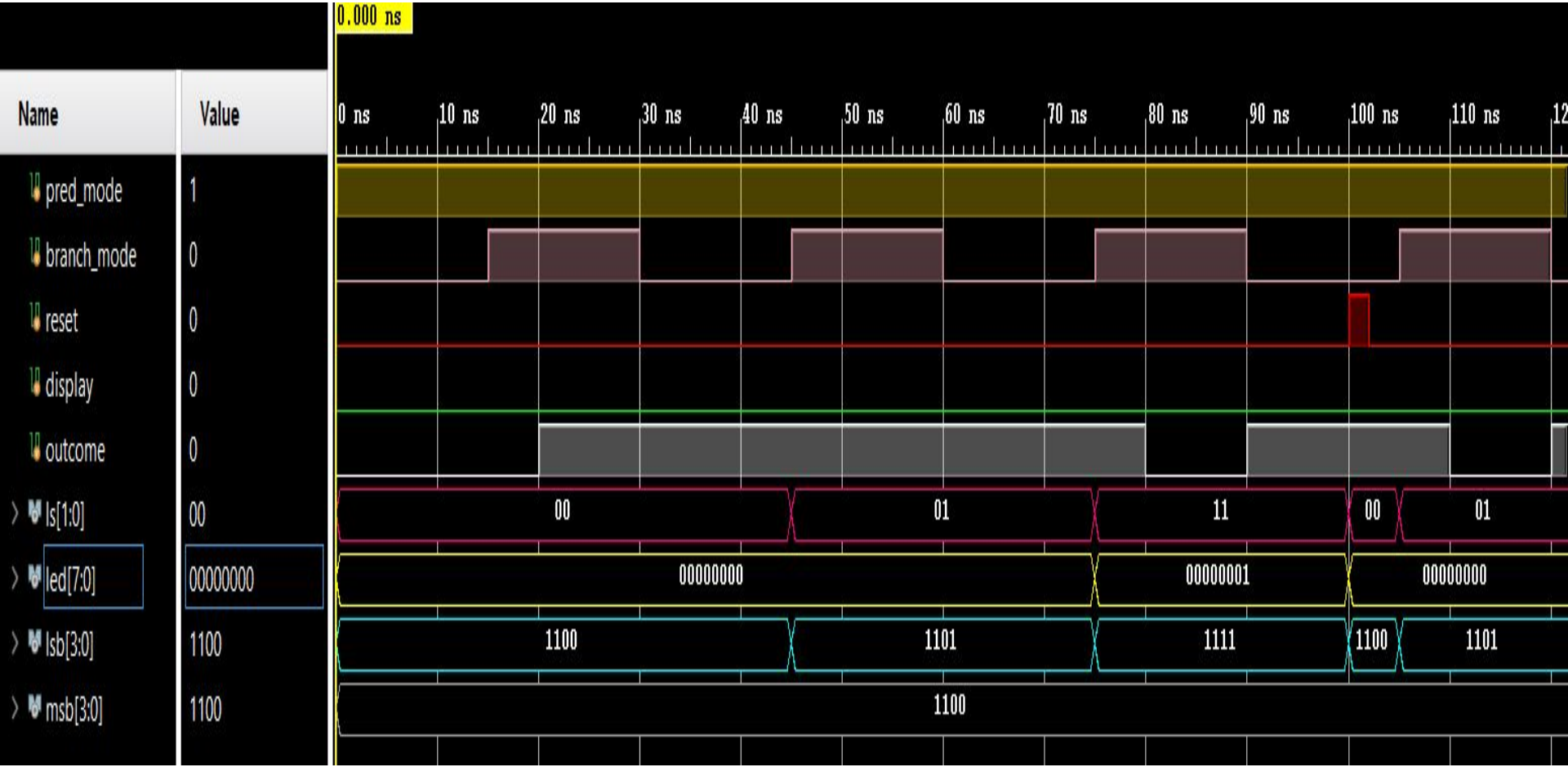

Name
Value
200 ns
210 ns
220 ns
230 ns
240 ns
250 ns
260 ns
270 ns
280 ns
290 ns
300 ns
310 ns
pred_mode
0
branch_mode
0
reset
0
display
1
outcome
0
ls[1:0]
01
01
00
01
10
01
00
led[7:0]
10001111
10101101
00001111
10001111
00001111
lsb[3:0]
1101
0111
1100
1101
1100
msb[3:0]
1100
1100

Explanation of the simulation:

The various input mode pulses are indicated by pred_mode, branch_mode, reset display and the actual outcome is fed using the outcome pulse. Whenever the branch mode is triggered at the positive edge of the branch_mode pulse, it takes into consideration the output waveform's value at that instant as the actual outcome to facilitate the FSM state changes.

The MSB waveform is the output pulse representing the MSB of the FSM status of the BHT entries, and similarly the LSB waveform. The leftmost bit of the MSB register represents the MSB of TT, then MSB of TN, then MSB of NT, and the rightmost bit the MSB of NN. Similarly, the corresponding bits in the LSB register represent the LSB of the FSM status of the 4 entries in BHT in the same order.

The LED waveform represents the MSB and LSB of all the 4 entries in the BHT in order. Hence the eighth and seventh bit (rightmost two bits) of the LED register represent the MSB and LSB of TT, sixth and fifth the MSB and LSB of TN, fourth and third the MSB and LSB of NT, and second and first (leftmost two bits) the MSB and LSB of NN.


0.000 ns
Name
Value
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
90 ns
100 ns
110 ns
pred_mode
1
branch_mode
0
reset
0
display
0
outcome
0
ls[1:0]
00
00
01
11
00
01
led[7:0]
00000000
00000000
00000001
00000000
lsb[3:0]
1100
1100
1101
1111
1100
1101
msb[3:0]
1100
1100

Explanation of the simulation:

In the prediction mode, the rightmost bit of the LED register represents the predicted outcome. All other registers perform the same job as explained in the previous case.