Assignment 2

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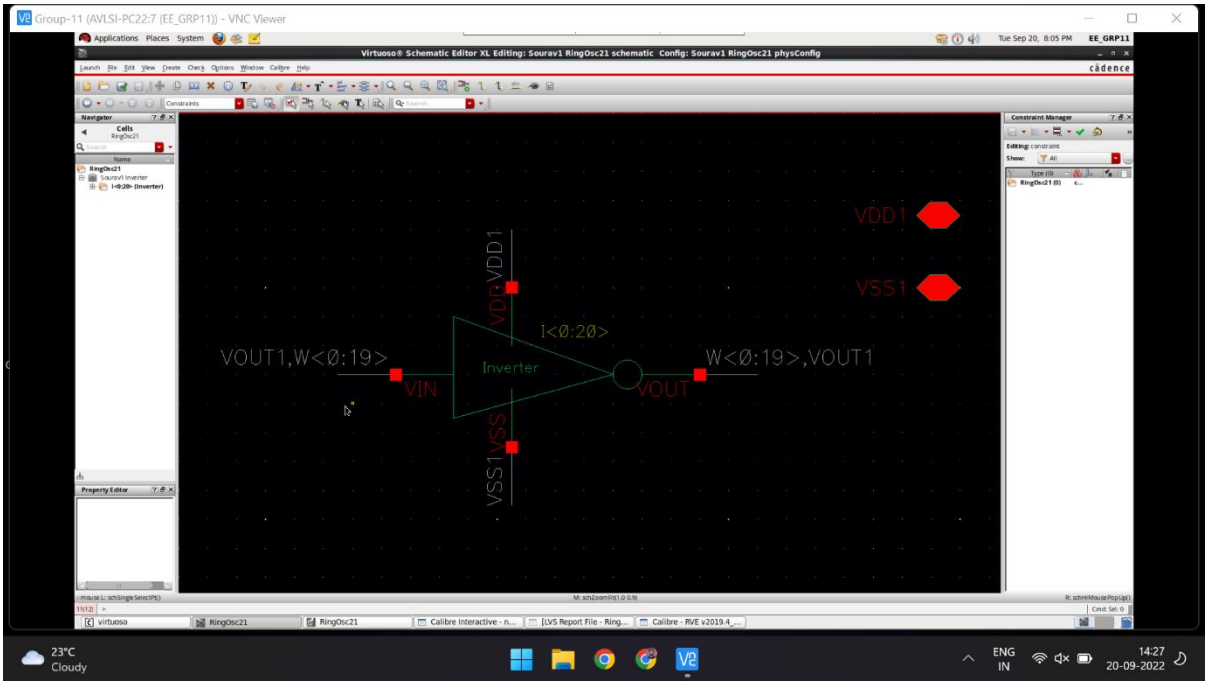
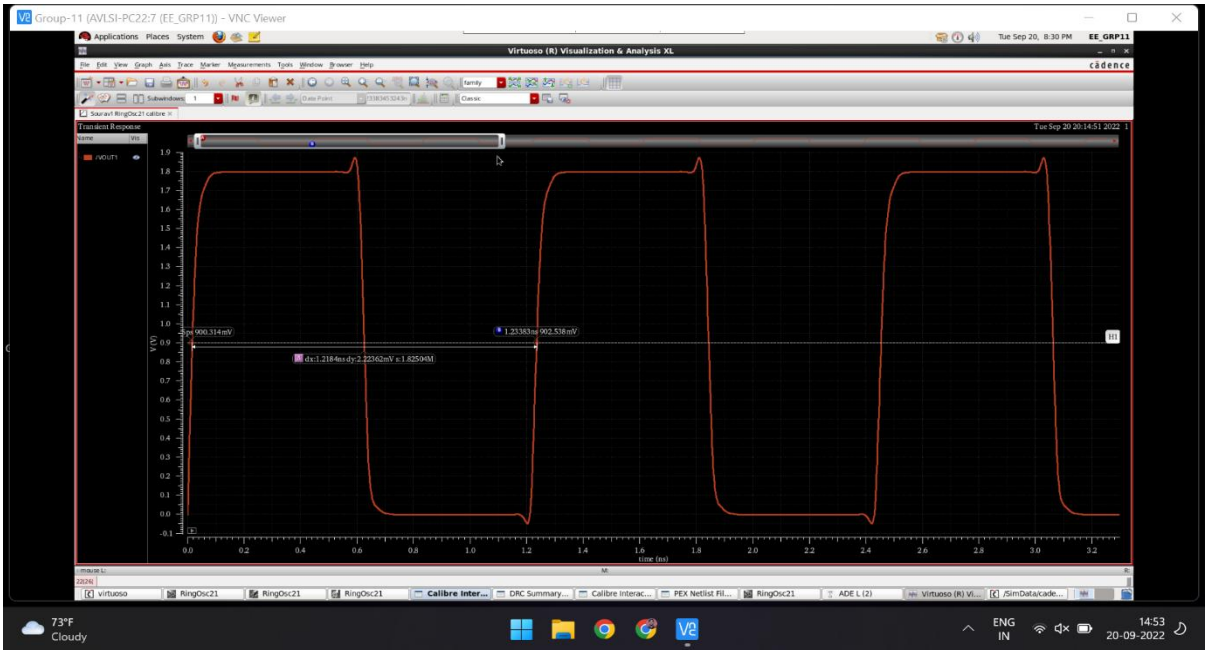
- ***Performing the simulation and layout of the Ring Oscillator circuit and verifying the operation of the circuit by performing LVS.***

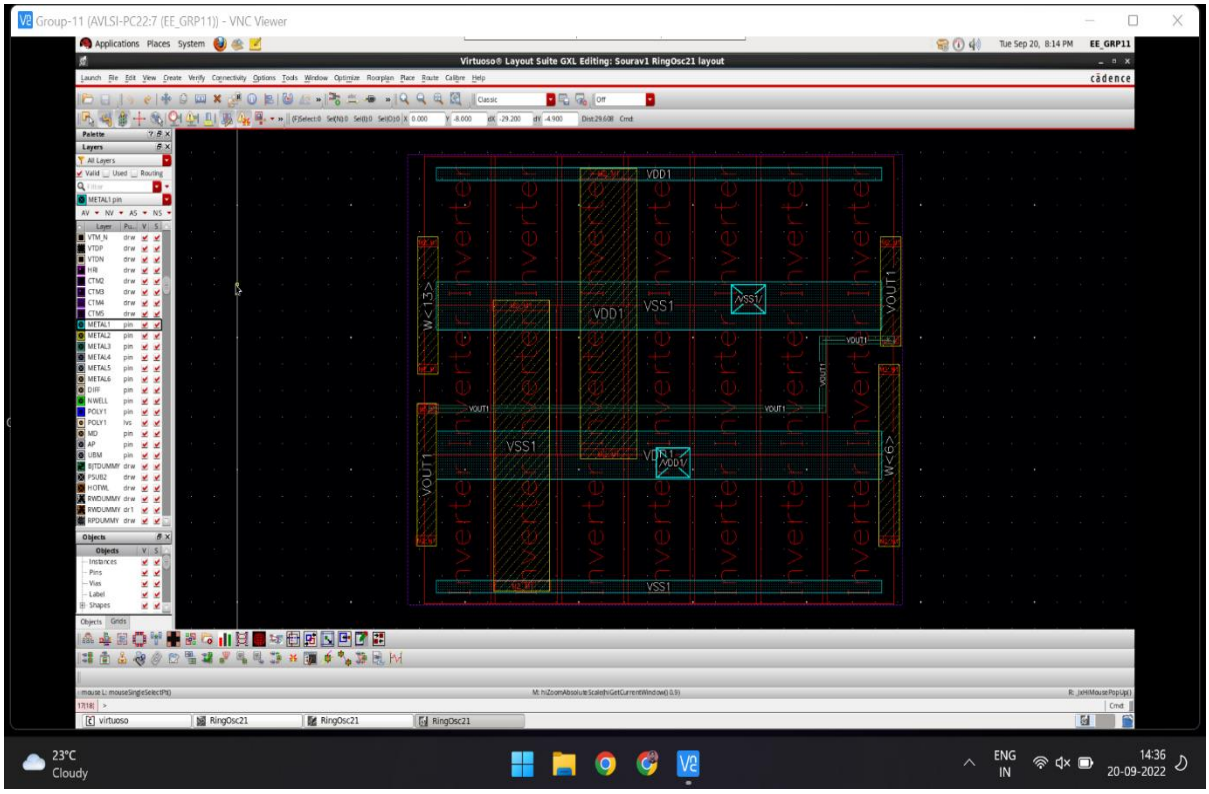
1. Schematic of Ring Oscillator with 21 inverters



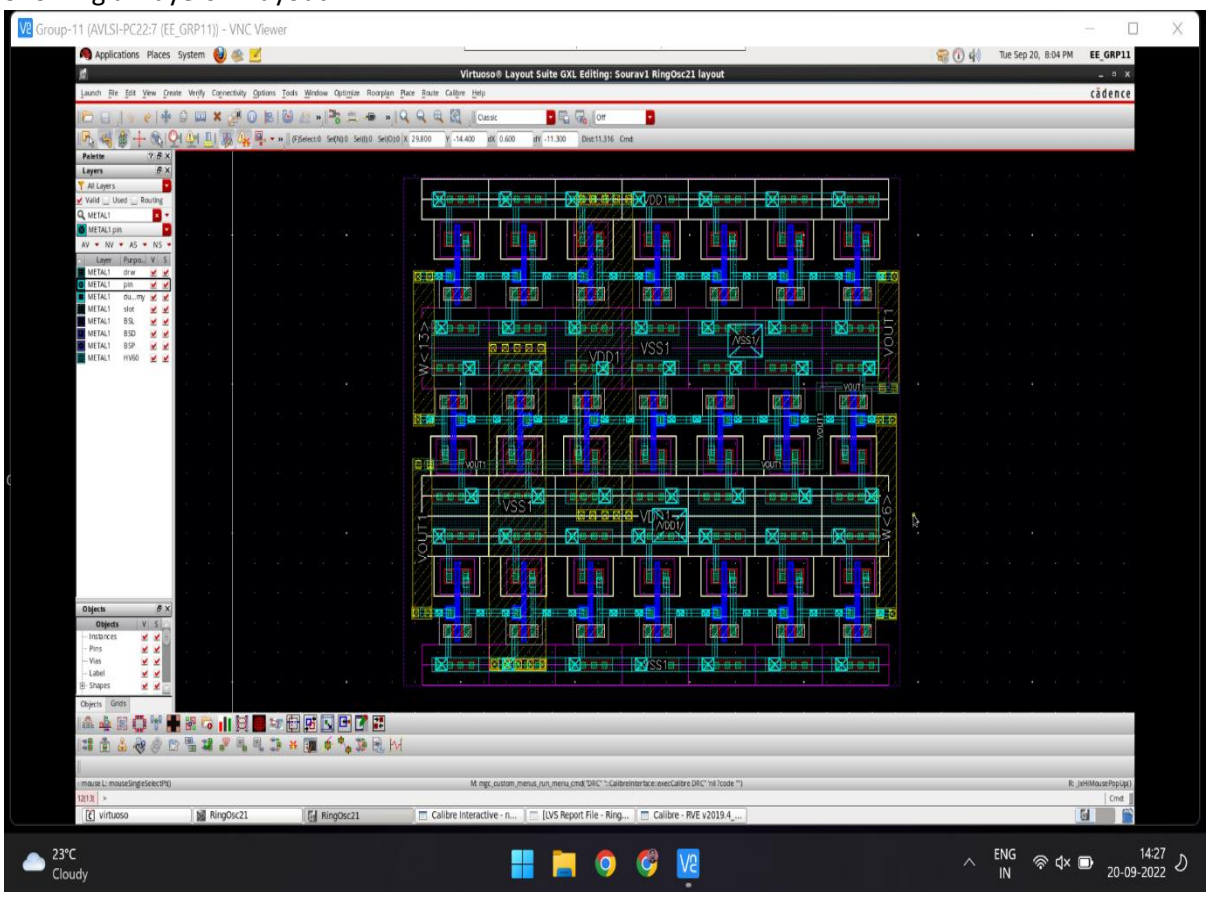
2. Simulation of the above ring oscillator schematic (time delay=1.218/(2*21)=29ps)



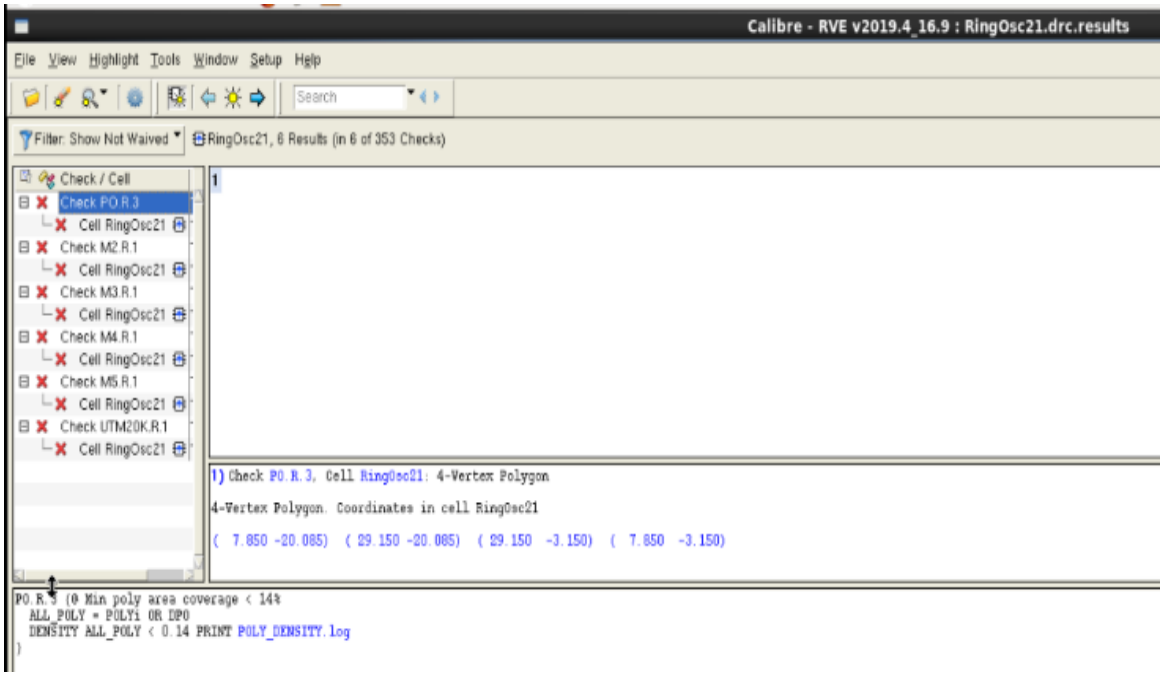
3. Layout of the Ring oscillator



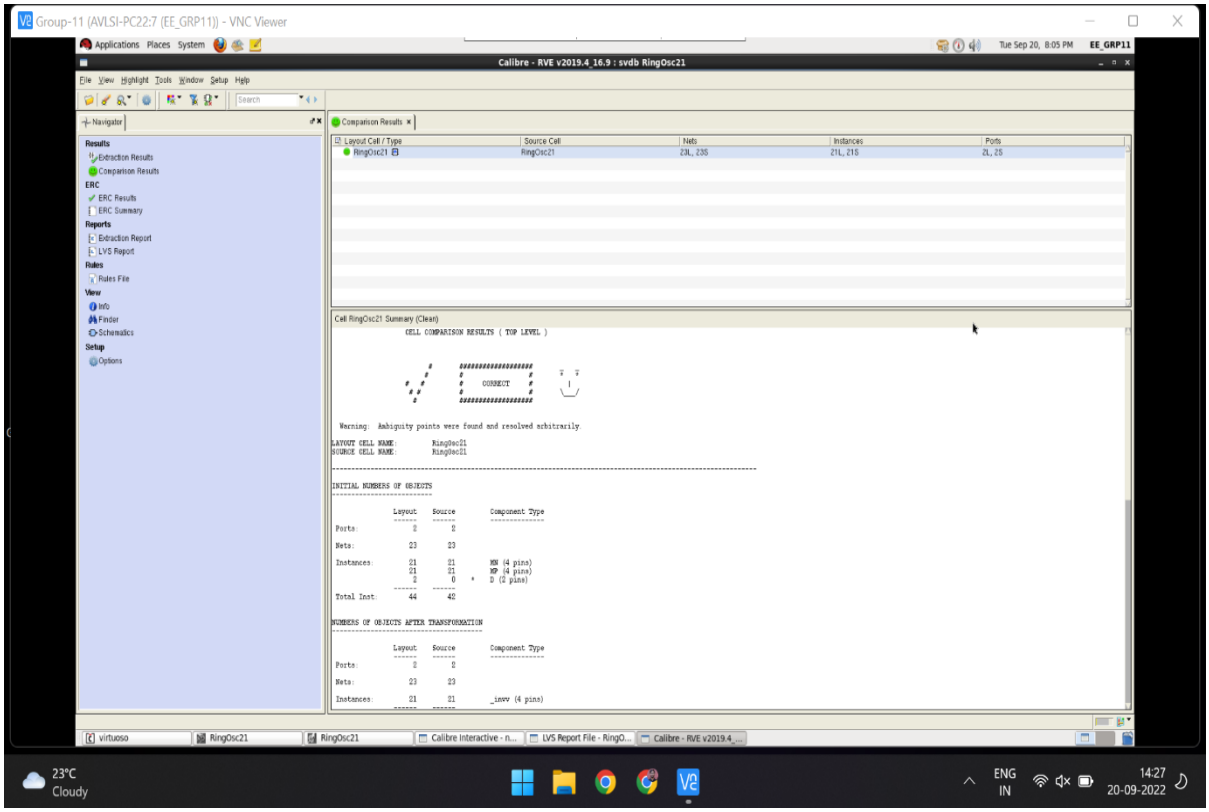
4. Showing all layers in layout



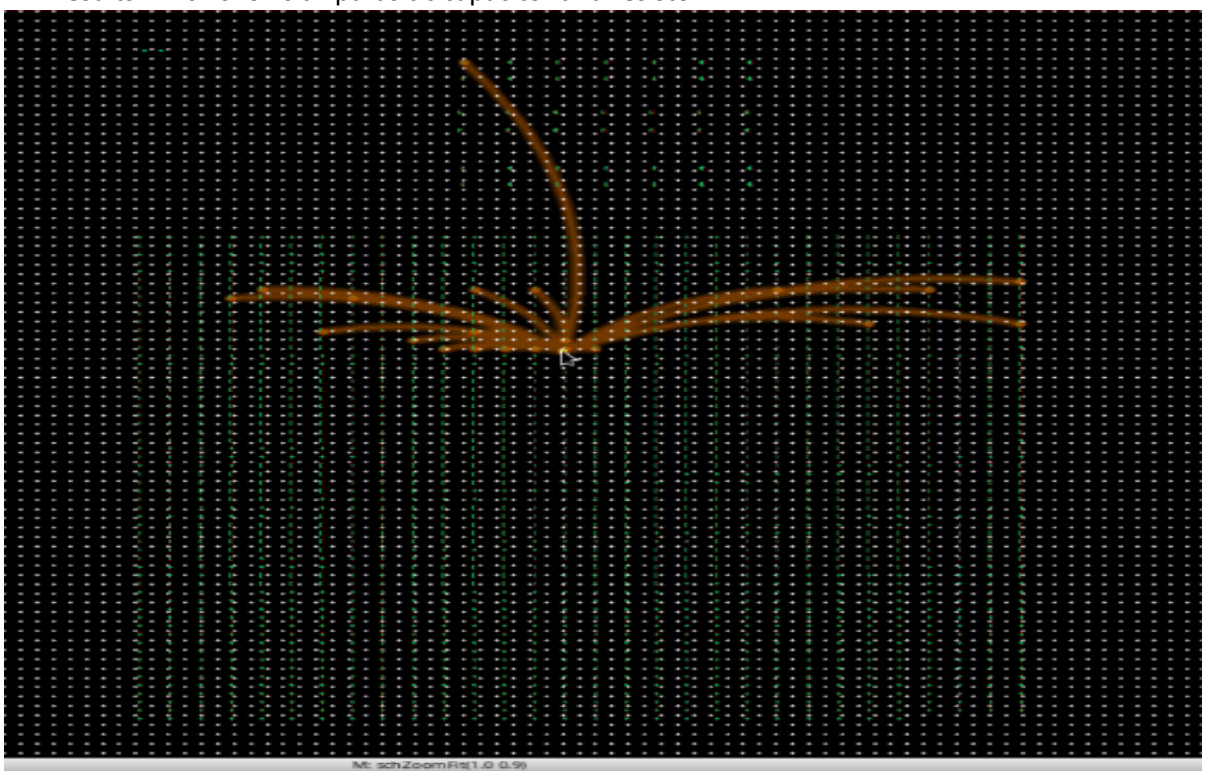
5. DRC check results (only density errors are coming which we can ignore)

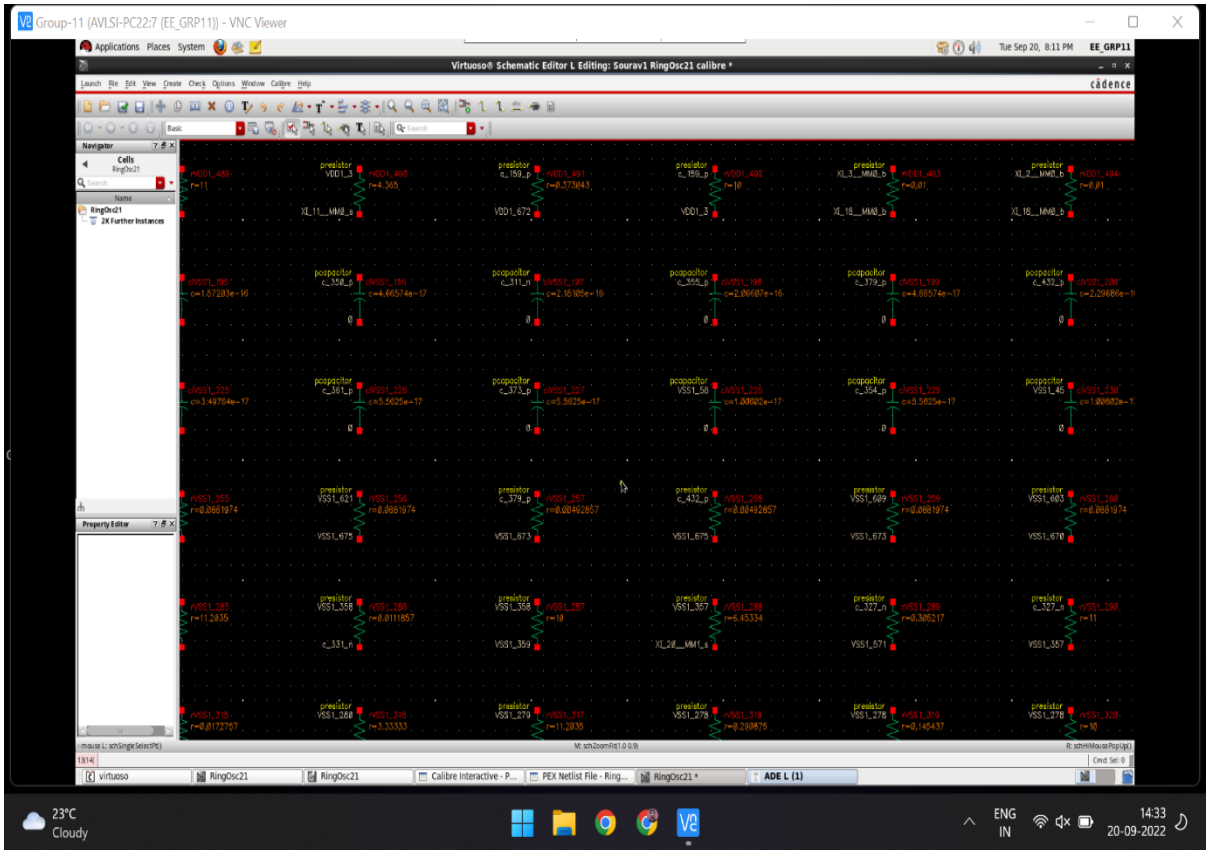


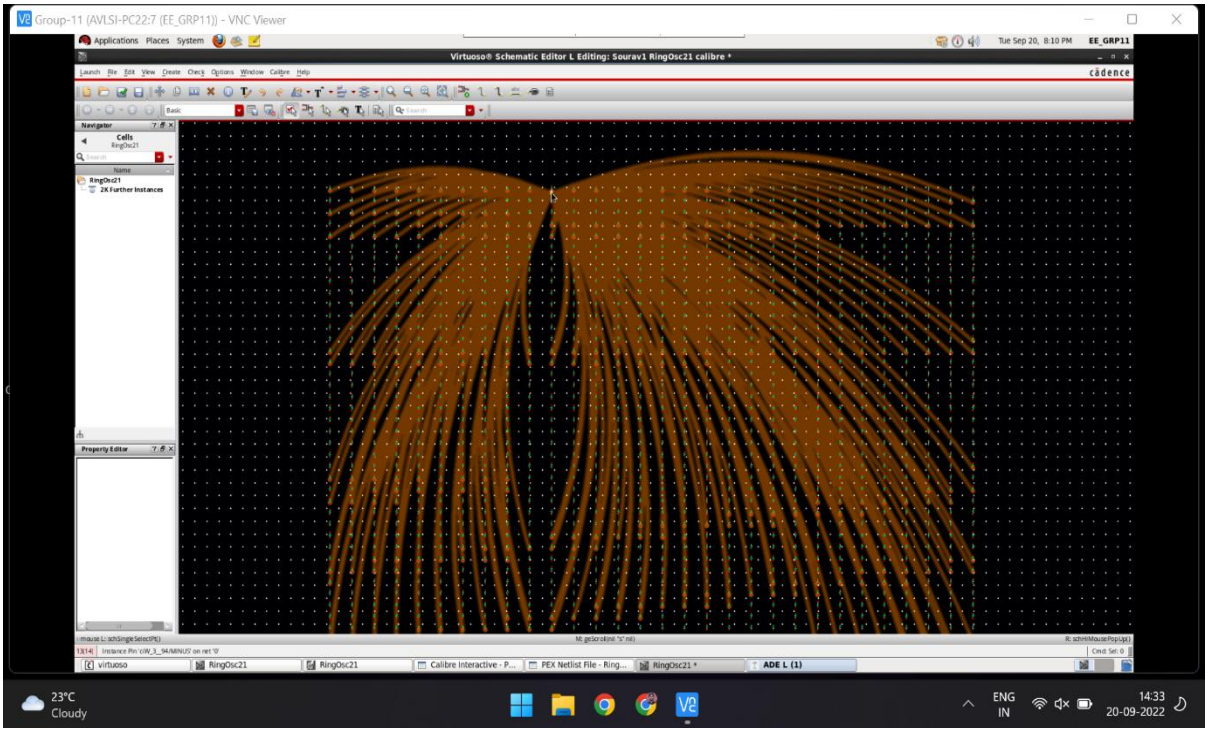
6. LVS check results (no errors)



7. PEX results which shows all parasitic capacitor and resistor



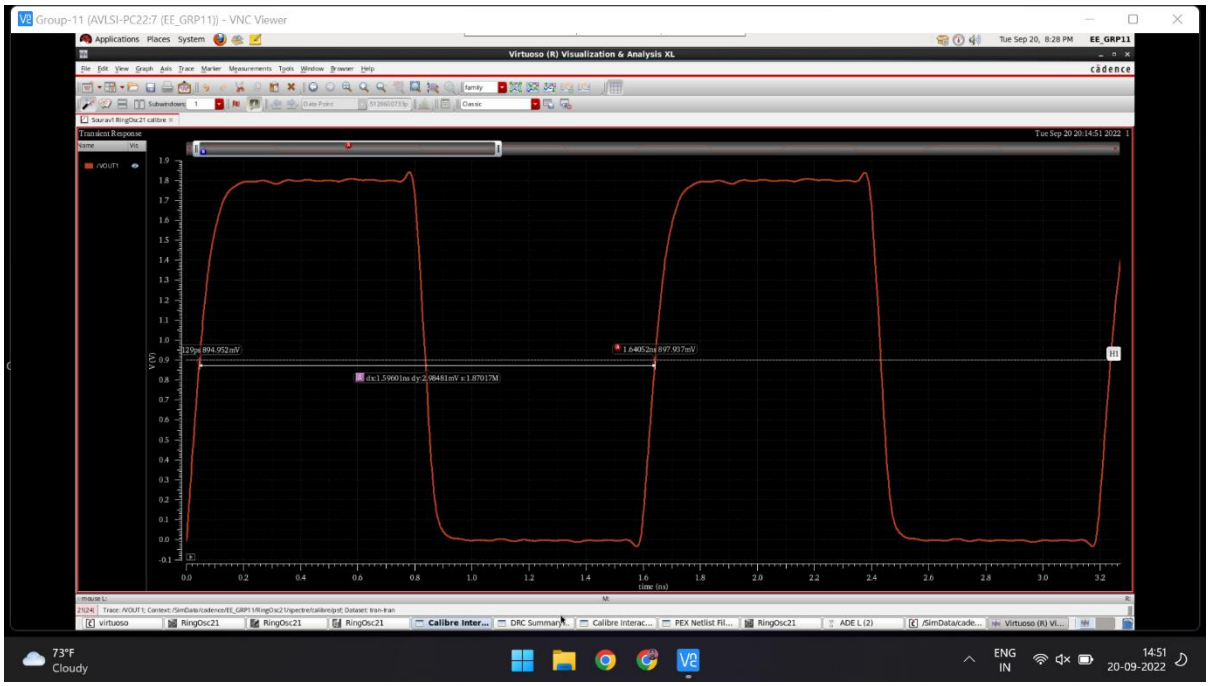




8. Simulation results of Ring oscillator layout with Parasitic capacitors and resistors

9. Time period of ring oscillator (T) = 1.596ns.

   So time delay of a single inverter (t_p) = $\frac{1.596}{2*21} = 38\text{ps}$



Conclusions:

1.) Time delay of individual inverter in schematic is $t_p = \left[\frac{29.75+18.88}{2}\right] = \mathbf{24.315ps}$.

2.) Time delay of individual inverter in layout is $t_p = \left[\frac{35.19+22.87}{2}\right] = \mathbf{29.03ps}$.

3.) Time delay of a single inverter using ring oscillator schemmatic is $t_p = \left[\frac{1.218}{2*21}\right] = \mathbf{29ps}$.

4.) Time delay of a single inverter using ring oscillator layout is $t_p = \left[\frac{1.596}{2*21}\right] = \mathbf{38ps}$.