4-Bit Asynchronous Up Counter

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Abstract—

An asynchronous counter is where all the clock contributions of the flip-flops have a novel information that isn't imparted to some other flip-flops in the framework. Offbeat counters can be effectively planned by T flip lemon or D flip failure. These are likewise called as Ripple counters and are utilized in low-speed circuits. On the off chance that the UP input and down sources of info are 1 and 0 separately, at that point the NAND doors between the primary flip lemon to third flip failure will pass the non-modified yield of FF 0 to the clock contribution of FF 1. Correspondingly, the Q yield of FF 1 will go to the clock contribution of FF 2. In this way, the UP counter performs up tallying. A 4-piece offbeat up counter worked from four positive edge-set off D type flip-flops associated in switch mode. In the no concurrent 4-piece up counter, the flip flop is associated in switch mode. They are utilized as Divide by-n counters, which partition the contribution by n, where n is a number. It is equipped for checking numbers from 0 to 15. 4-piece Offbeat counters are likewise utilized as Truncated counters. These can be utilized to plan any mod number counters, for example indeed, even Mod (ex: mod 4) or odd Mod (ex: mod3). At times additional flip failure might be required for "Resynchronization".

Index Terms—Counter, flip-flop, asynchronous, clock

1. INTRODUCTION

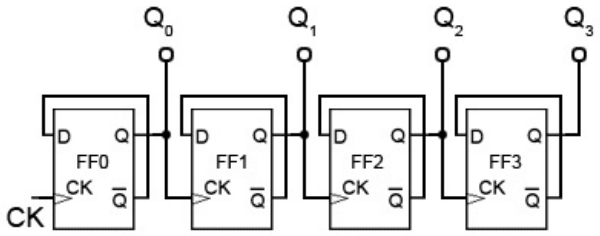
Asynchronous counters are those whose output is free from the clock signals. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output.

The required number of logic gates to design 4-bit asynchronous counters are very less. The number of flips flops used in an asynchronous counter is depends up on the number of states of counter. The maximum number of states that a counter can have is 2^n where n represents the number of flip flops used in counter. In a 4-bit asynchronous up counter,

The number of states for the counter=2^n =2^4=16.

So, we have 16 states in case of 4-bit up counters.

We can also find out the maximum count=2^n-1=2^4-1=15. That means it can count maximum number 15.the binary conversion of 15=111. The initial count of the counter is 0000.



The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop. That means the flip flops will toggle at each active edge or positive edge of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q' output of previous flip flop. The output of the first flip flop will change, when the positive edge on clock signal occurs. In the asynchronous 4- bit up counter, the flip flops are connected in toggle mode. The rising edge of the Q output of each flip flop triggers the clock input of its next flip flop. It triggers the next clock frequency to half of its applied input.

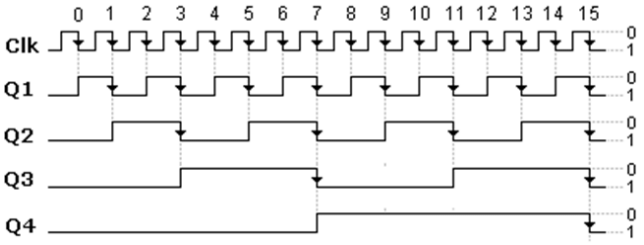


Fig: Timing Diagram of 4-bit Asynchronous up Counter

While using the Asynchronous up counter, an additional re-synchronizing output flip-flops required for resynchronizing the flipflops. Also, For the truncated sequence count, when it is not equal to, extra feedback logic is needed.

When counting a large number of bits, due to the chain system, propagation delay by successive stages became too large which is very difficult to get rid of. In such a situation, Synchronous counters are faster and reliable. There are also counting errors in Asynchronous Counter when high clock frequencies are applied across it.

II. METHODOLOGY

Let us assume that the 4 Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the FF0, then the output Q0 will change to logic 1 and the next clock pulse will change the Q0 output to logic 0. This means the output state of the clock pulse toggles (changes from 0 to1) for one cycle.

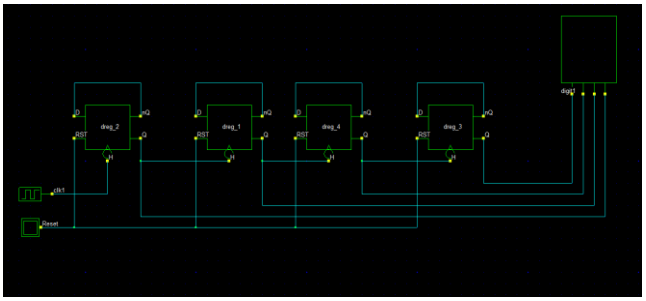


Fig: 4-bit Asynchronous up Counter

As the Q' of FF0 is connected to the clock input of FF1, then the clock input of second flip flop will become 1. This makes the output of FF1 to be high (i.e. Q1 = 1), which indicates the value 20. In this way the next clock pulse will make the Q0 to become high again.

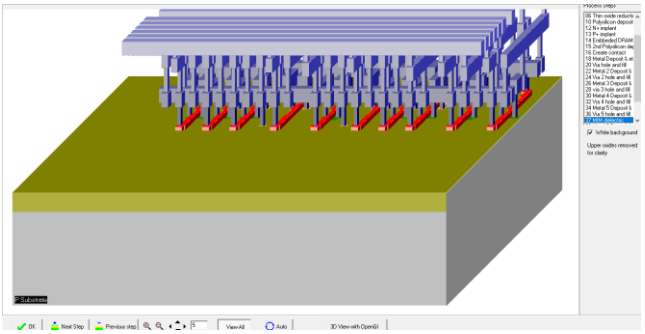


Fig: 3D Process View of 4-bit Asynchronous Up Counter

So now both Q0 and Q1 are high, this results in making the 4-bit output 11002. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the FF2. So, the output Q2 will become 0010¬2. As this circuit is 4-bit up counter, the output is sequence of binary values from 0, 1, 2, 3….15.

III. RESULT

In this section the simulation of DSCH simulation of 4 Bit asynchronous counter is given:

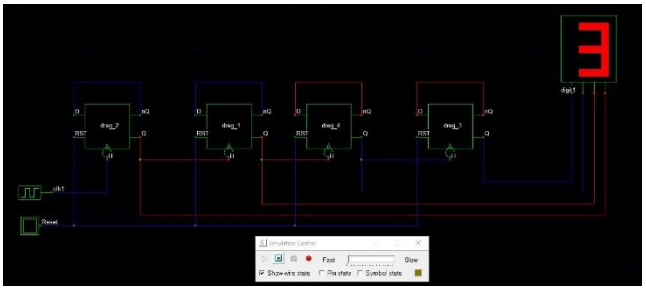
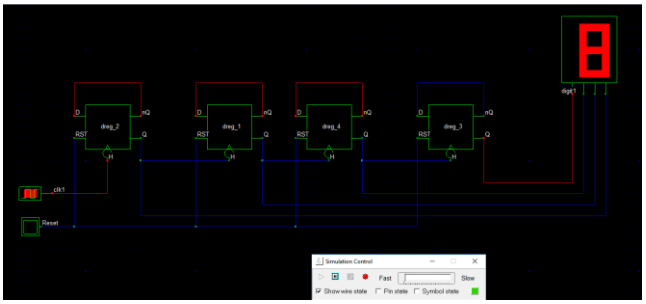


Fig: 4-bit Asynchronous up counter



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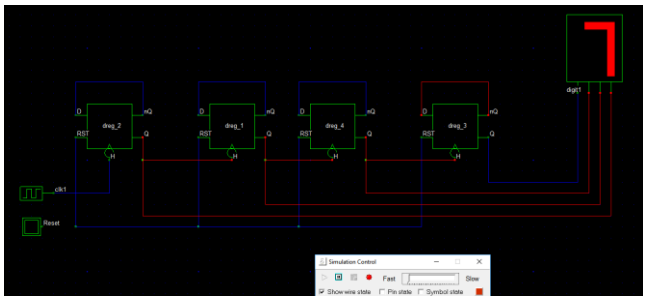

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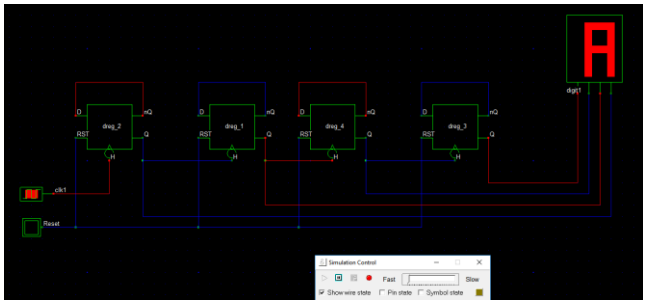

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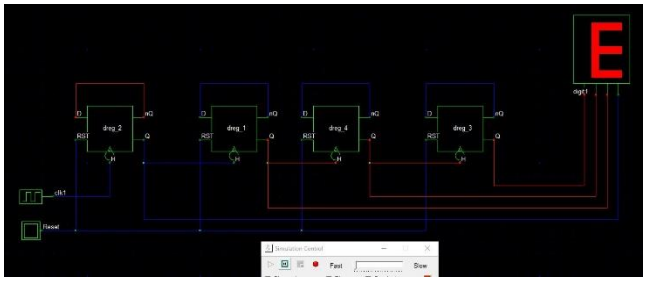

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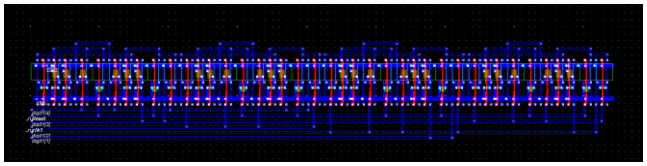

Fig: 3D Image of 4-bit Asynchronous Up Counter in MICROWIND

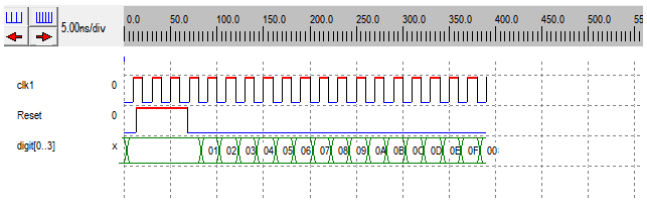

Fig: Timing Diagram of 4-bit asynchronous up Counter

TRUTH TABLE

CLK	Q4	Q3	Q2	Q1	Decimal No.
Initial	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	1	1	0	0	12
13	1	1	0	1	13
14	1	1	1	0	14
15	1	1	1	1	15

IV. Conclusion

The key commitment of this paper was completed for the of flip failure and no concurrent counter. The proposed acknowledgment offbeat counter plans tally successively on each clock beat the subsequent yields tally upwards from 0 (0000) to 15 (1111).

The beat set off flip failure was to give a sign feed through from input source to the interior hub of the hook, which would encourage additional heading to abbreviate the progress time, dodges pointless semiconductor and upgrade both force and speed execution the rationale and qualities of the flip-flop and offbeat 4-piece up counter are handily confirmed with the recreation results.

Reference

[1] https://www.electronics-tutorials.ws/counter/count_3.html.

[2] https://www.electronicshub.org/asynchronous-counter/

[3] A testable asynchronous counter

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