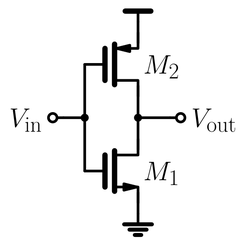
JOHANNES KEPLER UNIVERSITY LINZ

Fifty$^+$ Nifty Variations of Two-Transistor Circuits

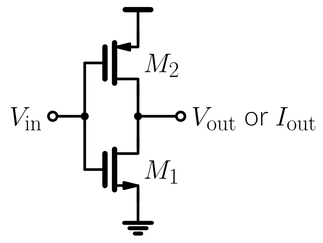
INSTITUTE FOR INTEGRATED CIRCUITS

Circuit No. 1



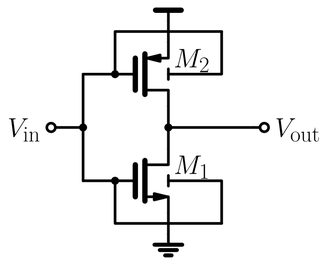
This is the ubiquitous digital **inverter**. The input voltage V_{in} switches one of both transistors on while the other is off.

Circuit No. 2



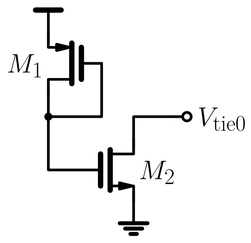
The same structure can be used as a **voltage amplifier** (V_{out}, with high-Z loading) or low-voltage complementary **transconductance stage** (I_{out}, with low-Z loading) when both MOS-FET are held in saturation.

Circuit No. 3



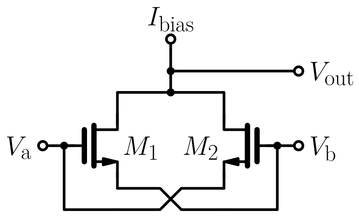
The (dynamic threshold) **DT-MOS inverter** achieves an improved current drive at low leakage current. It needs to be operated at low supply voltages to avoid a forward bias of the well diodes.

Circuit No. 4



An ESD-safe **tie-zero** for unused CMOS logic inputs (no MOS-FET gate should be tied directly to a supply rail). The tie-one can be constructed accordingly.

Circuit No. 5

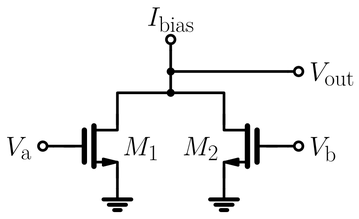


Using a current source I_{bias} with finite output impedance to bias this structure, this circuit implements an **XNOR** logic function ($V_{\text{out}} = \overline{V_{\text{a}} \oplus V_{\text{b}}}$). The logic inputs V_{a} and V_{b} must be driven by low-ohmic logic levels between V_{DD} and V_{SS}.

Circuit No. 6

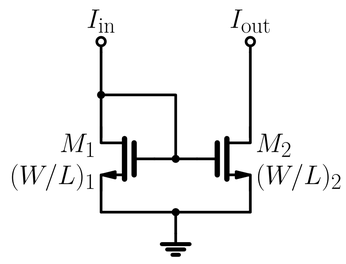
This series connection of two MOS-FETs realizes a logical **NAND** function ($V_{\text{out}} = \overline{V_{\text{a}} \wedge V_{\text{b}}}$) when driven by logic inputs.

Circuit No. 7



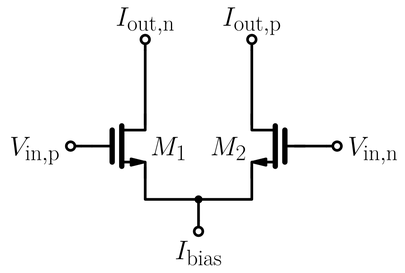
This circuit complements the logic gates and realizes a **NOR** function ($V_{\text{out}} = \overline{V_{\text{a}} \vee V_{\text{b}}}$).

Circuit No. 8



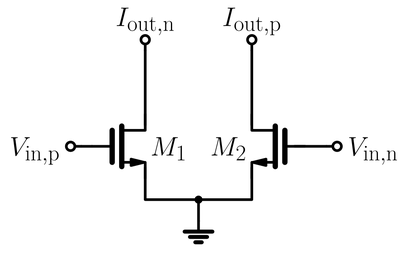
This circuit is the basic **current mirror**, simultaneously copying and sizing of $I_{\text{out}} = (W/L)_2/(W/L)_1 \cdot I_{\text{in}}$ according to the dimensions of M_1 and M_2.

Circuit No. 9



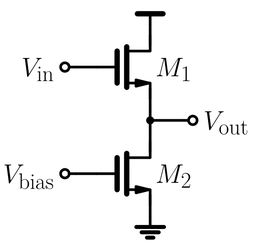
The ubiquitous **differential pair** (or long-tailed pair), like the current mirror, is a fundamental building block in integrated circuits.

Circuit No. 10



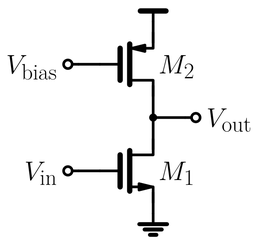
The **pseudo-differential pair** spares the tail current source's headroom in exchange for reduced common-mode rejection, but with the benefit of class-AB operation.

Circuit No. 11



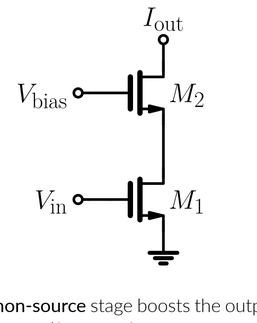
This is the **source follower** (or common-drain stage), utilizing M_2 as a current source to bias M_1.

Circuit No. 12



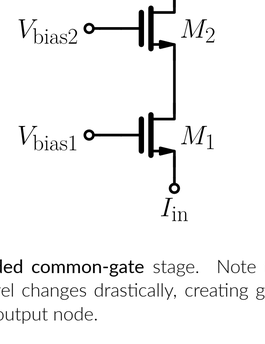
The **common-source** amplifier stage with active load.

Circuit No. 13



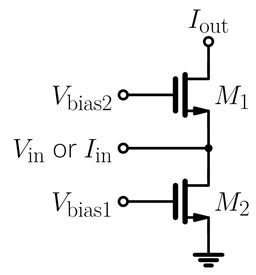
The **cascoded common-source** stage boosts the output impedance of M_1 considerably to $r_{\text{out}} \approx g_{m2}/(g_{ds1} \cdot g_{ds2})$.

Circuit No. 14



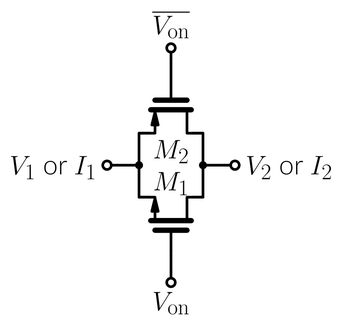
This is the **cascoded common-gate** stage. Note that $I_{\text{out}} \approx I_{\text{in}}$, but the impedance level changes drastically, creating gain or a high output impedance at the output node.

Circuit No. 15



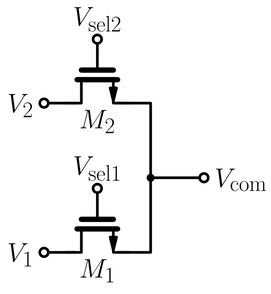
The **common-gate stage**, employing M_2 as a current source to bias transistor M_1. The input can be either a voltage- or a current-signal.

Circuit No. 16



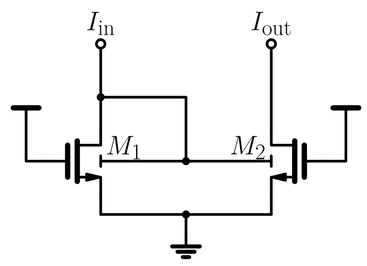
The **transmission gate** switches either voltage (V_1 and V_2) or current (I_1 and I_2) (and it works rail to rail, too).

Circuit No. 17



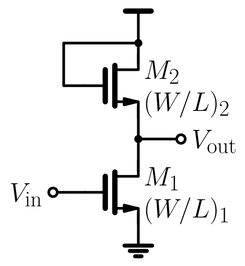
The 2-to-1 **multiplexer**, connecting either V_1 or V_2 to V_{com}. Depending on V_{sel1} and V_{sel2}, the MOS-FETs are alternately switched on or off.

Circuit No. 18



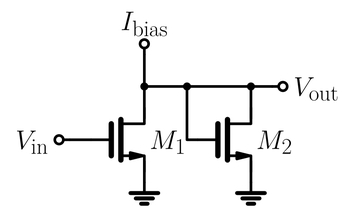
This circuit is an improved **bulk-driven current mirror** that allows low voltage operation, requiring a voltage headroom substantially less than V_{GS1}.

Circuit No. 19



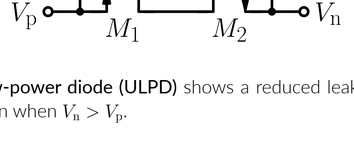
The **common-source amplifier with diode load** is sometimes called a wide-band amplifier due to its potentially high-speed operation. Here, the gain is set precisely to $A_v = V_{\text{out}}/V_{\text{in}} = -\sqrt{(W/L)_1/(W/L)_2}$, only depending on transistor sizing (if we neglect the body effect and finite output conductance).

Circuit No. 20



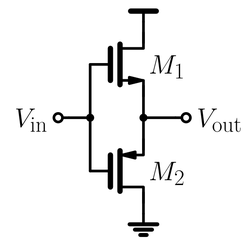
This **wide-band amplifier** has the advantage of a removed body effect in M_2 and a ground-referred output node.

Circuit No. 21



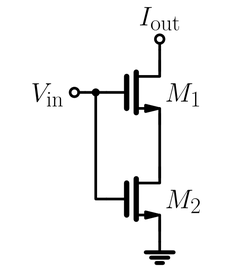
This **ultra-low-power diode (ULPD)** shows a reduced leakage in the reverse direction when $V_{\text{n}} > V_{\text{p}}$.

Circuit No. 22



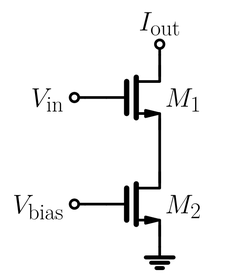
This class-B **push-pull follower** can be considered an enhanced version of the simple source follower. However, lacking a class-A bias component, this structure is subject to cross-over distortion.

Circuit No. 23



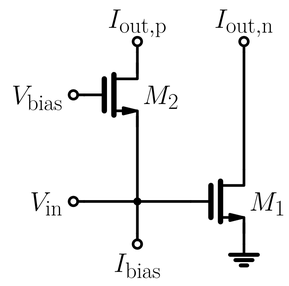
This circuit is a **MOS-FET-R degenerated common-source** stage. By sizing M_2 appropriately, the degeneration can be adapted. This arrangement using two transistors can also increase the length of a (compound) device, for example, in current mirrors, as otherwise, MOS-FETs with different L will not match well.

Circuit No. 24



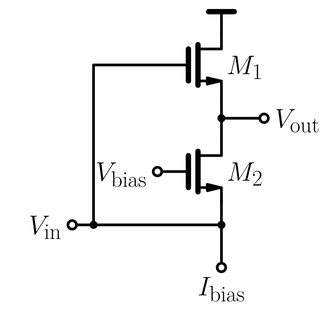
This is a variation of the implementation shown earlier, where the **degeneration** of M_1 can be **adapted** by tuning V_{bias}.

Circuit No. 25



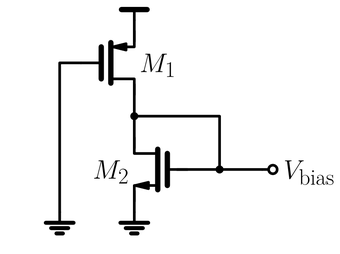
This **common-gate–common-source** topology offers an impedance-matched single-ended input and a differential output while simultaneously canceling noise and distortion.

Circuit No. 26



This **low-noise amplifier** was discovered by doing an exhaustive search for potential two-transistor wide-band amplifiers. For practical implementation, M_1 requires an ac-coupling (and proper biasing) in its gate connection to keep M_2 in saturation.

Circuit No. 27



This (simple) **bias voltage generator** uses the current source M_1 to bias M_2 so that $V_{\text{bias}} = V_{\text{GS2}}$. Note that the generated voltage is susceptible to changes in process, supply voltage, and temperature (PVT).

Based on: Harald Pretl and Matthias Eberlein, "Fifty Nifty Variations of Two-Transistor Circuits: A tribute to the versatility of MOSFETs," in *IEEE Solid-State Circuits Magazine*, Summer 2021.
doi: 10.1109/MSSC.2021.3088968, harald.pretl@jku.at